Part B

```
(2) /*
module my_firstmodule (input A, input B, output C);
and(C, A, B);
endmodule
*/

(3) /*
module my_firstmodule (input A, input B, output C);
assign C = A | B;
endmodule
*/

(4) /*
module my_firstmodule (input A, input B, output C);
assign C = A ^ B;
endmodule
*/
```

Part C

```
/*
module my_firstmodule (input A, input B, input C, output D);
assign D = (A & B) | (B & C) | (A & C);
endmodule
*/
```

-> above Verilog code is a 3 input majority gate, that is if at least 2 inputs (out of A, B, C) are 1, then output D will be equal to 1.