Common Signal Names & Naming Conventions

Signals beginning with capital letters denote an I/O pin
Signals beginning with lower case letters are internal to a cell

VDD – Supply Voltage
$\overline{\text{RST}}$ – Reset (Active Low)
RST – Reset (Active High)
GND – Ground or VSS equivalent

L – Left (DI Encoded Input Channel)
Le – Left enable

R – Right (DI Encoded Output Channel)
Re – Right enable

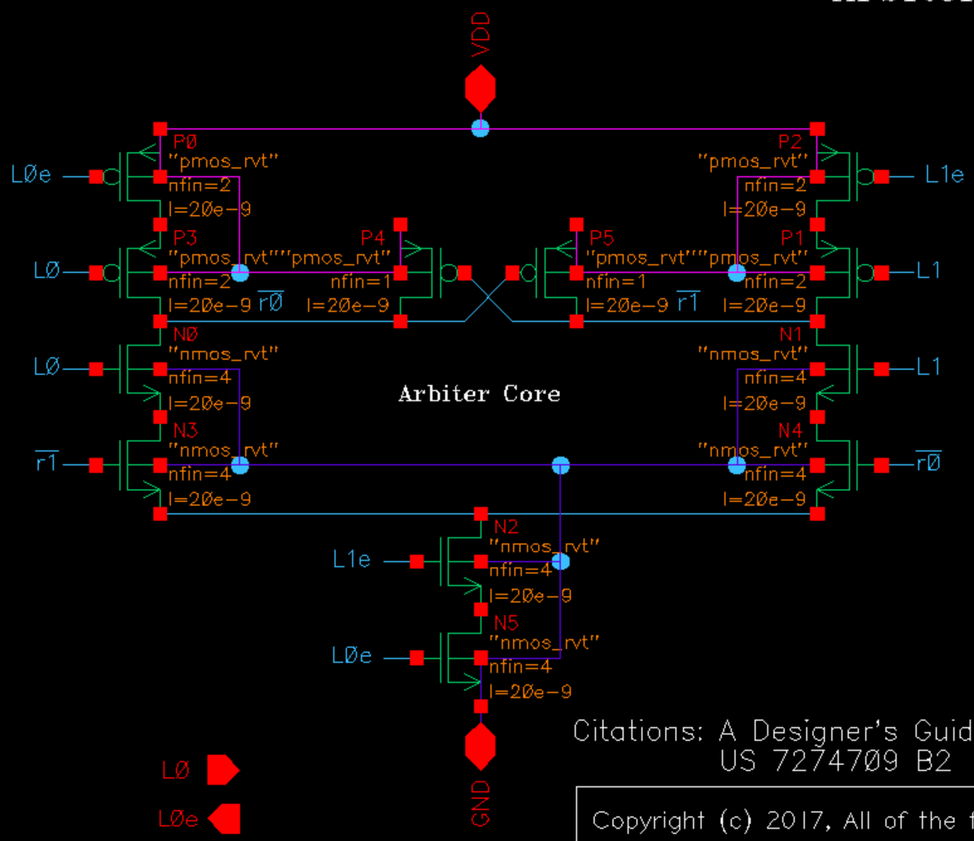
S – Split (DI Encoded Input Control Channel)
SLe – Split & Left Enable

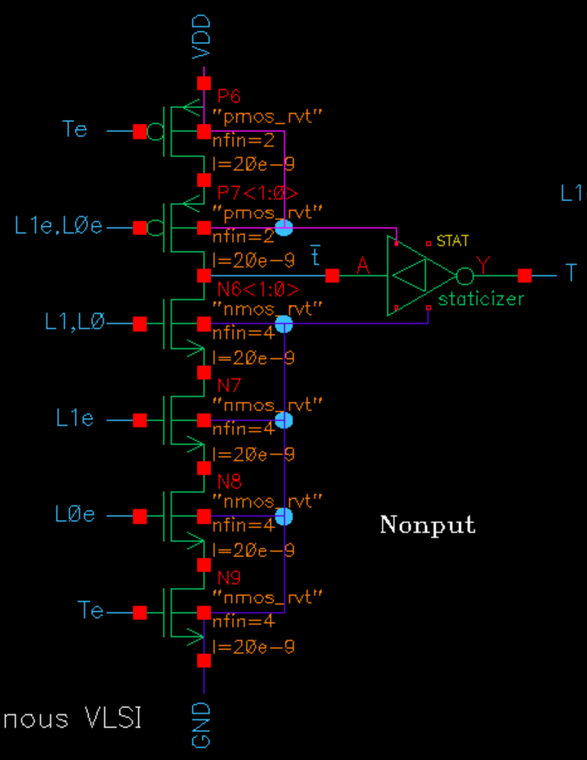
M – Merge (DI Encoded Input Control Channel)
Me – Merge Enable

A, Ae; B, Be; C, Ce; D, De; etc:
Input or output channels (cell dependent) w/ corresponding enable signals

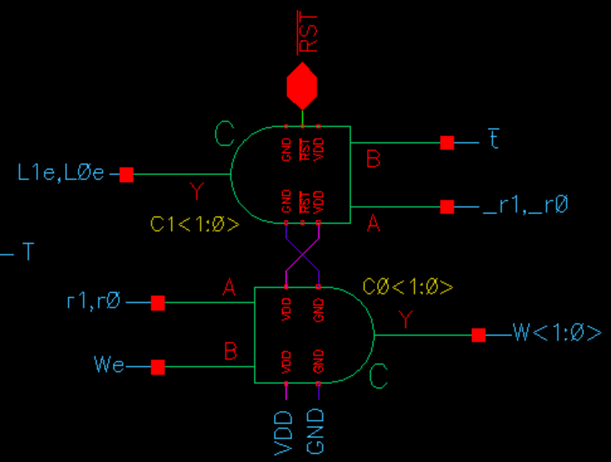
en – internal enable
lv – left valid
rv – right valid
sv – split valid
$\underline{\text{slv}}$ – split & left valid
$\overline{\text{slv}}$ – not split & left valid (inverted slv)
etc.

Arbiter_QDI_Nonput

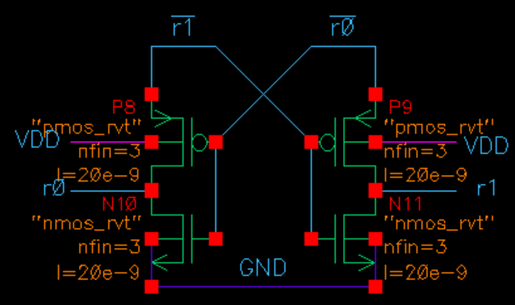




Nonput

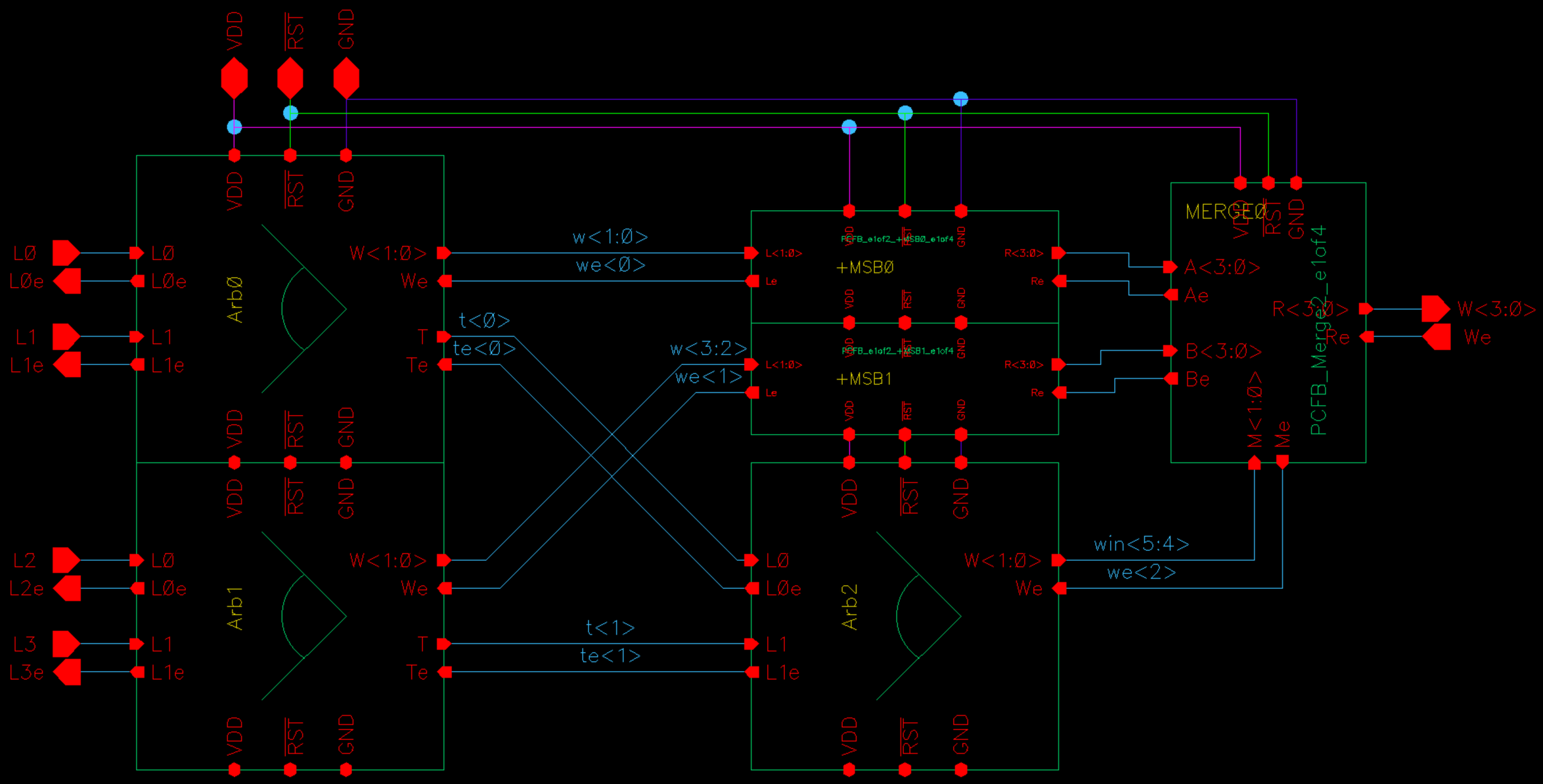


Winner Output Rails

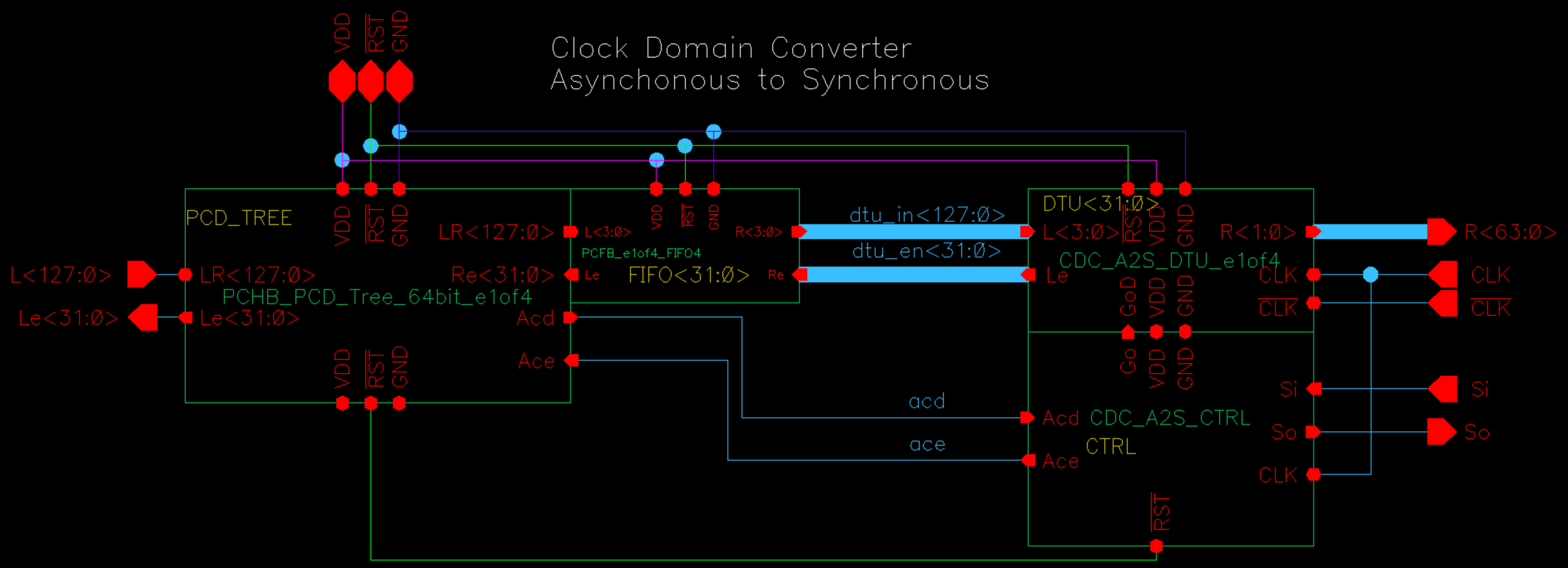


Metastability Filter

Citations: A Designer's Guide to Asynchronous VLSI
US 7274709 B2



Citation: A Designer's Guide to Asynchronous VLSI



Citation: US 6961863 B2

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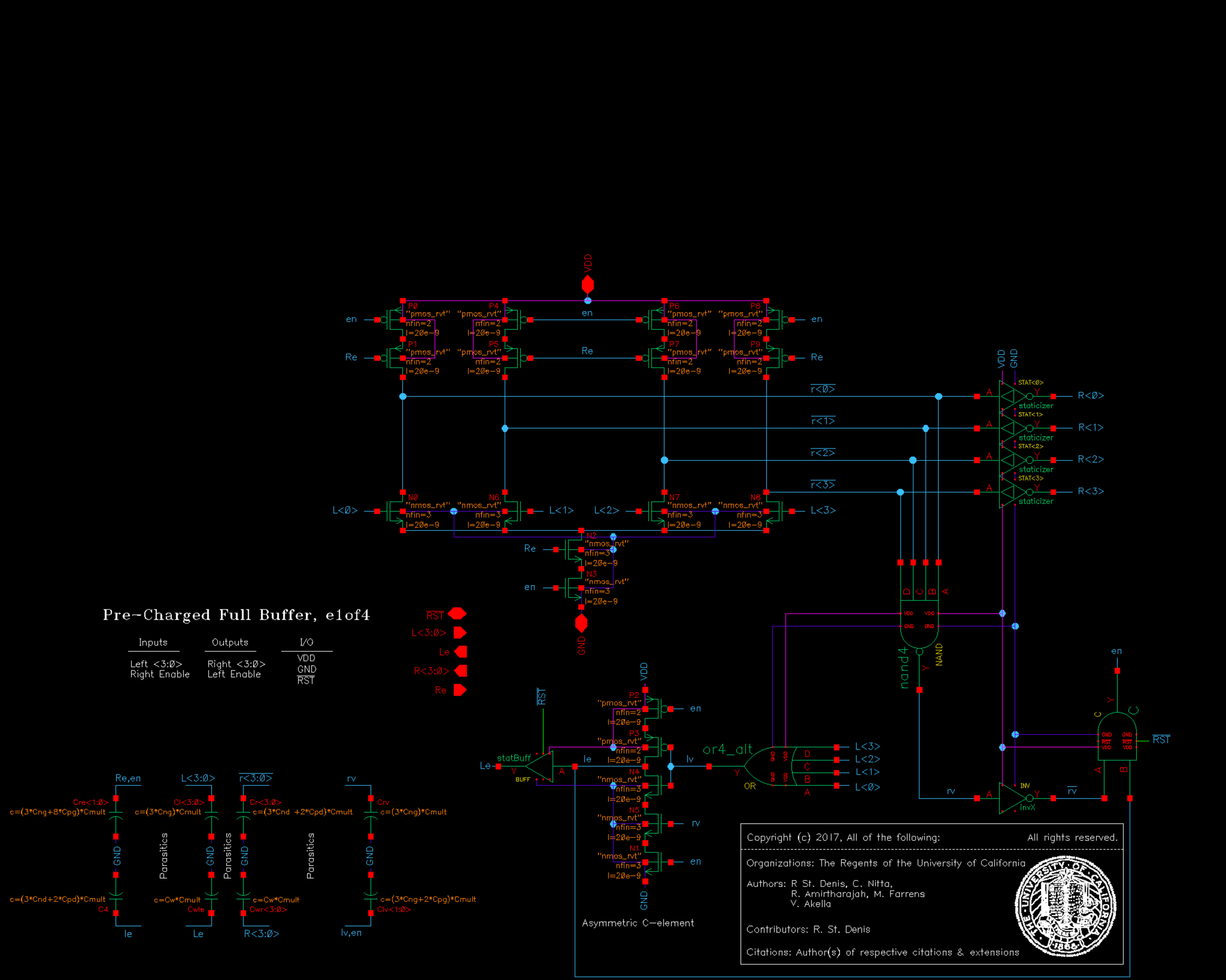

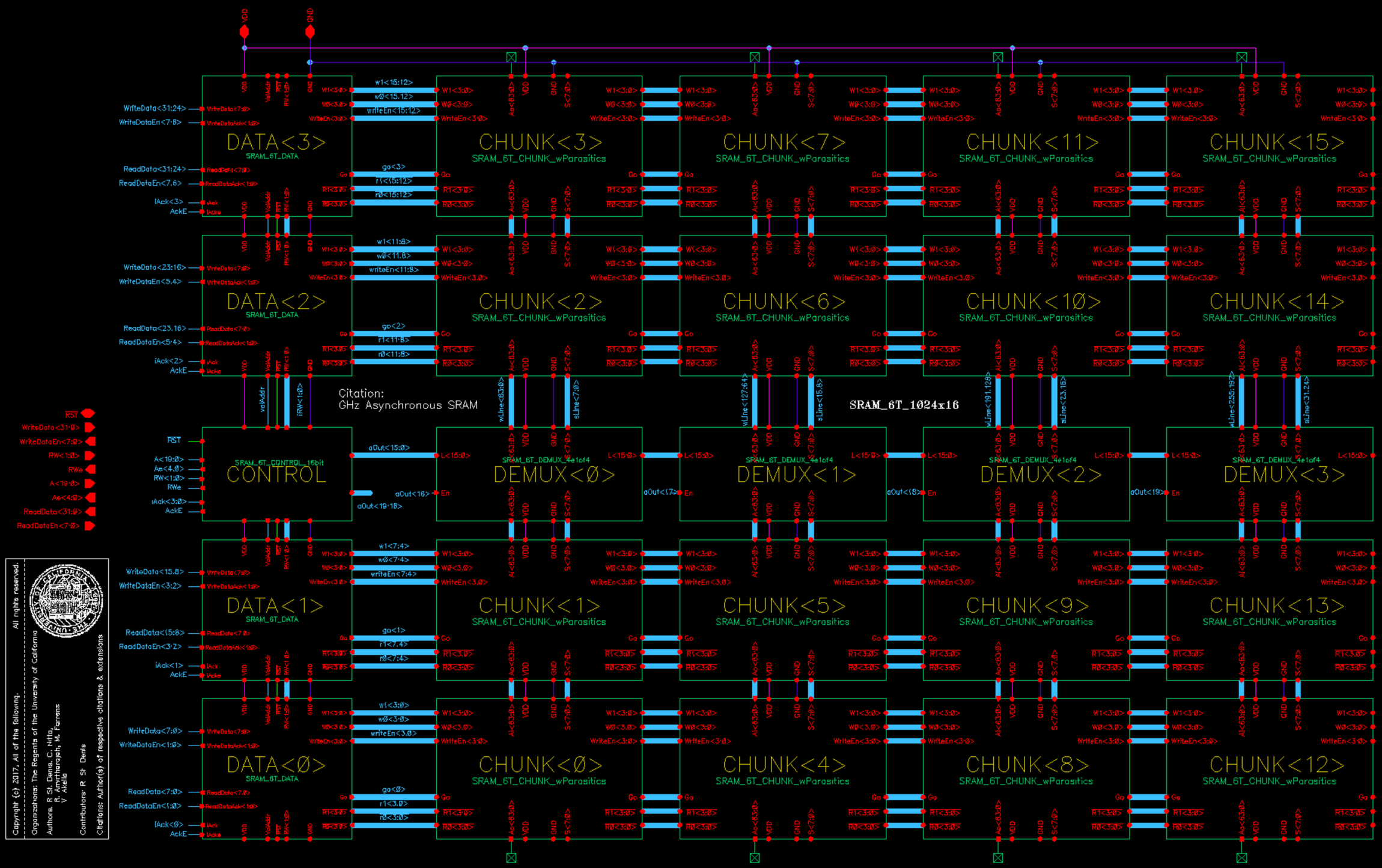
DATA<3>
SRAM_6T_DATA
CHUNK<3>
CHUNK<7>
CHUNK<11>
CHUNK<15>
SRAM_6T_CHUNK_wParasitics
DATA<2>
CHUNK<2>
CHUNK<6>
CHUNK<10>
CHUNK<14>
DATA<1>
CHUNK<1>
CHUNK<5>
CHUNK<9>
CHUNK<13>
DATA<0>
CHUNK<0>
CHUNK<4>
CHUNK<8>
CHUNK<12>
CONTROL
SRAM_6T_CONTROL_16bit
DEMUX<0>
DEMUX<1>
DEMUX<2>
DEMUX<3>
SRAM_6T_DEMUX_4e1of4
Citation:
GHz Asynchronous SRAM
SRAM_6T_1024x16
RST
WriteData<31:0>
WriteDataEn<7:0>
RW<1:0>
RWe
A<19:0>
Ae<4:0>
ReadData<31:0>
ReadDataEn<7:0>
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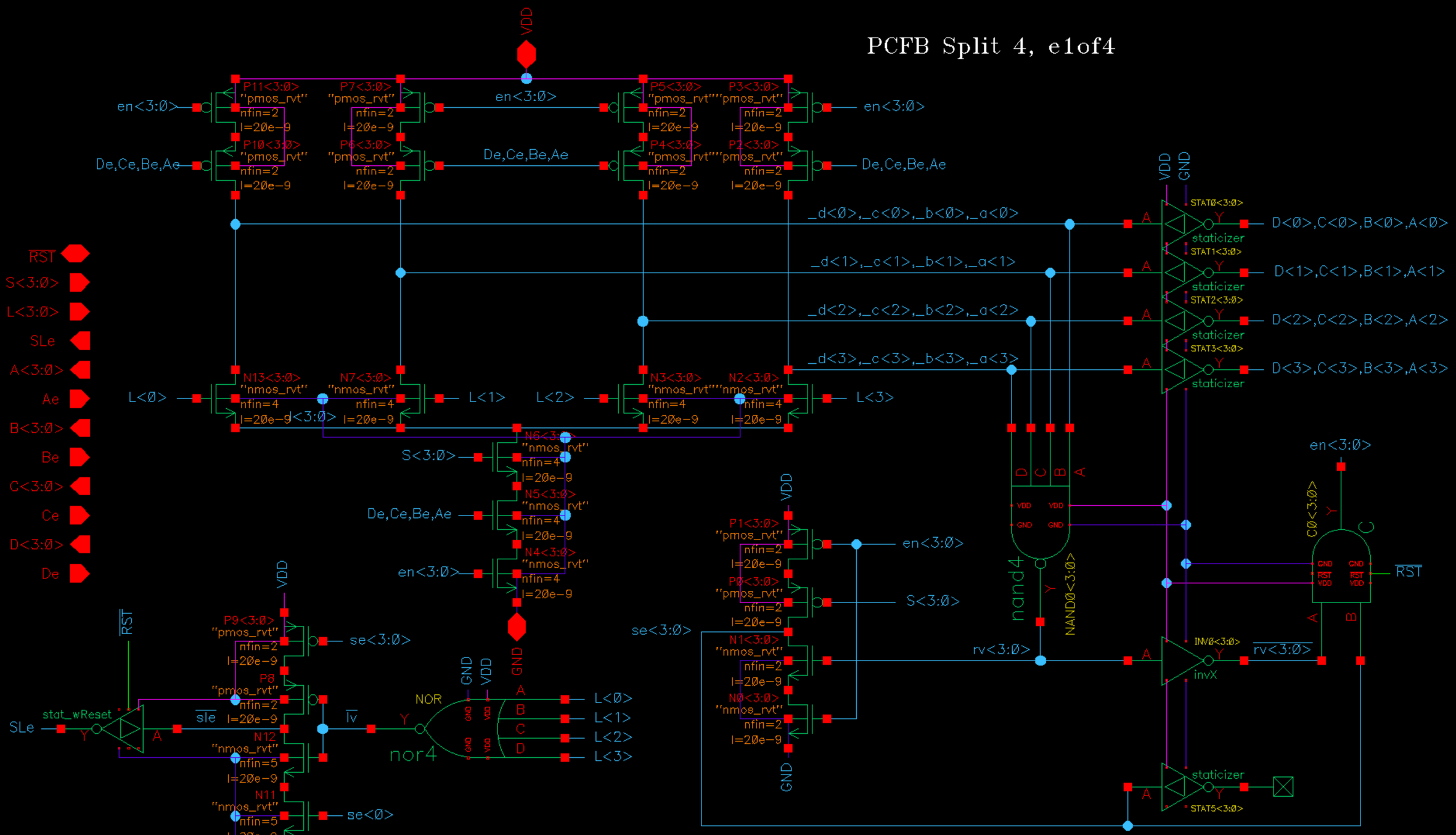
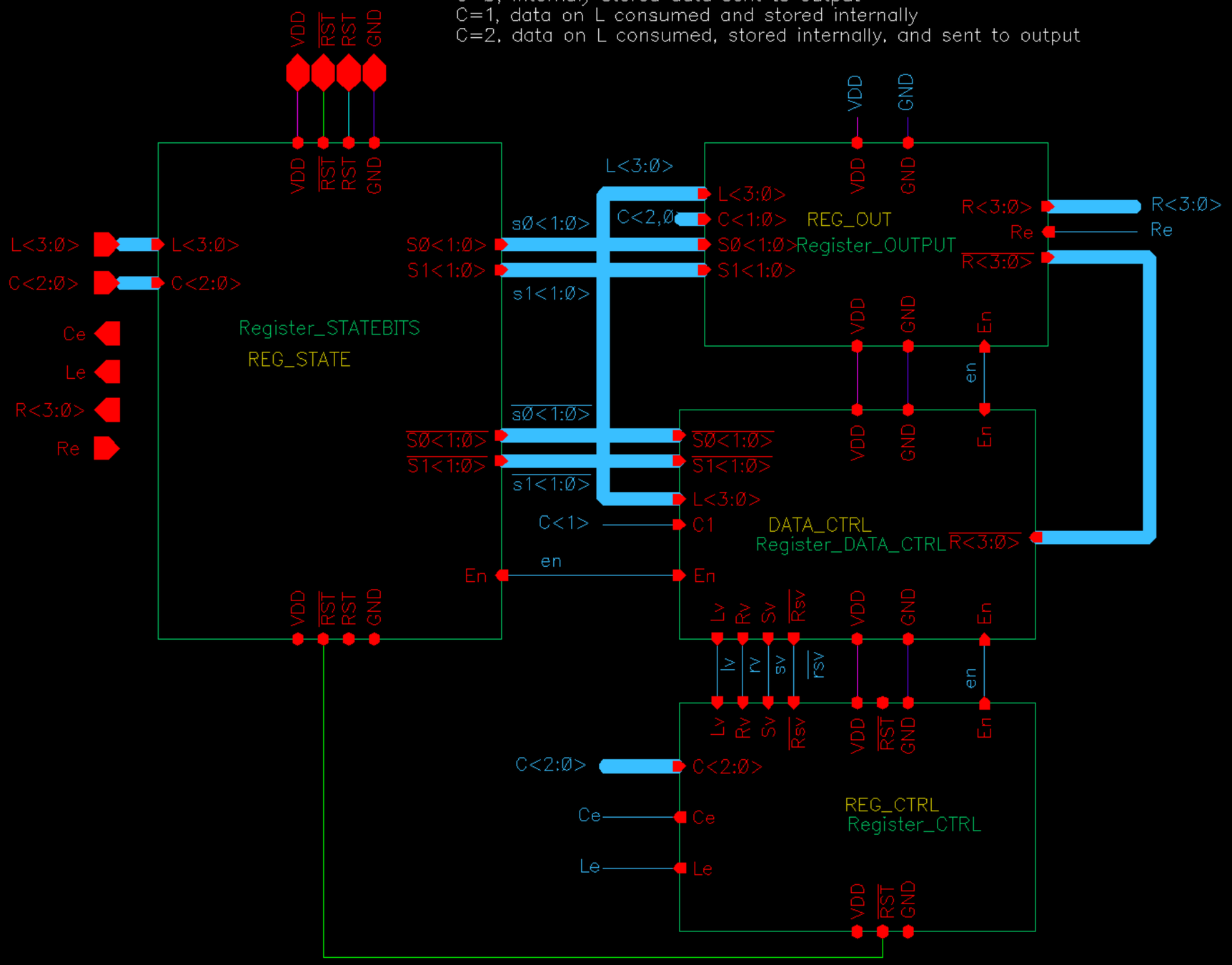
PCFB Split 4, e1of4

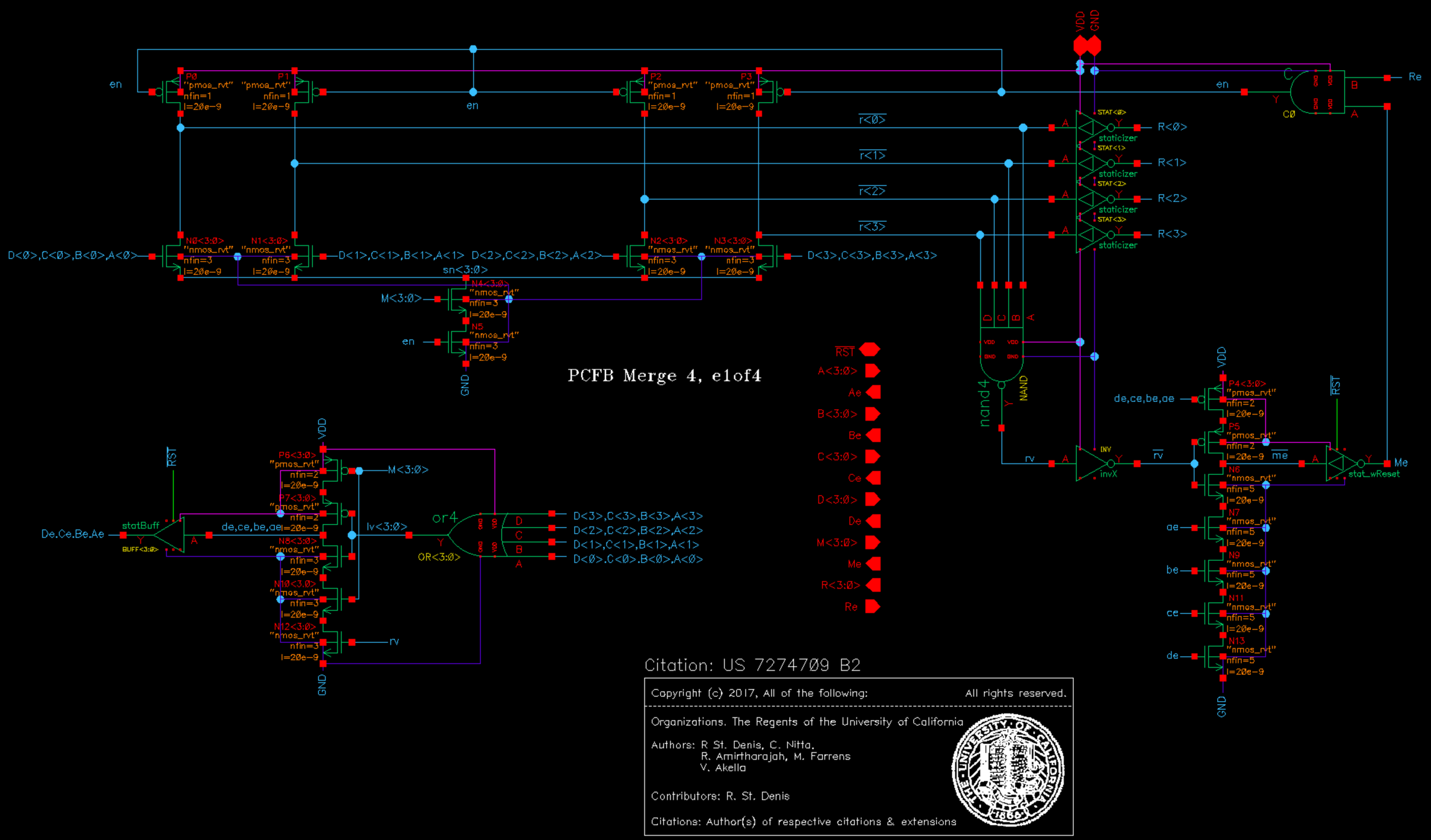


Citation: US 7274709 B2

Register_e1of4

C=Ø, internaly stored data sent to output
C=1, data on L consumed and stored internally
C=2, data on L consumed, stored internally, and sent to output





Citation: US 7274709 B2