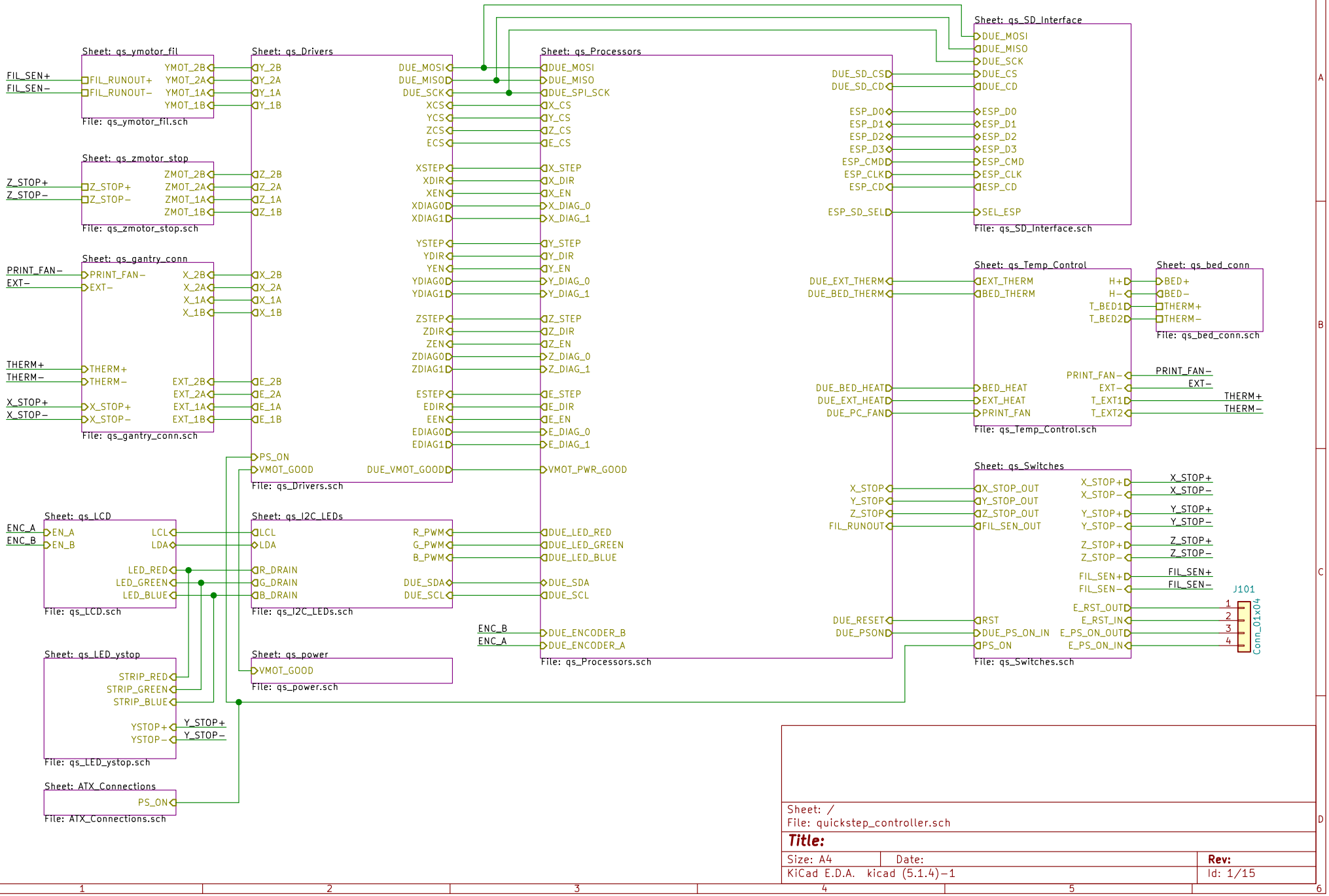
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File: qs_zmotor_stop.sch
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File: qs_gantry_conn.sch
Sheet: qs_Drivers
File: qs_Drivers.sch
Sheet: qs_Processors
File: qs_Processors.sch
Sheet: qs_SD_Interface
File: qs_SD_Interface.sch
Sheet: qs_Temp_Control
File: qs_Temp_Control.sch
Sheet: qs_bed_conn
File: qs_bed_conn.sch
Sheet: qs_Switches
File: qs_Switches.sch
Sheet: qs_LCD
File: qs_LCD.sch
Sheet: qs_I2C_LEDs
File: qs_I2C_LEDs.sch
Sheet: qs_LED_ystop
File: qs_LED_ystop.sch
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File: qs_power.sch
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File: ATX_Connections.sch
J101
Conn_01x04
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Rev:
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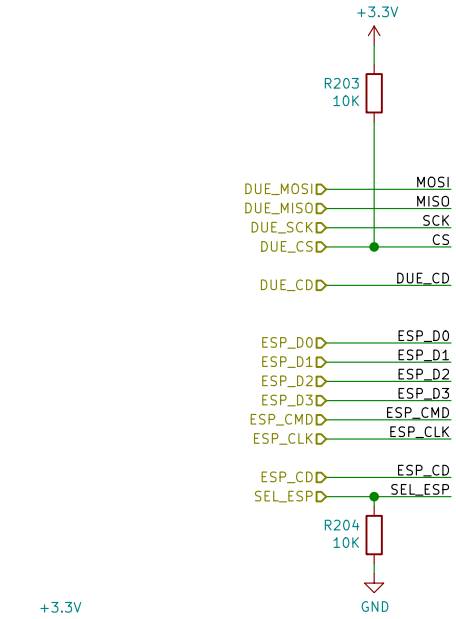
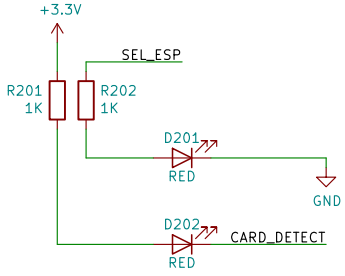
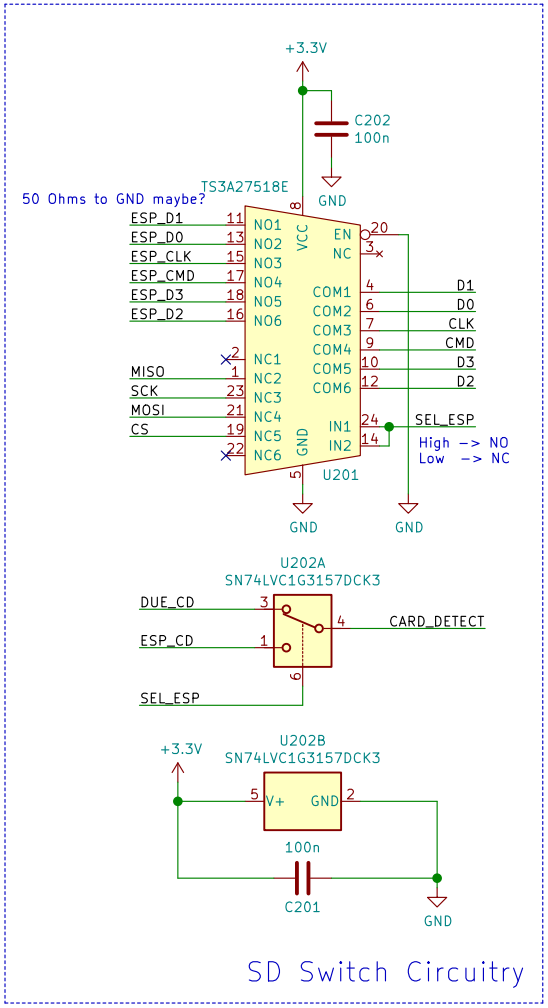
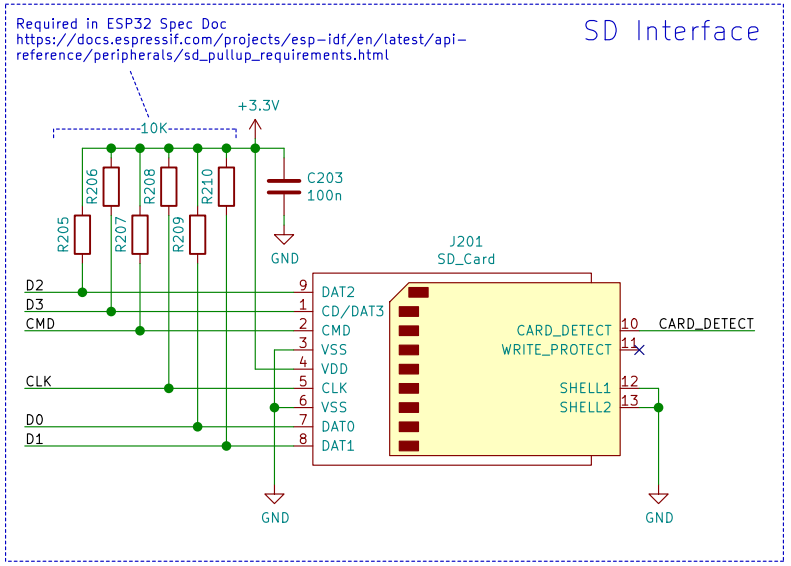
Id: 1/15









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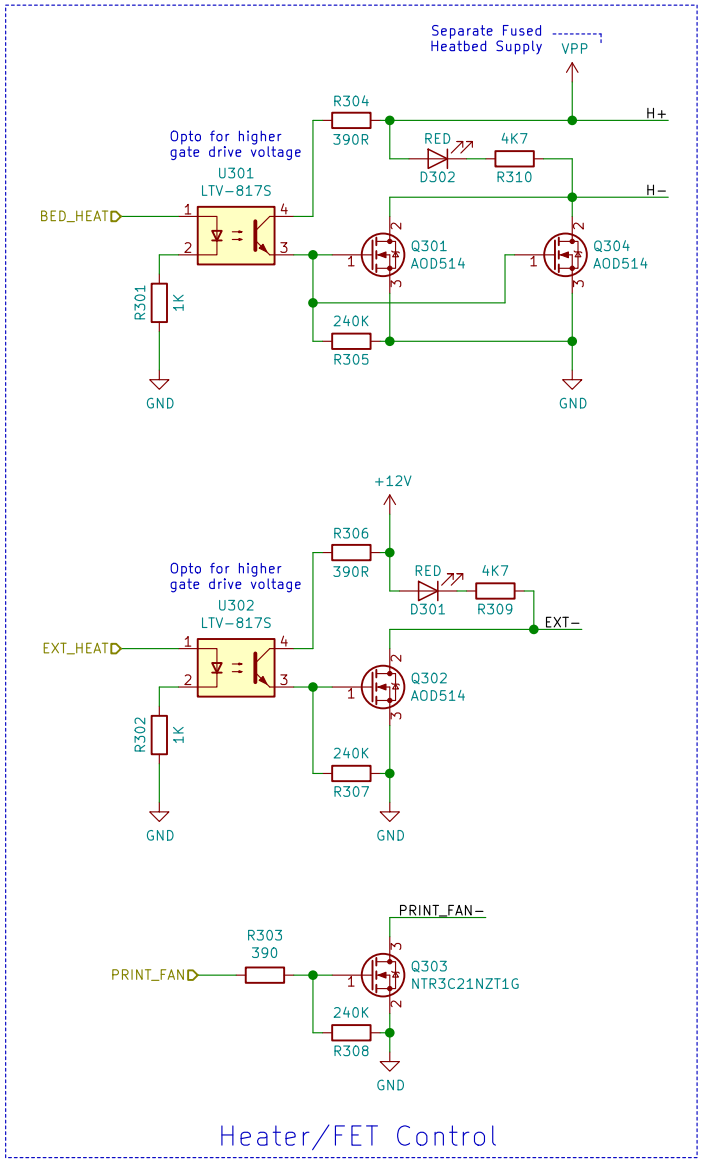

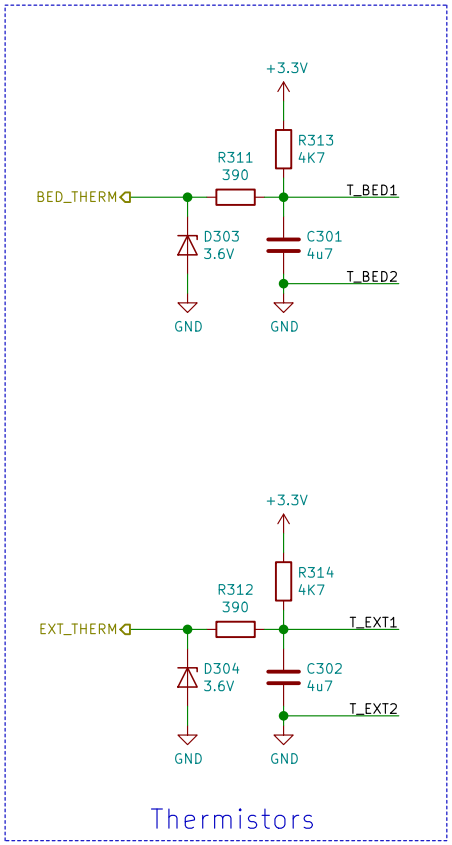

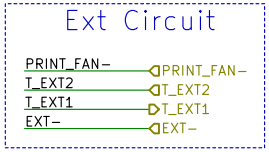

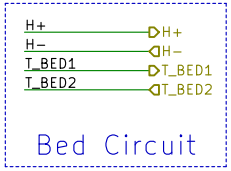

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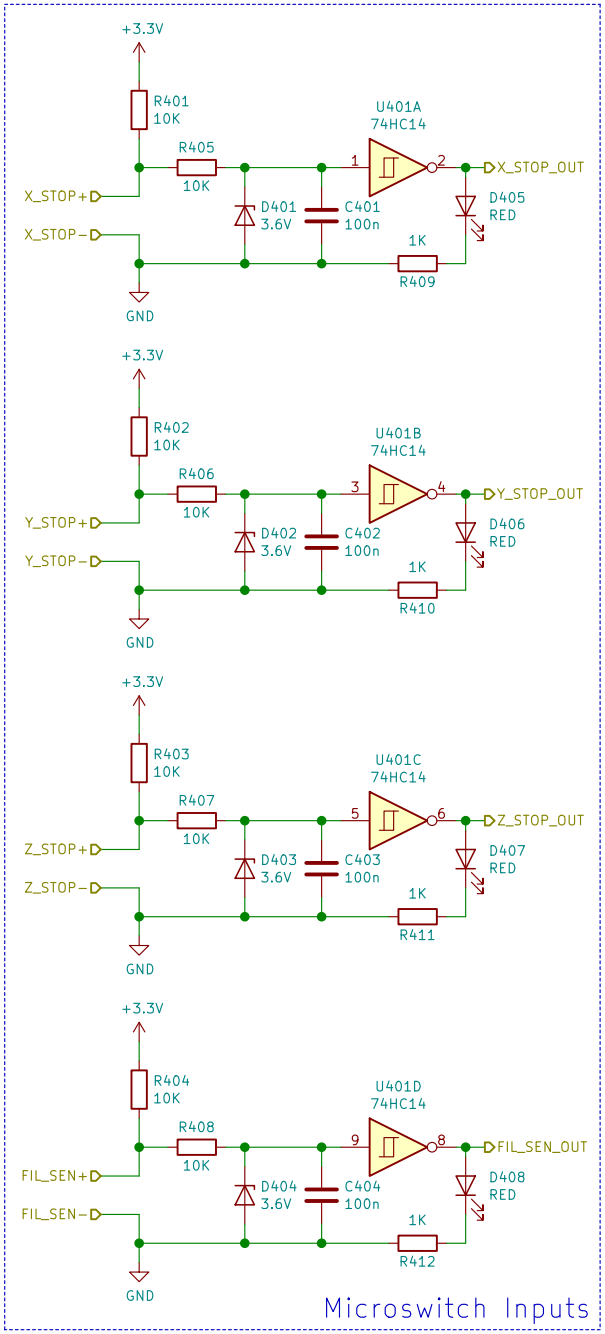

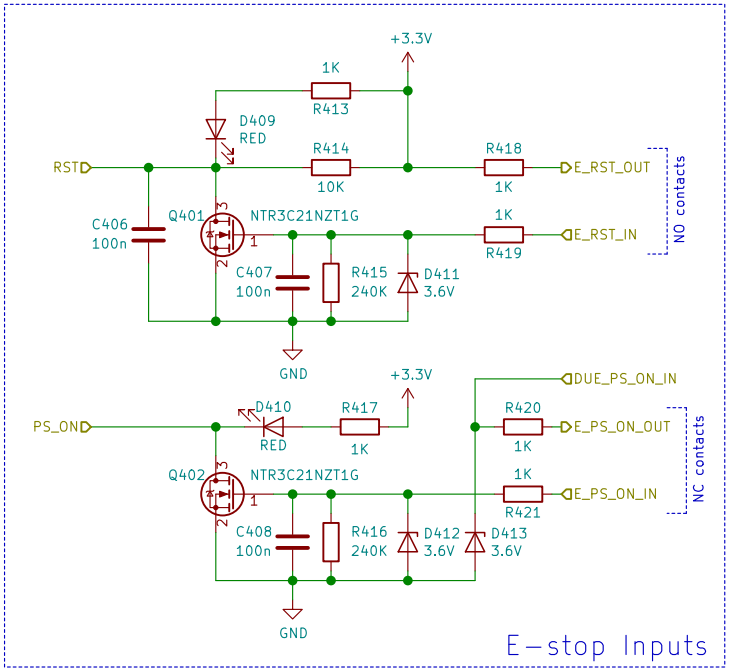

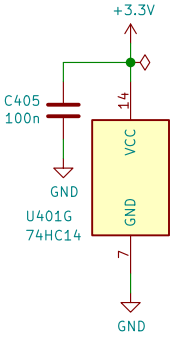

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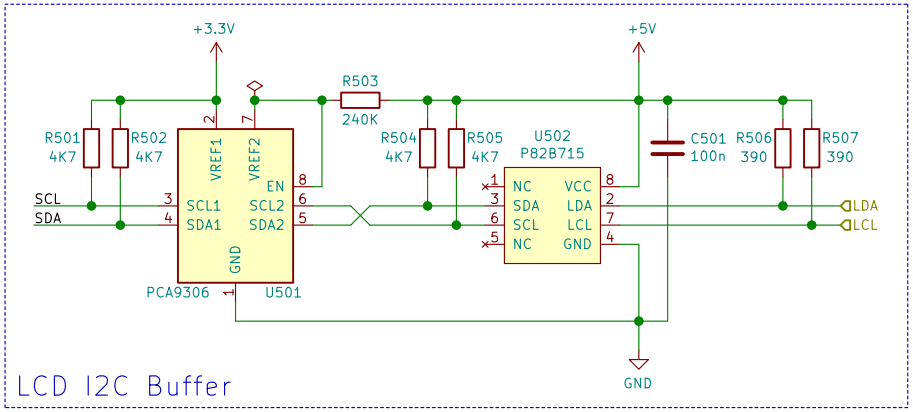

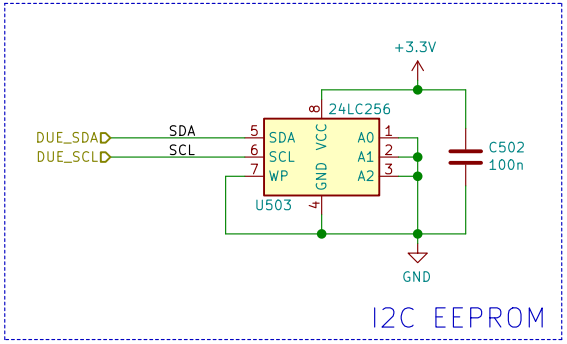

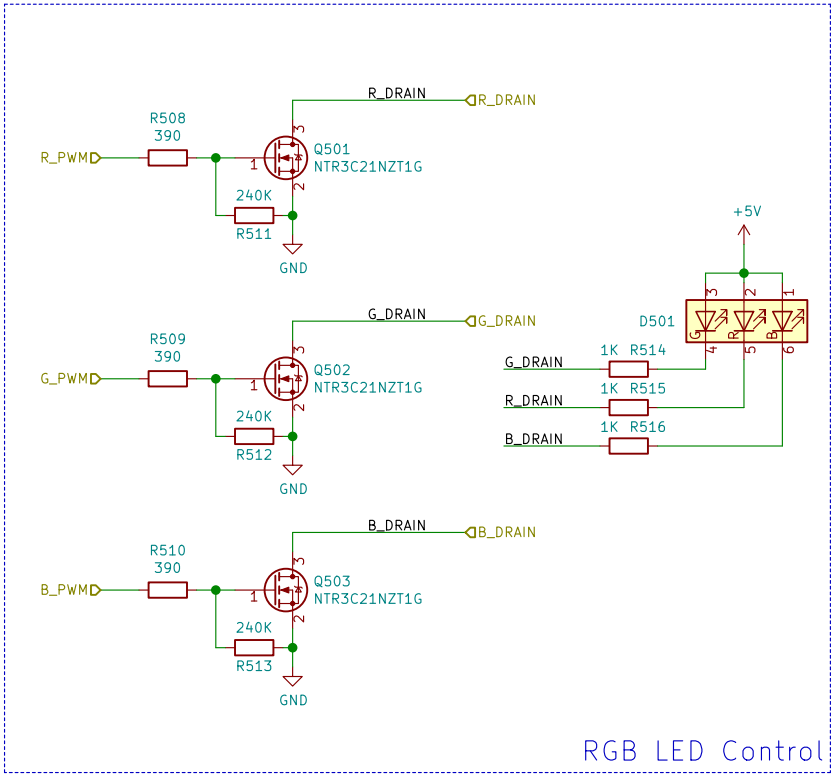

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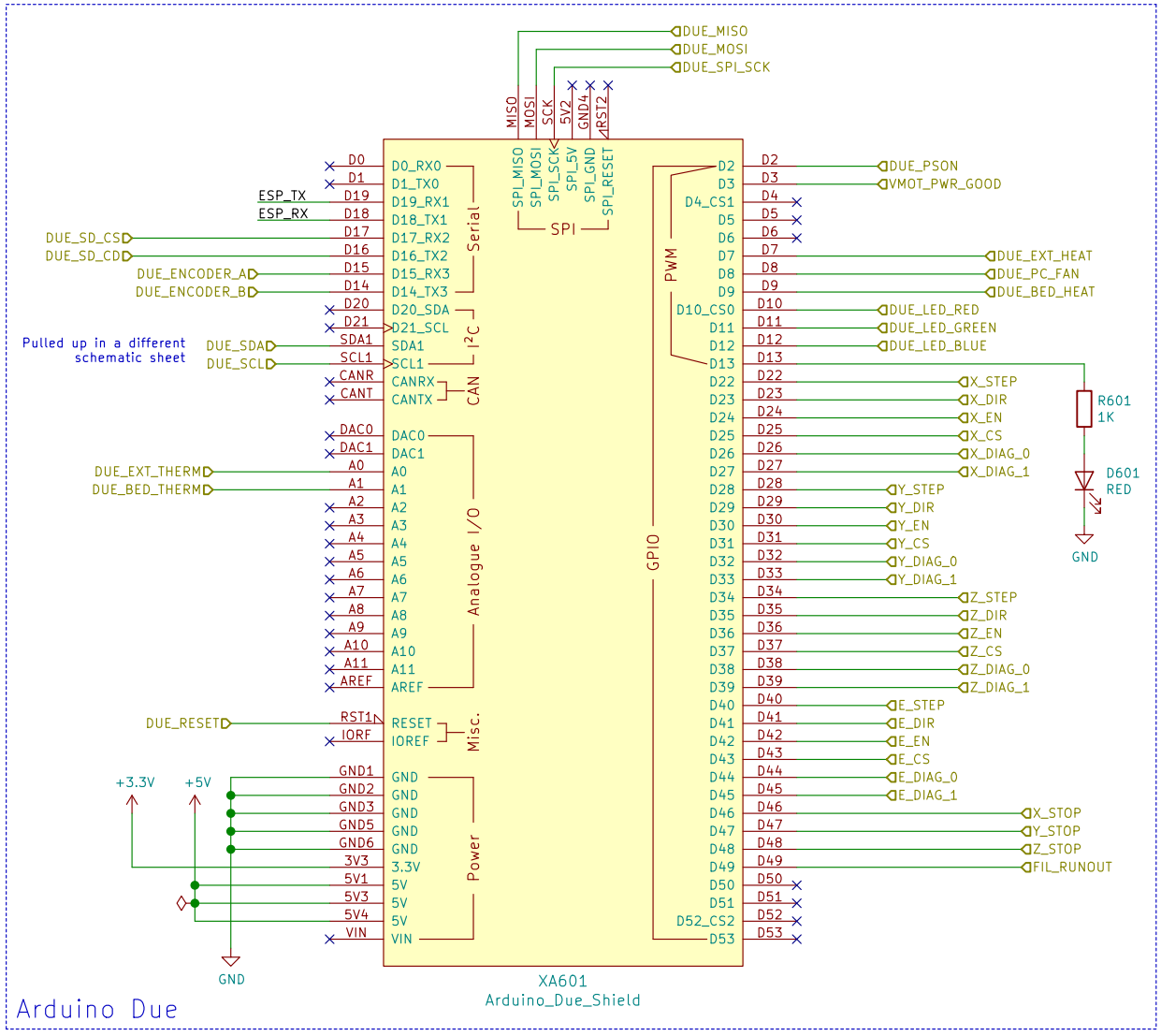

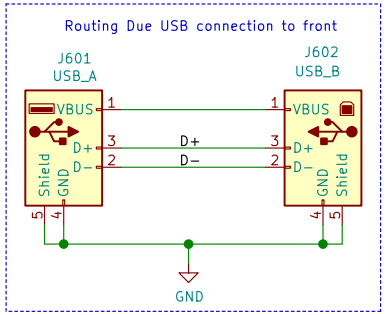

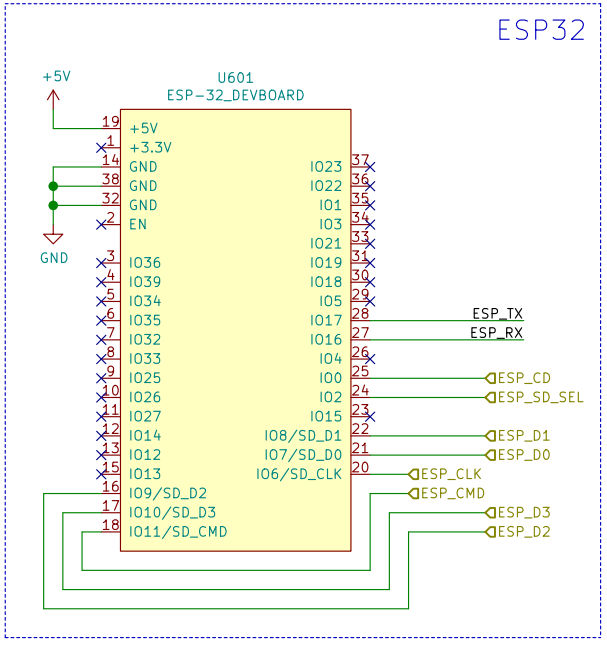

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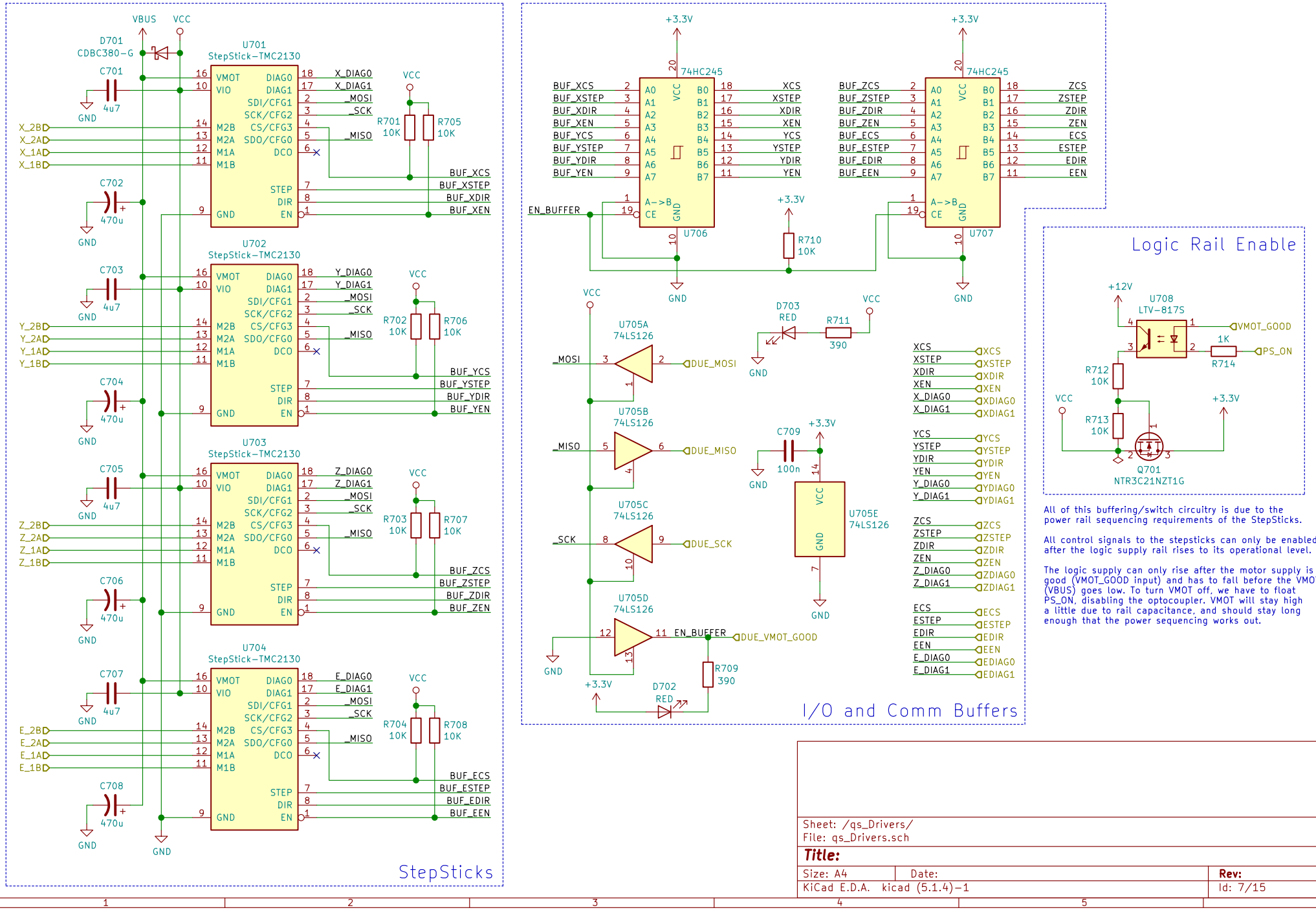
StepSticks
I/O and Comm Buffers
Logic Rail Enable
U701
StepStick–TMC2130
U702
StepStick–TMC2130
U703
StepStick–TMC2130
U704
StepStick–TMC2130
D701
CDBC380–G
VBUS
VCC
GND
C701
C702
C703
C704
C705
C706
C707
C708
4u7
470u
X_2B
X_2A
X_1A
X_1B
Y_2B
Y_2A
Y_1A
Y_1B
Z_2B
Z_2A
Z_1A
Z_1B
E_2B
E_2A
E_1A
E_1B
VMOT
VIO
M2B
M2A
M1A
M1B
DIAG0
DIAG1
SDI/CFG1
SCK/CFG2
CS/CFG3
SDO/CFG0
DCO
STEP
DIR
EN
X_DIAG0
X_DIAG1
_MOSI
_SCK
_MISO
Y_DIAG0
Y_DIAG1
Z_DIAG0
Z_DIAG1
E_DIAG0
E_DIAG1
R701
R702
R703
R704
R705
R706
R707
R708
10K
BUF_XCS
BUF_XSTEP
BUF_XDIR
BUF_XEN
BUF_YCS
BUF_YSTEP
BUF_YDIR
BUF_YEN
BUF_ZCS
BUF_ZSTEP
BUF_ZDIR
BUF_ZEN
BUF_ECS
BUF_ESTEP
BUF_EDIR
BUF_EEN
+3.3V
74HC245
U706
U707
A–>B
CE
A0
A1
A2
A3
A4
A5
A6
A7
B0
B1
B2
B3
B4
B5
B6
B7
XCS
XSTEP
XDIR
XEN
YCS
YSTEP
YDIR
YEN
ZCS
ZSTEP
ZDIR
ZEN
ECS
ESTEP
EDIR
EEN
EN_BUFFER
R710
10K
U705A
U705B
U705C
U705D
U705E
74LS126
_MOSI
_MISO
_SCK
DUE_MOSI
DUE_MISO
DUE_SCK
EN_BUFFER
DUE_VMOT_GOOD
D702
RED
R709
390
D703
R711
C709
100n
XDIAG0
XDIAG1
YDIAG0
YDIAG1
ZDIAG0
ZDIAG1
EDIAG0
EDIAG1
+12V
U708
LTV–817S
VMOT_GOOD
PS_ON
1K
R714
R712
10K
R713
Q701
NTR3C21NZT1G
All of this buffering/switch circuitry is due to the power rail sequencing requirements of the StepSticks.
All control signals to the stepsticks can only be enabled after the logic supply rail rises to its operational level.
The logic supply can only rise after the motor supply is good (VMOT_GOOD input) and has to fall before the VMOT (VBUS) goes low. To turn VMOT off, we have to float PS_ON, disabling the optocoupler. VMOT will stay high a little due to rail capacitance, and should stay long enough that the power sequencing works out.
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Size: A4
Date:
Rev:
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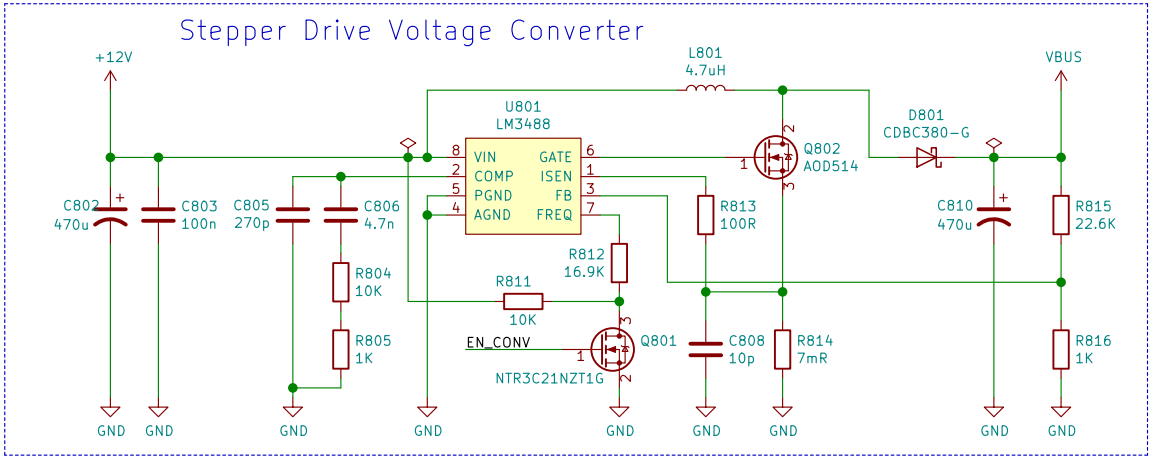
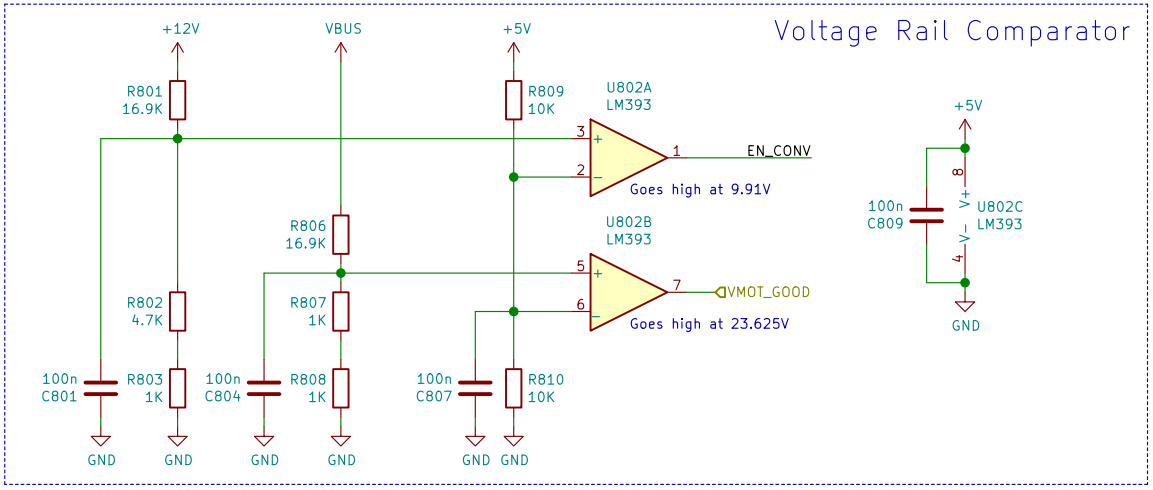
Id: 7/15





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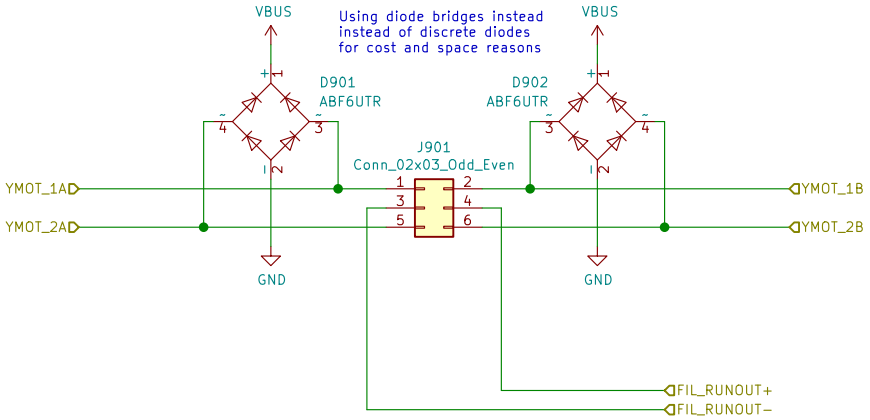

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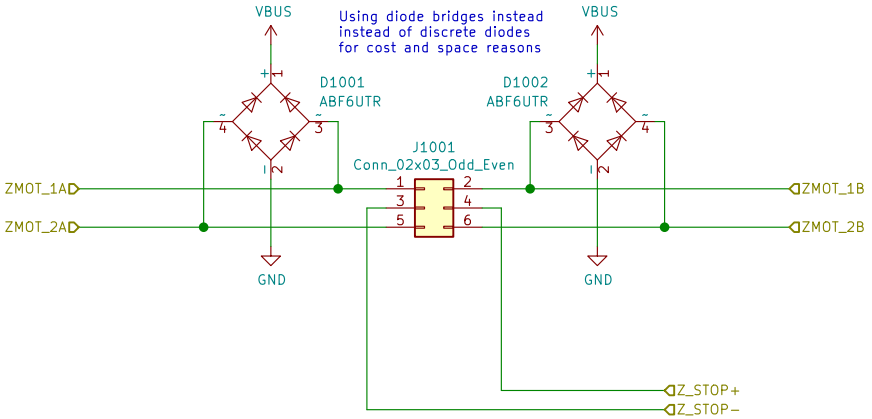

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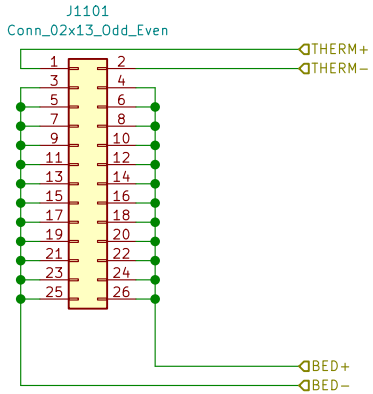

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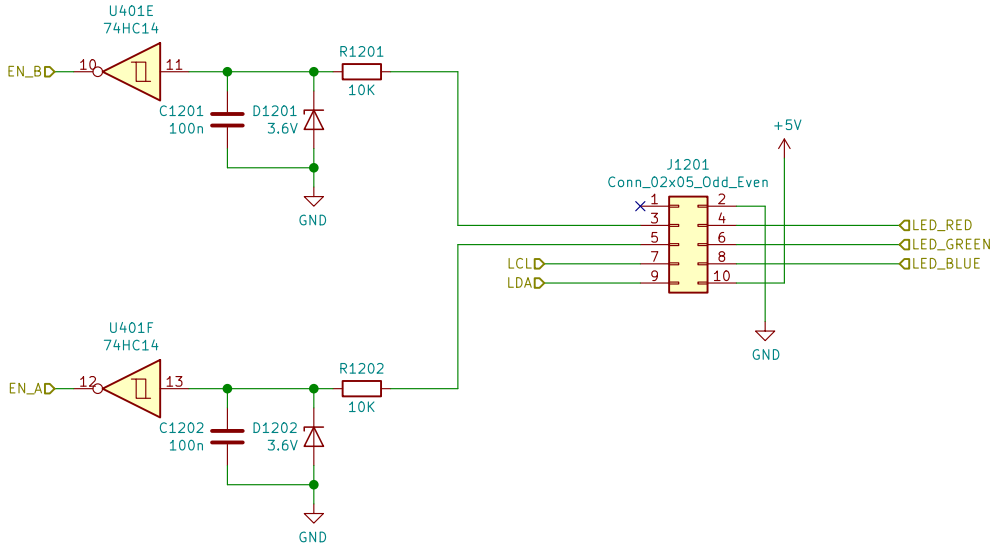

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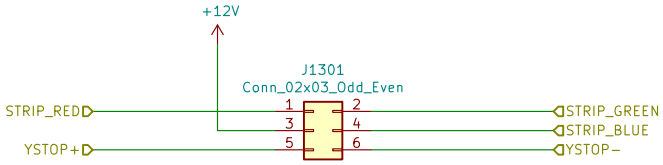

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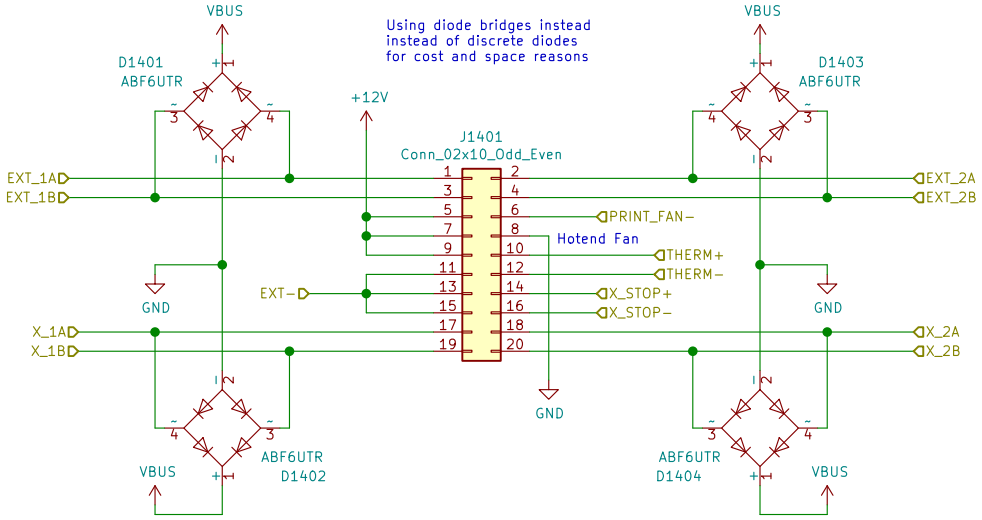

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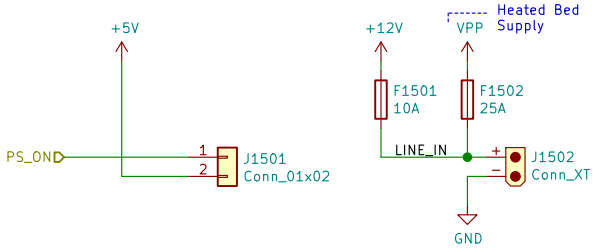

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