IMPLEMENTATION OF XILINX BASED ELECTRONIC VOTING MACHINE USING FPGA

A PROJECT REPORT

Submitted by,

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BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING.

Under the guidance of

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING,
RAJIV GANDHI UNIVERSITY OF KNOWLEDGE TECHNOLOGIES,
RK VALLEY, KADAPA (DIST.), ANDHRA PRADESH, PINCODE – 516330.

SEPTEMBER– 2022.

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in the partial fulfilment for the award of the degree of

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CERTIFICATE

This is to certify that this dissertation work entitled as ***" IMPLEMENTATION OF XILINX BASED ELECTRONIC VOTING MACHINE USING FPGA "*** *i.e., on Zedboard was successfully carried out by* ***V.HIMABINDHU(R170673),P.SHASHIKALA*** **(R170638) & S.GOWSIYA TAJ (R170640)** *in partial fulfilment of the requirements leading to the award of the degree of Bachelor of Technology in the* the *Department of* ***ELECTRONICS AND COMMUNICATION ENGINEERING*** *by* ***RAJIV GANDHI UNIVERSITY OF KNOWLEDGE TECHNOLOGIES , RK VALLEY.*** *This is a bonafide record of the work and investigations carried out under supervision and guidance , during the academic year of 2021 - 2022.*

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DECLARATION

I hereby declare that the work which is being presented in this project which is entitled as ***" IMPLEMENTATION OF XILINX BASED ELECTRONIC VOTING MACHINE USING FPGA "*** *submitted to* ***RAJIV GANDHI UNIVERSITY OF KNOWLEDGE TECHNOLOGIES, RK VALLEY*** *in the partial fulfilment of the requirements for the award of the degree of* ***BACHELOR OF TECHNOLOGY*** *in* ***ELECTRONICS AND COMMUNICATION ENGINEERING.*** *This is an authentic record of our own work carried out under the supervision of* ***Mr. K ABDUL MUNAF , Assistant Professor*** *in the* ***Department of Electronics and Communication Engineering , RGUKT, RK Valley****.*

The matter embodied in this project report has not been submitted by us for the award of any other degree. Whenever we have used materials (data, theoretical analysis, figures and text) from other sources, we have given due credit to them by citing them in the text of the report and giving their details in the references. Further, we have taken permission from the copyright owners of the sources, whenever necessary.

Date : March 2,2022
Place : RK VALLEY

By , V.HIMABINDHU (R170673)
P.SHASHIKALA (R170638)
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Finally, we express our thanks to our parents and our friends and well-wishers for their timely suggestions and encouragement. Without their presence we would not have achieved anything in our life.

Above all, it is true that the grace and blessing of God the Almighty that made this endeavour a success.

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ABSTRACT :

Electronic Voting Machine is a simple electronic device used to record votes automatically without the need of manual operation of ballot papers. Fundamental right to vote forms the basis of any Democracy. In all earlier elections, voters casted their votes to their favourite candidates by putting the stamp against his/her name. This is a long time consuming process and is prone to errors and can at times be an unfair process.

To overcome all these difficulties and make the electoral process a fair one, implementation of electronic voting machines in the digital domain is presented in our project. It is difficult to tamper votes in the digital domain and provides a secure and safe method for conducting elections.

Polling by Electronic Voting Machine (EVM) is an easy, safe and secure methodology that takes minimum of our time .In order to perform this mechanism, there were several phases in the design process such as designing a flow chart, algorithm and simultaneously the code is developed to implement & stimulate the logic.

The proposed digital EVM was designed on Xilinx ISE using verilog HDL and can also be implemented on an FPGA board i.e., on Zedboard zynq - 7000 for real time purposes. The proposed method consists of 3 stages, in the first stage we decide the total no.of voters and the total number of contestants taking part in the election process .We have assigned Voting enable which is active high input signal for the voter in order to cast his vote by using voter switch input signal for making this election process more secure and safe.

In stage two, the voting process begins when the voter casts his vote to a particular party or contestants the polled vote is registered in the individual contestant registry. In stage three after completion of the voting process the votes are validated by comparing the votes polled to the contestants in their registries after which the election process ends by declaring the winner. The above proposed method can be implemented on FPGA board for real time applications ranging from university level elections to Assembly and LokSabha elections, as it has the advantage that it can be reprogrammed over and over for various tasks according to their requirement which helps in reducing the expenditure.

INTRODUCTION:

Voting is the sole criteria for choosing their representatives by people in any democracy. So, this entire process should be done with utmost care so that only a fair and deserving candidate is selected that is solely based on public opinion. In earlier days, elections were conducted using a ballot paper system whereby people casted their votes to their favourite candidate, merely, by putting stamp against his/her name but this method often suffered from various flaws such as stealing of votes and unfair results . To overcome all these discrepancies, an electronic voting machine was designed. But the design of a simple electronic voting machine with a removable memory card was not enough as access to the memory card for even a minute can tamper all the votes with some other malicious code. So we needed a system which could provide some better way of implementing the Electronic Voting Machine.

Since we all know that it is very difficult to manipulate signals, we have designed an electronic voting machine in VHDL/VERILOG using XILINX ISE as a platform which can be implemented on FPGA (Field Programmable Gate Array) hardware using ZedBoard zynq - 7000 Development kit. Since FPGAs have in-built RAM and each vote requires only one bit of memory, this implementation is quite memory and cost efficient. Further, this implementation also contains a password which itself is digital in nature and is very difficult to be hacked.

ELECTRONIC VOTING MACHINE SCHEMATIC :

The fig.1 shows the Schematic of the proposed Electronic Voting Machine with input and output signals.

The block diagram consists of clock , reset , mode , button1 (Candidate 1) , button2 (Candidate 2) , button3 (Candidate 3) , button4 (Candidate 4) as input signals and Output LEDs as output signals . The valid_vote_1 , valid_vote_2 , valid_vote_3 , valid_vote_4 , cand1_vote_recvd , cand2_vote_recvd , cand3_vote_recvd , cand4_vote_recvd and anyValidVote are the intermediate signals which are used to enable the corresponding LEDs . Here these intermediate signals are not displayed.

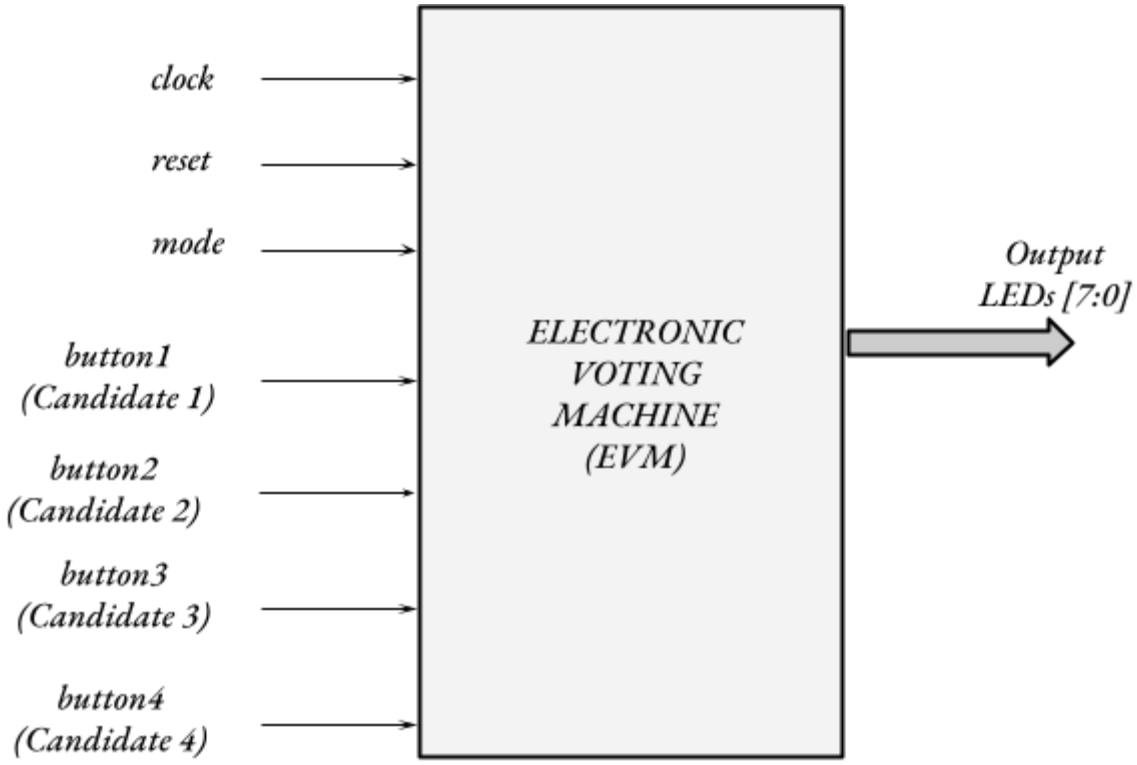


FIG 1 : EVM SCHEMATIC

DESCRIPTION OF SIGNALS USED IN IMPLEMENTATION :

The Description of various signals those are used in implementation of Electronic Voting Machine are :

SL.No :	***Signal :***	***Signal Type :***	***Description :***
1.	*clock*	*Input*	*This signal is used to cast the vote. Vote will be casted on positive or negative edge of clock depending on priority of programmer. The clock will last for a particular period of time in which the voter has to cast his/her vote. Basically the clock frequency used is 100 MHz.*

2.	*reset*	*Input*	*It is a Active High signal to reset all the data present in the intermediate signal register.For Normal operation of EVM reset is 0 (Active Low Input Signal).*
3.	*mode*	*Input*	*Mode signal is used to switch from voting mode to result mode. If mode = 0 , i.e., in Voting mode and mode = 1, i.e., in Result mode.*
4.	*button1 (candidate 1)*	*Input*	*To vote for candidate 1 , we need to press the button1 until all leds blinks. For voting to candidate2 , 3 and 4 the procedure is the same.*
5.	*leds[7:0]*	*Output*	*To display the no.of votes casted for each candidate and to display the vote is successfully casted for a respective candidate by blinking all leds at once.*
6.	*valid_vote_1*	*Intermediate*	*valid_vote_1 is 1 if successful vote is cast for candidate 1 and cand1_vote_recvd is incremented by 1. For valid_vote_2 , 3 and 4 the similar procedure is followed.*
7.	*cand1_vote_recvd*	*Intermediate*	*cand1_vote_recvd acts like a register that stores count values of candidate 1 received votes. For cand2_vote_recvd , cand3_vote_recvd and cand4_vote_recvd follows a similar procedure.*
8.	*anyValidVote*	*Intermediate*	*anyValidVote is an active high signal that is high if any valid_vote_1 is high.*

TABLE 1 : DESCRIPTION OF SIGNALS USED IN IMPLEMENTATION

FLOW CHART OF ELECTRONIC VOTING MACHINE :

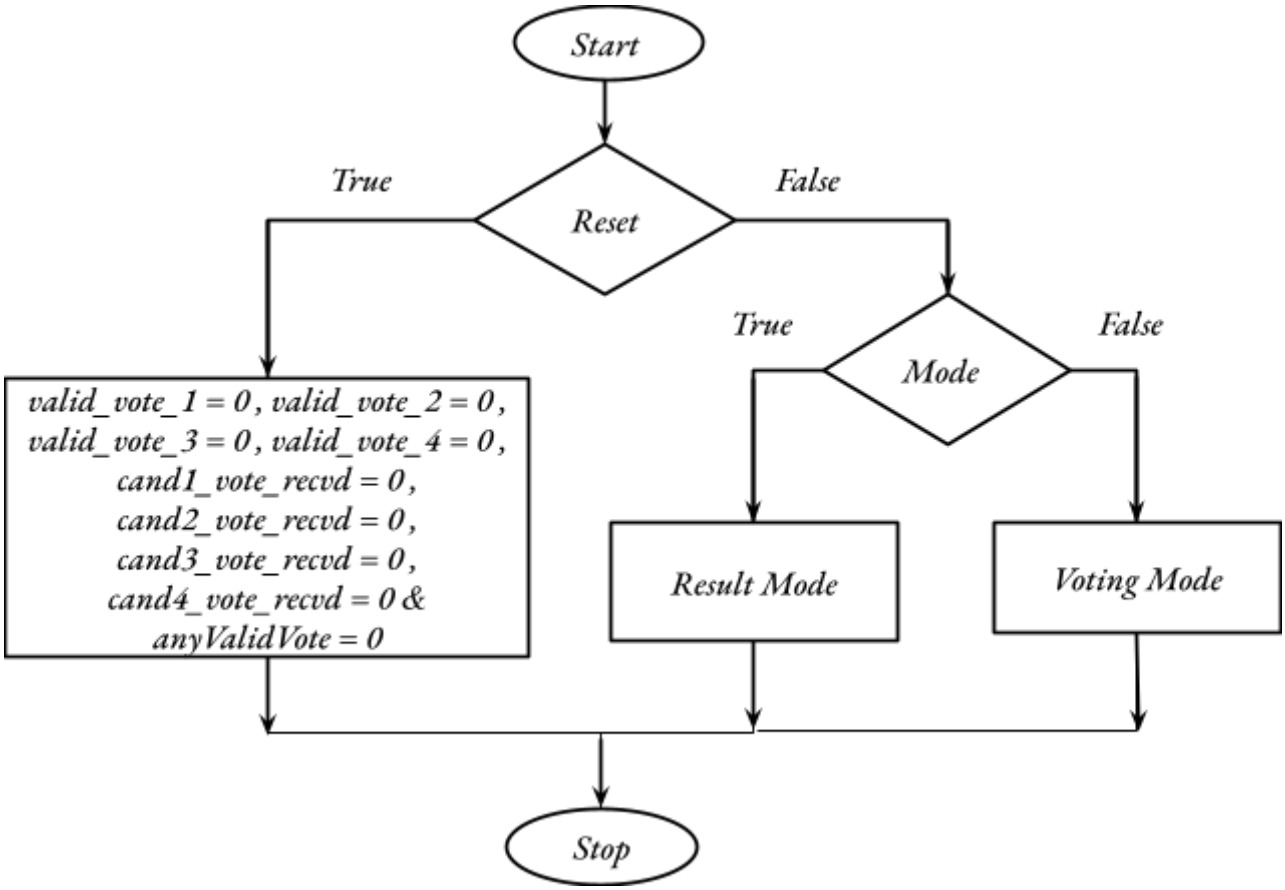


FIG 2 : FLOW CHART OF ELECTRONIC VOTING MACHINE

WORKING :

The flow chart depicts the working flow of the Electronic Voting Machine . When we dump our code into zedboard zynq - 7000 . If reset is active high then all intermediate signals and registers are forced to be 0 , for normal operation of Electronic Voting Machine the reset pin must be active low.

Mode is a signal which facilitates the Electronic Voting Machine working in Result Mode and Voting Mode. If mode is active high signal then the Electronic Voting Machine is in Result Mode , it refers to displaying of result i.e., no.of votes that each candidate received. If mode is active low signal then the Electronic Voting Machine is in Voting Mode , it refers to voting to a particular candidate by using the push buttons.

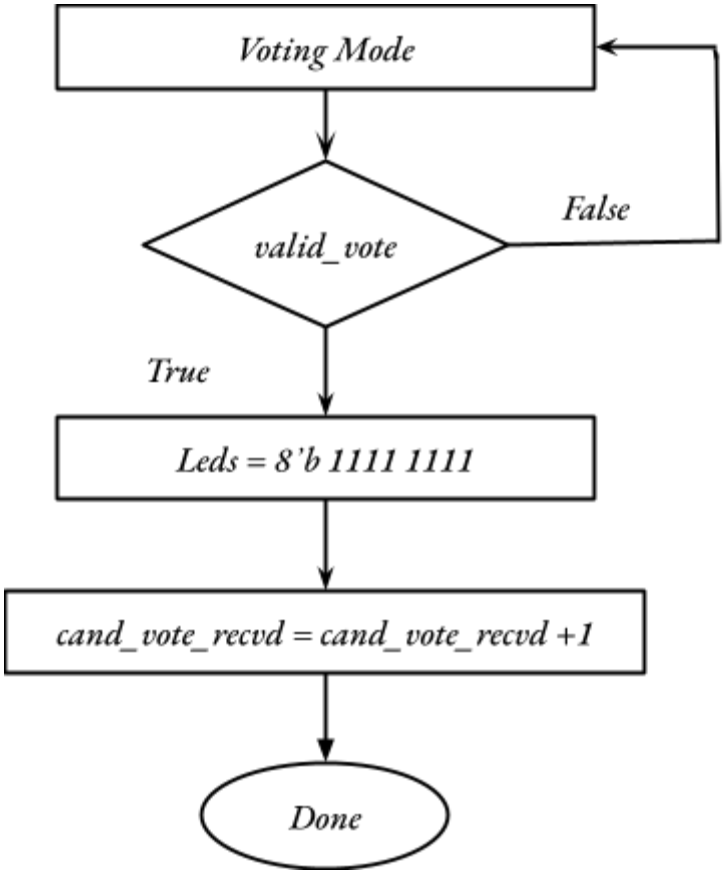
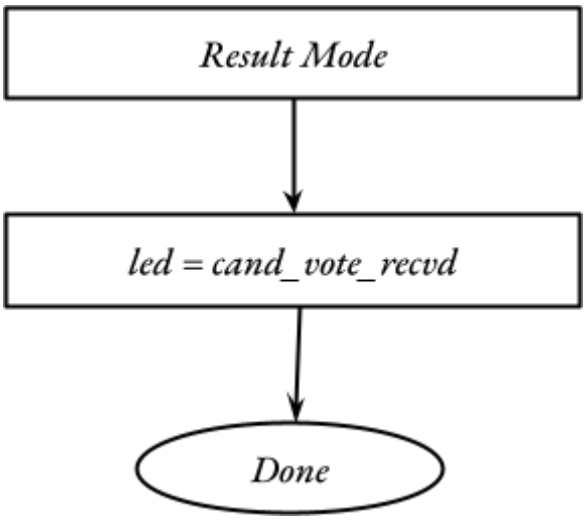


FIG 3 : FLOW OF VOTING MODE

During Voting Mode , if valid_vode is active high then the all leds blinks and cand_vote_recvd is incremented by 1. Blink of leds depicts the vote is successfully casted for the respective candidate.



During Result Mode , the data present in the cand_vote_recvd register is fed to the output leds. Basically the cand_vote_recvd stores the count of votes for a respective candidate.

FIG 4 : FLOW OF RESULT MODE

ABOUT ZEDBOARD ZYNQ - 7000 :

The ZYBO (ZYnq BOard) is a feature-rich, ready-to-use, entry-level embedded software and digital circuit development platform built around the smallest member of the Xilinx Zynq-7000 family, the Z-7010.

ZedBoard™ is a low-cost development board for the Xilinx Zynq - 7000 All Programmable SoC. This board contains everything necessary to create a Linux, Android, Windows or other OS/RTOS-based design. Additionally, several expansion connectors expose the processing system and programmable logic I/Os for easy user access. Take advantage of the Zynq-7000 AP SoC's tightly coupled ARM processing system and 7 series programmable logic to create unique and powerful designs with ZedBoard.

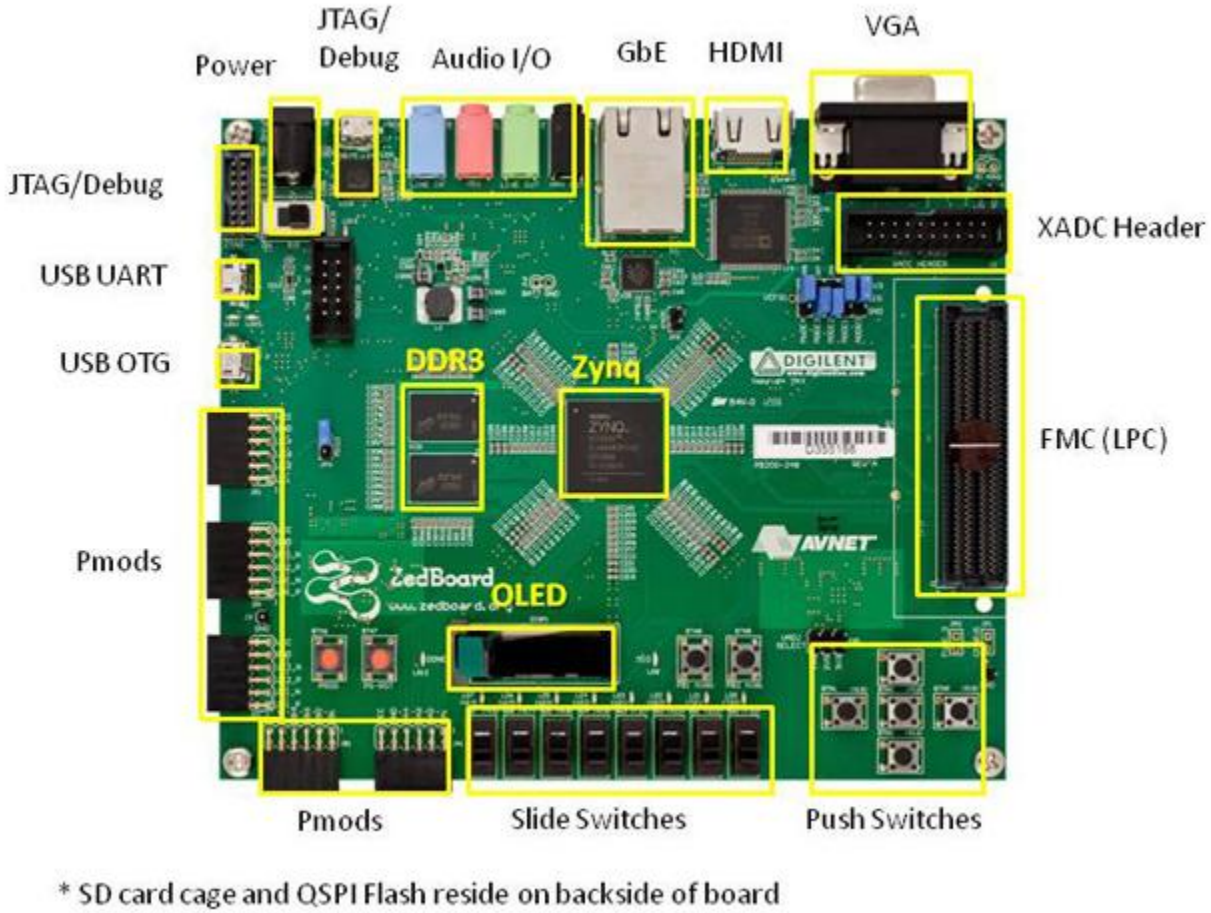


FIG 5 : ZEDBOARD ZYNQ - 7000

ZEDBOARD FEATURES :

- *Zynq - 7000 All Programmable SoC XC7Z020-CLG484-1*
- *Memory*
  - *512 MB DDR3 (Double Data Rate 3)*
  - *256 Mb Quad*
  - *SPI Flash (Serial Peripheral Interface Flash)*
- *4 GB SD card - Onboard USB-JTAG Programming*
- *10/100/1000 Ethernet*
- *USB OTG 2.0 and USB-UART*
- *PS & PL I/O expansion*
- *FMC, Pmod Compatible, XADC*
- *Multiple displays (1080p HDMI, 8-bit VGA, 128 x 32 OLED)*
- *I2S Audio CODEC (coder/decoder)*

ZEDBOARD APPLICATIONS :

- *Video processing*
- *Motor control*
- *Software acceleration*
- *Linux/Android/RTOS development*
- *Embedded ARM processing*
- *General Zynq - 7000 All Programmable SoC prototyping*
- *Applications related to LEDs and Switches etc....*

- *SD : Secure Digital Memory Card*
- *USB : Universal Serial Bus*
- *UART : Universal Asynchronous Receiver-Transmitter*
- *Pmod : Peripheral module interface*
- *HDMI :High-Definition Multimedia Interface*
- *OLED : Organic Light Emitting Diode*
- *RTOS : Real Time Operating System*
- *ARM : Advanced RISC Machine*

ZEDBOARD BLOCK DIAGRAM :

ZedBoard is basically classified into three units , those are :

1. *Programmable Logic (PL)*
2. *Processing System (PS)*
3. *Multiplexed I/O (MIO)*

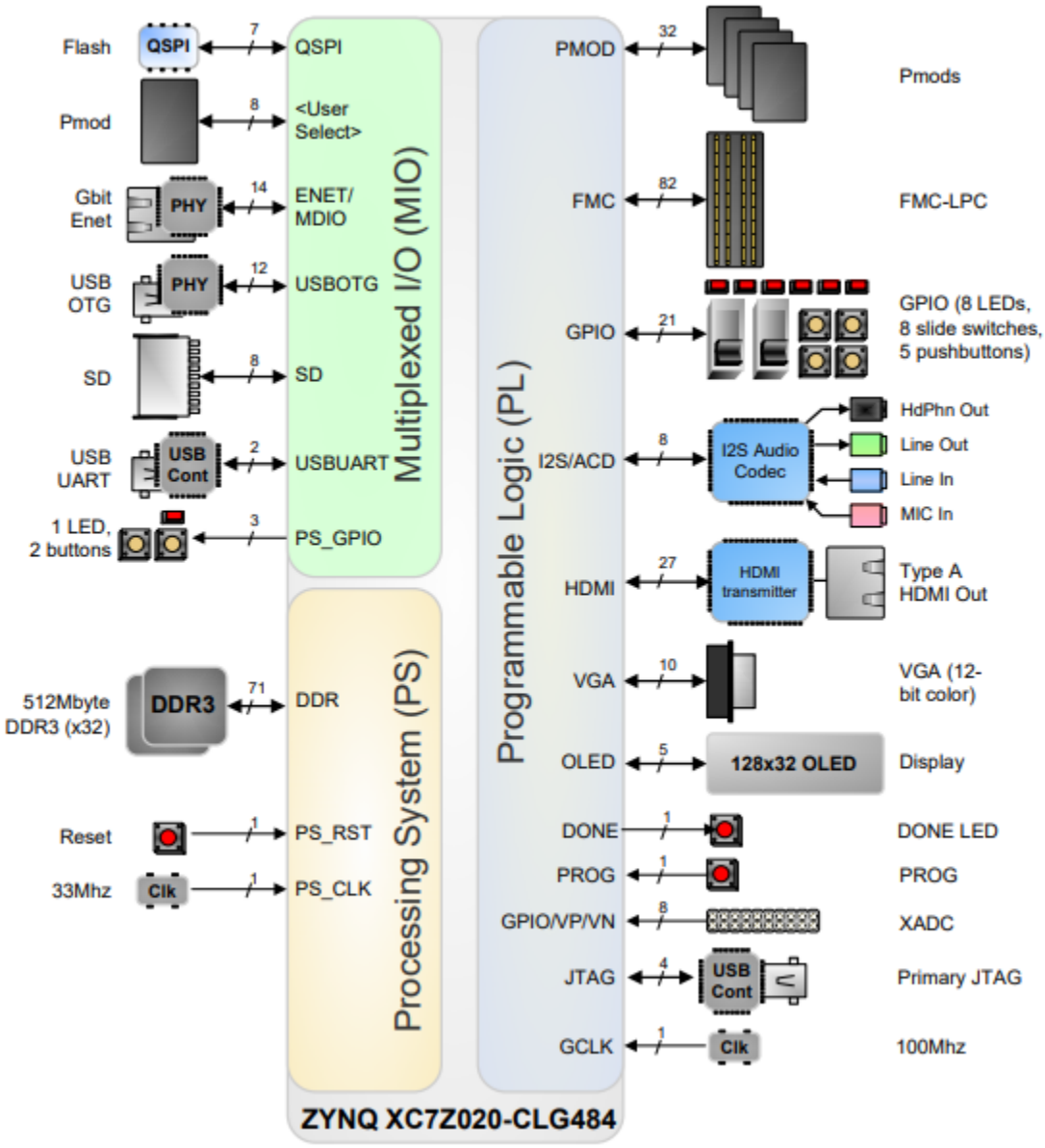


FIG 6 : BLOCK DIAGRAM OF ZEDBOARD ZYNQ - 7000

SIMULATION RESULTS :

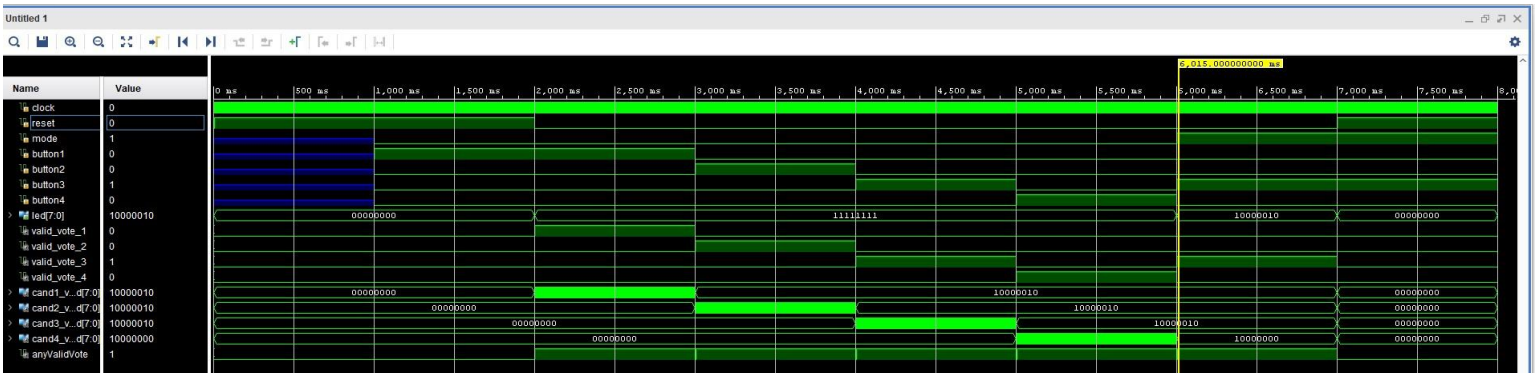


FIG 7 : SIMULATION RESULT OF ELECTRONIC VOTING MACHINE

If reset is Active High signal then the intermediate signals such as valid_vote and cand_vote_recvd are forced to be ' 0 '. For Normal Operation of Electronic Voting Machine the reset pin must be Active Low Signal. For Voting Mode the mode signal should be Active Low else it is in Result Mode.

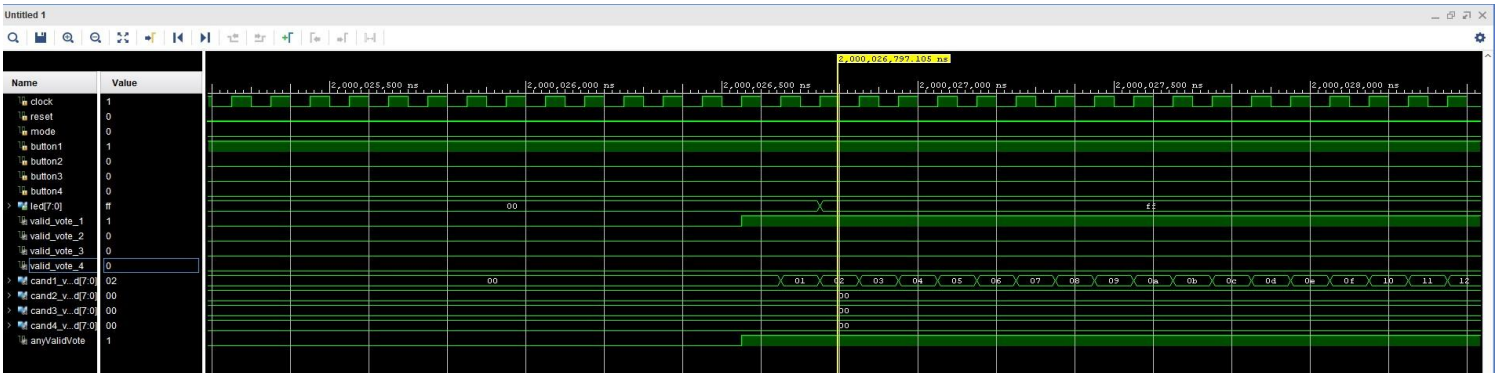


FIG 8 : DETAILED SIMULATION RESULT OF EVM

In fig.8 depicts that until button1 is Active High the valid_vote is Active High and the cand_vote_recvd will increment by 1 . Practically the button1 needs to be pressed until the all LEDs blink once, then the LEDs acknowledge the vote is successfully casted to the respective candidate.

The operating Clock frequency is 100 MHz and the candidate inputs i.e., buttons are Priority Encoder in Hardware Implementation.

REGISTER TRANSFER LEVEL (RTL) SCHEMATIC :

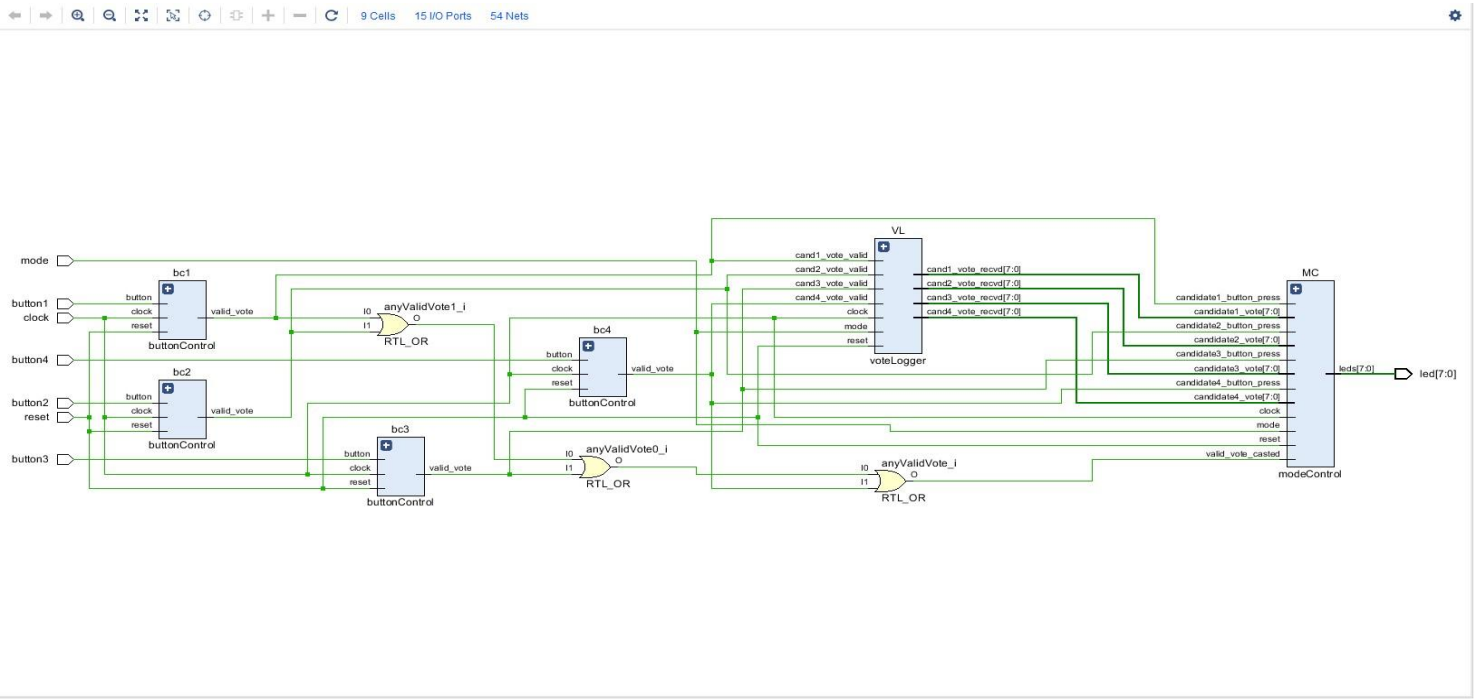


FIG 9 : REGISTER TRANSFER LEVEL (RTL) SCHEMATIC OF EVM

SYNTHESIS SCHEMATIC :

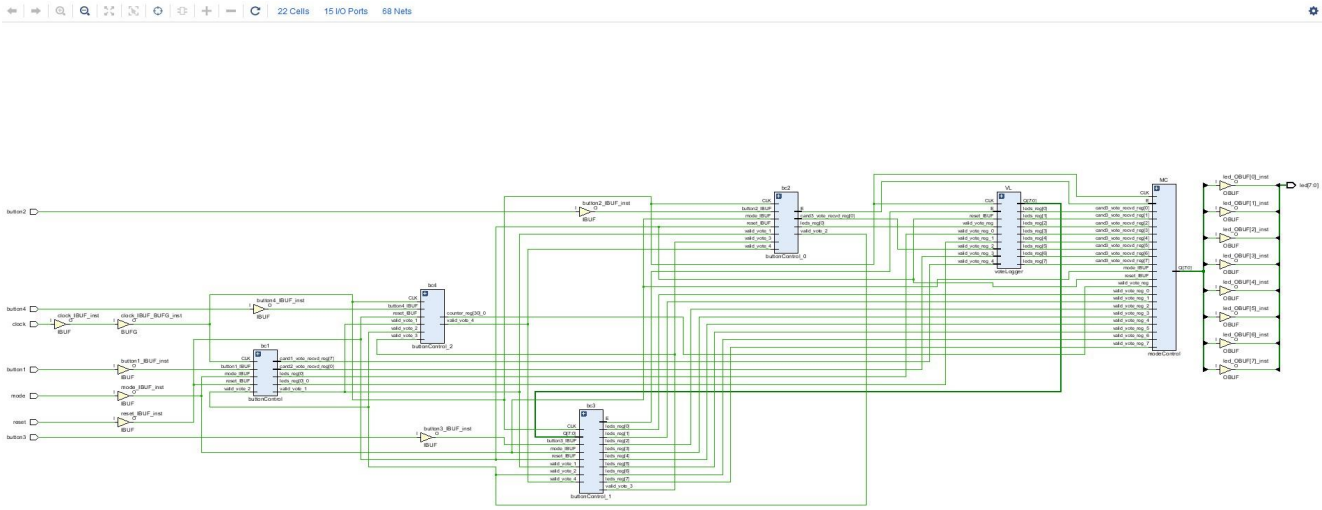


FIG 10 : SYNTHESIS SCHEMATIC OF EVM

FLOOR PLANNING SCHEMATIC :

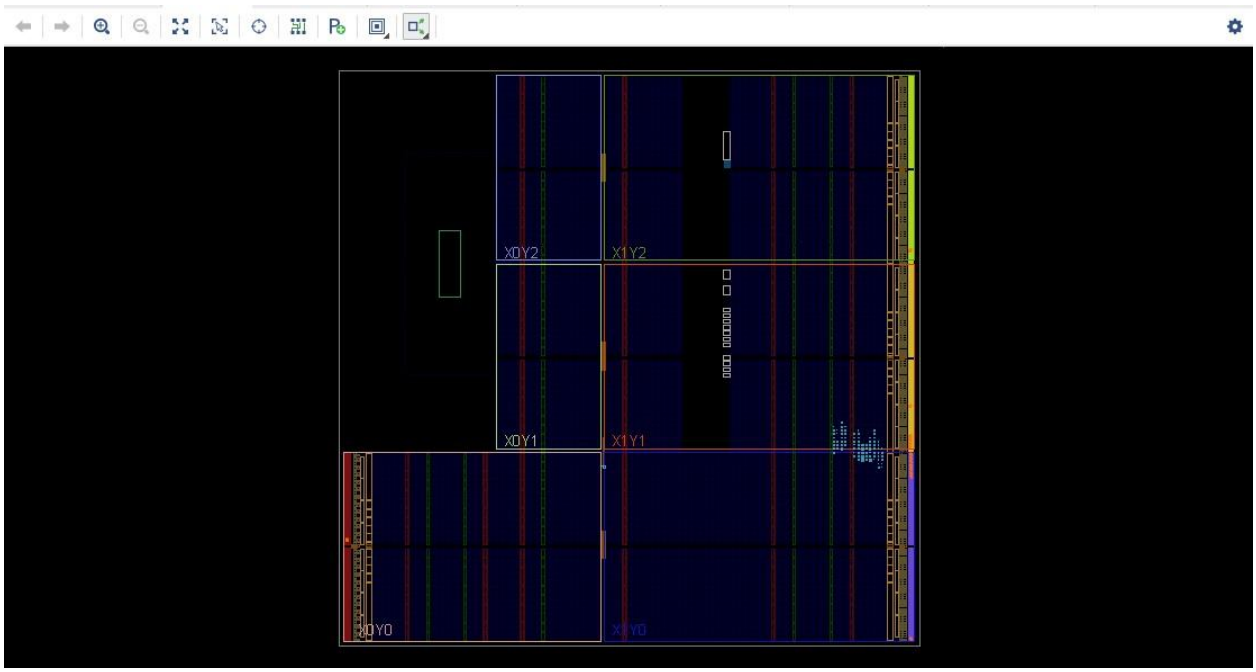


FIG 11 : FLOOR PLANNING SCHEMATIC OF EVM

I/O PLANNING SCHEMATIC :

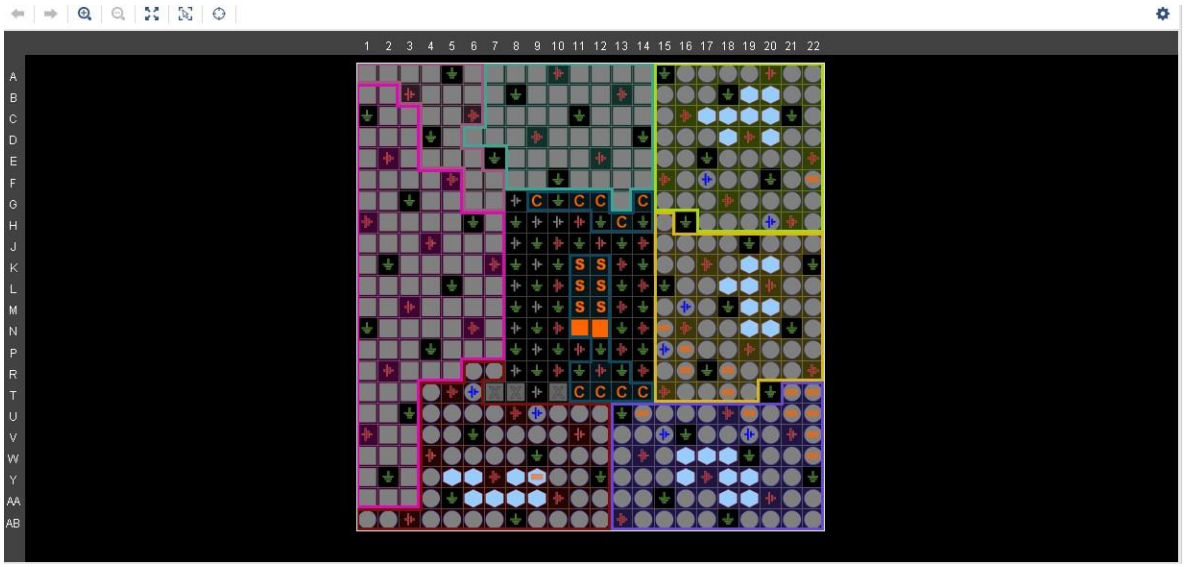


FIG 12 : I/O PLANNING SCHEMATIC OF EVM

UTILIZATION :

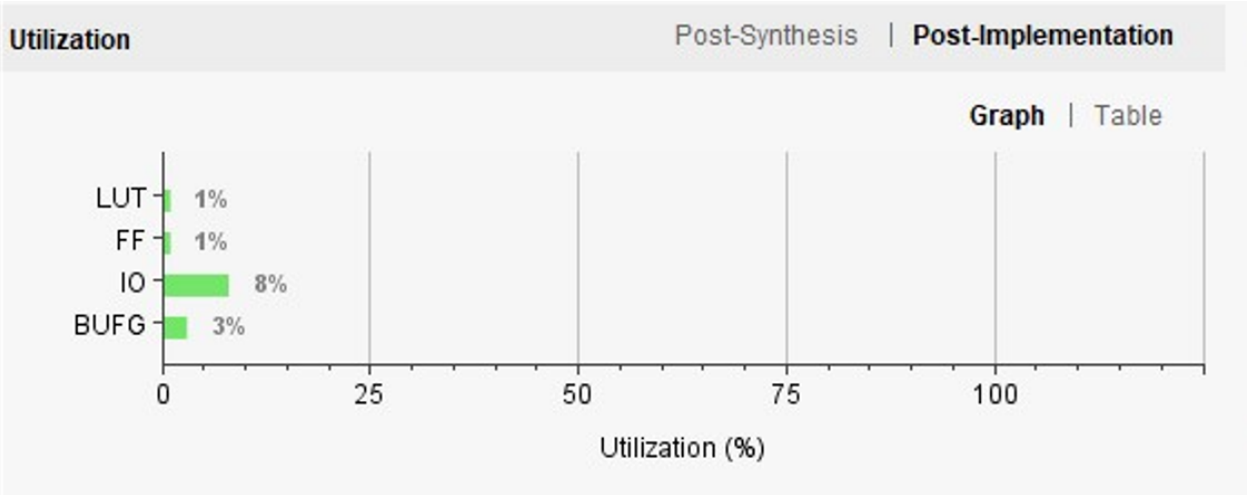


FIG 13 : UTILIZATION OF EVM

POWER ANALYSIS :

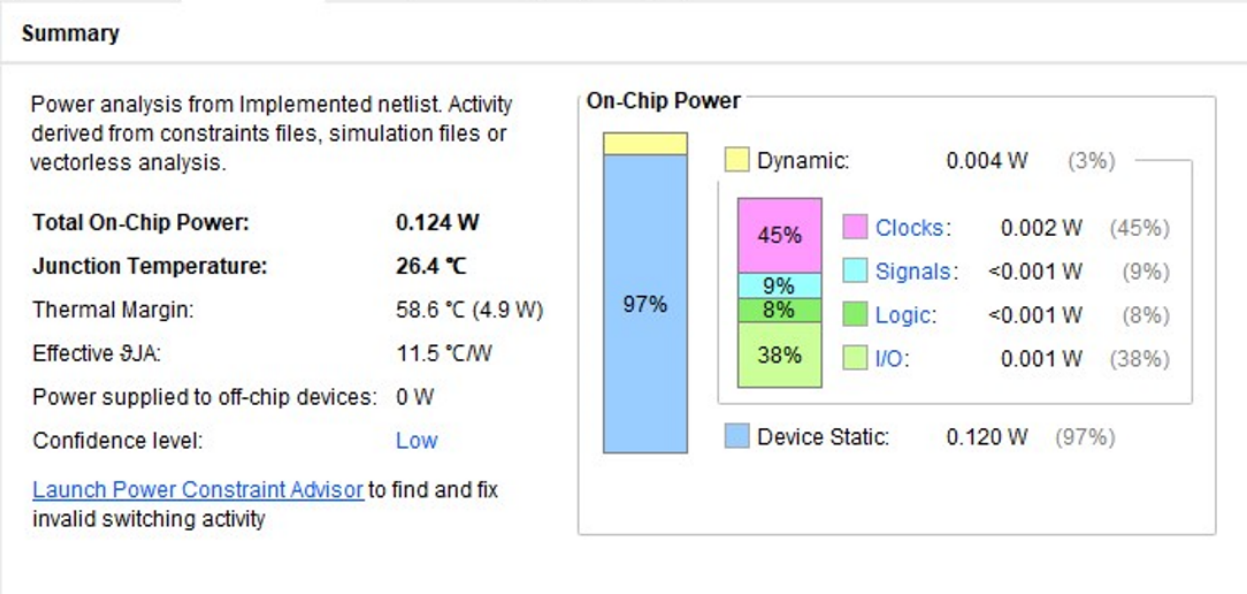


FIG 14 : POWER ANALYSIS OF EVM

CONCLUSION :

The Xilinx based designed Electronic Voting Machine can be used for secure voting, where the tampering of votes has very less probability. It is easy to build and a large number of votes can be casted and recorded depending on the memory of the system. Since it does not contain any memory card and can be provided a password which is digital in nature. It provides a secure system for conducting elections. This system is also memory efficient as it uses only one bit for recording a vote casted by user.Since the cost incurred in its manufacturing is less, therefore it can easily replace the paper ballot system present in certain areas.