A

Project Report

On

POWER REDUCTION OF HALF SUBTRACTOR

Submitted to

RAJIV GANDHI UNIVERSITY OF KNOWLEDGE TECHNOLOGIES, KADAPA

in partial fulfilment of the requirements for the award of the Degree of

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

Submitted by

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

RGUKT, RK VALLEY

(RGUKT KADAPA is approved by UGC, AICTE, established in 2008, provide Education opportunities for rural people)

Vempalli, Kadapa-516330

2019-2023

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CERTIFICATE

This is to certify that the project report entitled "**POWER REDUCTION OF HALF SUBTRACTOR**" a bonafide record of the project work done and submitted by

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	Head of Department of ECE

External Viva-Voice Exam Held on _____

INTERNAL EXAMINER ` EXTERNAL EXAMINER

DECLARATION

We hereby declare that the project report entitled "**POWER REDUCTION OF HALF SUBTACTOR** " submitted to the Department of **ELECTRONICS AND COMMUNICATION ENGINEERING** in partial fulfilment of requirements for the award of the degree of BACHELOR OF TECHNOLOGY. This project is the result of our own effort and that it has not been submitted to any other University or Institution for the award of any degree or diploma other than specified above.

M.SAIPRAKASH REDDY **R170797**

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ACKNOWLEDGEMENT

We are thankful to our guide **Mr K.ABDUL MUNAF** for her valuable guidance and encouragement. Her helping attitude and suggestions have helped us in the successful completion of the project.

We would like to express our gratefulness and sincere thanks to Prof. P.Janardhan Reddy, Head of the Department of **ELECTRONICS AND COMMUNICATION ENGINEERING**, for his kind help and encouragement during the course of our study and in the successful completion of the project work.

We have great pleasure in expressing our hearty thanks to our beloved Director **Prof. K. Sandhya Rani** for spending her valuable time with us to complete this project.

Successful completion of any project cannot be done without proper support and encouragement. We sincerely thanks to the Management for providing all the necessary facilities during the course of study.

We would like to thank our parents and friends, who have the greatest contributions in all our achievements, for the great care and blessings in making us successful in all our endeavors.

With Sincere Regards,

M**. SAIPRAKASH REDDY(R170797).**

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ABSTRACT

In VLSI, Arithmetic circuit plays an important role.In this Addition is one of the basic arithmetic operation.....

In this project, the Half Subtractor is being designed by using adaptivevoltage level techniques.This Technique is used for low power consumption. Low power subtractors are used to reduce the overall power consumption of micro-electronic systems. The role of subtractors are important in almost all fields .With the help of low power subtractors , all the other systems which make use of subtractors may dissipate less power. This project presents a detailed comparison between the Half subtractors designed using gates and different styles of Half subtractor designed using transistors.

This project focus mainly on the comparisons among conventionalCMOS subtractor which is static CMOS subtractor and Proposed Version subtractor which is Dynamic CMOS subtractor . The technique which was used for reducing power consumption is Adaptive Voltage Level at Supply(AVLS) .

All the simulation results are done using Digital Schematic editor (DSCH) and the functionality is verified using the layout editor tool, MICROWIND.

Main Objective:

The sole objective of this project to conclude with a better estimate and ease in selecting a low power consuming half subtractor.

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INTRODUCTION

1.2 Motivation of Work :

In Very Large Scale Integration the increasing demand for low power consumption is increased. Subtractor is a combinational circuit in which it represents the smallest unit used for the subtraction in the digital system. The subtractor is not only used for the arithmetic calculation in many device processors but also used in the other part of the processor for address calculations table indices, and similar operations. In these, the half subtractor is a simpler device compared to other subtractorss. This combinational circuit is used for the subtraction of two binary digits which is used for push-pop logical operation. Although subtractors can be constructed for many numerical representations, such as binary-coded decimal or excess-3, themost common subtractors operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an subtractor into an subtractor–adder. Other signed number representations require a more complex adder.

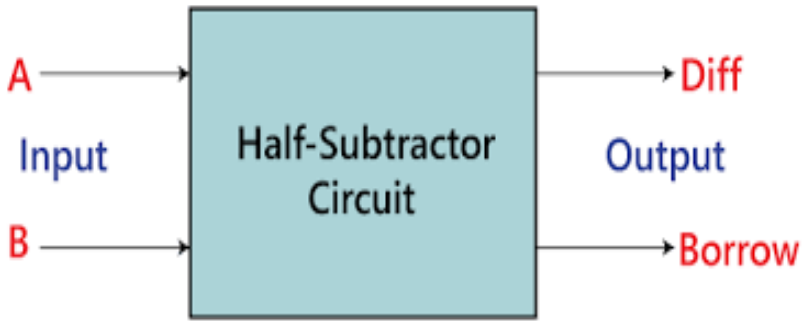
1.3 About Half Subtractor :

Half Subtractor is a combinational arithmetic circuit that adds two numbers and produces a difference bit (D) and borrow bit (B) as the output. If Aand B are the input bits, then difference bit (D) is the X-OR of A and B and the borrow bit (B) will be the AND of A’ and B. From this it is clear that a halfsubtractor circuit can be easily constructed using one X-OR gate and one AND gate.

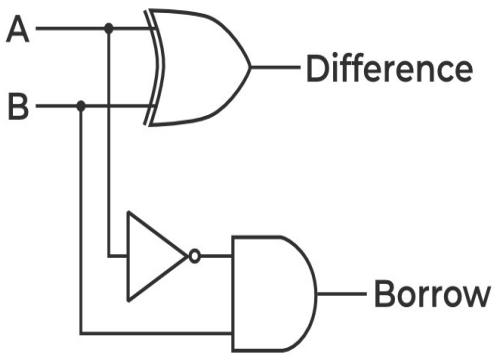
Half subtractor is the simplest of all subtractor circuit. So if the input to a half subtractor have a borrow, then it will be neglected it and subtracts only the A and B bits. That means the binary subtracttion process is not complete andthat’s why it is called a half subtractor. A half subtractor is a device that can subtracts two bits and returns the value, along with a carry value.

The difference between a half subtractor and a full subtractor is that a half subtractor only accepts two bits, while a full subtractor subtracts two bits and a borrow.

Logic Symbol of Half Subtractor:



Logic Diagram:



1.4 Truth Table of Half Subtractor:

Inputs		Output	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

1.5 Output Calculation:

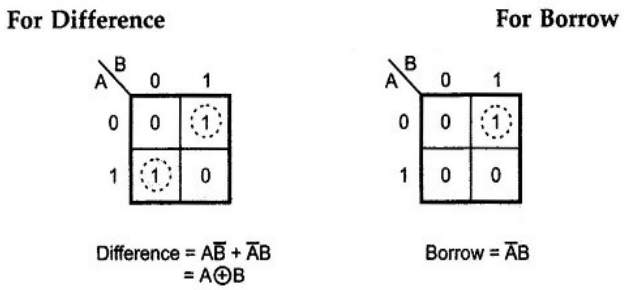


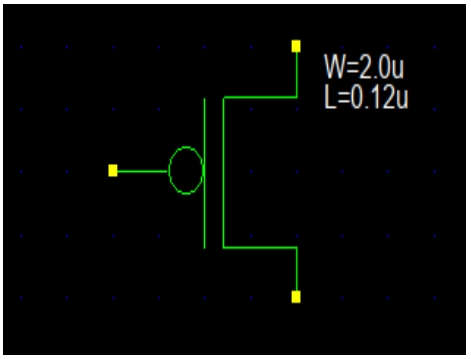
Fig. 3.19

This all above information design of half subtractor using gates.But ,We are going to design Half Subtractor using cmos Technology which uses transistorsnmos and pmos respectively. They are many papers that have publishedfor reducing the power consumption of the arithmetic circuits such as full subtractor circuit and half adder. In these ,we designed by using the adaptive voltage level technique which have two method such as adaptive voltage level at ground and adaptive voltage level at source based on the CMOS technology at different sizes.But here we focused mainly on adaptive voltage level at source (AVLS) Technique for the proposed version of half subtractor against conventional version of it...

CHAPTER 2

COMPONENTS USED :

2.1 P-Mosfet :



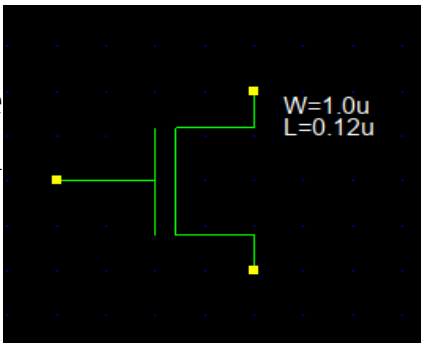
*Its p-channel metal-oxide semiconductor Transistor in which source and drain are made up of p-type Semiconductors.

* And Also p-type dopants are used in gate region (“the channel”)

*Its used to implement logic gates and other digital circuits

*In our Design ,We used W/L ratio is 16.67 i.e.,W=2.0u and L=0.12u

2.2 N-Mosfet :



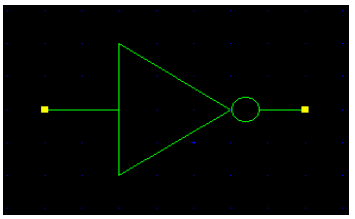
*Its stands for n-channel Metal Oxide Semiconductor Transistor in which source and drain are made up of n-type Semiconductors.

*Its used to implement logic gates and other digital circuits.

*In our Design ,We used W/L ratio is 16.67 i.e.,W=2.0u and L=0.12u

*n-MOS works faster than the p-MOS Semiconductor.

2.3 Inverter :



* Inverter is Not logical Gate which implements logical nagation or compliment.

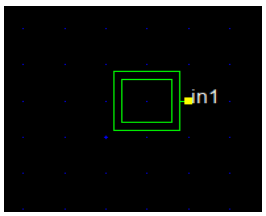
Truth Table:

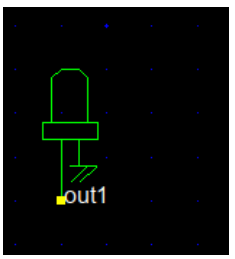
INPUT(A)	OUTPUT(A')
1	0
0	1

2.4 Input and Output :

* Input is to give the binary 0 and 1. Input light blinks when its 1.

*Output light blinks when output is Set





CHAPTER 3

CMOS TECHNOLOGY :

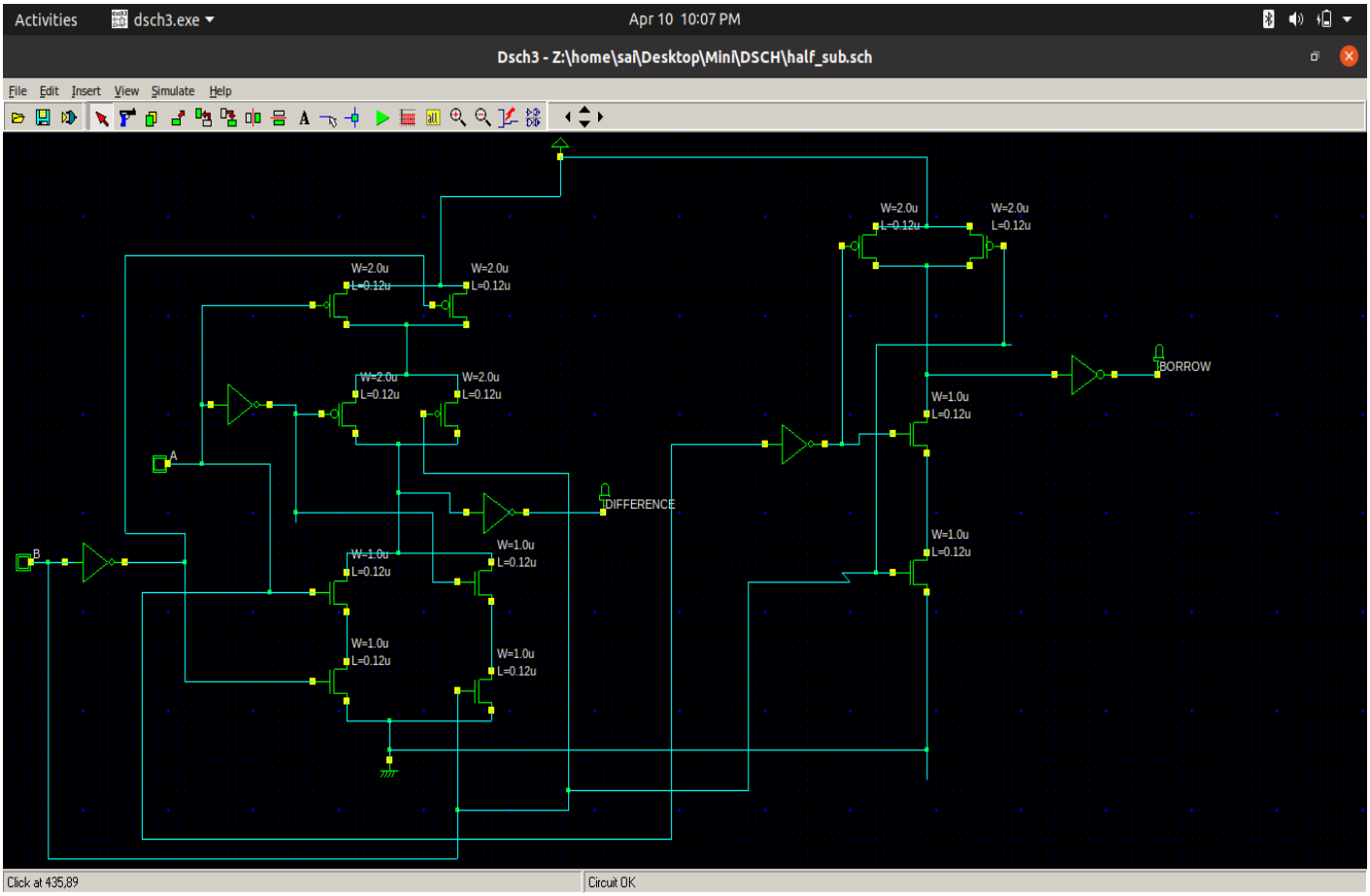
Complementary metal–oxide– semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors, data converters,and highly integrated transceivers for many types of communication. CMOS is also sometimes referred to as complementary-symmetry metal oxide–semiconductor (or COS-MOS). The words"complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic.

CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor Material. Aluminum was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-k dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nanometer node and beyond.

CHAPTER 4
CONVENTIONAL PROCESS AND RESULTS

4.1 Conventional Circuit of Half Subtractor:



* The above Circuit is General Circuit of Half Subtractor Circuit.

*It's CMOS based Technology Circuit in which it contains nearly 12 Transistors.

* And also It Contains Inverters for complement of input Signals.

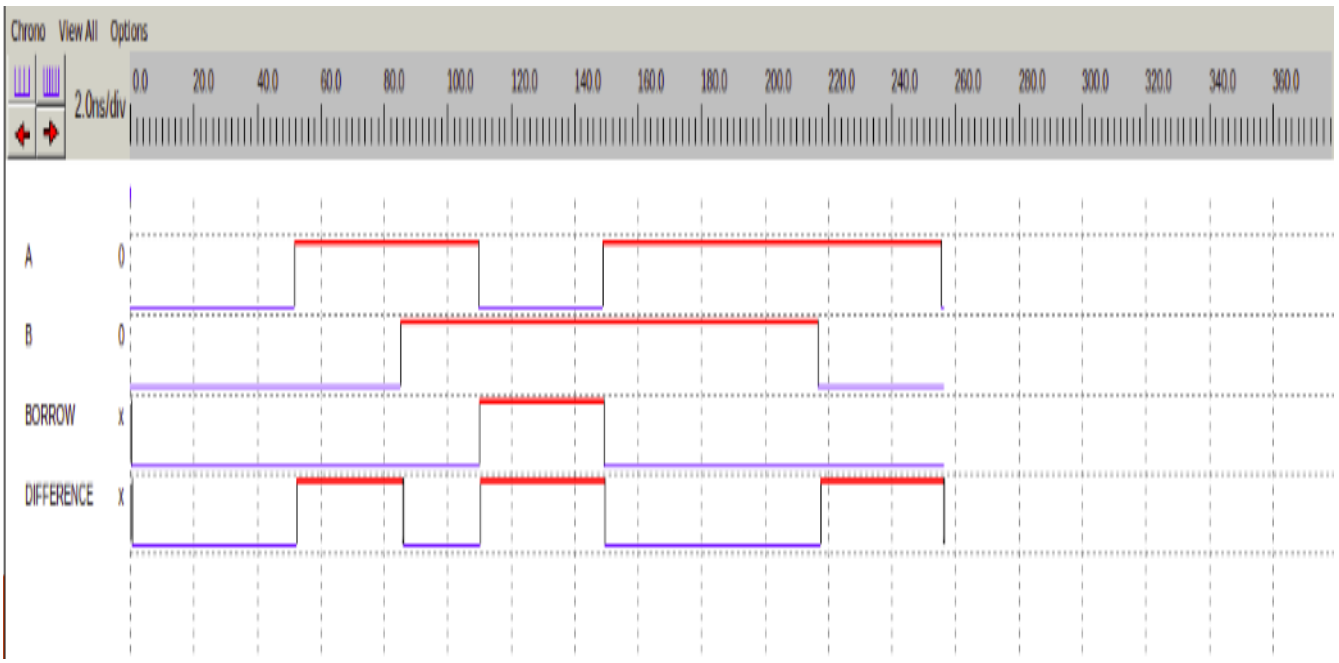
*Its Consumes more power as it contains more no of transistors.

*From DSCH and MICROWIND Software,We got Timing Diagram, Layout and its power Consumption for our General circuit.

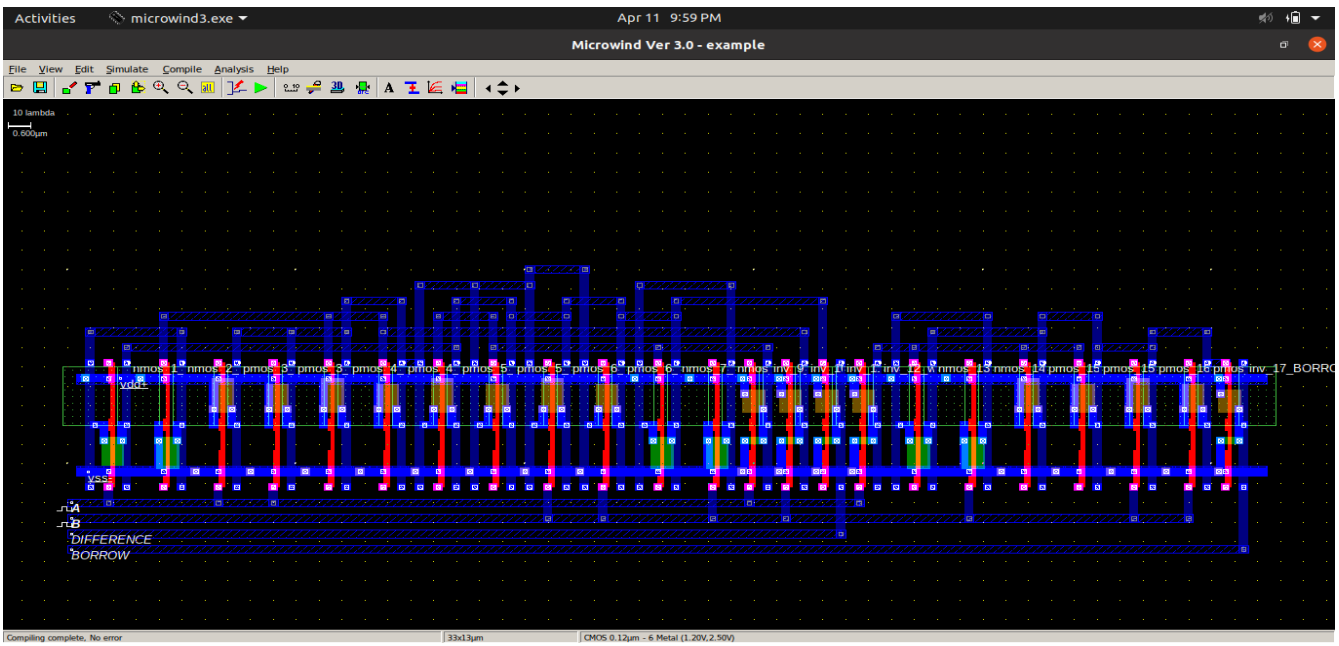
*Its a **Static Circuit** in which no clock is involved.

*Lets see them all in detail....

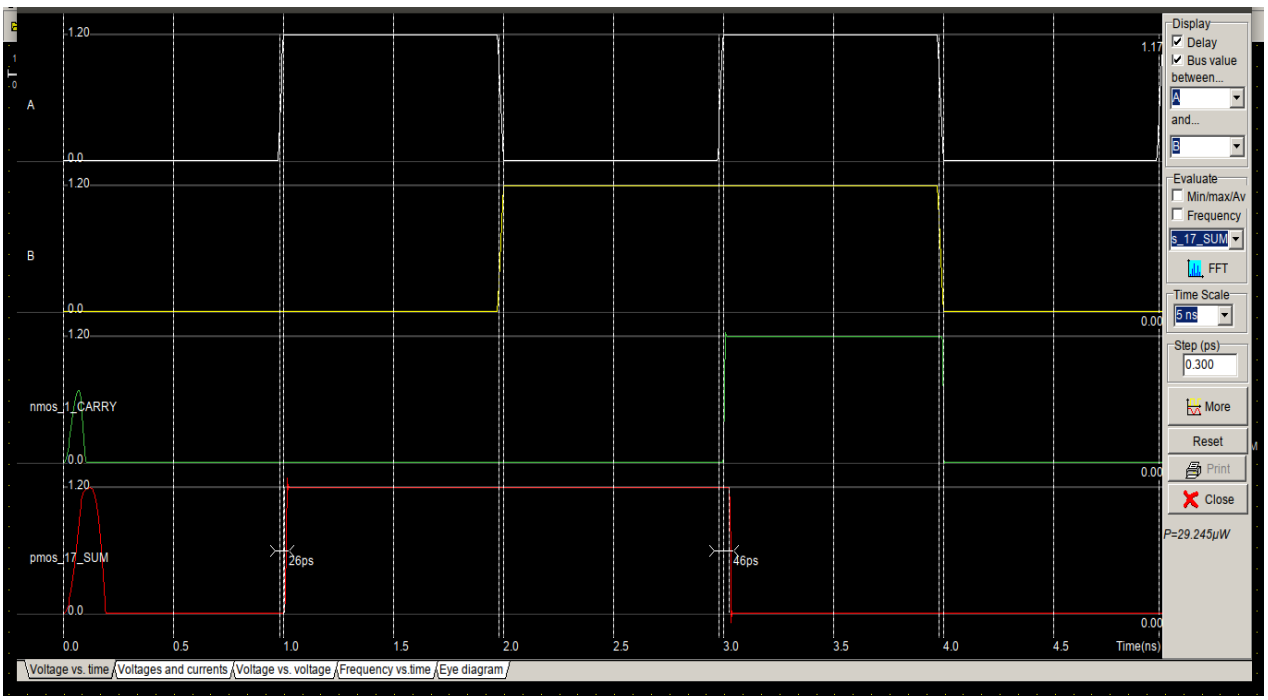
4.2 Timing Diagram :



4.3 Layout:



4.4 Power Consumption:



CHAPTER 5

PROPOSED CIRCUIT AND RESULTS :

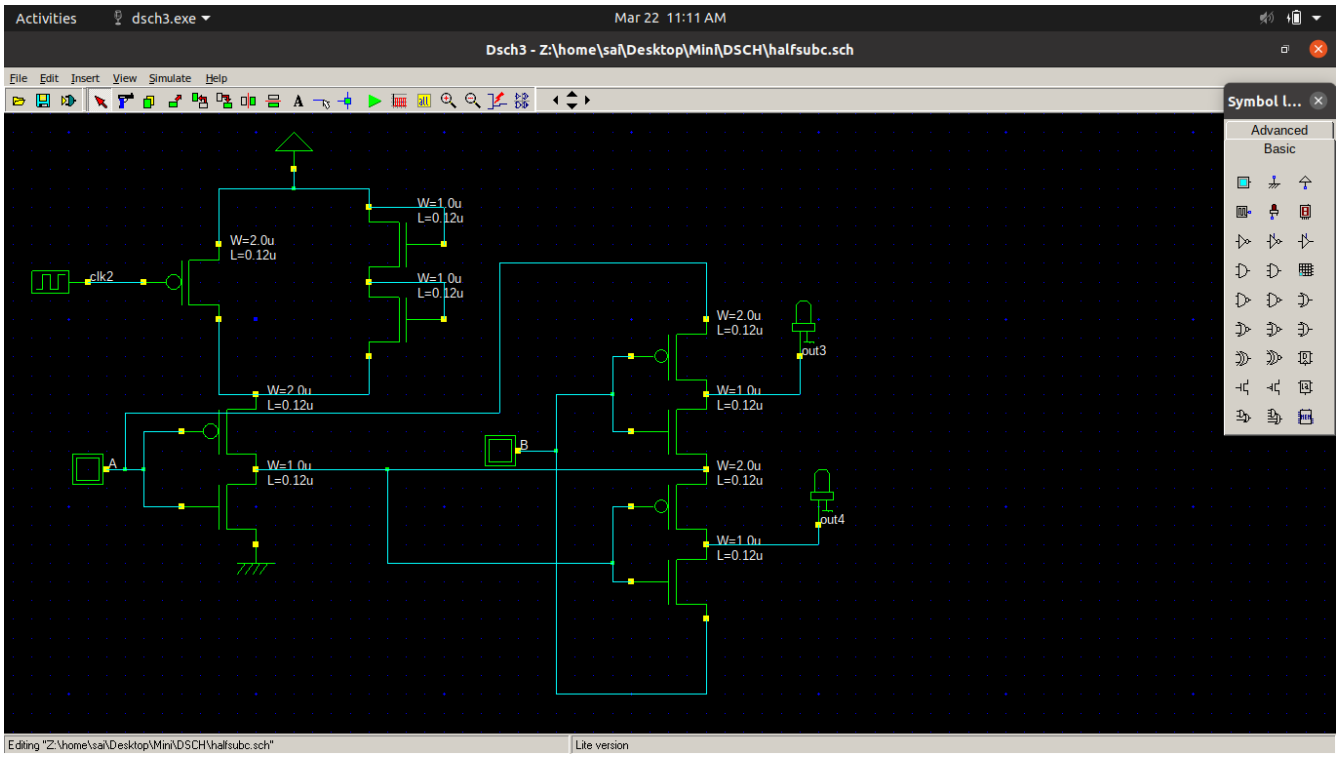
5.1 Proposed Methodology :

Actually, In the proposed Circuit, there is another reduced Half subtractor Circuit which consists of only 9 Transistors.Even though Transistor count is decreased here, power consumption is not good, means not a expecting level power.So proposed circuit designed again to that 9 T circuit by adding 3 transistors using AVLS Technique. The added 3 transistors had made a Control Circuit in which one p-MOS and two n-MOS transistors are there which are connected in parallel.This proposed Technique is called as Adaptive Voltage level at supply (AVLS) Technique.

5.2 AVLS Methodology :

In Adaptive Voltage Level at Supply (AVLS) technique .Here, Input clock is applied at the input terminal of the PMOS transistor and the rest of the NMOS transistor is connected to the drain terminal.This control circuit at the upper end would bring down the supply voltage given to the whole circuit inorder to reduce the power consumption of the conventional half subtractor design. When the input is varied corresponding output will be produced. It would reduce the leakage power by reducing the gate to source voltage and gate to drain voltage. This design would be responsible for very low power consumption.

5.3 Proposed Circuit of Half Subtractor using AVLS Teshnique :



* The above Circuit is Proposed Circuit of Half Subtractor Circuit.

*It's CMOS but AVLS based Technology Circuit in which it contains nearly 9 Transistors.

* And also It does not contains any Inverters for complement of input Signals.

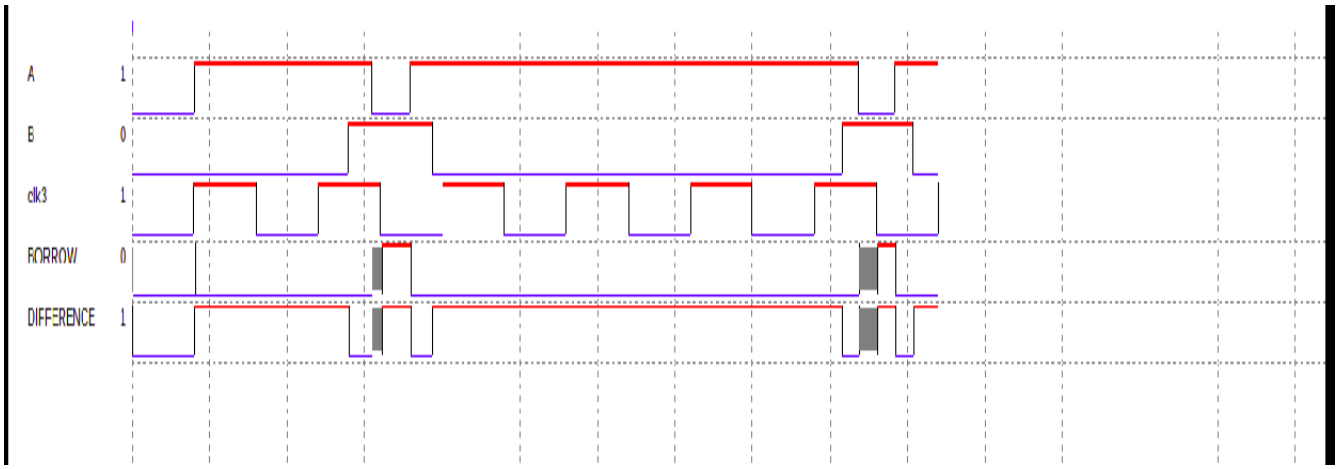
*Its Consumes less power as it contains less no of transistors.

*Its a **Dynamic Circuit** in which clock is involved.

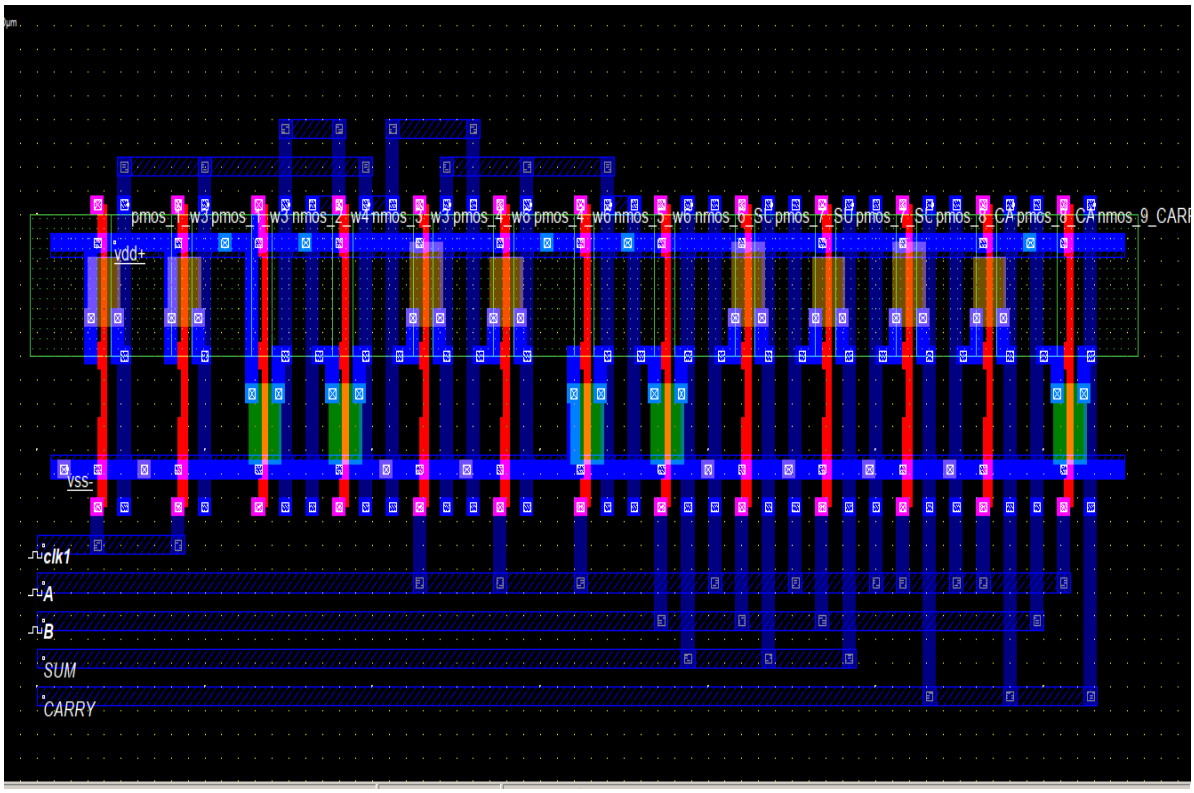
*From DSCH and MICROWIND Software,We got Timing Diagram, Layout and its power Consumption for our General circuit.

*Let see them all.....

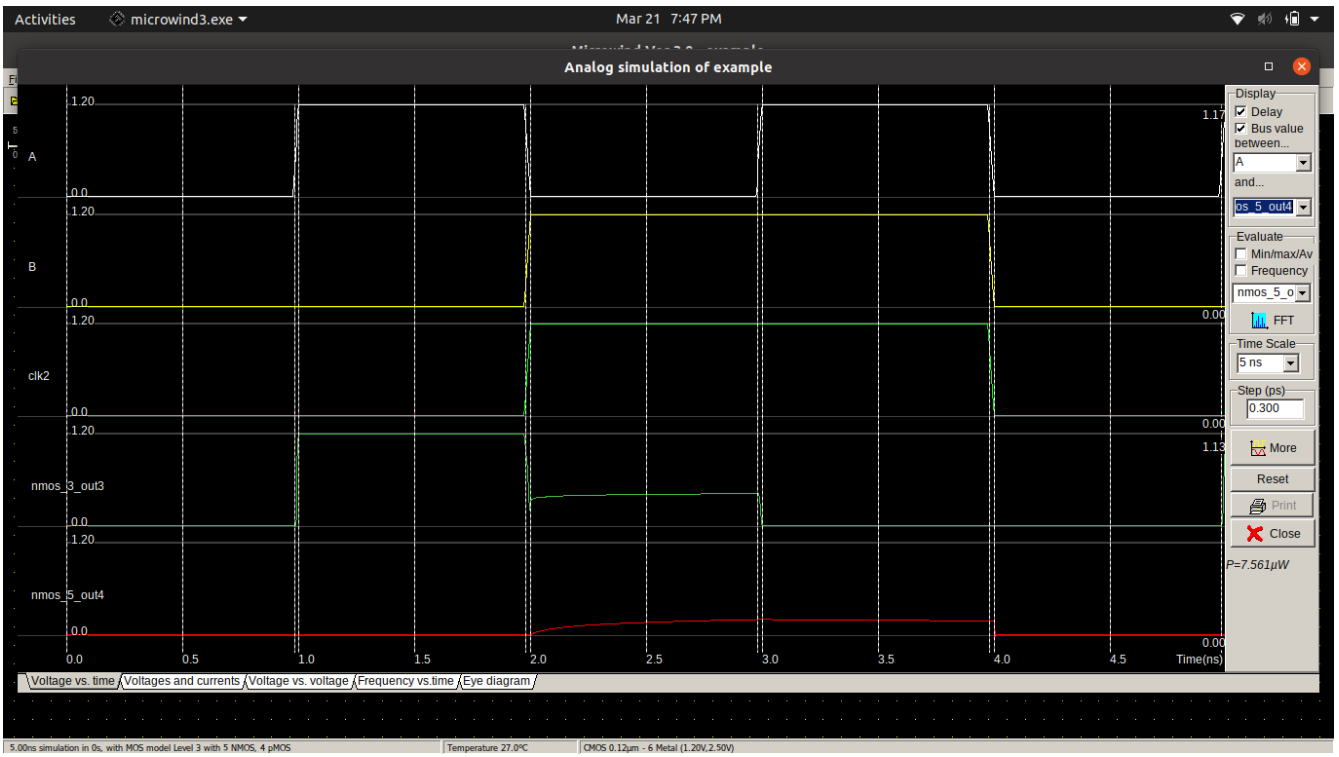
5.3 Timing Diagram :



5.4 Layout :



5.5 Power Consumption:



CHAPTER 6

COMPARISION TABLE

parameters	General Circuit	Proposed Circuit
Power consumption(micro watts)	28.056	7.561
No.PMOS,NMOS Transistors	6,6	4,5
No. of Gates	5	0

CHAPTER 7

7.1 Advantages:

- Power consumption is less.

- Low power design required to reduce the power in high end systems with hug integration density thus improves the speed of operation.

- Area consumption also reduces.

- Reducing power consumption in vlsi system is important since it is desirable to maximize the run time with minimum requirements on size ,battery life and weight allocated to batteries.

➔So the most important factor to consider while designing SoC for portable devices is “low power Design”.

7.2 Disadvantages:

➔ Even though power consmuption reduced,Half subtractors have no Scope of subtractingg the borrow bit resulting from the subtraction of previous bits

➔ Not suitable for cascading for multi-bit subtractions.

CHAPTER 8

8.1 Applications

➔As it is a basic arithmetic operation ,it will use in every chips.

➔ Used in Basic Calculators.

➔Used in Computers ,Digital devices ,Measuring Devices etc.

➔ When designing any Complex Gates ,this will be basic one to Choose.

CHAPTER 9

CONCLUSION :

The simulation result of this half subtractor design using AVL technique shown that the power consumption is reduced. Various parameters which have been shown in the simulation result have influence on designing in VLSI design. In this the half subtractor design using AVL technique are generated in both 65nm and 90nm CMOS technology to know and study about various parameters like propagation delay and the power consumption. From this parameter we can understood that the optimized half subtractor is produced. When compared to the other technique the AVLS design of half subtractor is more efficient in speed, power consumption and leakage current. It also uses less number of routed wires compared to other design technique.

The Half Subtractor for 2 bit input have been proposed and simulation results have been compared with the previous results using micro wind tool.

According to the simulation results this circuit reduces number of transistors (9T) and power consumption.

CHAPTER 10

REFERENCES :

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>>>>IJAREEIE Website