



# A PROJECT ON

# RISC-V

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**BPPD05**

# RISCV Synthesis script

```
set tech_file {../../ref/tech/saed32nm_1p9m.tf}
set synthetic_library dw.foundation.sldb
#set mw_path "../libs/mw_libs"
set mw_ref_libs "../libs/mw_libs/saed32_io_fc
../libs/mw_libs/saed32nm_lvt_1p9m"
set my_mw_lib RISC_V_mw.lib.mw

create_mw_lib $my_mw_lib \
-technology $tech_file \
-mw_reference_library $mw_ref_libs \
-open

set target_library {\
../../ref/DBs/saed32lvt_ss0p95v125c.db \
../../ref/DBs/saed32lvt_ss0p95v125c.db \
../../ref/DBs/saed32rvt_ss0p95v125c.db \
../../ref/DBs/saed32hvt_ss0p75v125c.db \
../../ref/DBs/saed32sramlp_ss0p95v125c_i0p95v.db}

set link library {\
../../ref/DBs/saed32lvt_ss0p95v125c.db \
../../ref/DBs/saed32lvt_ss0p95v125c.db \
../../ref/DBs/saed32rvt_ss0p95v125c.db \
../../ref/DBs/saed32hvt_ss0p75v125c.db \
../../ref/DBs/saed32sramlp_ss0p95v125c_i0p95v.db}

set ref libs {\
../../ref/DBs/saed32lvt_ss0p95v125c.db \
../../ref/DBs/saed32lvt_ss0p95v125c.db \
../../ref/DBs/saed32rvt_ss0p95v125c.db \
../../ref/DBs/saed32hvt_ss0p75v125c.db \
../../ref/DBs/saed32sramlp_ss0p95v125c_i0p95v.db}

Set tlu plus files\
    -max_tluplus ../../ref/tech/saed32nm_1p9m_Cmax.lv.tluplus \
    -min_tluplus ../../ref/tech/saed32nm_1p9m_Cmin.lv.tluplus
```

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```

source ./rtlV.tcl

current_design msrv32_top
source ../constraints/floorplan_constraints.pcon
read_sdc ../constraints/constraints_file.sdc
#set_wire_load_model -name wire_load.tcl
set_svf RISC_V.svf
# dft constraints
#set_dft_signal -view existing_dft -type ScanClock -port router_clock -timing
[list 45 55]
#set_dft_signal -view existing_dft -type Reset -port router_clock -active_state 1
#set_scan_configuration -chain_count 4
#create_test_protocol
#dft_drc
#preview_dft
#insert_dft

compile_ultra -no_automroup -no_boundary_optimization
write_icc2_files -output ..//results/riscv -force

write -hierarchy -format ddc -output ..//results/riscv.ddc
report_area > ..//reports/riscv_area.rpt
report_hierarchy > ..//reports/riscv_hierarchy.rpt
report_design > ..//reports/riscv_design.rpt
report_timing -path full > ..//reports/riscv_timing.rpt
write -hierarchy -format verilog -output ..//results/riscv.v
write_sdf ..//reports/riscv.sdf
write_parasitics -output ..//results/riscv_v_parastics_8_6
write_sdc ..//results/riscv.sdc
write -format ddc -h -o ..//results/riscv.ddc

puts "Finished"
#exit

```

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## RTL FILES

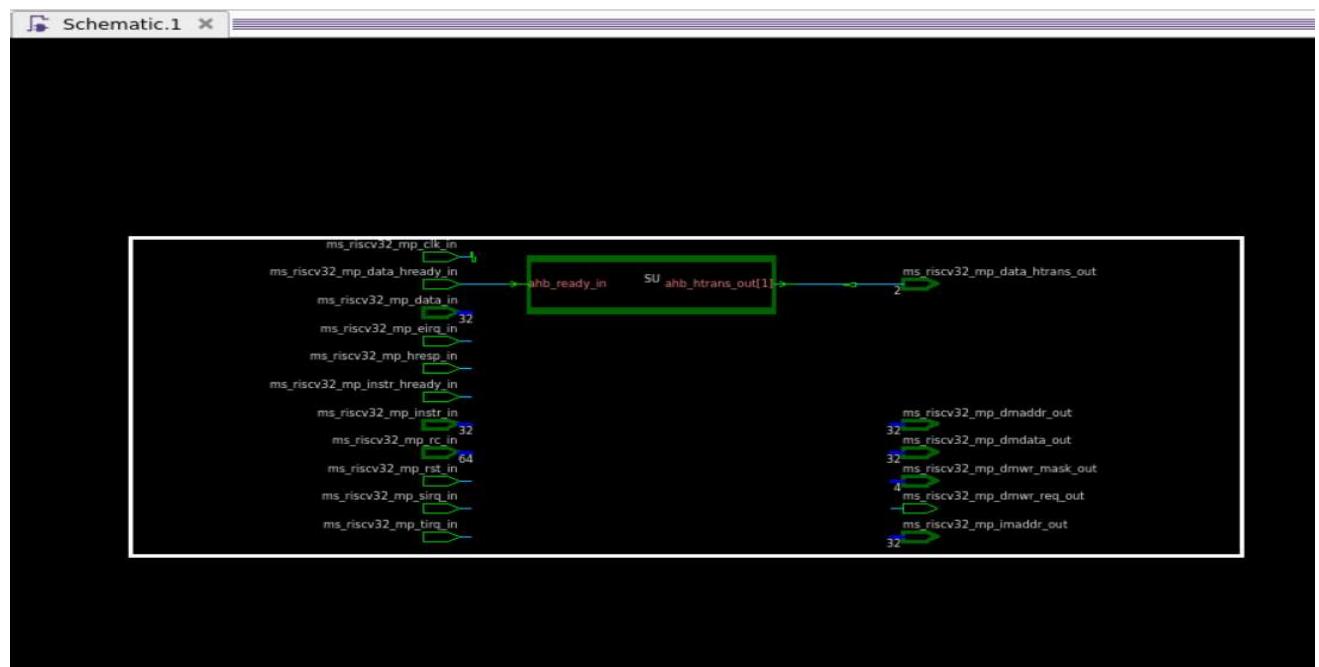
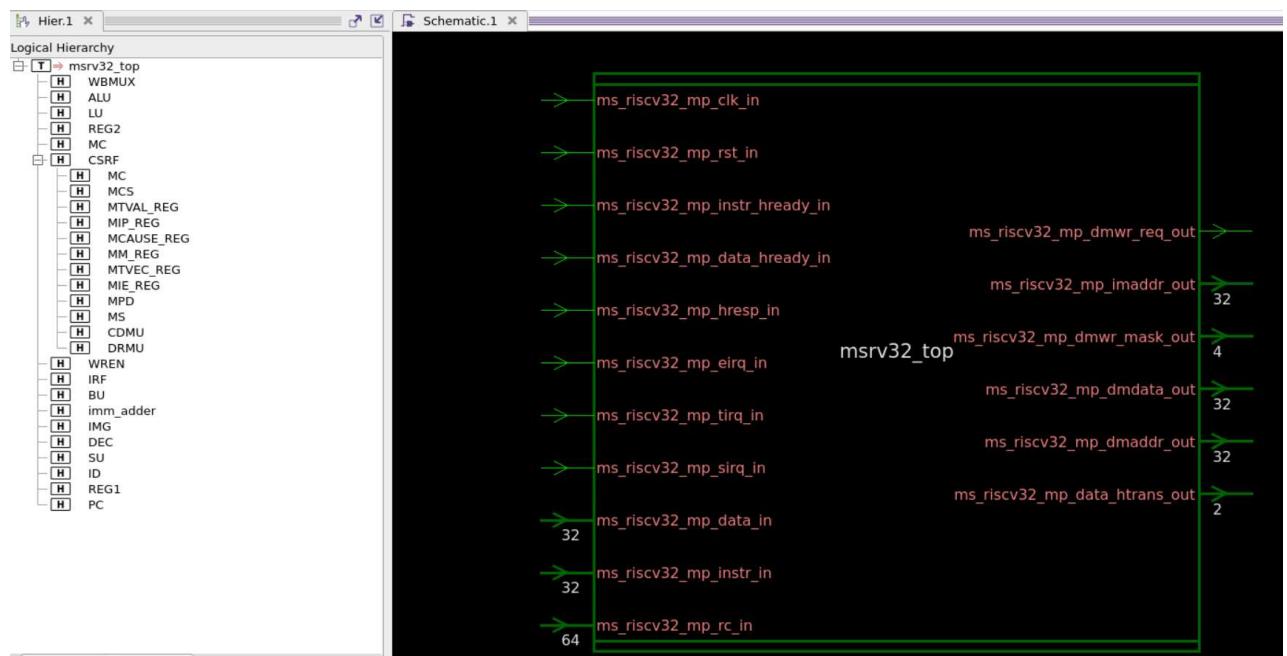
The screenshot shows a terminal window titled "BalluSanjeeV@mavenserver-RH2:~". The window contains a file listing for the directory "/home1/BPPD02/BalluSanjeeV/VLSI\_PD/Project/router\_pnr\_flow/synthesis\_DC/rtlV/". The file list includes numerous Verilog files (v and vh extensions) related to an RISC-V processor design, such as csr\_data\_mux\_unit.v, data\_wr\_mux\_unit.v, machine\_counter.v, mcause\_reg.v, mepc\_and\_mscratch\_reg.v, mie\_reg.v, mip\_reg.v, misa\_and\_pre\_data.v, msrv32\_alu.v, msrv32\_bu.v, msrv32\_csr\_file.v, msrv32\_dec.v, msrv32\_gdef.vh, msrv32\_img.v, msrv32\_immediate\_adder.v, msrv32\_instruction\_decoder.v, msrv32\_integer\_file.v, msrv32\_lu.v, msrv32\_machine\_control.v, msrv32\_pc.v, msrv32\_reg\_block\_1.v, msrv32\_reg\_block\_2.v, msrv32\_store\_unit.v, msrv32\_top.v, msrv32\_top\_wrapper.sv, msrv32\_wb\_mux\_sel\_unit.v, mstatus\_reg.v, mtval\_reg.v, mtvec\_reg.v, and wr\_en\_generator.v. The files were last modified on 2023-09-21 at 12:49, and the owner and group for all files are BalluSanjeeV.

Name	Size (KB)	Last modified	Owner	Group	Access
..					
csr_data_mux_unit.v	2	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
data_wr_mux_unit.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
machine_counter.v	2	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
machine_counter_setup.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
mcause_reg.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
mepc_and_mscratch_reg.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
mie_reg.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
mip_reg.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
misa_and_pre_data.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_alu.v	2	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_bu.v	2	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_csr_file.v	6	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_dec.v	8	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_gdef.vh	7	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_img.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_immediate_adder.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_instruction_decoder.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_integer_file.v	2	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_lu.v	2	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_machine_control.v	9	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_pc.v	2	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_reg_block_1.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_reg_block_2.v	3	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_store_unit.v	3	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_top.v	13	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_top_wrapper.sv	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
msrv32_wb_mux_sel_unit.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
mstatus_reg.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
mtval_reg.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
mtvec_reg.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--
wr_en_generator.v	1	2023-09-21 12:49	BalluSanjeeV	BalluSanjeeV	-rw-r--r--

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# SYNTHESIS USING DESIGN COMPILER (DC)

## SYNTHESIS TCL SCRIPT FOR RISC-V ---BLOCK AND SCHEMATIC OF RISC-V



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## RISC-V Netlist (Synthesis Output)

```
module msrv32_pc ( branch_taken_in, rst_in, ahb_ready_in, pc_src_in, epc_in,
    trap_address_in, pc_in, iaddr_in, pc_plus_4_out, i_addr_out,
    misaligned_instr_out, pc_mux_out );
  input [1:0] pc_src_in;
  input [31:0] epc_in;
  input [31:0] trap_address_in;
  input [31:0] pc_in;
  input [31:1] iaddr_in;
  output [31:0] pc_plus_4_out;
  output [31:0] i_addr_out;
  output [31:0] pc_mux_out;
  input branch_taken_in, rst_in, ahb_ready_in;
  output misaligned_instr_out;
  wire \pc_in[1], N20, N21, N22, N23, N24, N25, N26, N27, N28, N29, N30,
    N31, N32, N33, N34, N35, N36, N37, N38, N39, N40, N41, N42, N43, N44,
    N45, N46, N47, N48, N49, N50, n3, n4, n6, n7, n8, n9, n10, n11, n12,
    n13, n14, n15, n16, n17, n18, n19, n20, n21, n22, n23, n24, n25, n26,
    n27, n29, n30, n31, n32, n33, n34, n35, n36, n37, n38, n39, n40, n41,
    n42, n43, n44, n45, n46, n47, n48, n49, n50, n51, n52, n53, n54, n55,
    n56, n57, n58, n59, n60, n61, n62, n63, n64, n65, n66, n67, n68, n69,
    n70, n71, n72, n73, n74, n75, n76, n77, n78, n79, n80, n81, n82, n83,
    n84, n85, n86, n87, n88, n89, n90, n91, n92, n93, n94, n95, n96, n97,
    n98, n99, n100, n101, n102, n103, n104, n105, n106, n107, n108, n109,
    n110, n111, n112, n113, n114, n115, n116, n117, n122, n123, n124,
    n125, n126, n127, n128, n129, n134, n135, n137, n140, n148;
  assign pc_plus_4_out[1] = \pc_in[1];
  assign \pc_in[1] = pc_in[1];

LATCHX1_LVT \i_addr_reg[31] (.CLK(n137), .D(N50), .Q(i_addr_out[31]));
LATCHX1_LVT \i_addr_reg[30] (.CLK(n137), .D(N49), .Q(i_addr_out[30]));
LATCHX1_LVT \i_addr_reg[8] (.CLK(n137), .D(N27), .Q(i_addr_out[8]));
LATCHX1_LVT \i_addr_reg[7] (.CLK(n137), .D(N26), .Q(i_addr_out[7]));
LATCHX1_LVT \i_addr_reg[6] (.CLK(n137), .D(N25), .Q(i_addr_out[6]));
LATCHX1_LVT \i_addr_reg[5] (.CLK(n137), .D(N24), .Q(i_addr_out[5]));
LATCHX1_LVT \i_addr_reg[4] (.CLK(n137), .D(N23), .Q(i_addr_out[4]));
LATCHX1_LVT \i_addr_reg[3] (.CLK(n137), .D(N22), .Q(i_addr_out[3]));
LATCHX1_LVT \i_addr_reg[2] (.CLK(n137), .D(N21), .Q(i_addr_out[2]));
LATCHX1_LVT \i_addr_reg[1] (.CLK(n137), .D(N20), .Q(i_addr_out[1]));
AND2X1_LVT U3 (.A1(branch_taken_in), .A2(iaddr_in[1]), .Y(
    misaligned_instr_out));
AND2X1_LVT U4 (.A1(pc_src_in[1]), .A2(pc_src_in[0]), .Y(n6));
INVX1_LVT U5 (.A(branch_taken_in), .Y(n3));
INVX1_LVT U9 (.A(pc_src_in[0]), .Y(n9));
A0222X1_LVT U12 (.A1(n6), .A2(misaligned_instr_out), .A3(n4), .A4(
    \pc_in[1]), .A5(n8), .A6(epc_in[1]), .Y(pc_mux_out[1]));
NAND4X0_LVT U13 (.A1(pc_in[2]), .A2(pc_in[3]), .A3(pc_in[4]), .A4(pc_in[5]),
    .Y(n101));
INVX1_LVT U14 (.A(n101), .Y(n86));
NAND2X0_LVT U15 (.A1(n86), .A2(pc_in[6]), .Y(n85));
INVX1_LVT U16 (.A(n85), .Y(n82));
NAND2X0_LVT U17 (.A1(n82), .A2(pc_in[7]), .Y(n81));
INVX1_LVT U18 (.A(n81), .Y(n50));
NAND2X0_LVT U19 (.A1(n50), .A2(pc_in[8]), .Y(n49));
INVX1_LVT U20 (.A(n49), .Y(n46));
NAND2X0_LVT U21 (.A1(n46), .A2(pc_in[9]), .Y(n45));
INVX1_LVT U22 (.A(n45), .Y(n42));
NAND2X0_LVT U23 (.A1(n42), .A2(pc_in[10]), .Y(n41));
```

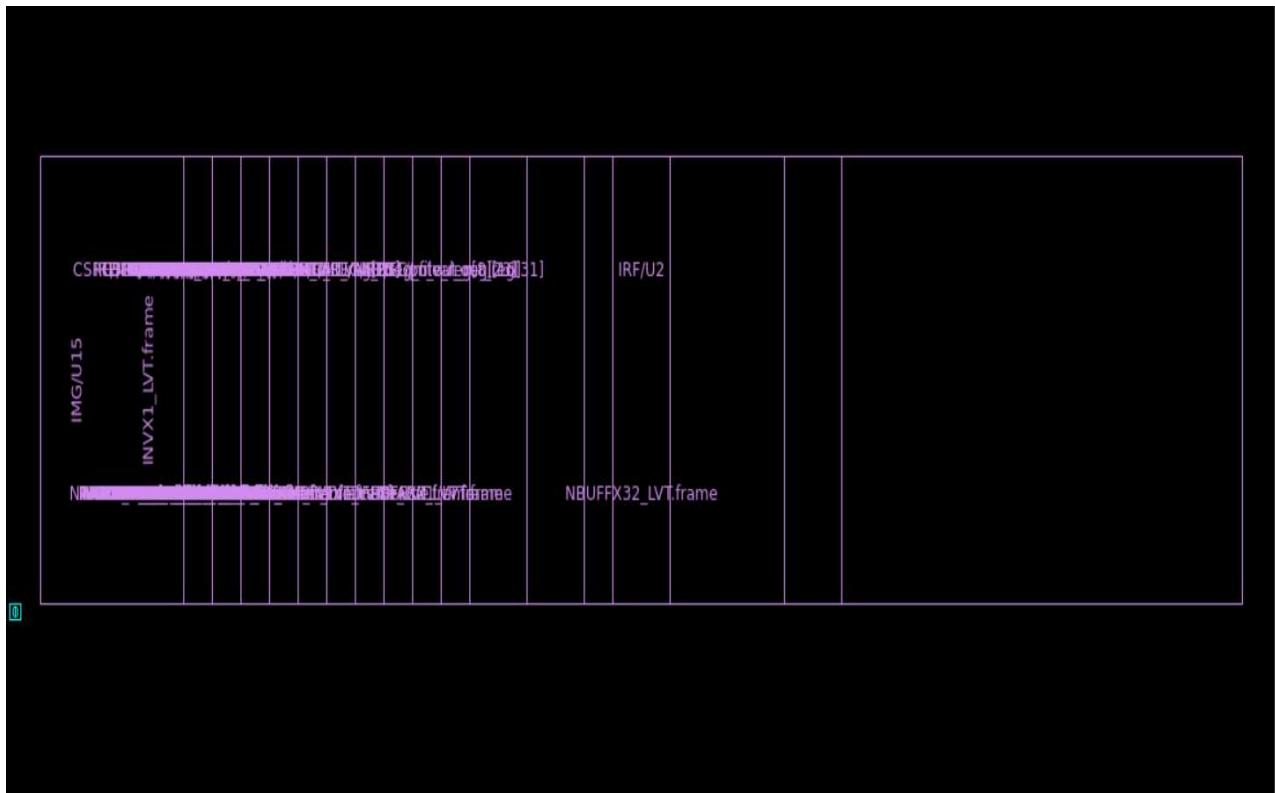
# PLACE AND ROUTE USING IC Compiler II

## P&R FLOW SCRIPT

```
#library creation
create_lib -technology ../../ref/tech/saed32nm_1p9m.tf -ref_libs \
{../../ref/CLIBs/saed32_1p9m_tech.ndm ../../ref/CLIBs/saed32_hvt.ndm \
../../ref/CLIBs/saed32_lvt.ndm ../../ref/CLIBs/saed32_rvt.ndm \
../../ref/CLIBs/saed32_sram_lp.ndm} riscv_block_2

# Creates the library {riscv_block_2}

#reading netlist and SDC
read_verilog ../netlist/riscv.v
read_sdc ./constraints/riscv.sdc
```



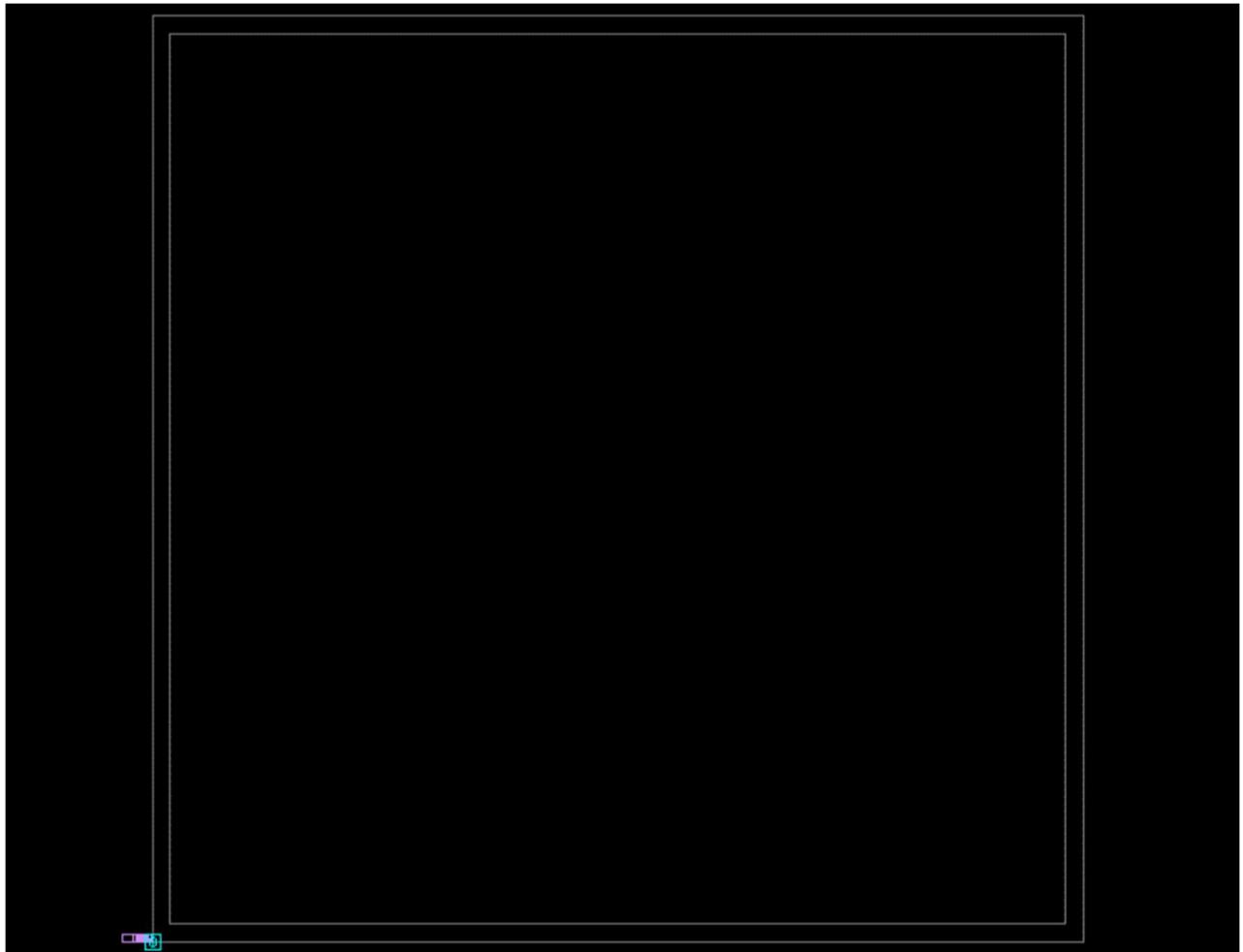
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```
#parasitic reading
read_parasitic_tech -name {new_model} -tlup {../../ref/tech/saed32nm_1p9m_Cmin.lv.tluplus} -
layermap \
{../../ref/tech/saed32nm_tf_itf_tluplus.map}
current_corner default
set_parasitic_parameters -early_spec new_model -late_spec new_model
set_process_number 0.99 -corners default
set_temperature 125 -corners default
set_voltage 0.75 -corners default
current_mode default
read_sdc ./constraints/riscv.sdc
set_scenario_status default -active true -setup true -hold true -max_transition true -max_capacitance
true -min_capacitance true -leakage_power true \
-dynamic_power true
```

link\_design

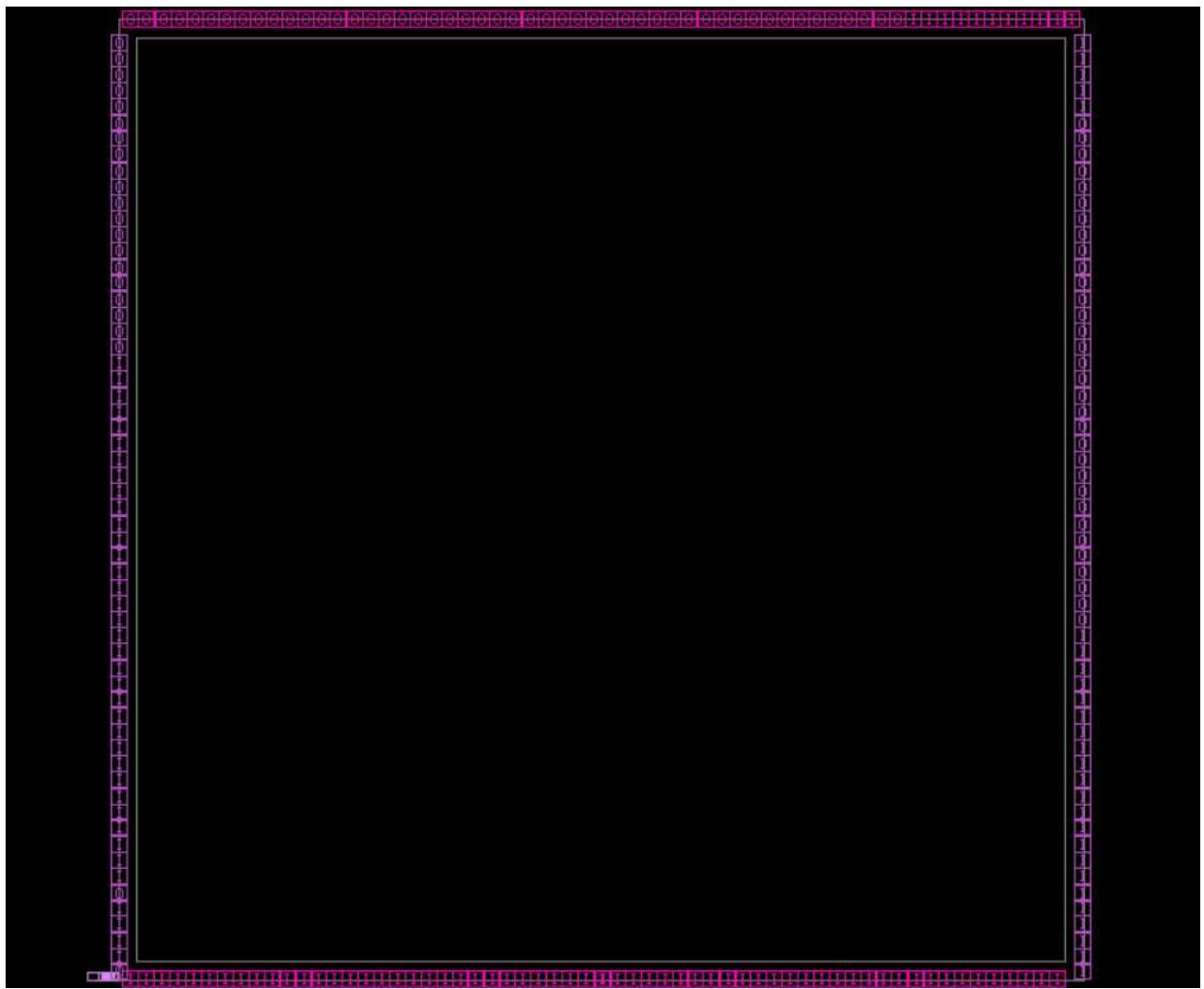
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```
initialize_floorplan -core_offset {4}
```



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```
#pins placement  
place_pins -self
```



```
# power plan  
source pns.tcl  
  
## create the PG nets  
create_net -power VDD  
create_net -ground VSS  
  
## Making Logical Connections  
connect_pg_net -net VDD [get_pins -hierarchical "*/VDD"]  
connect_pg_net -net VSS [get_pins -hierarchical "*/VSS"]  
  
connect_pg_net  
  
set_pg_via_master_rule pgvia_8x10 -via_array_dimension {8 10}  
  
create_pg_mesh_pattern top_layers \  
    -layers { {horizontal_layer: M7} {width: 1.104} {spacing: interleaving} {pitch: 13.376} {offset: 0.856} {trim : true} } \  
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```

```

    { {vertical_layer: M8} {width: 4.64} {spacing: interleaving} {pitch: 19.456} {offset: 6.08} {trim : true} } \
}
-via_rule { {intersection: adjacent} {via_master : pgvia_8x10} }

#{ {vertical_layer: M8} {width: 4.64 } {spacing: interleaving} {pitch: 19.456} {offset: 6.08} {trim : true} } \

create_pg_mesh_pattern m2_layer \
-layers { \
    { {vertical_layer: M2} {track_alignment : track} {width: 0.44 0.192} {spacing: 3.724 4.456} {pitch: 9.728} {offset:2.216} \
{trim : true} } \
}

set_pg_strategy S_default_vddvss \
-core \
-pattern { {name: top_layers} {nets:{VSS VDD}} {offset_start: {4 4}} } \
-extension { {{stop:design_boundary_and_generate_pin}} }

set_pg_strategy S_m2_vddvss \
-core \
-pattern { {name: m2_layer} {nets: {VDD VSS}} {offset_start: {4 4}} } \
-extension { {{direction:BT} {stop:core_boundary}} }

set_pg_strategy_via_rule S_via_m2_m7 \
-via_rule { \
    { {{strategies: {S_m2_vddvss}} {layers: { M2 }} {nets: {VDD}} } \
{{strategies: {S_default_vddvss}} {layers: { M7 }} } \
{ via_master: {default}} } \
    { {{strategies: {S_m2_vddvss}} {layers: { M2 }} {nets: {VSS}} } \
{{strategies: {S_default_vddvss}} {layers: { M7 }} } \
{ via_master: {default}} } \
}
}

compile_pg -strategies {S_default_vddvss S_m2_vddvss} -via_rule {S_via_m2_m7}

```

```

suppress_message PGR-599

create_pg_ring_pattern P_HM_ring -horizontal_layer M5 -horizontal_width {1} -vertical_layer M6 -vertical_width {1} -corner_bridge false
set_pg_strategy S_HM_ring_top -core -pattern { {pattern: P_HM_ring} {nets: {VSS VDD}} {offset: {0.3 0.3}} }
set_pg_strategy_via_rule S_ring_vias -via_rule { \
    {{{strategies: {S_HM_ring_top}} {layers: {M5}}} {existing: {strap }}{via_master: {default}}}} \
    {{{strategies: {S_HM_ring_top}} {layers: {M6}}} {existing: {strap }}{via_master: {default}}}} \
}
compile_pg -strategies {S_HM_ring_top} -via_rule S_ring_vias

#create_pg_macro_conn_pattern P_HM_pin -pin_conn_type scattered_pin -layers {M5 M4}
#set_pg_strategy S_HM_top_pins -core -pattern { {pattern: P_HM_pin} {nets: {VSS VDD}} }

#compile_pg -strategies {S_HM_top_pins}

```

```

create_pg_std_cell_conn_pattern P_std_cell_rail -layers {M1 M2}

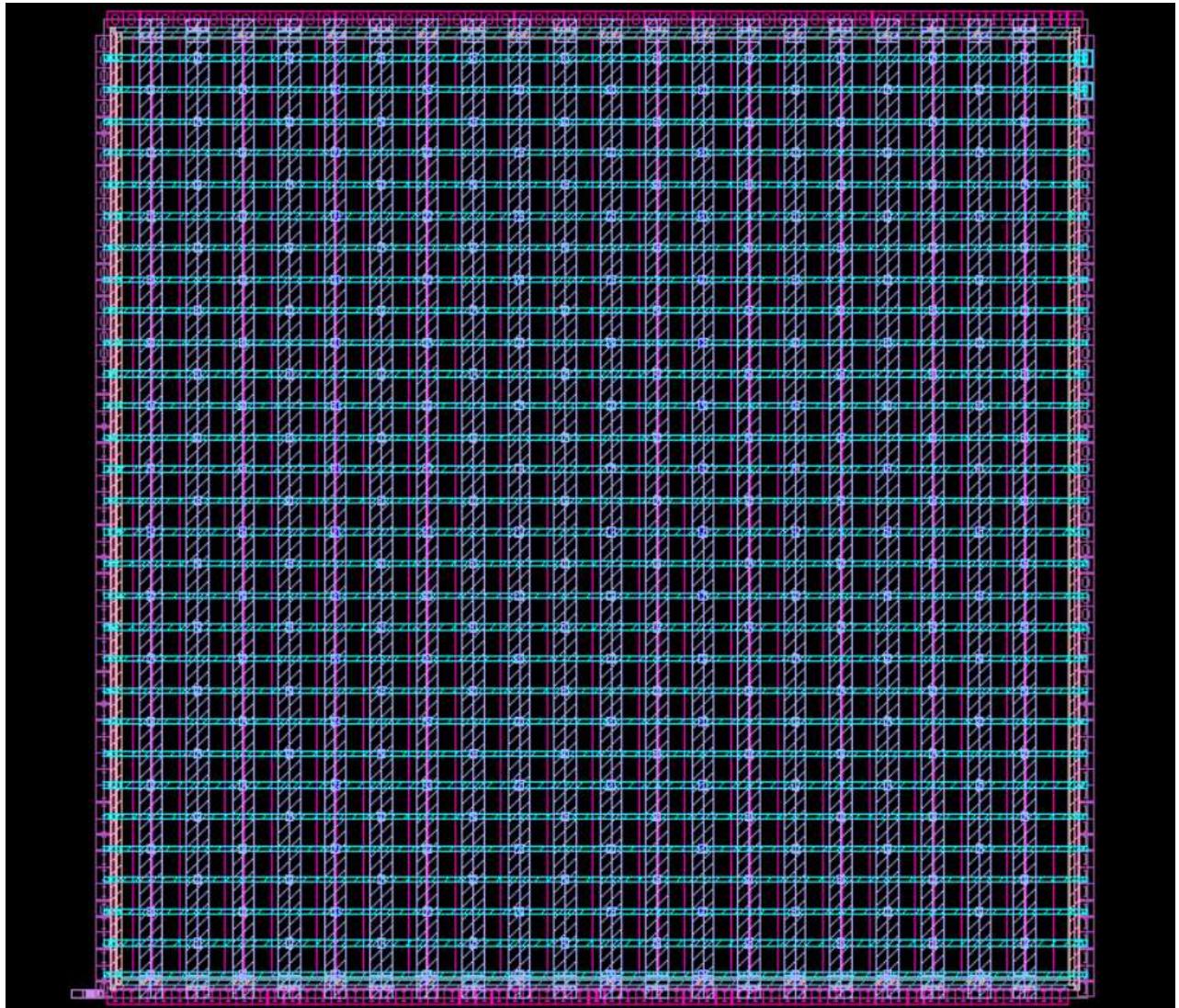
set_pg_strategy S_std_cell_rail_VSS_VDD \
-core \
-pattern {{pattern: P_std_cell_rail}{nets: {VSS VDD}}}} \
-extension { {{direction:BT} {stop:core_boundary}} } \
#{{stop: outermost_ring}{direction: L B R T }}

set_pg_strategy_via_rule S_via_stdcellrail \
-via_rule {{intersection: adjacent}{via_master: default} }

compile_pg -strategies {S_std_cell_rail_VSS_VDD} -via_rule {S_via_stdcellrail}

```

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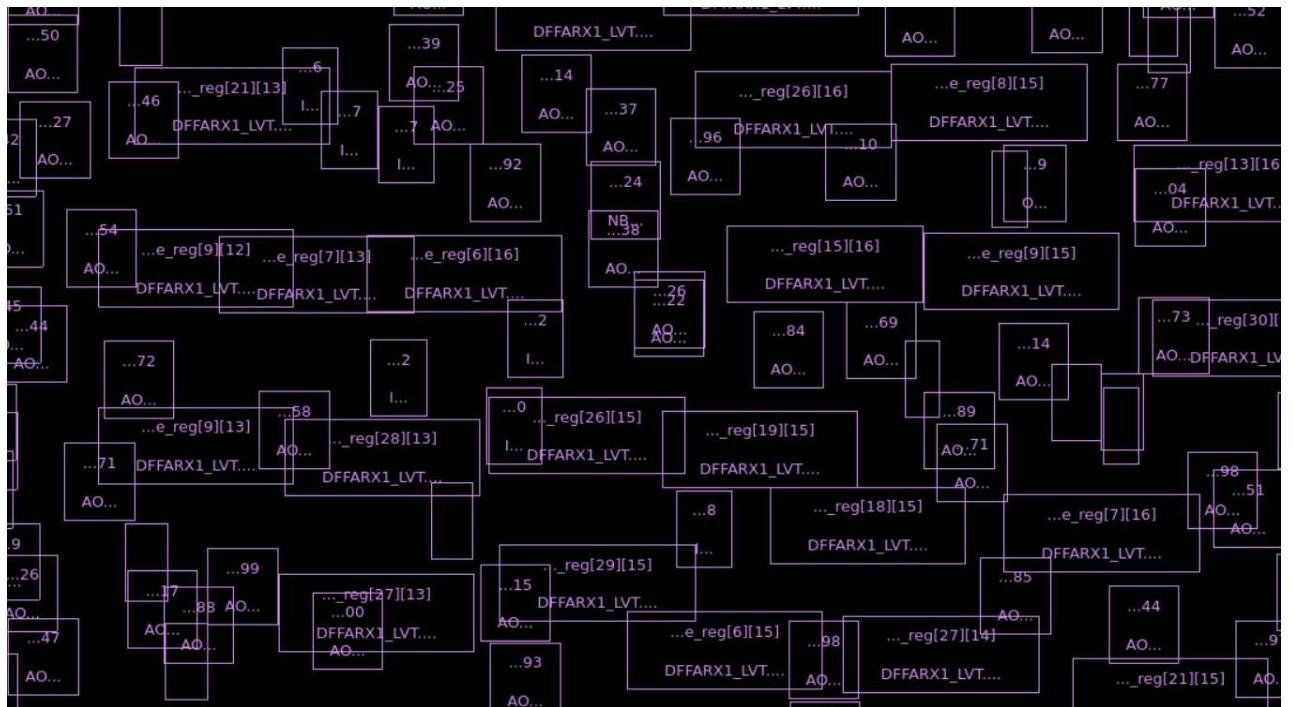


check\_pg\_drc

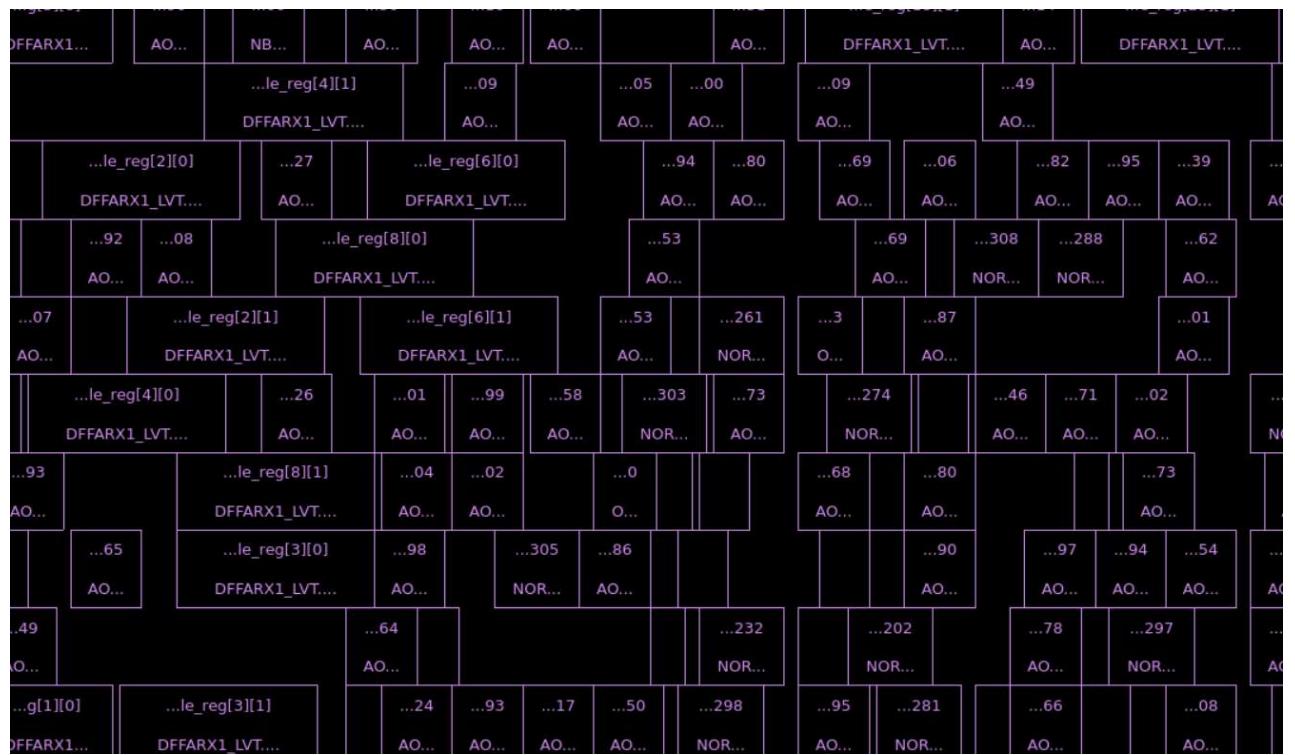
```
icc2_shell> check_pg_drc
Command check_pg_drc started at Fri Mar 29 10:19:28 2024
Command check_pg_drc finished at Fri Mar 29 10:19:28 2024
CPU usage for check_pg_drc: 0.24 seconds ( 0.00 hours)
Elapsed time for check_pg_drc: 0.24 seconds ( 0.00 hours)
No errors found.
icc2_shell> █
```

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```
#placement
create_placement -floorplan
```



```
legalize_placement
```



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### check\_pg\_connectivity

```
icc2_shell> check_pg_connectivity
Checking secondary net through power switch is enabled.
Secondary net will be checked together from primary net. They will be treated as the same net
Primary Net : VDD Secondary Net:
Primary Net : VSS Secondary Net:
Loading cell instances...
Number of Standard Cells: 8694
Number of Macro Cells: 0
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 1370
Number of VDD Vias: 3079
Number of VDD Terminals: 50
*****Verify net VDD connectivity*****
Number of floating wires: 0
Number of floating vias: 0
Number of floating std cells: 0
Number of floating hard macros: 0
Number of floating I/O pads: 0
Number of floating terminals: 0
Number of floating hierarchical blocks: 0
*****
Loading cell instances...
Loading P/G wires and vias...
Number of VSS Wires: 1429
Number of VSS Vias: 2194
Number of VSS Terminals: 54
*****Verify net VSS connectivity*****
Number of floating wires: 120
Number of floating vias: 0
Number of floating std cells: 0
Number of floating hard macros: 0
Number of floating I/O pads: 0
Number of floating terminals: 4
Number of floating hierarchical blocks: 0
*****
```

### #create SDC for clock

```
create_clock -period 10 -name risc_v_clk [get_port ms_riscv32_mp_clk_in]
```

```
icc2_shell> report_clocks
*****
Report : clock
Design : msrv32_top
Mode : default
Version: T-2022.03-SP4
Date : Fri Mar 29 10:28:45 2024
*****
```

#### Attributes:

- p - Propagated clock
- G - Generated clock
- U - Unexpanded generated clock

Clock	Period	Waveform	Attrs	Sources
risc_v_clk	10.00	{0 5}		{ms_riscv32_mp_clk_in}

```
#clock route
set_app_options -name time.remove_clock_reconvergence_pessimism -value true
report_clock_settings
```

```
icc2_shell> report_clock_settings
*****
Report : clock settings
Design : msrv32_top
Date   : Fri Mar 29 10:37:34 2024
*****

=====
Configurations
=====

##Global
Corner = default
  Max transition: around 0.500 (default)
  Max capacitance: 0.600 (default)
  Target skew: 0 (default)
  Target latency: Not specified

##risc_v_clk
Corner = default
  Max transition: around 0.500 (default)
  Max capacitance: 0.600 (default)
  Target skew: 0 (default)
  Target latency: Not specified

=====
Routing Rules
=====

##Global
Routing rule for sink nets: Not specified
Routing rule for internal nets: Not specified
Routing rule for root nets: Not specified
Routing rule for all nets: Not specified
Net-based routing rules (by set_clock_routing_rule): Not specified
Net-based routing rules (by set_routing_rule): Not specified
```

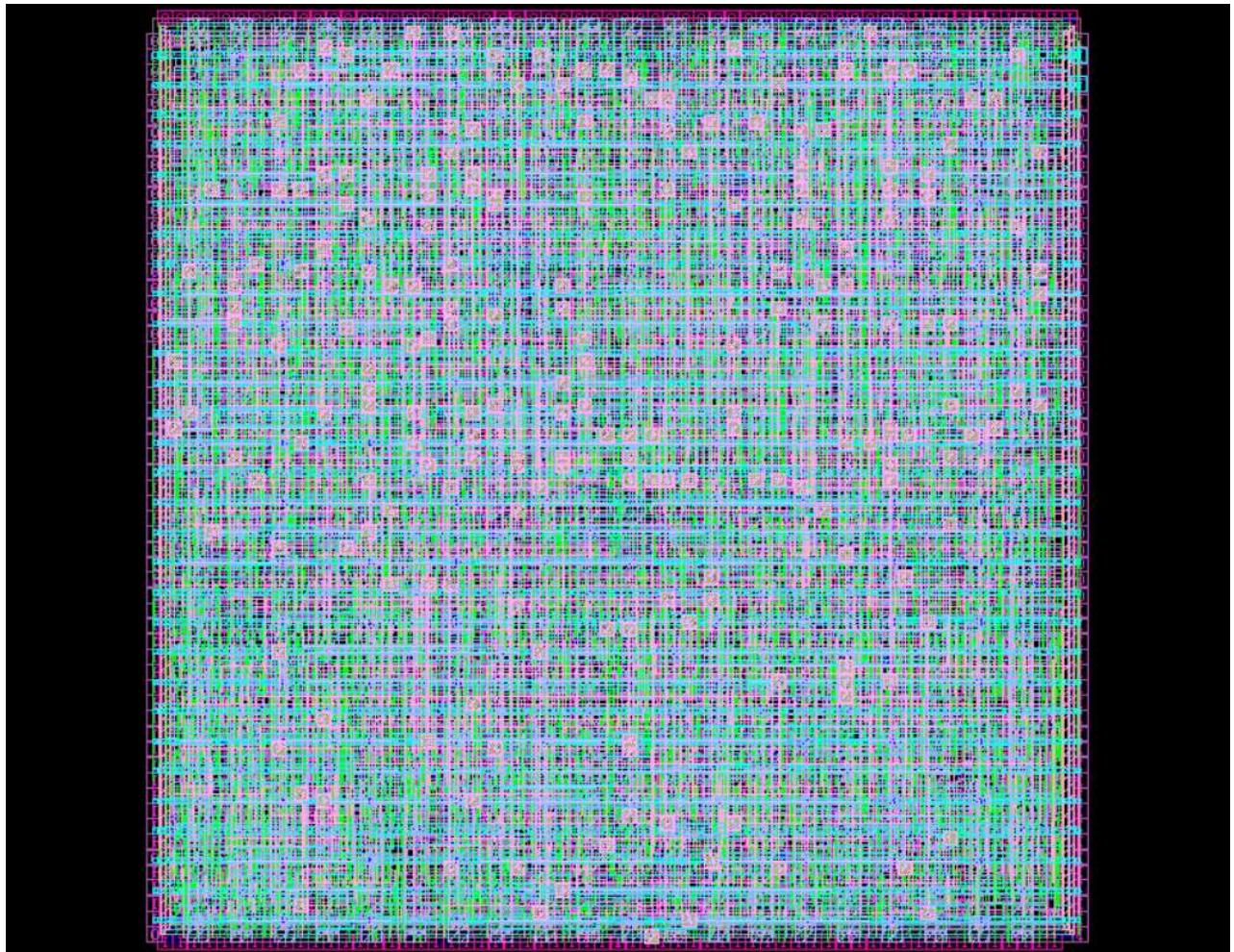
report\_qor -summary

```
-summary
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Fri Mar 29 10:42:39 2024
*****
Information: The stitching and editing of coupling caps is turned OFF for design 'riscv_block_8:msrv32_top.design'. (TIM-125)
Information: Design Average RC for design msrv32_top. (NEX-011)
Information: r = 1.076275 ohm/um, via_r = 0.459058 ohm/cut, c = 0.077313 ff/um, cc = 0.000000 ff/um (X dir) (NEX-017)
Information: r = 1.485994 ohm/um, via_r = 0.577011 ohm/cut, c = 0.099719 ff/um, cc = 0.000000 ff/um (Y dir) (NEX-017)
Information: The RC mode used is VR for design 'msrv32_top'. (NEX-022)
Information: Update timing completed net estimation for all the timing graph nets (TIM-111)
Information: Net estimation statistics: timing graph nets = 8989, routed nets = 0, across physical hierarchy nets = 0, parasitics cached nets = 8988, delay annotated nets = 0, parasitics annotated nets = 0, multi-voltage nets = 0. (TIM-112)
*****
Timer Settings:
Delay Calculation Style:          auto
Signal Integrity Analysis:       disabled
Timing Window Analysis:          disabled
Advanced Waveform Propagation:   disabled
Variation Type:                  fixed_deterate
Clock Reconvergence Pessimism Removal: enabled
Advanced Receiver Model:         disabled
ML Acceleration:                off
*****
Information: Timer using 'CRPR'. (TIM-050)

Timing
-----
Context           WNS      TNS      NVE
-----
Design    (Setup)    0.54      0.00      0
Design    (Hold)     0.22      0.00      0
-----
Miscellaneous
-----
Cell Area (netlist):            28013.53
Cell Area (netlist and physical only): 28013.53
Nets with DRC Violations:      593
```

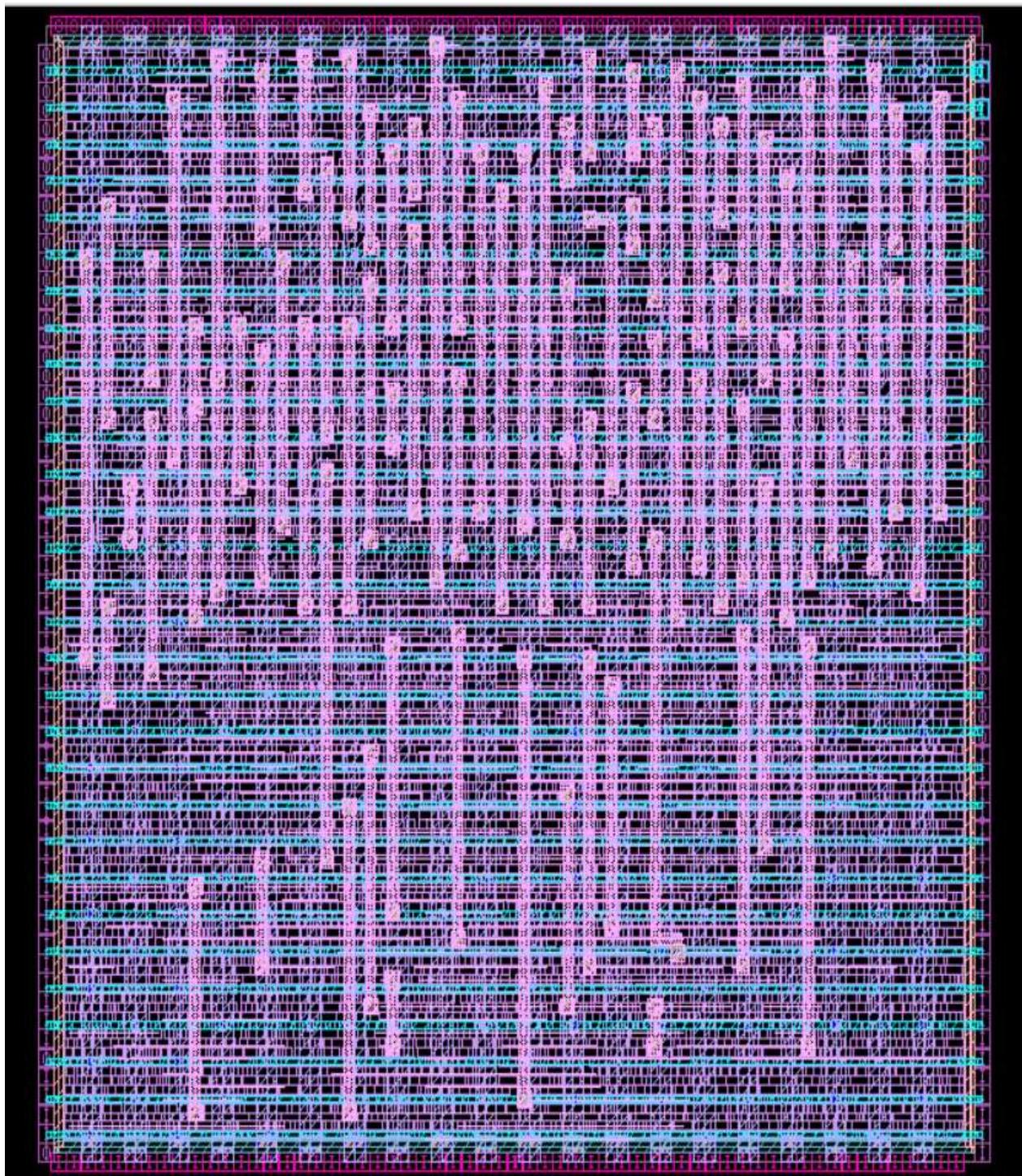
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clock\_opt



```
#routing
#set_routing_rule all -clear -default_rule -min_routing_layer 1 -max_routing_layer 9
route_auto -max_detail_route_iterations 30
route_eco
```

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To reduce DRC violations that occurs post routing , perform route optimization and if the violations are not completely fixed go for cell sizing or buffer insertion or removal of buffers.

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route\_opt

Number of max_transition violation(s): 0					
Mode: default Corner: default					
Scenario: default					
max_capacitance					
Net	Required Capacitance	Actual Capacitance	Slack	Violation	
IRF/ropt_net_145	16.00	16.09	-0.09	(VIOLATED)	
PIN : IRF/ropt_mt_inst_162/Y	16.00	16.09	-0.09	(VIOLATED)	
ms_riscv32_mp_imaddr_out[31]	8.00	8.09	-0.09	(VIOLATED)	
PIN : PC/i_addr_reg[31]/Q	8.00	8.09	-0.09	(VIOLATED)	
WBMUX/ropt_net_134	16.00	16.08	-0.08	(VIOLATED)	
PIN : WBMUX/ropt_mt_inst_151/Y	16.00	16.08	-0.08	(VIOLATED)	
IRF/ropt_net_534	16.00	16.08	-0.08	(VIOLATED)	
PIN : IRF/ropt_mt_inst_585/Y	16.00	16.08	-0.08	(VIOLATED)	
pc[1]	8.00	8.08	-0.08	(VIOLATED)	
PIN : REG1/pc_out_reg[1]/Q	8.00	8.08	-0.08	(VIOLATED)	
ALU/n421	16.00	16.06	-0.06	(VIOLATED)	
PIN : ALU/U398/Y	16.00	16.06	-0.06	(VIOLATED)	
IRF/ropt_net_416	16.00	16.06	-0.06	(VIOLATED)	
PIN : IRF/ropt_mt_inst_462/Y	16.00	16.06	-0.06	(VIOLATED)	
IRF/ropt_net_274	16.00	16.03	-0.03	(VIOLATED)	
PIN : IRF/ropt_mt_inst_301/Y	16.00	16.03	-0.03	(VIOLATED)	

Number of max\_capacitance violation(s): 8

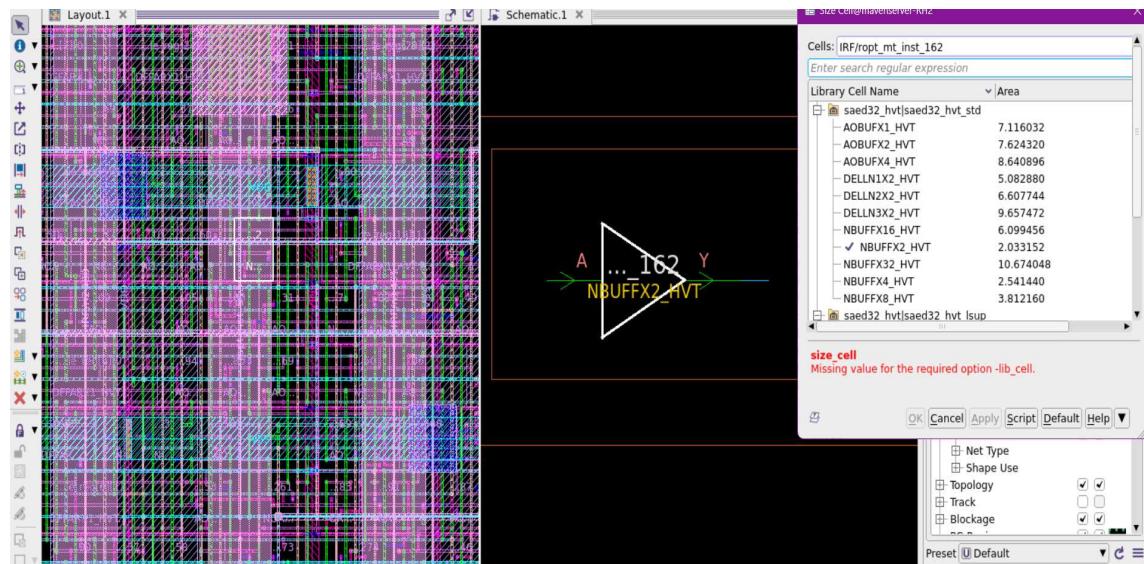
Mode: default Corner: default

Scenario: default

Number of min\_capacitance violation(s): 0

Total number of violation(s): 8

Cell sizing or we can proceed with adding buffers and remove unwanted extra nets



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## report\_constraints

```
*****
Report : constraint
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Fri Mar 29 11:27:38 2024
*****
```

Group (min_delay/hold)	Cost	Weight	Weighted		Scenario
			Cost	Scenario	
**default**	0.00	1.00	0.00	default	
**async_default**	0.00	1.00	0.00	default	
**clock_gating_default**	0.00	1.00	0.00	default	
**in2reg_default**	0.00	0.10	0.00	default	
**reg2out_default**	0.00	0.10	0.00	default	
**in2out_default**	0.00	0.10	0.00	default	
risc_v_clk	0.00	1.00	0.00	default	
min_delay/hold			0.00		
Group (max_delay/setup)	Cost	Weight	Weighted		Scenario
			Cost	Scenario	
**default**	0.00	1.00	0.00	default	
**async_default**	0.00	1.00	0.00	default	
**clock_gating_default**	0.00	1.00	0.00	default	
**in2reg_default**	0.00	0.10	0.00	default	
**reg2out_default**	0.00	0.10	0.00	default	
**in2out_default**	0.00	0.10	0.00	default	
risc_v_clk	0.00	1.00	0.00	default	
max_delay/setup			0.00		
Constraint	Cost				
min_delay/hold	0.00	(MET)			
max_delay/setup	0.00	(MET)			
max_transition	0.00	(MET)			
max_capacitance	0.00	(MET)			
min_capacitance	0.00	(MET)			

```
report_qor -summary
```

```
icc2_shell> report_qor -summary
*****
Report : qor
    -summary
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Fri Mar 29 11:32:20 2024
*****
Information: Timer using 'CRPR'. (TIM-050)

Timing
-----
Context          WNS      TNS      NVE
-----
Design (Setup)   0.00    0.00     0
Design (Hold)    0.12    0.00     0
-----

Miscellaneous
-----
Cell Area (netlist):           29642.09
Cell Area (netlist and physical only): 29642.08
Nets with DRC Violations:     0
```

```
check_lvs
```

```
Information: Using 1 threads for LVS
[Check Short] Stage 1 Elapsed = 0:00:00, CPU = 0:00:00
[Check Short] Stage 1-2 Elapsed = 0:00:00, CPU = 0:00:00
[Check Short] Stage 2 Elapsed = 0:00:01, CPU = 0:00:01
[Check Short] Stage 2-2 Elapsed = 0:00:07, CPU = 0:00:07
[Check Short] Stage 3 Elapsed = 0:00:07, CPU = 0:00:07
[Check Short] End Elapsed = 0:00:07, CPU = 0:00:07
[Check Net] Init Elapsed = 0:00:07, CPU = 0:00:07
[Check Net] 10% Elapsed = 0:00:09, CPU = 0:00:09
[Check Net] 20% Elapsed = 0:00:10, CPU = 0:00:10
[Check Net] 30% Elapsed = 0:00:11, CPU = 0:00:10
[Check Net] 40% Elapsed = 0:00:11, CPU = 0:00:10
[Check Net] 50% Elapsed = 0:00:11, CPU = 0:00:11
[Check Net] 60% Elapsed = 0:00:11, CPU = 0:00:11
[Check Net] 70% Elapsed = 0:00:11, CPU = 0:00:11
[Check Net] 80% Elapsed = 0:00:11, CPU = 0:00:11
[Check Net] 90% Elapsed = 0:00:11, CPU = 0:00:11
[Check Net] All nets are submitted.
[Check Net] 100% Elapsed = 0:00:12, CPU = 0:00:11
[Check Net] 100% Elapsed = 0:00:12, CPU = 0:00:11

=====
Maximum number of violations is set to 20
Abort checking when more than 20 violations are found
All violations might not be found.

=====
Total number of input nets is 9390.
Total number of short violations is 0.
Total number of open nets is 0.
Total number of floating route violations is 0.

Elapsed = 0:00:12, CPU = 0:00:11
1
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```

```
#script writing
write_script -force -format icc2 -output ../reports/riscv_spef
write_parasitics -output ../reports/riscv_spef_generation_1
write_sdf ../results/riscv_1.sdf
write_verilog ../results/riscv_1.v
write_gds ../results/riscv.gds
write_sdc -output ../results/riscv_v.sdc
```

## Reports

📁	riscv_spef		2024-03-27 14:21	DhanusHS	DhanusHS	drwxrwxr-x
📄	spef_generation_1.spef_scenario	1	2024-03-20 15:15	DhanusHS	DhanusHS	-rw-r-r--
📄	spef_generation_1.new_model_125.spef	3 165	2024-03-20 15:15	DhanusHS	DhanusHS	-rw-rw-r--
📄	riscv_spef_generation_1.spef_scenario	1	2024-03-27 14:21	DhanusHS	DhanusHS	-rw-rw-r--
📄	riscv_spef_generation_1.new_model_125.spef	18 298	2024-03-27 14:21	DhanusHS	DhanusHS	-rw-rw-r--

## Results

📄	riscv_v.sdc	1	2024-03-27 14:22	DhanusHS	DhanusHS	-rw-rw-r--
📄	riscv_1.v	1 007	2024-03-27 14:22	DhanusHS	DhanusHS	-rw-rw-r--
VMLINUX	riscv_1.sdf	5 615	2024-03-27 14:21	DhanusHS	DhanusHS	-rw-rw-r--
📄	riscv.gds	12 742	2024-03-27 14:22	DhanusHS	DhanusHS	-rw-rw-r--

report\_congestion (Post Routing)

```
icc2_shell> report_congestion
```

```
*****
```

```
Report : congestion
```

```
Design : msrv32_top
```

```
Version: T-2022.03-SP4
```

```
Date   : Fri Mar 29 11:53:34 2024
```

```
*****
```

Layer	overflow		# GRCs has	
Name	total	max	overflow (%)	max overflow
<hr/>				
Both Dirs	7810	6	6371 (20.89%)	1
H routing	5254	6	4134 (27.10%)	1
V routing	2556	3	2237 (14.67%)	28

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## report\_timing

```
icc2_shell> report_timing -path_type short
*****
Report : timing
    -path_type short
    -delay_type max
    -max_paths 1
    -report_by design
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Fri Mar 29 12:03:46 2024
*****
Information: Timer using 'CRPR'. (TIM-050)

Startpoint: MC/curr_state_reg[1] (rising edge-triggered flip-flop clocked by risc_v_clk)
Endpoint: MC/cause_out_reg[3] (rising edge-triggered flip-flop clocked by risc_v_clk)
Mode: default
Corner: default
Scenario: default
Path Group: risc_v_clk
Path Type: max

Point          Incr      Path
-----
clock risc_v_clk (rise edge)      0.00      0.00
clock network delay (propagated)  0.26      0.26
MC/curr_state_reg[1]/CLK (DFFX1_LVT) 0.00      0.26 r
MC/curr_state_reg[1]/Q (DFFX1_LVT)  0.20      0.45 f
...
MC/cause_out_reg[3]/D (DFFX1_RVT)   9.63     10.08 f
data arrival time                  10.08

clock risc_v_clk (rise edge)      10.00     10.00
clock network delay (propagated)  0.17      10.17
clock reconvergence pessimism    0.00      10.17
MC/cause_out_reg[3]/CLK (DFFX1_RVT) 0.00     10.17 r
library setup time                -0.08     10.09
data required time                10.09

data required time                10.09
data arrival time                 -10.08

-----
slack (MET)                      0.00
```

```
report_utilization
```

```
icc2_shell> report_utilization
*****
Report : report_utilization
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Fri Mar 29 12:12:56 2024
*****
Utilization Ratio:          0.7448
Utilization options:
- Area calculation based on: site_row of block msrv32_top
- Categories of objects excluded: hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area:                 39799.9670
Total Capacity Area:        39799.9670
Total Area of cells:        29642.0854
Area of excluded objects:
- hard_macros      : 0.0000
- macro_keepouts   : 0.0000
- soft_macros      : 0.0000
- io_cells         : 0.0000
- hard_blockages   : 0.0000
Utilization of site-rows with:
- Site 'unit':       0.7448
0.7448
```

## report\_power

```
Cell Internal Power = 5.23e+08 pW ( 78.5%)
Net Switching Power = 1.44e+08 pW ( 21.5%)
Total Dynamic Power = 6.67e+08 pW (100.0%)

Cell Leakage Power = 3.34e+08 pW
```

### Attributes

-----  
u - User defined power group  
i - Includes clock pin internal power

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	( % )	Attrs
io_pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	( 0.0%)	
memory	0.00e+00	0.00e+00	0.00e+00	0.00e+00	( 0.0%)	
black_box	0.00e+00	0.00e+00	0.00e+00	0.00e+00	( 0.0%)	
clock_network	4.67e+08	9.40e+07	7.12e+06	5.68e+08	( 56.8%)	i
register	2.85e+07	4.30e+06	1.07e+08	1.39e+08	( 13.9%)	
sequential	9.47e+05	5.18e+05	9.55e+06	1.10e+07	( 1.1%)	
combinational	2.64e+07	4.48e+07	2.11e+08	2.82e+08	( 28.2%)	
Total	5.23e+08 pW	1.44e+08 pW	3.34e+08 pW	1.00e+09 pW		

## report\_design

```
icc2_shell> report_design
*****
Report : design
Design : msrv32_top
Version: T-2022.03-SP4
Date   : Fri Mar 29 12:13:13 2024
*****

Total number of std cells in library : 1025
Total number of dont_use lib cells  : 80
Total number of dont_touch lib cells : 80
Total number of buffers            : 69
Total number of inverters          : 45
Total number of flip-flops         : 318
Total number of latches           : 36
Total number of ICGs              : 36

Cell Instance Type Count      Area
-----
TOTAL LEAF CELLS    8880  29642.085
Standard cells       8880  29642.085
Hard macro cells     0     0.000
Soft macro cells     0     0.000
Always on cells      0     0.000
Physical only        0     0.000
Fixed cells          0     0.000
Moveable cells        8880  29642.085
Sequential           1705  11651.740
Buffer/inverter      1333  2910.457
ICG cells            0     0.000

Logic Hierarchies      : 27
Design Masters count   : 159
Total Flat nets count  : 9186
Total FloatingNets count : 12
Total no of Ports      : 241
Number of Master Clocks in design : 1
Number of Generated Clocks in design : 0
Number of Path Groups in design : 7 (1 of them Non Default)
Number of Scan Chains in design : 0
List of Modes           : default
List of Corners         : default
List of Scenarios       : default

Core Area               : 39799.967
Chip Area               : 43055.967
Total Site Row Area     : 39799.967
Number of Blockages     : 0
Total area of Blockages : 0.000
Number of Power Domains : 1
Number of Voltage Areas : 1
Number of Group Bounds  : 0

Number of Exclusive MoveBounds : 0
Number of Hard or Soft MoveBounds : 0
Number of Multibit Registers : 0
Number of Multibit LS/ISO Cells : 0
Number of Top Level RP Groups : 0
Number of Tech Layers     : 71 (61 of them have unknown routing dir.)

Total wire length       : 305692.11 micron
Total number of wires    : 150400
Total number of contacts : 131860
```