

**Name:** Gowtham  
**Batch:** BPPD05

**Router 1x3\_Fusion Compiler**

```
#####
```

**### Source Files ###**

**# Script: run.tcl ###**

```
#####
```

```
echo "hello world"
source -echo ./setup.tcl
create_lib -technology $TECH_FILE -ref_libs $REFERENCE_LIBRARY router.dlib
analyze -format verilog [glob router_rtl/*.v]
elaborate router_top
set_top_module router_top
```

**#UPF file reading**

```
load_upf router_top.upf
commit_upf
check_mv_design
```

**#clock creation**

```
create_clock -period 3.0 [get_ports clock]
```

**#read parasitics**

```
read_parasitic_tech -layermap ..../ref/tech/saed32nm_tf_itf_tluplus.map -tlup
..../ref/tech/saed32nm_1p9m_Cmax.lv.nxtgrd -name maxTLU
read_parasitic_tech -layermap ..../ref/tech/saed32nm_tf_itf_tluplus.map -tlup
..../ref/tech/saed32nm_1p9m_Cmin.lv.nxtgrd -name minTLU
```

```
report_lib -parasitic_tech router.dlib
```

```
#
```

```
#####
```

**## MCMM Setup**

```
#####
```

```
source -echo mcmm_router_top.tcl
report_scenarios
foreach_in_collection mode [all_modes] {
    current_mode $mode
    remove_propagated_clocks [all_clocks]
    remove_propagated_clocks [get_ports]
    remove_propagated_clocks [get_pins -hierarchical]
}
```

```

current_mode
current_corner
current_scenario
current_corner ff_m40c
current_scenario
current_mode
current_scenario
current_scenario func.ff_m40c
current_mode
current_corner

#current_scenario func.ss_m40c
report_modes
view report_pvt

#####
compile_fusion
#####
compile_fusion -from initial_map -to initial_map
report_unloaded_registers
report_clock_gating
compile_fusion -from logic_opto -to logic_opto
create_test_protocol
dft_drc -v
set_app_option -name dft.insertion_post_logic_opto -value true
insert_dft
save_block
# review layout: auto-floorplan created, first wire-length driven placement

#####
compile_fusion -from initial_place -to initial_place
# review layout: buffering aware timing driven placement
all_high_transitive_fanout -nets -threshold 100
report_design
#####
compile_fusion -from initial_drc -to initial_drc
report_design
# cell count should have increased
all_high_transitive_fanout -nets -threshold 100
all_high_transitive_fanout -nets -threshold 40
get_scan_chain_count
# GUI: bring up congestion map
# This will run: report_congestion -rerun_global_router

#####
compile_fusion -from initial_opto -to initial_opto

```

```

get_scan_chain_count
# GUI: visualize scan chains
check_legality
report_optimization_history

#####
compile_fusion -from final_place -to final_place
# review layout: final placement, placement legalized
check_legality
report_qor -summary
report_power

#####
compile_fusion -from final_opto -to final_opto
report_power
report_qor -summary
Save_block

```

#####7th lab floorplan #####

#### Lab 1 - Floorplanning

```

initialize_floorplan -boundary {{133.937 110.633} {-4.535 110.633} {-4.535 48.769}
                                {75.873 48.769} {75.873 17.001} {-4.687 17.001} {-4.687 -1.391} {133.937 \
-1.391} {133.937 58.801} {55.657 58.801} {55.657 80.537} {133.937 80.537}} -core_offset
                                {5}

shape_blocks
create_placement -floorplan
set_block_pin_constraints -self -allowed_layers {M3 M4 M5 M6}
place_pins -self
change_selection [get_ports *clk]

```

##powerplan  
source scripts/pns.tcl

```
#####
Placement check_legalitylegalize_placement
place_opt
```

#####CTS#####3

```

report_clock_balance_points
report_clock_qor -type structure
## CTS NDRs
#####
```

```

source scripts/ndr.tcl
report_routing_rules -verbose
report_clock_routing_rules

## Timing and DRC Setup
#####
# Ensure that driving cells are specified on all clock ports
report_ports -verbose [get_ports *clock]
report_clocks -skew
report_clock_settings
clock_opt -to route_clock
report_qor -summary
current_mode
current_mode func
report_clocks
report_clocks -skew
report_clocks -groups
report_clock_qor -mode func
report_clocks

## Setup
#####
get_scenario -filter active&&hold
report_scenarios

## Final Checking prior to CTS
#####
check_clock_trees

#####
## Option A: Classic CTS
#####
clock_opt -to route_clock
report_clock_qor
report_clock_qor -type area
source scripts/margins_for_ccd.tcl
report_qor -summary
reset_app_options clock_opt.flow.enable_ccd
clock_opt -to route_clock
#####
## Post-CTS optimization
#####
report_scenarios

```

```

report_qor -summary
#Set up the design for signal routing
source scripts/route_setup.tcl
clock_opt -from final_opto
save_block

##### routing# Fusion Compiler
check_design -checks pre_route_stage

# Antenna
report_app_options route.detail.*antenna*
# Set application options for track and detail routing
set_app_options -name route.track.timing_driven -value true
set_app_options -name route.track.crosstalk_driven -value true
set_app_options -name route.detail.timing_driven -value true
set_app_options -name route.detail.force_max_number_iterations -value false
# Check the power supplies
Report_power_domains

## Routing
#####
route_auto
check_routes
report_global_timings
save_block

## Post-Route Timing Analysis
#####
# PTdelaycalc is on-by-default if time.enable_ccs_rcv_cap is true and CLIBs were
generated using LibraryManager >= 2018.06
# set_app_options -name time.use_pt_delay -value true

# Configure StarRC extraction
set_starrc_in_design -config ./scripts/starrc_config.txt
report_qor -summary
set_app_options -name time.si_enable_analysis -value true
set_app_options -name time.enable_ccs_rcv_cap -value true
# Will only work with CCS libraries:
set_app_options -name time.delay_calc_waveform_analysis_mode -value full_design
# set_app_options -name time.awp_compatibility_mode -value false ;# false by
default
report_qor -summary
report_qor -summary -pba_mode path

## Post-Route Optimization
#####

```

```

# power optimization, CCD, CTO are controlled via app options.
# report_app_options route_opt.*
# Note: For this lab, leave these disabled. Not required, and will lead to longer
runtimes...
# set_app_options -name route_opt.flow.enable_ccd -value true
# set_app_options -name ccd.post_route_buffer_removal -value true

route_opt
report_qor -summary

## To disable soft-rule-based timing optimization during ECO routing, uncomment the
following.
# This is to limit spreading which can touch multiple routes and impact convergence.
#set_app_options -name
route.detail.eco_route_use_soft_spacing_for_timing_optimization -value false
set_app_options -name route_opt.flow.enable_ccd -value false
# For more accuracy, you could switch to PBA now.
# For this lab, it's not necessary
# set_app_options -name time.pba_optimization_mode -value path
route_opt
report_qor -summary -pba_mode path

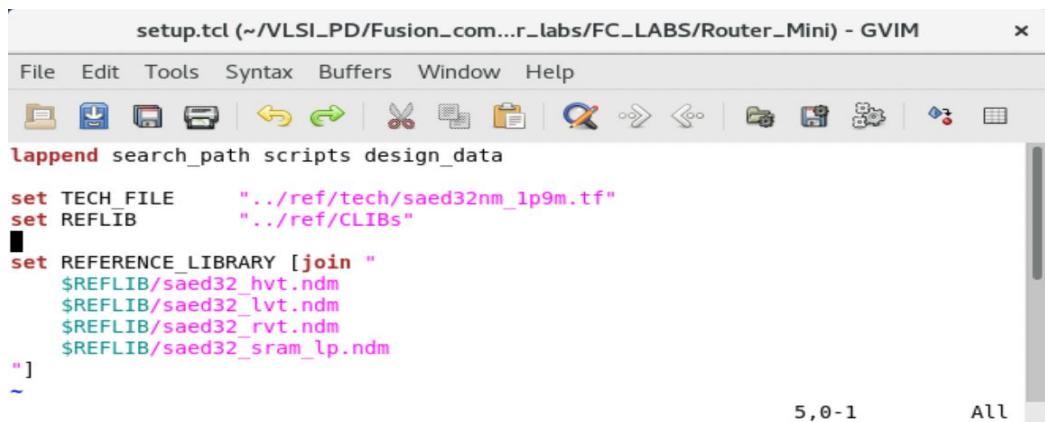
##
rename_block -to_block ORCA_TOP/route_opt
save_lib

```

RTL Files:

---

## Setup.tcl:

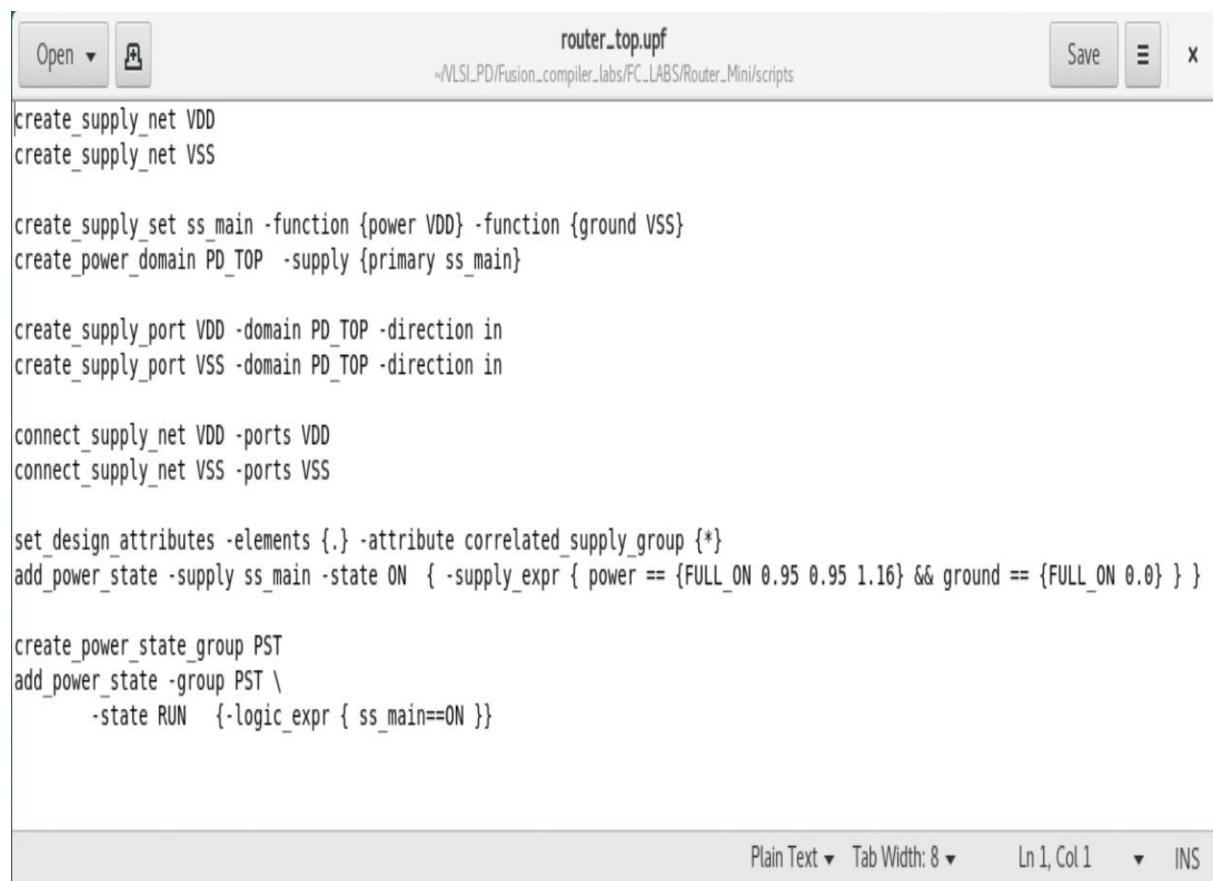


setup.tcl (~VLSI\_PD/Fusion\_com...r\_labs/FC\_LABS/Router\_Mini) - GVIM

```
File Edit Tools Syntax Buffers Window Help
lappend search_path scripts design_data
set TECH_FILE      "../ref/tech/saed32nm_1p9m.tf"
set REFLIB         "../ref/CLIBs"
set REFERENCE_LIBRARY [join "
$REFLIB/saed32_hvt.ndm
$REFLIB/saed32_lvt.ndm
$REFLIB/saed32_rvt.ndm
$REFLIB/saed32_sram_lp.ndm
"]
~
```

5,0-1 All

## router\_top.upf:



router\_top.upf  
~/VLSI\_PD/Fusion\_compiler\_labs/FC\_LABS/Router\_Mini/scripts

```
Open Save X
create_supply_net VDD
create_supply_net VSS

create_supply_set ss_main -function {power VDD} -function {ground VSS}
create_power_domain PD_TOP -supply {primary ss_main}

create_supply_port VDD -domain PD_TOP -direction in
create_supply_port VSS -domain PD_TOP -direction in

connect_supply_net VDD -ports VDD
connect_supply_net VSS -ports VSS

set_design_attributes -elements {*} -attribute correlated_supply_group {*}
add_power_state -supply ss_main -state ON { -supply_expr { power == {FULL_ON 0.95 0.95 1.16} && ground == {FULL_ON 0.0} } }

create_power_state_group PST
add_power_state -group PST \
    -state RUN {-logic_expr { ss_main==ON }}
```

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### mcmm\_router\_top.tcl:

```
mcmm_router_top.tcl = (~VLSI_P...C_LABS/Router_Mini/scripts) - GVIM x
File Edit Tools Syntax Buffers Window Help
remove_modes -all
remove_corners -all
remove_scenarios -all

create_corner ss_125c
set_parasitic_parameters -early_spec maxTLU -late_spec maxTLU
set_process_number 0.99
set_process_label slow
set_voltage -object_list VDD 0.95
set_voltage -object_list VSS 0.0
set_temperature 125
#
create_mode func
create_scenario -mode func -corner ss_125c
set_scenario_status func::ss_125c -hold true
~
~
~
```

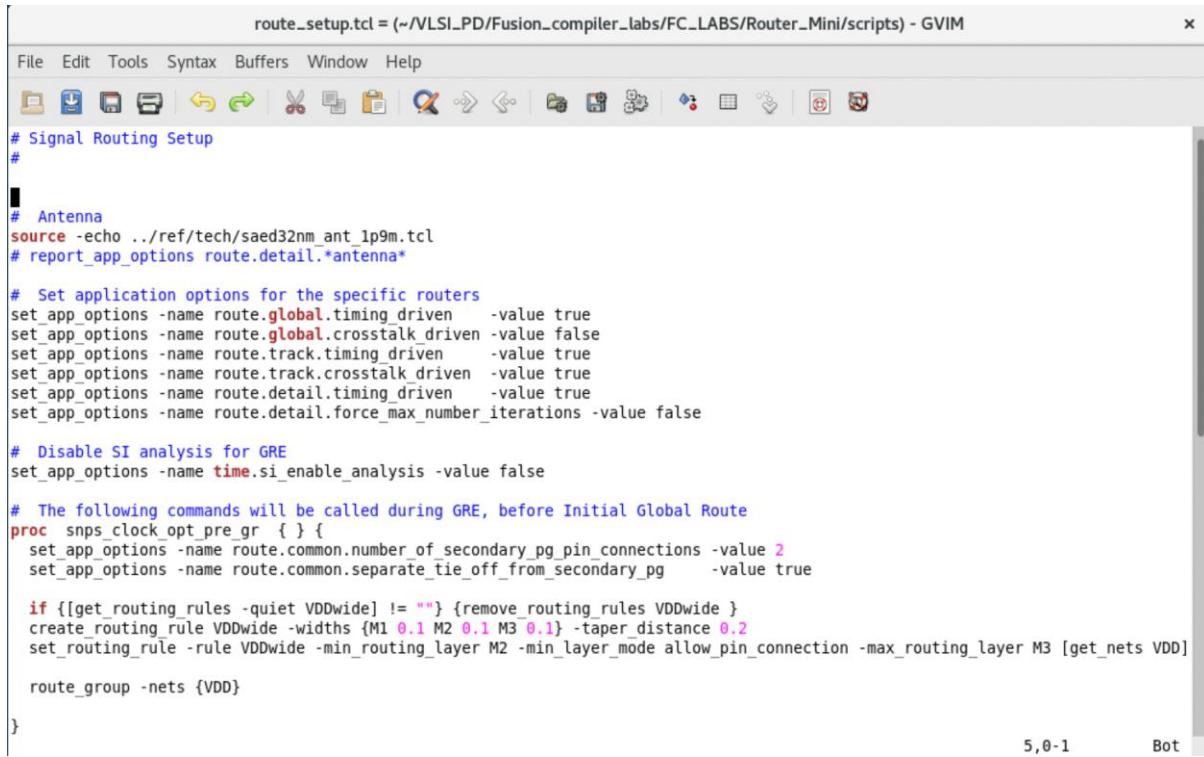
12,0-1 All

### pns.tcl:

```
pns.tcl (~VLSI_PD/Fusion_compiler_labs/FC_LABS/Router_Mini/scripts) - GVIM x
File Edit Tools Syntax Buffers Window Help
connect_pg_net -automatic
create_pg_mesh_pattern mesh_pattern -layers {{horizontal_layer: M9} {width: 2.4} {pitch: 24} {spacing: interleaving}} {{vertical_layer: M8} {width: 0 .84} {pitch: 8.4} {spacing: interleaving}} {{horizontal_layer: M7} {width: 0.84} {pitch: 8.4} {spacing: interleaving}} {{vertical_layer: M6} {width: 0 .84} {pitch: 8.4} {spacing: interleaving}}
set_pg_strategy mesh_strategy -core -pattern {{pattern: mesh_pattern}{nets: {VDD VSS}}} -blockage {macros: all}
create_pg_std_cell_conn_pattern std_cell_pattern
set_pg_strategy std_cell_strategy -core -pattern {{pattern: std_cell_pattern}{nets: {VDD VSS}}}
compile_pg -ignore_via_drc
#
~
~
~
~
~
~
```

8,0-1 All

### route\_setup.tcl:



The screenshot shows a GVIM window with the title "route\_setup.tcl = (~VLSI\_PD/Fusion\_compiler\_labs/FC\_LABS/Router\_Mini/scripts) - GVIM". The menu bar includes File, Edit, Tools, Syntax, Buffers, Window, and Help. Below the menu is a toolbar with various icons. The main text area contains a TCL script for signal routing setup. The script includes comments, source commands, and various set\_app\_options commands to configure routers and disable SI analysis for GRE. It also defines a proc for smps\_clock\_opt\_pre\_gr and uses if statements for routing rules.

```
route_setup.tcl = (~VLSI_PD/Fusion_compiler_labs/FC_LABS/Router_Mini/scripts) - GVIM
File Edit Tools Syntax Buffers Window Help
# Signal Routing Setup
#
# Antenna
source -echo ../ref/tech/saed32nm_ant_1p9m.tcl
# report_app_options route.detail.*antenna*

# Set application options for the specific routers
set_app_options -name route.global.timing_driven -value true
set_app_options -name route.global.crosstalk_driven -value false
set_app_options -name route.track.timing_driven -value true
set_app_options -name route.track.crosstalk_driven -value true
set_app_options -name route.detail.timing_driven -value true
set_app_options -name route.detail.force_max_number_iterations -value false

# Disable SI analysis for GRE
set_app_options -name time.si_enable_analysis -value false

# The following commands will be called during GRE, before Initial Global Route
proc smps_clock_opt_pre_gr {} {
    set_app_options -name route.common.number_of_secondary_pg_pin_connections -value 2
    set_app_options -name route.common.separate_tie_off_from_secondary_pg -value true

    if {[get_routing_rules -quiet VDDwide] != ""} {remove_routing_rules VDDwide}
    create_routing_rule VDDwide -widths {M1 0.1 M2 0.1 M3 0.1} -taper_distance 0.2
    set_routing_rule -rule VDDwide -min_routing_layer M2 -min_layer_mode allow_pin_connection -max_routing_layer M3 [get_nets VDD]
}

route_group -nets {VDD}
}

#####
##### Setup #####
source -echo ./setup.tcl

create_lib -technology $TECH_FILE -ref_libs $REFERENCE_LIBRARY router_mini.dlib
save_lib
analyze -format verilog [glob rtl/*.v]

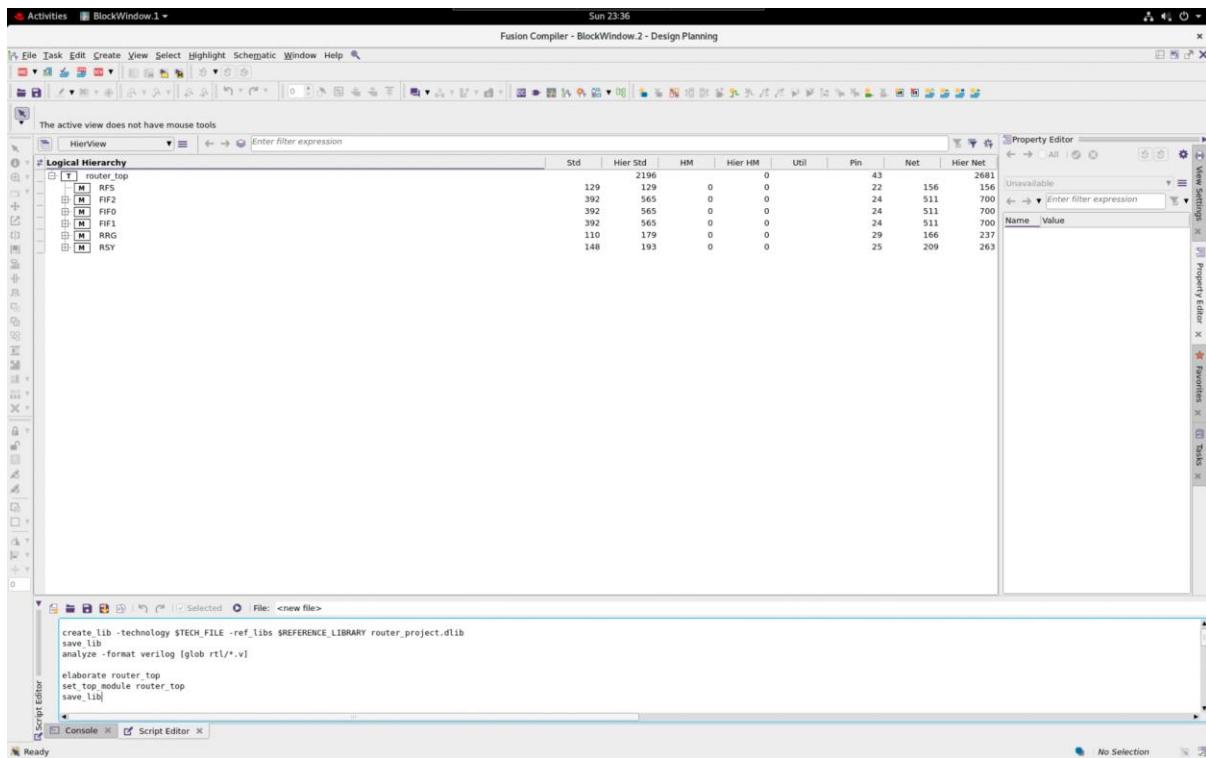
elaborate router_top
set_top_module router_top
Save_lib
```

### ### Setup ###

```
source -echo ./setup.tcl

create_lib -technology $TECH_FILE -ref_libs $REFERENCE_LIBRARY router_mini.dlib
save_lib
analyze -format verilog [glob rtl/*.v]

elaborate router_top
set_top_module router_top
Save_lib
```



### **### Technology Setup ###**

```

read_parasitic_tech -layermap ..//ref/tech/saed32nm_tf_itf_tluplus.map -tlup
..//ref/tech/saed32nm_1p9m_Cmax.lv.nxtgrd -name maxTLU
read_parasitic_tech -layermap ..//ref/tech/saed32nm_tf_itf_tluplus.map -tlup
..//ref/tech/saed32nm_1p9m_Cmin.lv.nxtgrd -name minTLU

```

```
report_lib -parasitic_tech router_core.dlib
```

```

get_site_defs
set_attribute [get_site_defs unit] symmetry Y
set_attribute [get_site_defs unit] is_default true

```

```

set_attribute [get_layers {M1 M3 M5}] routing_direction horizontal
set_attribute [get_layers {M2 M4}] routing_direction vertical
get_attribute [get_layers M?] routing_direction

```

```

report_ignored_layers
set_ignored_layers -max_routing_layer M5
report_ignored_layers

```

### **### UPF ###**

```
load_upf ./scripts/router_top.upf
```

```
commit_upf  
check_mv_design
```

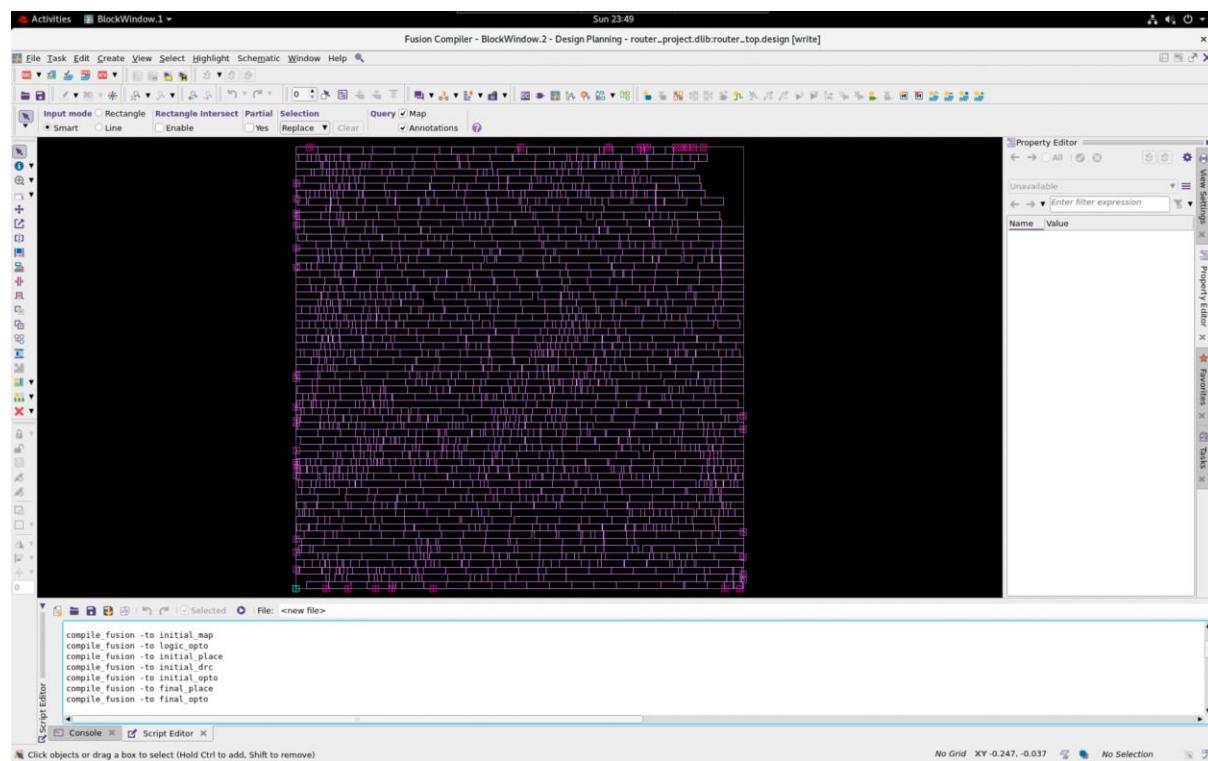
### **### Modes And Corners ###**

```
source ./scripts/mcmm_router_top.tcl  
report_scenario
```

### **### Stages Of Compile Fusion ###**

```
set_app_option -name dft.insertion_post_logic_opto -value false  
set_app_option -name place.coarse.continue_on_missing_scandef -value true  
compile_fusion -to initial_map  
compile_fusion -to logic_opto  
compile_fusion -to initial_place  
compile_fusion -to initial_drc  
compile_fusion -to initial_opto  
compile_fusion -to final_place  
compile_fusion -to final_opto
```

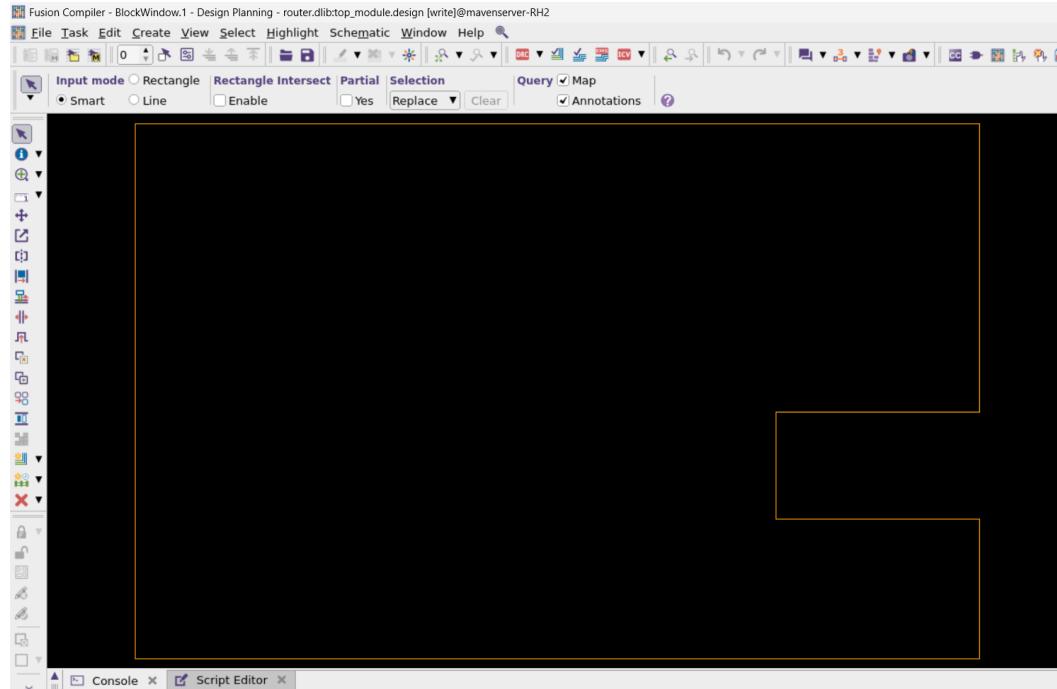
```
save_lib  
save_block
```



### ### Floor Planning ###

initialize\_floorplan

```
initialize_floorplan -boundary {{28.286 142.320} {64.520 142.320} {64.520 95.719} {102.612  
95.719} {102.612 48.359} {64.520 48.359} {64.520 1.758} {28.286 1.758} {28.286 48.359} {-  
9.108 48.359} {-9.108 95.719} {28.286 95.719}} -core_offset \
```



shape\_blocks

create\_placement -floorplan

Legalize\_placement

set\_block\_pin\_constraints -self -allowed\_layers {M1 M2 M3 M4 M5 M6 M7 M8}

place\_pins -self

change\_selection [get\_ports \*clock]

gui\_set\_setting -window [gui\_get\_current\_window -types Layout -mru] -setting

showPinGuide -value true

create\_pin\_guide \

-boundary {{105.118 46.211} {111.728 98.112}} [get\_ports \

-design [current\_block] {{data\_out\_2[6]} {data\_out\_2[7]} {data\_out\_2[5]} {data\_out\_2[4]}  
{data\_out\_2[3]} {data\_out\_2[2]} {data\_out\_0[0]} {data\_out\_0[5]} valid\_out\_1 valid\_out\_0

{data\_out\_0[6]} {data\_out\_0[2]} busy error {data\_out\_0[3]} {data\_out\_0[4]} valid\_out\_2

{data\_out\_0[1]} {data\_out\_0[7]} {data\_out\_2[0]} {data\_out\_1[0]} {data\_out\_1[1]}

{data\_out\_1[2]} {data\_out\_1[3]} {data\_out\_1[4]} {data\_out\_1[5]} {data\_out\_1[6]}

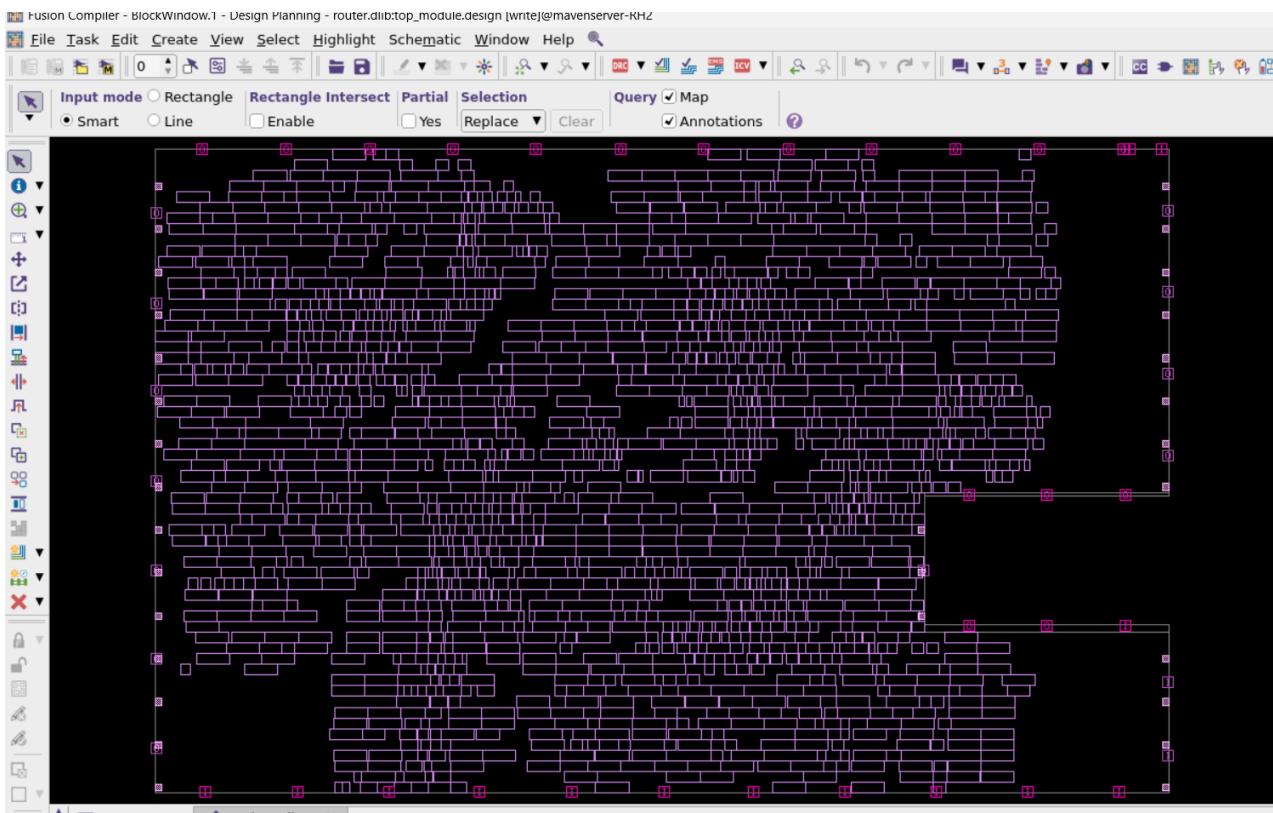
{data\_out\_1[7]} {data\_out\_2[1]}}

create\_pin\_guide \

-boundary {{-19.518 46.161} {-11.755 98.858}} [get\_ports \

-design [current\_block] {resetn read\_enb\_2 read\_enb\_1 {data\_in[3]} {data\_in[1]} clock  
{data\_in[2]} {data\_in[0]} {data\_in[4]} {data\_in[6]} {data\_in[7]} {data\_in[5]} pkt\_valid

read\_enb\_0]}



```
create_pin_constraint -type individual -ports [get_ports *clock] -width 0.1 -length 0.4  
place_pins -self  
report_block_shaping -utilization_from_target -core_areaViolations -overlaps -  
chimney_area -detour_estimate -unaligned_pins_estimate -flyline_crossing -  
orientation_violations -hierarchical  
report_placement -physical_hierarchy_violations all -wirelength all -swimming_pool_area -  
thin_channel_area -hard_macro_overlap -user_grid -hierarchical -ignore_fixed -poly_rule -  
macro_spacing_rule  
connect_pg_net -automatic
```

```
source -echo scripts/pns.tcl
```

### ### Check PG NETS DRC ####

```
check_pg_connectivity  
check_pg_drc  
check_pg_missing_vias  
check_lvs  
save_lib  
save_block
```

### **### SDC ###**

```
report_clock  
create_clock -period 10.0 -name router_clock [get_ports clock]
```

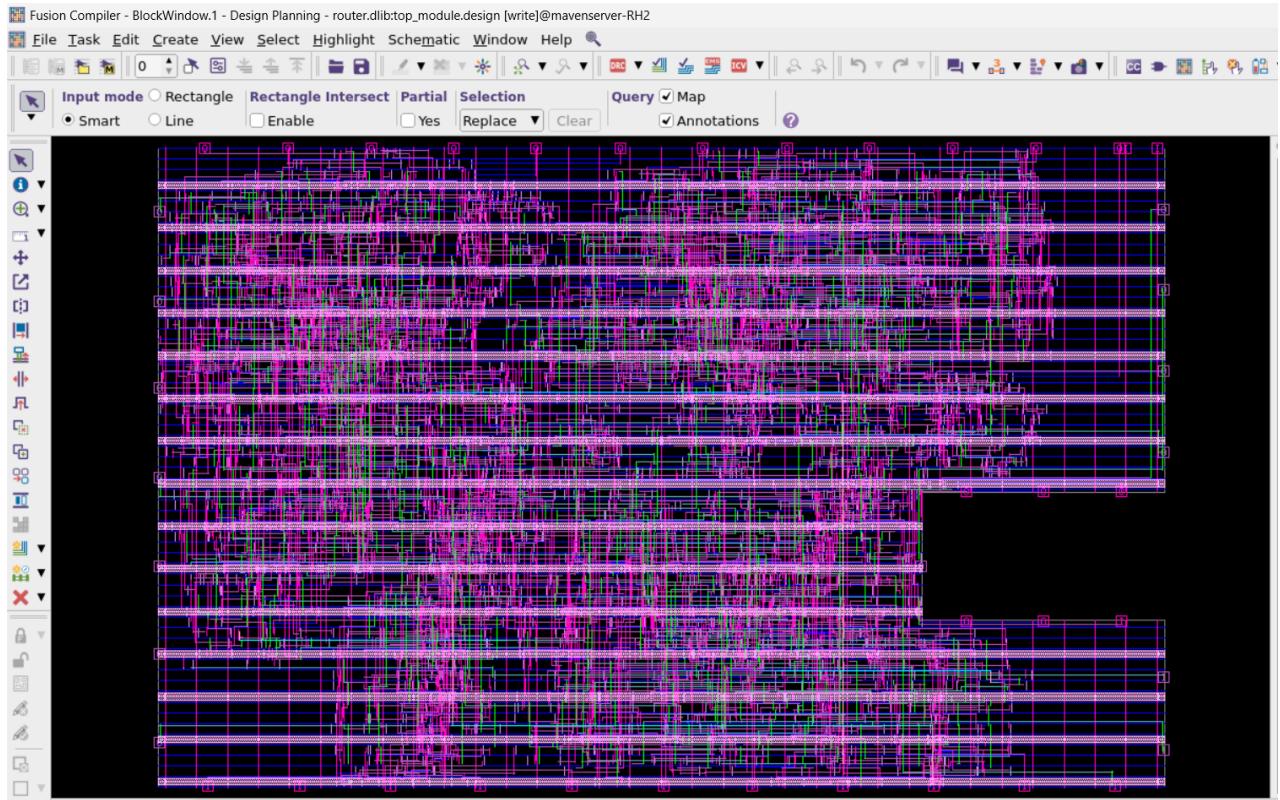
### **### Classic CTS ###**

```
set_app_options -name clock_opt.flow.enable_ccd -value false  
set_app_options -name cts.compile.enable_local_skew -value true  
set_app_options -name cts.optimize.enable_local_skew -value true  
clock_opt -to route_clock
```

```
report_clock_qor
```

### **### Post-CTS Optimization ###**

```
report_scenarios  
report_qor -summary  
  
source scripts/route_setup.tcl  
  
clock_opt -from final_opto  
  
save_block
```



### **### Pre-Route ###**

```
report_timing
```

```
report_qor -summary
```

```
set_app_options -name route.common.verbose_level -value 1
```

```
check_design -checks pre_route_stage
```

```
set_app_options -name route.common.verbose_level -value 0
```

```
source -echo ..//ref/tech/saed32nm_ant_1p9m.tcl
```

```
report_app_options route.detail.*antenna*
```

```
set_app_options -name route.track.timing_driven -value true
```

```
set_app_options -name route.track.crosstalk_driven -value true
```

```
set_app_options -name route.detail.timing_driven -value true
```

```
set_app_options -name route.detail.force_max_number_iterations -value false
```

```
report_power_domains
```

```
change_selection [get_cells -hierarchical -filter {is_level_shifter&&full_name=~*ROUTER*}]
```

```
#####
#####
```

### **### Routing ###**

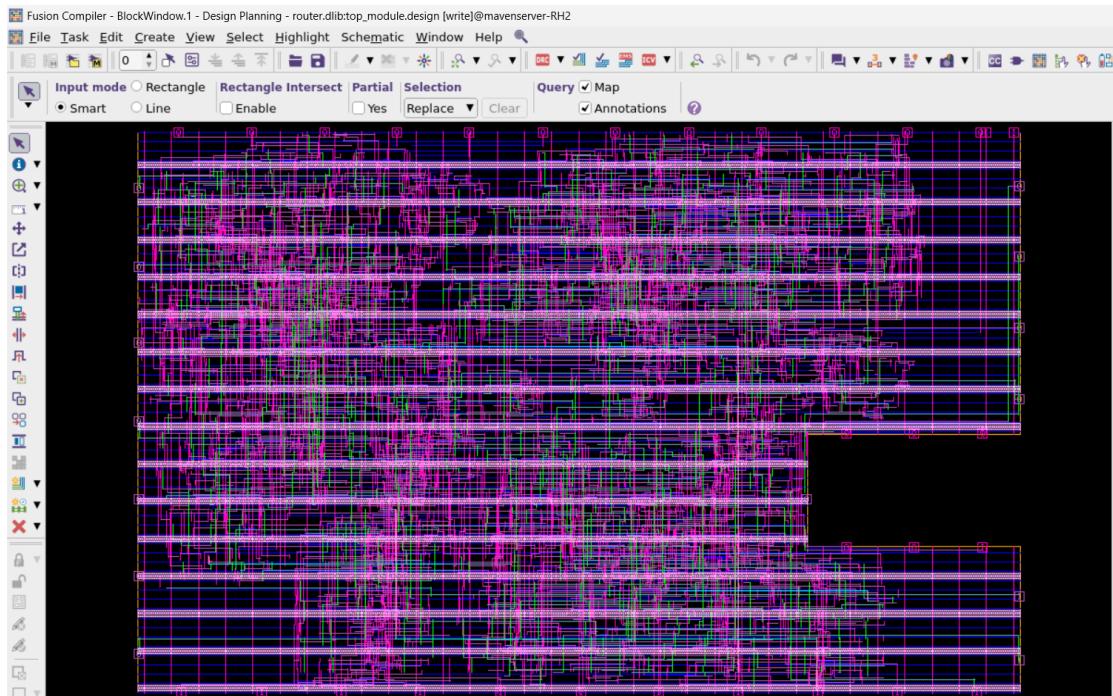
```
route_auto
```

```
check_routes
```

```
route_detail -incremental true -initial_drc_from_input true
```

```
route_eco -utilize_dangling_wires true -open_net_driven true
```

## Save block



```
#####
### Post-Route Timing Analysis ###
```

```
set_app_options -name time.use_pt_delay -value true  
report_qor -summary  
set_app_options -name time.si_enable_analysis -value true  
set_app_options -name time.enable_ccs_rcv_cap -value true
```

```
set_app_options -name time.delay_calc_waveform_analysis_mode -value full_design  
report_qor -summary  
report_qor -summary -pba_mode path
```

```
#####
### Post-Route Optimization ###
```

```
route_opt  
report_qor -summary
```

```
set_app_options -name route_opt.flow.enable_ccd -value false
```

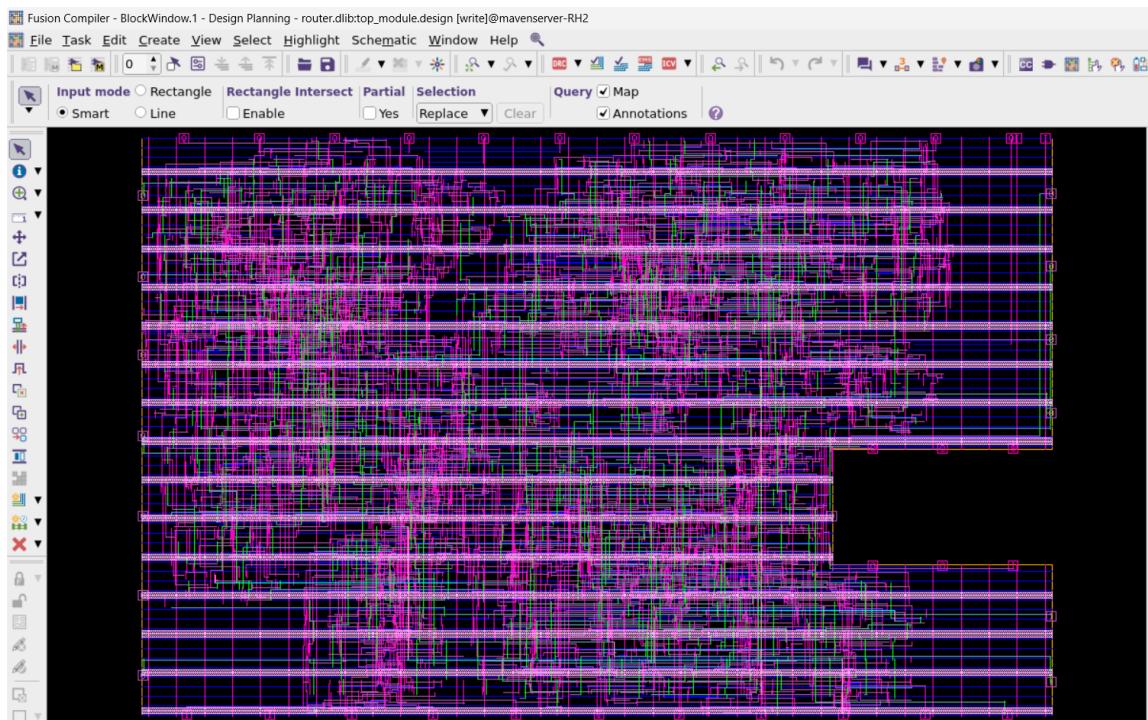
```
route_opt  
report_qor -summary -pba_mode path
```

```
rename_block -to_block Router_Mini/route_opt  
save_lib
```

```
report_qor -summary
```

```
#####
```

## Final Layout View



## ### Reports ###

### Report\_qor

```
Fusion Compiler - BlockWindow.1 - Design Planning - router.dlib:router_top.design [write]@mavenserver-RH2
File Task Edit Create View Select Highlight Schematic Window Help

fc shell> report_qor
0
=====
Report : qor
Design : router_top
Version: U-2022.12
Date  : Thu Feb 29 01:05:04 2024
=====
Warning: Corner ff_m40c: 0 process number, 0 process label, 2 voltage, and 0 temperature mismatches. (PVT-030)
Warning: 1 cells affected for early, 1 for late. (PVT-031)
Warning: 0 port driving_cells affected for early, 0 for late. (PVT-034)
INFO: updateGlobalOptions
INFO: use Native GDC
Information: The stitching and editing of coupling caps is turned OFF for design 'router.dlib:router_top.design'. (TIM-125)
Information: Design router_top has 1540 nets, 0 global routed, 1538 detail routed. (NEX-024)
Information: The RC mode used is DR for design 'router_top'. (NEX-022)
---extraction options---
Corner: ff_m40c
late_cap_scale      : 1
late_res_scale      : 1
early_cap_scale     : 1
early_res_scale     : 1
Global options:
reference_direction   : use_from_tluplus
real_metalfill_extraction : none
virtual_shield_extraction : true
---app options---
host.max_cores       : 1
extract.connect_open  : true
extract.enable_coupling_cap : false
Extracting design: router_top
Information: coupling capacitance is lumped to ground. (NEX-030)
Information: 1538 nets are successfully extracted. (NEX-028)
Warning: Advanced receiver model has not been enabled for detailed routed design. (TIM-204)

Log History
```

```

Fusion Compiler - BlockWindow.1 - Design Planning - router.dlib:router_top.design [write]@mavenserver-RH2
File Task Edit Create View Select Highlight Schematic Window Help 🔎

Warning: Advanced receiver model has not been enabled for detailed routed design. (TIM-204)
Information: Update timing completed net estimation for all the timing graph nets (TIM-111)
Information: Net estimation statistics: timing graph nets = 1538, routed nets = 1538, across physical hierarchy nets = 0, parasitics cached nets = 1538, del ****
*****  

Timer Settings:  

Delay Calculation Style: auto  

Signal Integrity Analysis: disabled  

Timing Window Analysis: disabled  

Advanced Waveform Propagation: disabled  

Variation Type: fixed_determinate  

Clock Reconvergence Pessimism Removal: disabled  

Advanced Receiver Model: disabled  

ML Acceleration: off  

*****  

*****  

Scenario 'func.ff_m40c'  

Timing Path Group '**in2reg_default**'  

-----  

Levels of Logic: 9  

Critical Path Length: 0.88  

Critical Path Slack: 29.15  

Critical Path Clk Period: 30.00  

Total Negative Slack: 0.00  

No. of Violating Paths: 0  

-----  

Scenario 'func.ff_m40c'  

Timing Path Group '**reg2out_default**'  

-----  

Levels of Logic: 7  

Critical Path Length: 0.31  

Critical Path Slack: 29.00  

Critical Path Clk Period: 30.00  

Total Negative Slack: 0.00  

No. of Violating Paths: 0  

-----  


```

```

Fusion Compiler - BlockWindow.1 - Design Planning - router.dlib:router_top.design [write]@mavenserver-RH2
File Task Edit Create View Select Highlight Schematic Window Help 🔎

Critical Path Length: 0.31
Critical Path Slack: 29.00
Critical Path Clk Period: 30.00
Total Negative Slack: 0.00
No. of Violating Paths: 0
-----  

Scenario 'func.ff_m40c'
Timing Path Group 'clock'
-----  

Levels of Logic: 14
Critical Path Length: 0.56
Critical Path Slack: 29.18
Critical Path Clk Period: 30.00
Total Negative Slack: 0.00
No. of Violating Paths: 0
-----  

Cell Count
-----  

Hierarchical Cell Count: 0
Hierarchical Port Count: 0
Leaf Cell Count: 1482
Buf/Inv Cell Count: 119
Buf Cell Count: 58
Inv Cell Count: 61
CT Buf/Inv Cell Count: 0
Combinational Cell Count: 831
    Single-bit Isolation Cell Count: 0
    Multi-bit Isolation Cell Count: 0
    Isolation Cell Banking Ratio: 0.00%
    Single-bit Level Shifter Cell Count: 1
    Multi-bit Level Shifter Cell Count: 0

```

```
Fusion Compiler - BlockWindow.1 - Design Planning - router.dlib:router_top.design [write]@mavenserver-RH2
File Task Edit Create View Select Highlight Schematic Window Help

Single-bit ELS Cell Count: 0
Multi-bit ELS Cell Count: 0
ELS Cell Banking Ratio: 0.00%
Sequential Cell Count: 651
Integrated Clock-Gating Cell Count: 77
Sequential Macro Cell Count: 0
Single-bit Sequential Cell Count: 574
Multi-bit Sequential Cell Count: 0
Sequential cell Banking Ratio: 0.00%
BitsPerflop: 1.00
Macro Count: 0

Area
-----
Combinational Area: 2265.95
Noncombinational Area: 6959.23
Buf/Inv Area: 304.97
Total Buffer Area: 222.12
Total Inverter Area: 82.85
Macro/Black Box Area: 0.00
Net Area: 0
Net XLength: 16084.63
Net YLength: 15814.31
-----
Cell Area (netlist): 9225.17
Cell Area (netlist and physical only): 9225.17
Net Length: 31898.94

Design Rules
-----
Total Number of Nets: 1540

Console
Log History
fc_shell>
```

```
Fusion Compiler - BlockWindow.1 - Design Planning - router.dlib:router_top.design [write]@mavenserver-RH2
File Task Edit Create View Select Highlight Schematic Window Help

Multi-bit Sequential Cell Count: 0
Sequential Cell Banking Ratio: 0.00%
BitsPerflop: 1.00
Macro Count: 0

Area
-----
Combinational Area: 2265.95
Noncombinational Area: 6959.23
Buf/Inv Area: 304.97
Total Buffer Area: 222.12
Total Inverter Area: 82.85
Macro/Black Box Area: 0.00
Net Area: 0
Net XLength: 16084.63
Net YLength: 15814.31
-----
Cell Area (netlist): 9225.17
Cell Area (netlist and physical only): 9225.17
Net Length: 31898.94

Design Rules
-----
Total Number of Nets: 1540
Nets with Violations: 0
Max Trans Violations: 0
Max Cap Violations: 0

1
fc_shell>

Console
Log History
fc_shell>
```

## Report\_constraints -all\_violators

```
fc_shell> report_constraint -all_violators
*****
Report : constraint
      -all_violators
Design : router_top
Version: U-2022.12
Date   : Wed Feb 28 23:01:15 2024
*****
late_timing
-----
Information: Timer using 1 threads
Warning: Corner ff_m40c: 0 process number, 0 process label, 2 voltage, and 0 temperature mismatches. (PVT-030)
Warning: 1 cells affected for early, 1 for late. (PVT-031)
Warning: 0 port driving cells affected for early, 0 for late. (PVT-034)
INFO: updateGlobalOptions
INFO: use Native GDC
Information: The stitching and editing of coupling caps is turned OFF for design 'router.dlib:router_top.design'. (TIM-125)
Information: Design router_top has 1540 nets, 0 global routed, 1538 detail routed. (NEX-024)
Information: The RC mode used is DR for design 'router_top'. (NEX-022)
--extraction options---
Corner: ff_m40c
late_cap_scale      : 1
late_res_scale      : 1
early_cap_scale     : 1
early_res_scale     : 1
Global options:
reference direction : use_from_tluplus
real_metalfill_extraction : none
virtual_shield_extraction : true
--app options---
host_max_cores      : 1
extract.connect_open : true
Extracting design: router_top
Information: coupling capacitance is lumped to ground. (NEX-030)
Information: 1538 nets are successfully extracted. (NEX-028)
Warning: Advanced receiver model has not been enabled for detailed routed design. (TIM-204)
Information: Update timing completed net estimation for all the timing graph nets (TIM-111)
Information: Net estimation statistics: timing graph nets = 1538, routed nets = 1538, across physical hierarchy nets = 0, parasitics cached nets = 1538, d
*****
Timer Settings:
Delay Calculation Style:          auto
Signal Integrity Analysis:        disabled
Timing Window Analysis:          disabled
Advanced Waveform Propagation:    disabled
Variation Type:                  fixed_determinate
Clock Reconvergence Pessimism Removal: disabled
Advanced Receiver Model:         disabled
ML Acceleration:                 off
*****
Endpoint          Path Delay  Path Required  CRP  Slack Group Scenario
-----  
No paths.

early_timing
-----
Warning: Scenario func.ff_m40c is not configured for hold analysis: skipping. (UIC-058)
Error: None of the specified scenarios are active for hold analysis. (UIC-057)
Endpoint          Path Delay  Path Required  CRP  Slack Group Scenario
-----  
No paths.

Mode: func Corner: ff_m40c
fc_shell>
```

```
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) No Grid XY 166.775, -5.820 Script Editor 23:05 28-02-2024
24°C Partly cloudy Search ENG IN
Fusion Compiler - BlockWindow.1 - Design Planning - router.dlib:router_top.design [write]@mavenserver-RH2
File Task Edit Create View Select Highlight Schematic Window Help
fc_shell> report_constraint -all_violators
*****
Report : constraint
      -all_violators
Design : router_top
Version: U-2022.12
Date   : Wed Feb 28 23:01:15 2024
*****
host.max_cores      : 1
extract.connect_open : true
extract.enable_coupling_cap : false
Extracting design: router_top
Information: coupling capacitance is lumped to ground. (NEX-030)
Information: 1538 nets are successfully extracted. (NEX-028)
Warning: Advanced receiver model has not been enabled for detailed routed design. (TIM-204)
Information: Update timing completed net estimation for all the timing graph nets (TIM-111)
Information: Net estimation statistics: timing graph nets = 1538, routed nets = 1538, across physical hierarchy nets = 0, parasitics cached nets = 1538, d
*****
Timer Settings:
Delay Calculation Style:          auto
Signal Integrity Analysis:        disabled
Timing Window Analysis:          disabled
Advanced Waveform Propagation:    disabled
Variation Type:                  fixed_determinate
Clock Reconvergence Pessimism Removal: disabled
Advanced Receiver Model:         disabled
ML Acceleration:                 off
*****
Endpoint          Path Delay  Path Required  CRP  Slack Group Scenario
-----  
No paths.

early_timing
-----
Warning: Scenario func.ff_m40c is not configured for hold analysis: skipping. (UIC-058)
Error: None of the specified scenarios are active for hold analysis. (UIC-057)
Endpoint          Path Delay  Path Required  CRP  Slack Group Scenario
-----  
No paths.

Mode: func Corner: ff_m40c
fc_shell>
```

Fusion Compiler - BlockWindow.1 - Design Planning - router.dlib:router\_top.design [write]@mavenserver-RH2

**File Task Edit Create View Select Highlight Schematic Window Help**

```

0 Mode: func Corner: ff_m40c
Scenario: func.ff_m40c
max_transition
Required Actual
Net Transition Transition Slack Violation
-----
dout[3] 0.05 0.04 0.00 (MET)

Number of max_transition violation(s): 0

Mode: func Corner: ff_m40c
Scenario: func.ff_m40c
max_capacitance
Required Actual
Net Capacitance Capacitance Slack Violation
-----
aps_rename_25_ 8.00 7.95 0.05 (MET)

Number of max_capacitance violation(s): 0

Mode: func
Corner: ff_m40c
Scenario: func.ff_m40c

Number of min_pulse_width violation(s): 0
Total number of violation(s): 0
1 fc_shell>

```

Console Log History fc\_shell> report\_constraint -all\_violators

Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) No Grid XY 166.775, -5.820 23:06 ENG IN 28-02-2024 Script Editor No Selection

Nets with DRC Violations: 0  
 Total number of violations: 0

## Report\_design

Fusion Compiler - BlockWindow.1 - Design Planning - router.dlib:router\_top.design [write]@mavenserver-RH2

**File Task Edit Create View Select Highlight Schematic Window Help**

```

fc_shell> report_design
*****
Report : design
Design : router_top
Version: U-2022.12
Date : Thu Feb 29 01:19:01 2024
*****

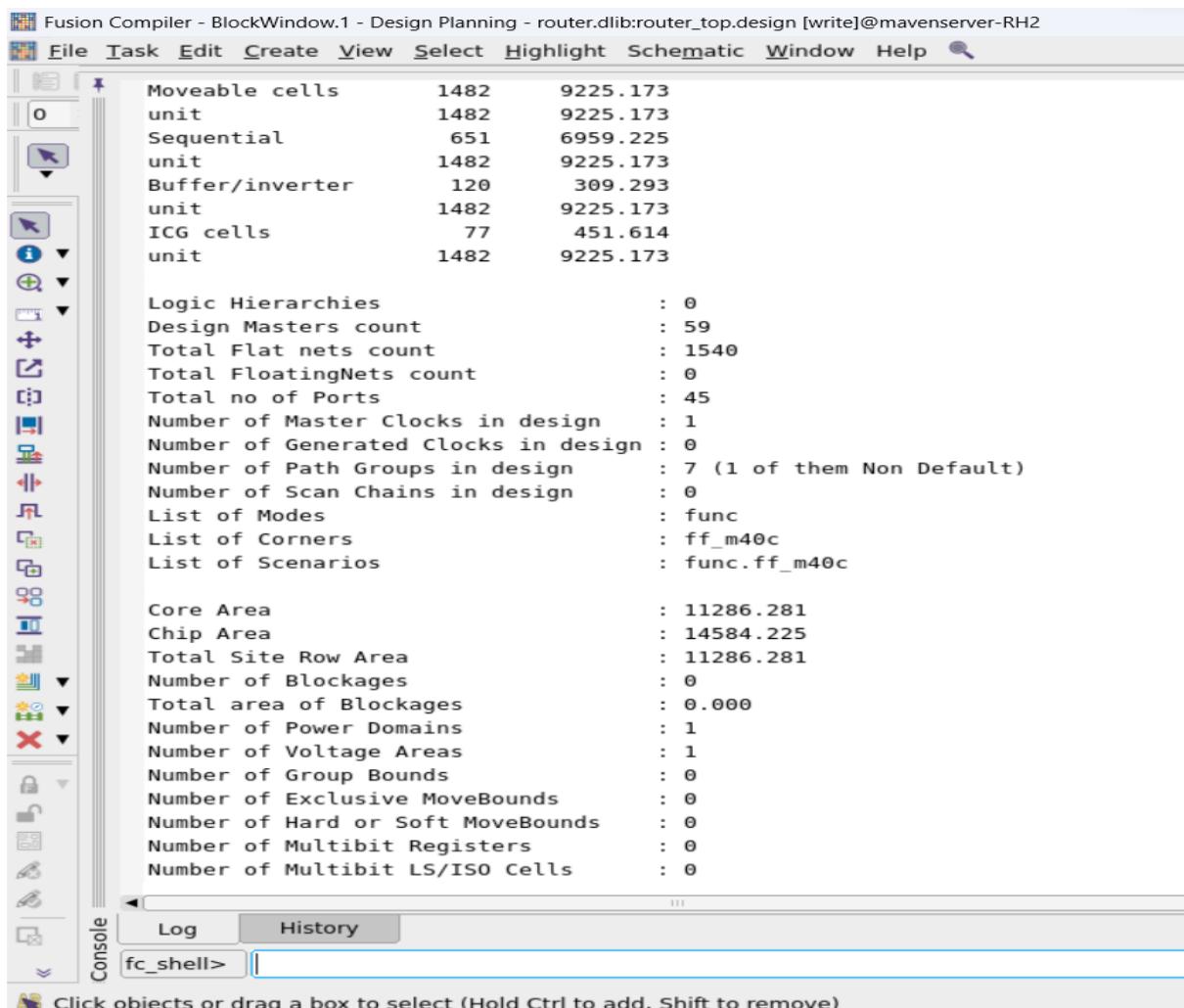
Total number of std cells in library : 1025
Total number of dont_use lib cells : 80
Total number of dont_touch lib cells : 80
Total number of buffers : 69
Total number of inverters : 45
Total number of flip-flops : 318
Total number of latches : 36
Total number of ICGs : 36

Cell Instance Type Count Area
-----
TOTAL LEAF CELLS 1482 9225.173
unit 1482 9225.173
Standard cells 1482 9225.173
unit 1482 9225.173
Hard macro cells 0 0.000
unit 1482 9225.173
Soft macro cells 0 0.000
unit 1482 9225.173
Always on cells 14 107.757
unit 1482 9225.173
Physical only 0 0.000
unit 1482 9225.173
Fixed cells 0 0.000
unit 1482 9225.173
Moveable cells 1482 9225.173

```

Console Log History fc\_shell>

Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)



```
Number of Hard or Soft MoveBounds : 0
Number of Multibit Registers : 0
Number of Multibit LS/ISO Cells : 0
Number of Top Level RP Groups : 0
Number of Tech Layers : 71 (61 of them have unknown routing dir.)

Total wire length : 31898.94 micron
Total number of wires : 15660
Total number of contacts : 25085
1
fc_shell>
```

### THE END ###