MAJOR PROJECT

I2C PROTOCOL USING UVM

Abstract:

The I2C (Inter-Integrated Circuit) protocol is a popular synchronous serial communication standard for connecting microcontrollers and peripheral devices in embedded systems. It operates in a master-slave configuration with two bidirectional lines: SDA for data and SCL for clock synchronization. Each slave device has a unique address, and communication begins with a start condition followed by the address of the target device. Data transfer occurs in byte-oriented transactions, with support for both read and write operations. Multi-master capability allows multiple devices to control the bus, with arbitration to resolve conflicts. The protocol includes mechanisms for acknowledging successful data reception and allows for variable clock rates. Pull-up resistors are necessary to maintain the bus lines when not actively driven. Overall, I2C offers simplicity, versatility, and efficiency for connecting multiple devices on a single bus in various embedded applications.

Outcomes:

- Module Design: Create modules for both master and slave devices, encapsulating their functionality including start/stop conditions, data transfer, addressing, and clock synchronization.
- Transaction Simulation: Simulate I2C transactions between the master and slave devices to verify correct protocol adherence and data integrity. This involves generating stimuli to initiate communication, simulate clock signals, and monitor data transfer.
- Clock Generation: Design clock generation logic within the master module to generate the clock signal (SCL) for synchronizing data transfer.
- Verification: Using UVM testbenches to thoroughly verify the design, ensuring that it meets the I2C protocol specifications and behaves correctly under various scenarios and corner cases.