

# **RELEASE 2020-A**

#### **Hardware**

- DS1403 Processor
  - DS1514 FPGA Board
    - Xilinx® Kintex-7 FPGA which can be programmed by the user
  - DS1553 Piggyback Board
    - 8 A/D channels with 10 MHz sample rate and adjustable voltage range
    - 2 D/A channels with 10 MHz update rate and ±20 V voltage range
    - 8 digital single-ended or differential 5V input channels
    - 24 digital single-ended 5 V output channels
    - 4 RS485 digital differential bi-directional channels
    - 1 resolver IC with 16 bit position resolution and 500 kHz update rate







### **Hardware**

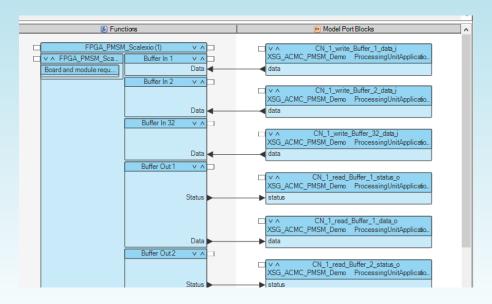
- RapidPro Power Unit
- Motor: 4 pole Permanent Magnet Machine
- Load: Electric Load
- DC Link Voltage up to 60V



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### **Configuration Desk**

- XSG based FPGA firmware for 1514 and piggyback board 1553
- Position Encoder (Input)
  - Hall Encoder
  - Incremental
- Analog to Digital Converters (Input)
  - 4X ADC with PT1 Filters (3x Current, 1x DC Link Voltage)
- FPGA and Processor based Current Controller
  - PM machine Vector Control (Id, Iq)
- FPGA Based Space Vector Modulator and PWM Generation(Output)
- Extras
  - FPGA Scope
  - Overcurrent Protection (I2t Protection)
  - Automatic Position Sensor Offset Calibration



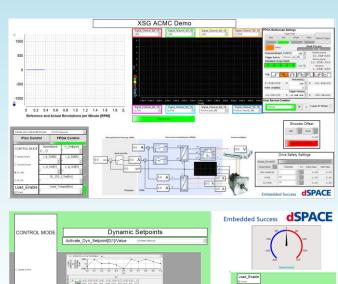
### **Communication (FPGA & Processor)**

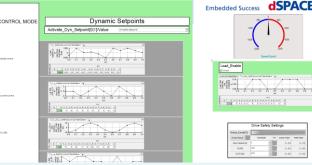
- Buffer Communication
  - Buffer 1(Base Task)
    - FPGA Scope, Version Information, Current Controller and Sensor Parameters
  - Buffer 2 (Controller task)
    - Setpoints from Speed Control or Processor based Current control
  - Buffer 32 (Scale IO)
    - Scaling Factors ADC and PT1 Filter time constant

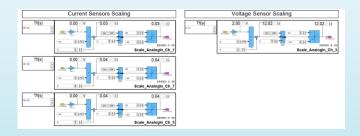


#### **Control Desk**

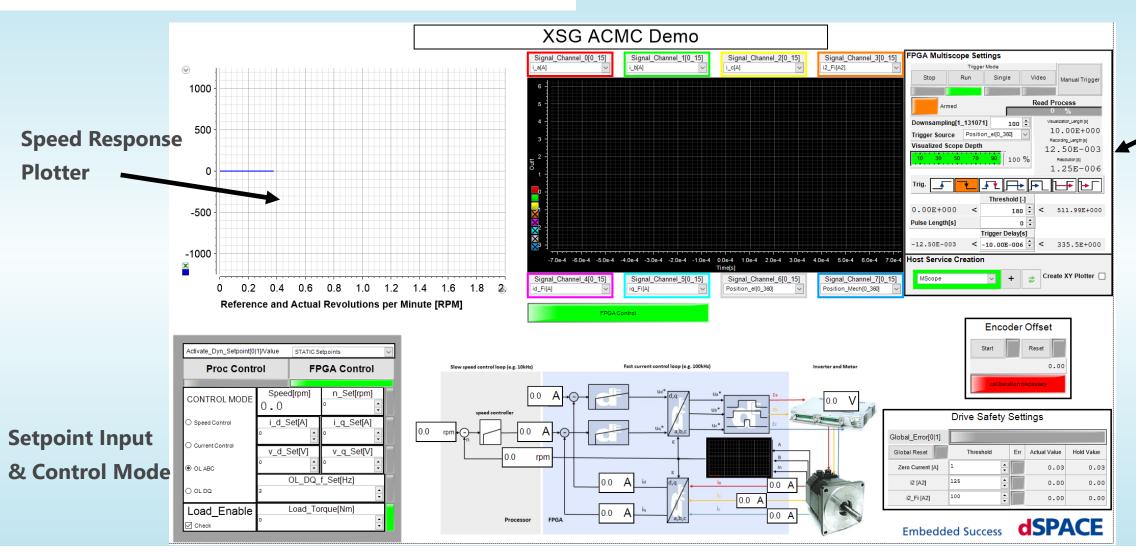
- Controller Layout
  - Speed Control (Processor Based)
  - Current Control (FPGA and Processor based)
  - Over Current Protection
  - Automatic Position Sensor Offset Caliberation
- Dynamic Setpoint
  - Lookup table based Speed Current (Iq) Open loop Voltage and Frequency setpoints
- ADC
  - Scaling factor for ADC
  - Filter Time Constants
- System Information
  - Library Version number and Task turnaround time information









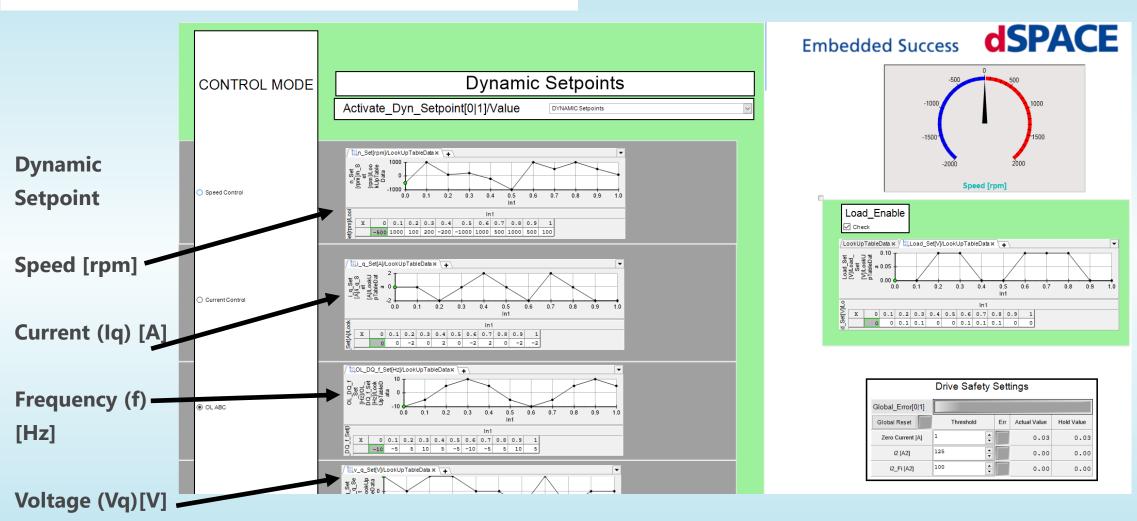


FPGA Scope

Offset Caliberation

Over Current Protection





Load [Nm]



### **RELEASE 2020-A**

#### **Folder Structure**

- Configuration
  - XSG\_ACMC\_Demo.zip (Configuration Desk back up project)
- Instrumentation
  - XSG\_ACMC\_PMSM\_Demo.zip (Control Desk back up project)
- Simulation
  - \_ControlPMSM (Controller Parameter)
  - IniFiles (IO Initilization Parameter)
  - Model (Simulink Model)
  - XSG\_ACMC\_PMSM\_rtiFPGA (Firmware Files)
  - go.m (Matlab Script)
- Documentation

Configuration	27.04.2020 15:10	File folder
Documentation	27.04.2020 15:10	File folder
Instrumentation	27.04.2020 15:10	File folder
Simulation	27.04.2020 15:10	File folder

Data (D:) > XSG_ACMC_PMSM_Demo_Scalexio > Simulation					
Name	Date modified	Туре	Size		
	27.04.2020 15:10	File folder			
IniFiles	27.04.2020 15:10	File folder			
Model	27.04.2020 15:10	File folder			
XSG_ACMC_PMSM_rtifpga	27.04.2020 15:10	File folder			
🖺 go.m	01.04.2020 19:41	MATLAB Code	5 KB		
SimulationInit.m	08.08.2019 10:23	MATLAB Code	31 KB		

# **ACMC Motor Control Demo (Workflow to Edit Demo Model)**

#### **Simulink Demo**

### Step 1

 The Xilinx system generator should be opened and thereafter Demo folder /Simulation should be selected. System Generat...

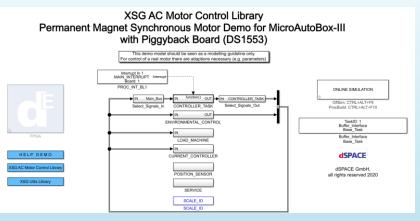
go.m should be executed and corresponding Simulink File is opened by the script.

### Step 2

- Configuration Desk –Implementation version should be opened
- XSG\_ACMC\_Demo.zip Configuration Desk Back up project should be opened.
- Platform, if need, must be registered.
- Add Simulink Model to Configuration Desk and Analyze Model

# Step 3

- Any conflicts that may appear in Configuration Desk must be resolved
- A test build needs to be performed.
- The test build should generate a SDF file successfully.



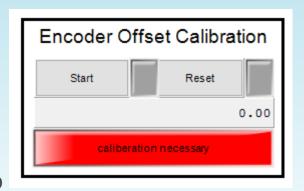


#### **Control Desk Before Start**

- Step 4
  - XSG\_ACMC\_PMSM\_Demo.zip Control Desk Back up Project must be loaded.
  - The Platform connection is checked SDF file provided with the control Desk backup experiment is loaded.
  - Note SDF file generated in Step 3 can be loaded if needed by navigating to Configuration desk project build Folder.

### Step 5

- Check the encoder offset calibration instrument if it shows drive ready
- If not then press **Start** on the Instrument.
- Check if the Drive safety status is OK (Global Error LED is NOT Red)



Drive Safety Settings					
Global_Error[0 1]					
Global Reset	Threshold	Err	Actual Value	Hold Value	
Zero Current [A]	1	+	0.01	0.01	
i2 [A2]	125	•	0.00	0.00	
i2_Fi [A2]	100	•	0.00	0.00	

NOTE: During Encoder Calibration make sure Processor Control is active. See Slide No 6

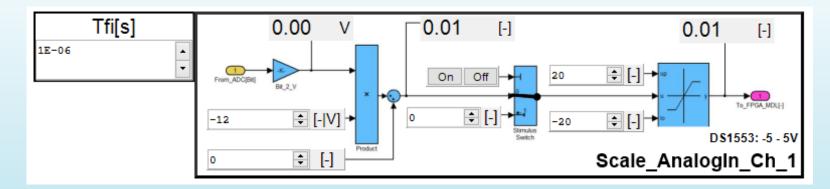


### **Control Desk Before Start Contd...**

### Step 6

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- The Scaling Factors of ADC from the ADC Layout must be checked
- Scaling Factor for Current sensors RapidPro Setup is usually -12
- Scaling Factor for DC link Voltage is usually 6. (Note that the scaling factor is not same for all ADC)
- Sensor PT1 Filter values, if necessary, should be adjusted



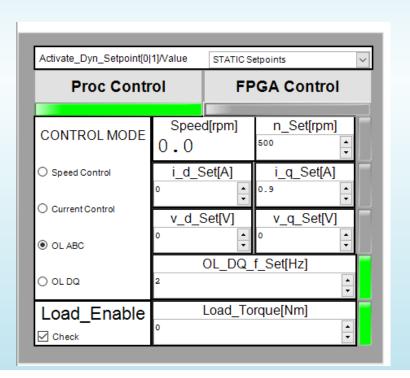


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### **Control Desk Static Setpoints**

### Step 7

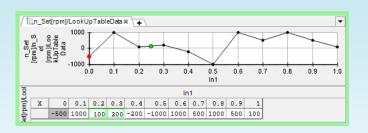
- Demo is ready for operation.
- Different Control Modes and set points from the Controller layout can be set.
- FPGA based Current Control or Processor based Current Control can be selected.
- Dynamic setpoints can be set using Dynamic setpoint layout

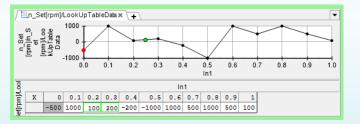


### **Control Desk Dynamic Setpoints**

### Step 7

- Different Control Modes can be selected in the Dynamic setpoints layout.
- Setpoint tables have Values that can be edited using the table editor tool
- Default time period of the entire cycle is 20 Seconds and can be changed in Real time from Control Desk







# **ACMC Motor Control Demo (Extras)**

### **Control Desk Extra – FPGA Scope**

- FPGA Scope can show signals directly from FPGA
  - FPGA Scope measures various signals within the FPGA and displays them on control Desk at FPGA clock. For Example: 12.5 nS in case of MABX.
  - The measurement can be triggered using signals mapped on the scope or from the Processor.
  - For more details on the scope refer to XSG\_Utils Documentation
  - NOTE: LED underneath the scope shows which control mode is currently on FPGA or Processor.





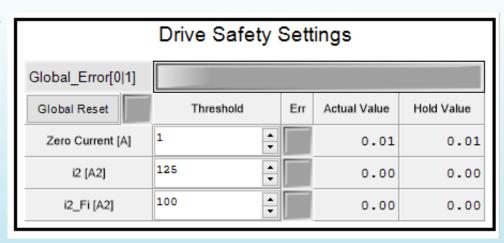
### **ACMC Motor Control Demo (Extras)**

### **Control Desk Extra Drive Safety**

- Drive Safety Instrument can Protect the motor against
  - Zero Current Error (If one or more ADCs are faulty)
  - i2 protection (Protects against exceeding maximum rated motor current)
  - i2\_Fi (Protects against high current applied to motor for a long period of time)

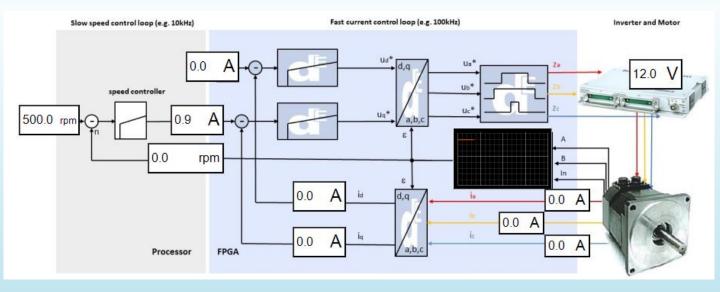
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- Actual Value on the instrument Shows the real time values
- Hold Values show values when error occurs.



### **Control Desk Extra Overview Diagram**

- Overview diagram shows the current state of the motor inverter setup i.e. 3 phase currents DC link voltage. D and q currents and various set points
- Speed Control of the motor is always in Processor. However the current control loop can be Processor based or FPGA based.



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