DS1553 FPGA Framework

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Embedded Success dSPACE

How to Contact dSPACE

Mail:	dSPACE GmbH Rathenaustraße 26 33102 Paderborn Germany
Tel.:	++49 5251 1638-0
Fax:	++49 5251 16198-0
E-mail:	info@dspace.de
Web:	http://www.dspace.com

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    support@dspace.de
    +49 5251 1638-941
  - SystemDesk Support:
    support.systemdesk@dspace.de
    +49 5251 1638-996
  - TargetLink Support:
    support.tl@dspace.de
    +49 5251 1638-700
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Important Notice

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About This Guide

Document Symbols and Conventions

Symbols

The following symbols may be used in this document:

	Indicates a general hazard that may cause personal injury of any kind if you do not avoid it by following the instructions given.
	Indicates the danger of electric shock which may cause death or serious injury if you do not avoid it by following the instructions given.
	Indicates a hazard that may cause material damage if you do not avoid it by following the instructions given.
	Indicates important information that should be kept in mind, for example, to avoid malfunctions.
	Indicates tips containing useful information to make your work easier.

Naming Conventions

The following abbreviations and formats are used in this document:

%name% Names enclosed in percent signs refer to environment variables for file and path names, for example, %DSPACE_PYTHON25% specifies the location of your dSPACE installation in the file system.

< > Angle brackets contain wildcard characters or placeholders for variable file and path names, etc.

 Precedes the document title in a link that refers to another document.

 Indicates that a link refers to another document, which is available in dSPACE HelpDesk.

I/O Read Functions

Overview

The DS1553 provides the following I/O read functions:

- 1x Status In
- 8x Digital In
- 8x ADC
- 4x RS485 In
- 1x Resolver IC
- 1x FPGA Temperature

Status In

Block

This block provides the internal status of the hardware initialization to the model.

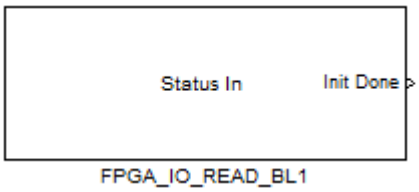

Figure 1: FPGA_IO_READ block (Status In)

Output

The main block has the following outputs:

Name	Unit	Description	Format
Init Done	-	Signals that the hardware is initialized	UFix_1_0

Digital In

Block

The 8 digital inputs provide a signal level of V_H=5V and are configurable between single-ended or differential input signal in groups.

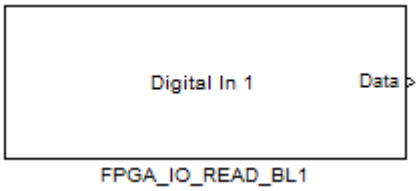

Figure 2: FPGA_IO_READ block (Digital In)

Block Dialog

The block provides the following dialog:

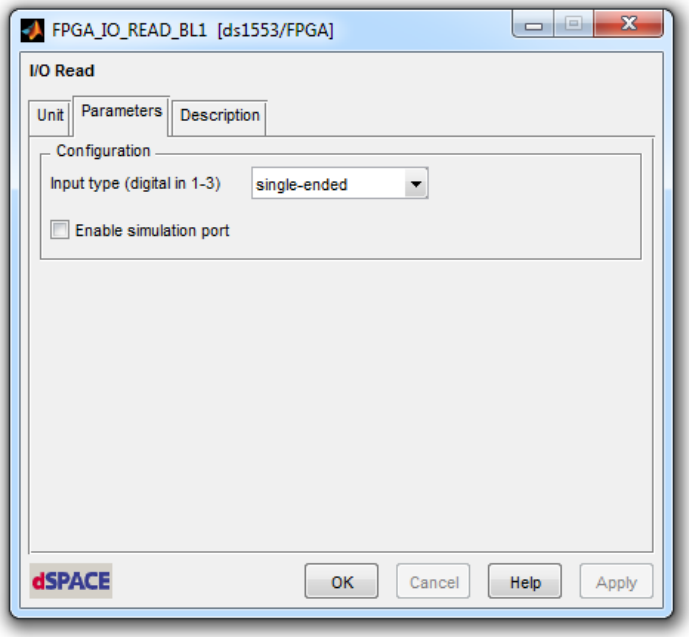

Figure 3: FPGA_IO_READ dialog (Digital In)

The blockset dialog has the following parameters:

Name	Unit	Description	Range
Input type	-	Set the digital input group to single ended or differential input. For the 1st group (1,2,3) this option is set in the block mask of Digital In 1, for the 2nd group (4,5,6) this option is set in the block mask of Digital In 4 and for the 3rd group (7,8) this option is set in the block mask of Digital In 7.	single ended | differential
Enable simulation port	-	Creates a stimulus input port for offline simulation of the I/O. The stimulus data has to be a Simulink input scaled in V.	on | off

Output

The main block has the following outputs:

Name	Unit	Description	Format
Data	-	The logical signal level at the digital input	UFix_1_0

For single-ended digital inputs, please connect the corresponding DigIn (-) pin to ground.

ADC

Block

The 8 differential ADCs provide a resolution of 14 bit, a sample rate of 10 MHz and a configurable voltage range.

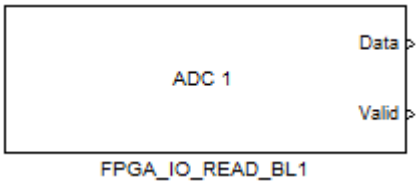

Figure 4: FPGA_IO_READ block (ADC)

Block Dialog

The block provides the following dialog:

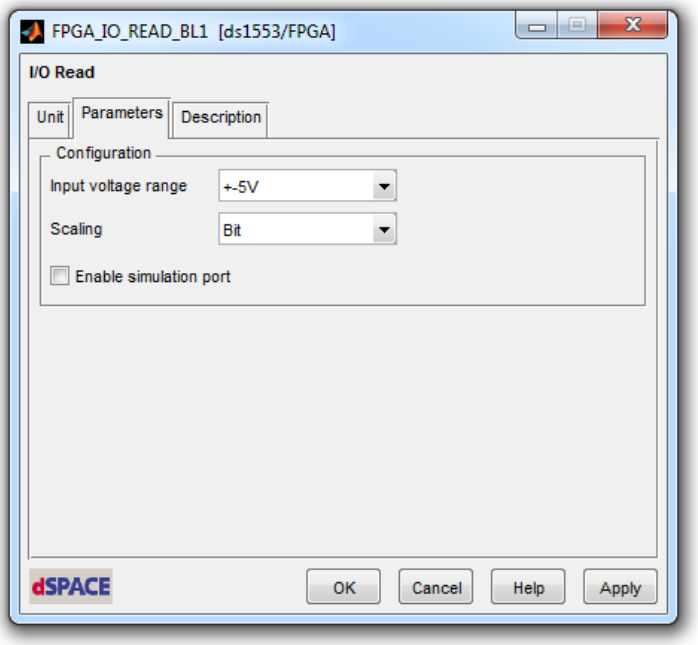

Figure 5: FPGA_IO_READ dialog (ADC)

The blockset dialog has the following parameters:

Name	Unit	Description	Range
Input voltage range	V	Set the ADC input voltage range to ±5V, ±15V or ±30V.	±5V | ±15V | ±30V
Scaling	-	Select if the output is scaled in ADC LSBs (bit) or mV.	Bit | mV
Enable simulation port	-	Creates a stimulus input port for offline simulation of the I/O. The stimulus data has to be a Simulink input scaled in V.	on | off

Output

The main block has the following outputs:

Name	Unit	Description	Format
Data	Bit | mV	The signal level at the analog input scaled in ADC LSBs (-8192…+8191) or mV.	Fix_16_0

RS485 In

Block

RS485 ports are bidirectional digital differential drivers with a signal low level of -2.5V and a signal high level of +2.5V. The ports RS485 In and RS485 out share the same physical driver.

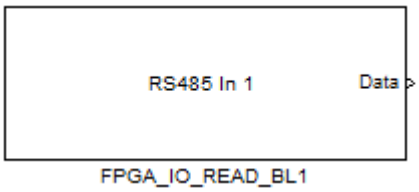

Figure 6: FPGA_IO_READ block (RS485 In)

Block Dialog

The block provides the following dialog:

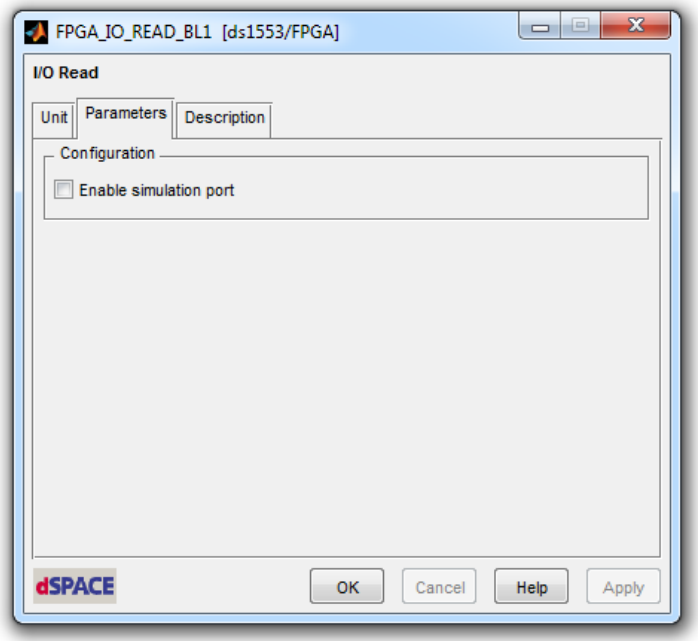

Figure 7: FPGA_IO_READ dialog (RS485 In)

The blockset dialog has the following parameters:

Name	Unit	Description	Range
Enable simulation port	-	Creates a stimulus input port for offline simulation of the I/O. The stimulus data has to be a Simulink input scaled in V.	on | off

Output

The main block has the following outputs:

Name	Unit	Description	Format
Data	-	The digital signal level at the RS485 input.	UFix_1_0

Resolver IC

Block

The DS1553 I/O board provides an integrated resolver processing IC. The IC provides position information of a resolver connected the FPGA model. It also provides warnings concerning signal quality. The update rate of the resolver IC is 500 kHz.

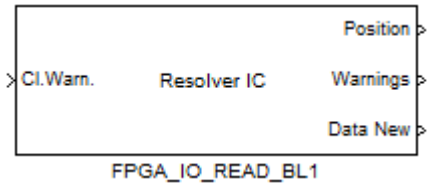

Figure 8: FPGA_IO_READ block (Resolver IC)

Block Dialog

The block provides the following dialog:

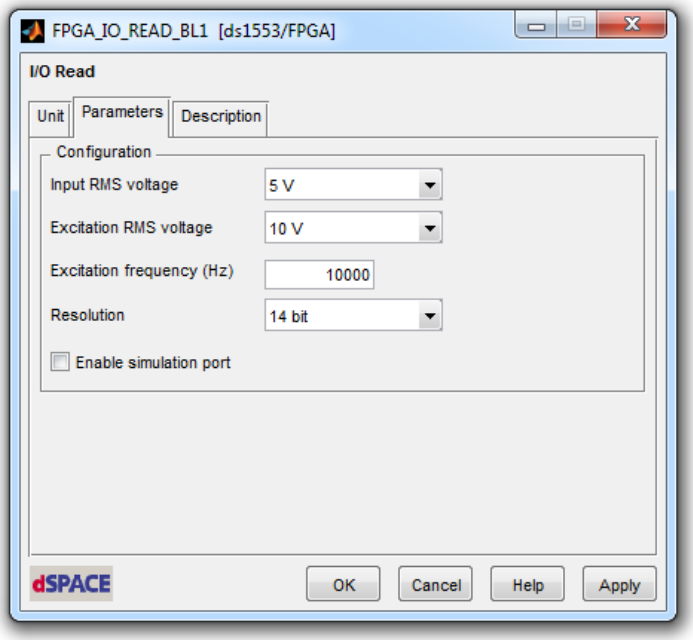

Figure 9: FPGA_IO_READ dialog (Resolver IC)

The blockset dialog has the following parameters:

Name	Unit	Description	Range
Sine / cosine RMS voltage	V	Selection of the input voltage range of the sine and cosine signal.	1.5V | 3.5V | 5V
Excitation RMS voltage	V	Selection of the RMS voltage of the generated excitation.	3V | 7V | 10V
Excitation Frequency	Hz	Selection of the frequency for the generated excitation.	Range:2kHz..20kHz Resolution: 250Hz
Resolution	Bit	Resolution of the resolver processing. The resolution effects the maximum trackable velocity as followed: 10 bit: 150000 rpm 12 bit: 60000 rpm 14 bit: 30000 rpm 16 bit: 7500 rpm	10bit | 12bit | 14 bit | 16 bit
Enable simulation port	-	Creates a stimulus input port for offline simulation of the I/O. The stimulus data (position) has to be a Simulink input scaled in degrees.	on | off

Input

The main block has the following inputs:

Name	Unit	Description	Format
Cl.Warn.	-	Resets warnings raised by the resolver IC.	UFix_1_0

Output

The main block has the following outputs:

Name	Unit	Description	Format
Position	-	The position output of the resolver IC. The position range (0…360°) is scaled to 0…1.	UFix_16_16
Warnings	-	The warnings raised by the resolver IC. The warnings are as followed: *Bit 0 – Input amplitude low:* The sine/cosine input amplitude is more than ~20% lower than specified. Once this warning occurs it can only be cleared manually. *Bit 1 – Input amplitude high:* The sine/cosine input amplitude is more than ~20% higher than specified. Once this warning occurred it can only be cleared manually. *Bit 2 – Loss of tracking:* The position could not be tracked. This warning will disappear if the position tracking could be successfully resynchronized. *Bit 3 – Velocity over-range:* The current velocity is higher than the resolver processing is able to track. This warning will disappear if the velocity is low enough again to be tracked. *Bit 4 – Phase lock error:* The phase of the sine/cosine input does not match the phase of the excitation output. Check if the resolver is plugged and correctly working. This warning will disappear once the sine/cosine phase matches the excitation phase again.	UFix_5_0
Data New	-	Flag indicating that the position data is updated.	UFix_1_0

FPGA Temperature

Block

The DS1514 base board contains an integrated FPGA temperature measurement. The raw value of the temperature measurement is provided to the user model.

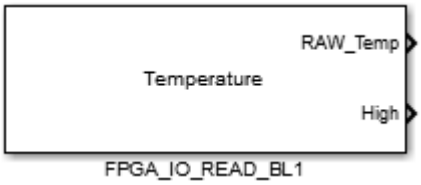

Figure 10: FPGA_IO_READ block (FPGA Temperature)

Block Dialog

The block provides the following dialog:

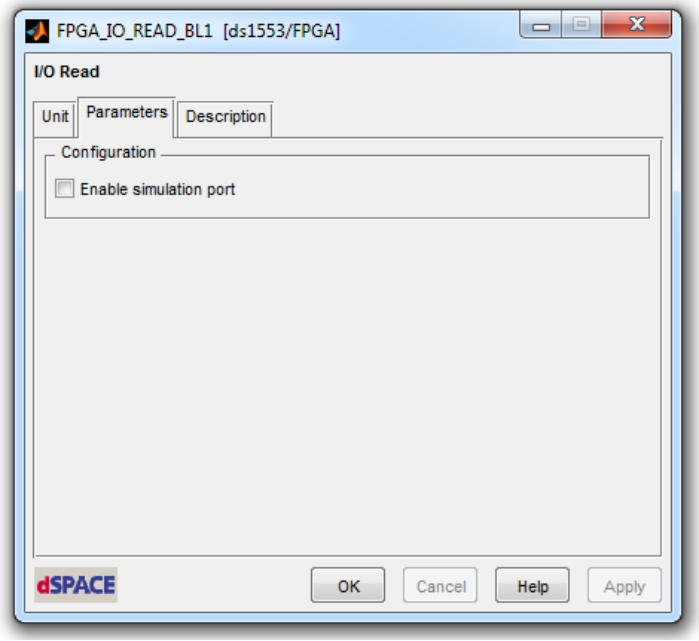

Figure 11: FPGA_IO_READ dialog (FPGA Temperature)

The blockset dialog has the following parameters:

Enable simulation port	-	Creates a stimulus input port for offline simulation of the I/O. The stimulus data (temperature) has to be a Simulink input scaled in °C.	on | off

Output

The main block has the following outputs:

Name	Unit	Description	Format
RAW_TEMP	-	The raw temperature sensor output. The scaling is 130 LSB/K.	UFix_16_0
High	-	Flag indicating that the FPGA temperature is >125°C.	UFix_1_0

I/O Write Functions

Overview

The DS1553 provides the following I/O write functions:

- 1x LED Out
- 24x Digital Out
- 2x DAC
- 4x RS485 Out

LED Out

Block

This block controls the status LED of the DS1514 FPGA board.

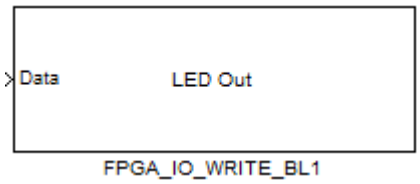

Figure 12: FPGA_IO_WRITE block (LED Out)

Input

The main block has the following Inputs:

Name	Unit	Description	Format
Data	-	Sets the color of the FPGA LED to orange (1) or green (0).	UFix_1_0

Digital Out

Block

The 24 digital outputs provide a signal level of V_H=5V.

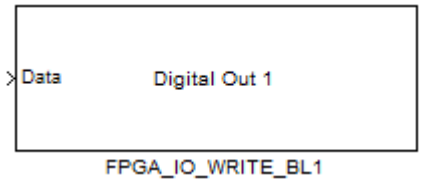

Figure 13: FPGA_IO_WRITE block (Digital Out)

Block Dialog

The block provides the following dialog:

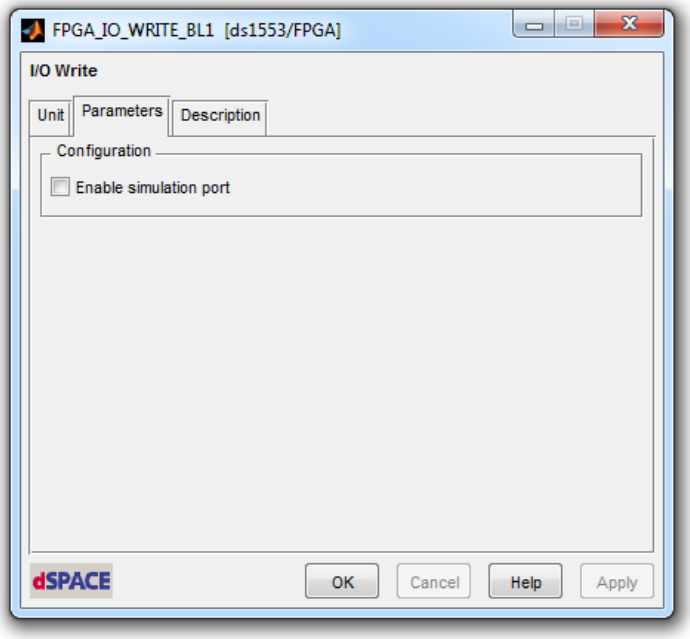

Figure 14: FPGA_IO_WRITE dialog (Digital Out)

The blockset dialog has the following parameters:

Name	Unit	Description	Range
Enable simulation port	-	Creates a stimulus output port for offline simulation of the I/O. The stimulus data is a Simulink output scaled in V.	on | off

Input

The main block has the following inputs:

Name	Unit	Description	Format
Data	-	The logical signal level to set at the digital output.	UFix_1_0

DAC

Block

The 2 differential DACs (referenced to ground) provide a resolution of 12 bit, an update rate of 20MHz and voltage range of -20V…+20.

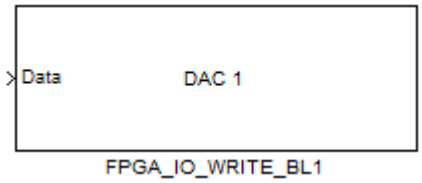

Figure 15: FPGA_IO_WRITE block (DAC)

Block Dialog

The block provides the following dialog:

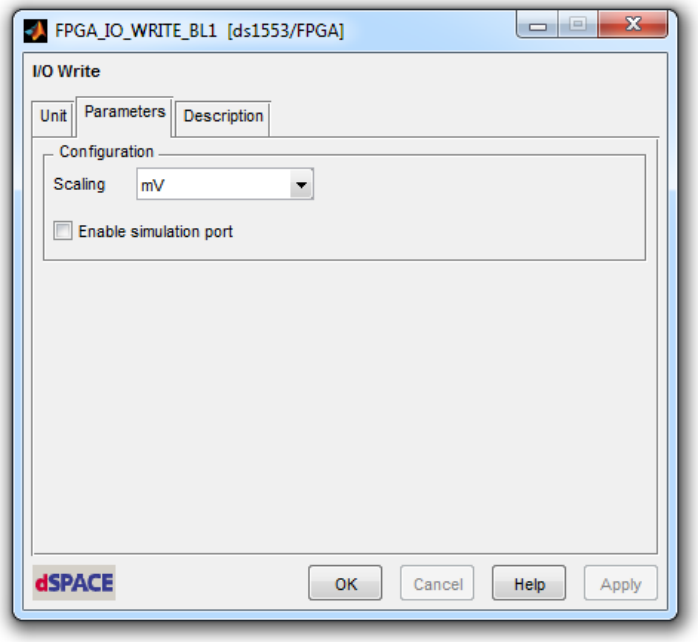

Figure 16: FPGA_IO_WRITE dialog (DAC)

The blockset dialog has the following parameters:

Name	Unit	Description	Range
Scaling	-	Select if the input is scaled in DAC LSBs (bit) or mV.	Bit | mV
Enable simulation port	-	Creates a stimulus output port for offline simulation of the I/O. The stimulus data is a Simulink output scaled in V.	on | off

Input

The main block has the following Inputs:

Name	Unit	Description	Format
Data	Bit | mV	The signal level set at the analog output scaled in DAC LSBs (-2048…+2047) or mV.	Fix_16_0

	The DAC (+) and DAC (-) pins are both referenced to ground. To change the voltage range to -10V…+10V connect to ground instead of DAC (-). The scaling in mV is not valid in this case, so it is recommended to use scaling in bit when applying the -10V...+10V range.

RS485 Out

Block

RS485 ports are bidirectional digital differential drivers with a signal low level of -2.5V and a signal high level of +2.5V. The ports RS485 In and RS485 out share the same physical driver.

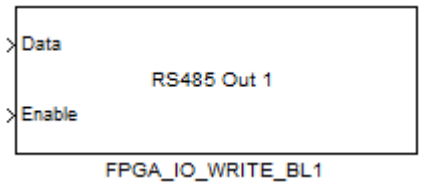

Figure 17: FPGA_IO_WRITE block (RS485 Out)

Block Dialog

The block provides the following dialog:

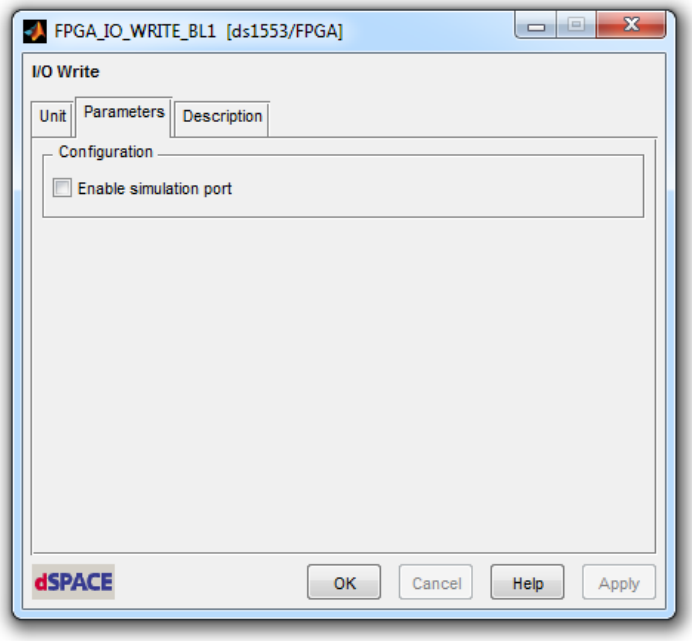

Figure 18: FPGA_IO_WRITE dialog (RS485 Out)

The blockset dialog has the following parameters:

Name	Unit	Description	Range
Enable simulation port	-	Creates a stimulus output port for offline simulation of the I/O. The stimulus data is a Simulink output scaled in V.	on | off

Input

The main block has the following inputs:

Name	Unit	Description	Format
Data	-	The digital signal level set at the RS485 output.	UFix_1_0
Enable	-	Sets the direction of the RS485 driver to output (1) or input (0).	UFix_1_0

Pin-Out

Layout

The pin-out of ZIF connector on the DS1553 ACMC I/O module is shown in the table on the next page. The layout of the ZIF connector (upper connector of the MicroAutoBox) is illustrated in the figure below. The location of ground pins can be seen in this figure as well.

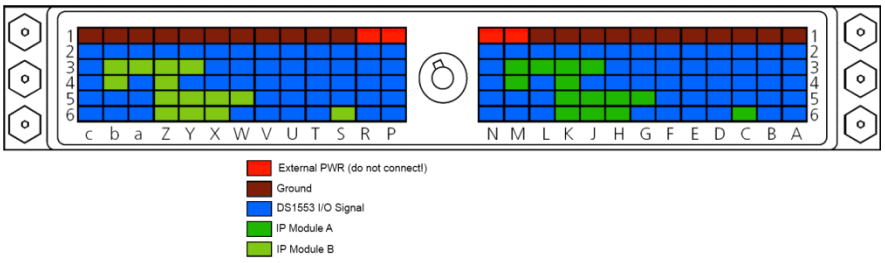

Figure 19: Layout of the DS1553 ZIF connector

Group	Pin	Signal	Dir.	Group	Pin	Signal	Dir.
Digital Input	D3	DigIn 1 (+)	in	Analog Input	A6	ADC 1 (+)	in
	E6	DigIn 1 (-)	in		A2	ADC 1 (-)	in
	D4	DigIn 2 (+)	in		A5	ADC 2 (+)	in
	D5	DigIn 2 (-)	in		A4	ADC 2 (-)	in
	E5	DigIn 3 (+)	in		A3	ADC 3 (+)	in
	E4	DigIn 3 (-)	in		B6	ADC 3 (-)	in
	U3	DigIn 4 (+)	in		B5	ADC 4 (+)	in
	U5	DigIn 4 (-)	in		B4	ADC 4 (-)	in
	T3	DigIn 5 (+)	in		c2	ADC 5 (+)	in
	U4	DigIn 5 (-)	in		c3	ADC 5 (-)	in
	V6	DigIn 6 (+)	in		b2	ADC 6 (+)	in
	V5	DigIn 6 (-)	in		c4	ADC 6 (-)	in
	T5	DigIn 7 (+)	in		a2	ADC 7 (+)	in
	U6	DigIn 7 (-)	in		Z2	ADC 7 (-)	in
	F6	DigIn 8 (+)	in		c5	ADC 8 (+)	in
	E3	DigIn 8 (-)	in		Y2	ADC 8 (-)	in
Digital Output	R3	DigOut 1	out	Resolver IC	a4	Excitation (+)	out
	R5	DigOut 2	out		b6	Excitation (-)	out
	S5	DigOut 3	out		a5	Sine (+)	in
	R4	DigOut 4	out		a6	Sine (-)	in
	R6	DigOut 5	out		c6	Cosine (+)	in
	S4	DigOut 6	out		b5	Cosine (-)	in
	H3	DigOut 7	out	RS485	W3	RS485 1 (+)	in/out
	H4	DigOut 8	out		X4	RS485 1 (-)	in/out
	G3	DigOut 9	out		V4	RS485 2 (+)	in/out
	G4	DigOut 10	out		V3	RS485 2 (-)	in/out
	S3	DigOut 11	out		W6	RS485 3 (+)	in/out
	F5	DigOut 12	out		W4	RS485 3 (-)	in/out
	F3	DigOut 13	out		X3	RS485 4 (+)	in/out
	T4	DigOut 14	out		Y4	RS485 4 (-)	in/out
	F4	DigOut 15	out	Analog Output	C3	DAC 1 (+)	out
	G6	DigOut 16	out		D6	DAC 1 (-)	out
	X6	DigOut 17 *	out		C5	DAC 2 (+)	out
	C6	DigOut 18 *	out		C4	DAC 2 (-)	out
	H6	DigOut 19 *	out	Sensor Supply	E2	Supply +5V	out
	X5	DigOut 20 *	out		F2	Supply +5V	out
	G5	DigOut 21 *	out		C2	Supply +12V	out
	H5	DigOut 22 *	out		D2	Supply +12V	out
	S6	DigOut 23 *	out				
	W5	DigOut 24 *	out				

The pins marked with an asterisk (*) are only available if the DS1514 base board hardware is reconfigured. Please inquire about hardware reconfiguration if these digital outputs are required. The use of additional IP modules will not be possible after modification!