Softwired Processor

Processor specification

1. Register (i). Special register- PC(program counter) – 11bit

MAR (memory address register) – 11bit

IR (instruction register) – 16bit

CAR (control address register)- 8bit

SBR (Subroutine register)- 8bit

(ii). General purpose register- B, C , D, A(accumulator)- 16 bit

(iii). I/O register - INR (input register)- 16bit

OUTR (output register)- 16bit

2.Memory- (i). RAM- 4KiB [2k*16 bit] (data portion(0x065-0x7FF)

code portion(0x000-0x064))

(ii).ROM- 256*38 bit

(iii). Cache -

tag	offset
5bit	3bit

- cache line- 2
- Bock size- 8*38 bit (offset 3 bit)
- 16*[5(tag)+1(Valid bit) + 38(cache
- Date width)] - total capacity
- 38*2*8 - data cache capacity
- Look through model
- Fully associative organization

3. Flag- N(negative), Z(zero), V(overflow)- based on output of ALU

R, W (read write flag based on I/O operation)

4. ALU (arithmetic logic unit)- work with accumulator with 16 bit
5. barrel shifter (one input of ALU bass by barrel shifter)

General working feature

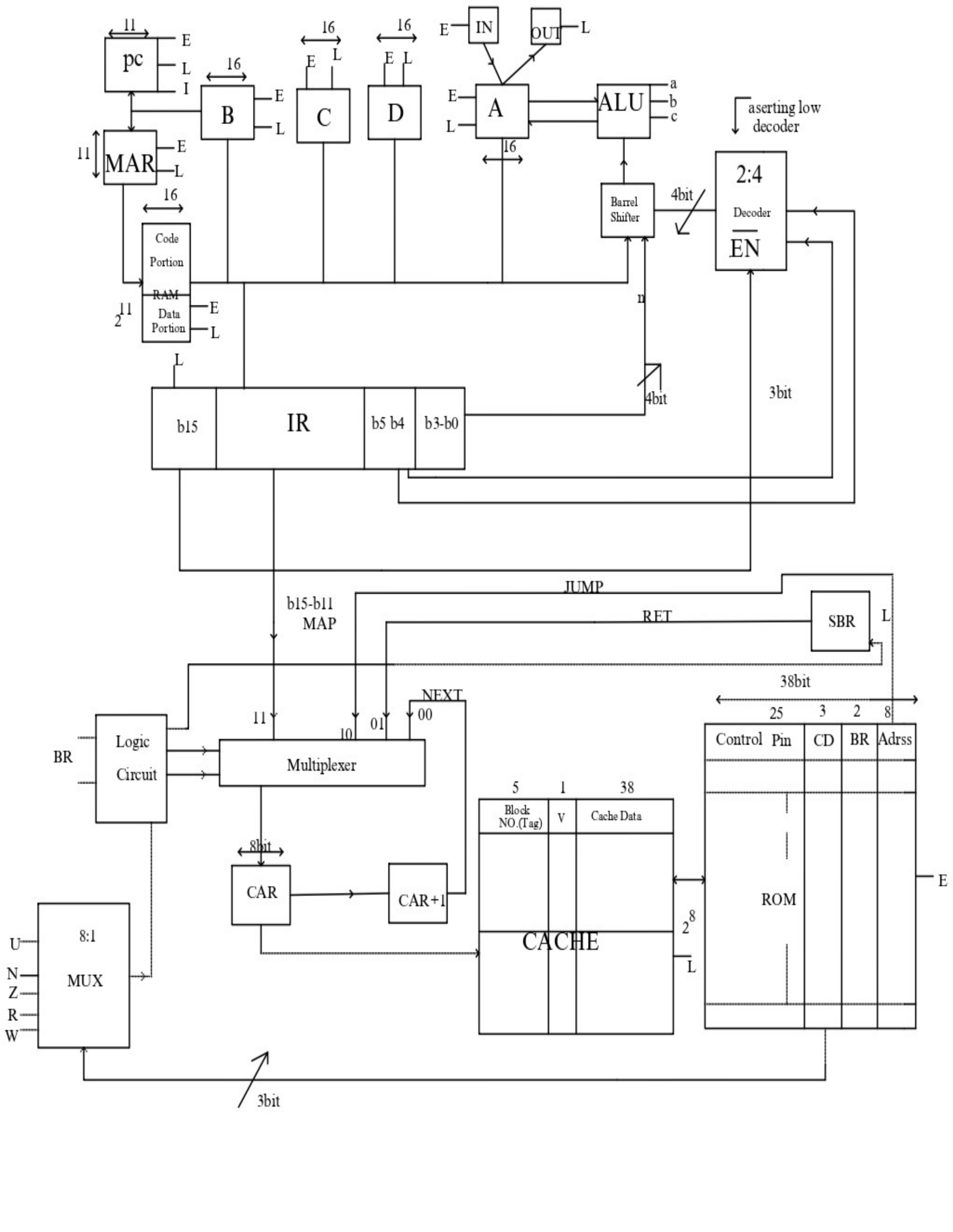
- We divide our instruction on basis of arithmetic and non-arithmetic which is decide by b15 bit of instruction which enable the decoder of barrel shifter for arithmetic operation.
    - Arithmetic instruction (b15 =0)

      ADD, SUB, INC, DEC, MUL, AND, OR, CMA, CLA
    - Non-arithmetic instruction (b15=1)

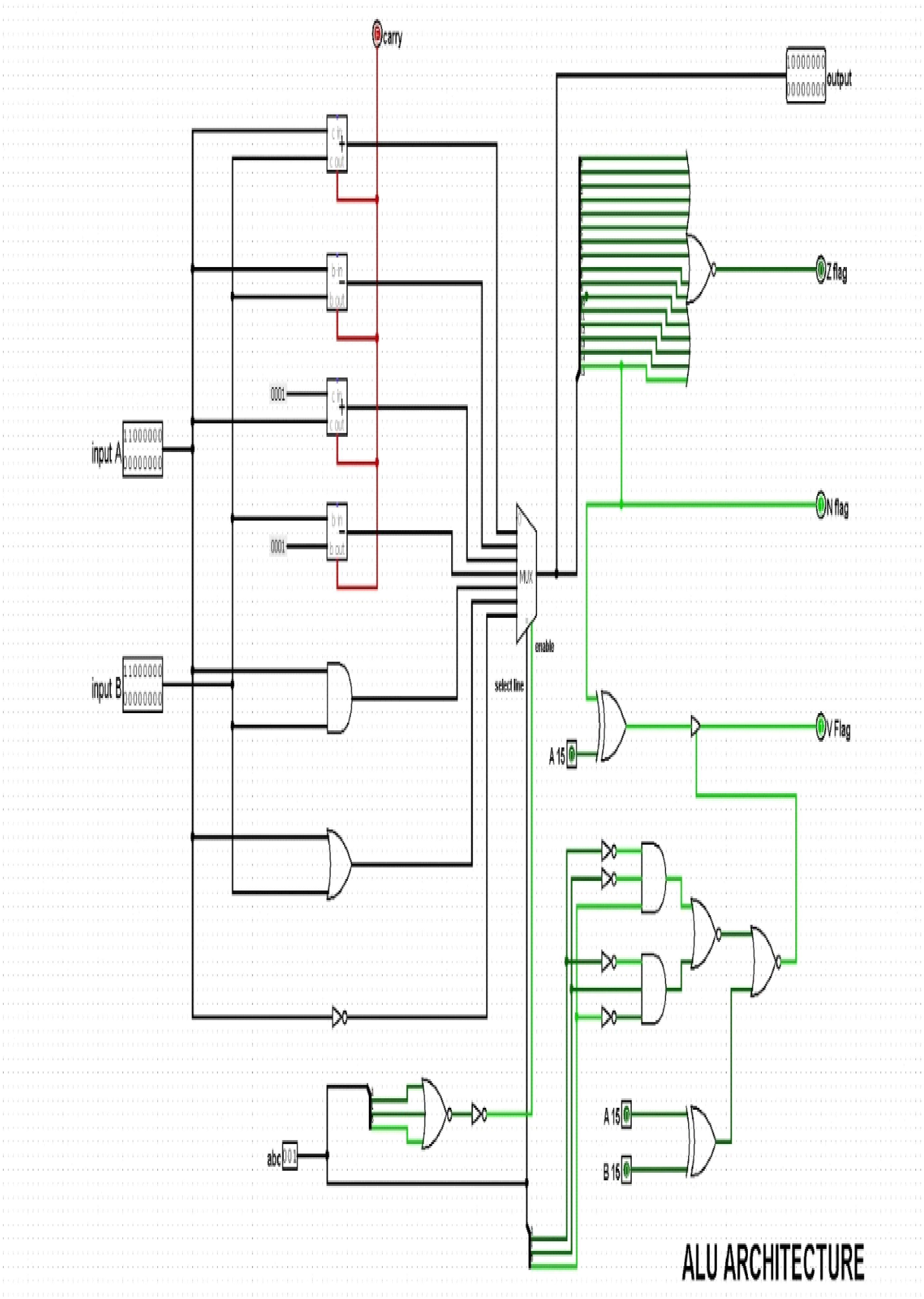
      LDA, STA, BUN, BSA, BZ, IN, OUT, HLT
- Only load, store and branching instruction are access to the memory(only directly).
- We have implicit operand destination register(A) and source register (A, B) in arithmetic instruction and register B is pass by barrel shifter.
- We divide our RAM memory in code and date portion.
- When power on then PC=0X000 and CAR=0XF8.

Unique concept in processor

- One input of ALU is pass by barrel shifter.by this we can implement divide and multiply fastly.
- We implement cache memory before ROM.by this instruction access time is decrease.
- We use branching in ROM using CAR. Due to this our ROM size is decrease.
- We implement multiplication using branching in ROM.
- We implement CLA (clear accumulator) using branching in ROM using concept A=A && (~A).



Architecture layout



ALU ARCHITECTURE

Arithmetic Operation implemented by ALU hardware

Arithmetic operation	**abc (control signal of ALU)**
NOP	000
ADD	001
SUB	010
INC	011
DEC	100
AND	101
OR	110
CMA	111

Barrel shifter hardware operation

Barrel shifter operation	***b5-b4(barrel shifter decoder control pin)***
LSL, n	00
LSR, n	01
NOP	11

Instruction set architecture

- ***Arithmetic instruction (b15- b0)***

These instruction is operate on implicit operand register A and B(pass by barrel shifter)

b15= 0

b15 b0

Arithmetic bit	opcode	-------------	Barrel shifter operation	n(shifted by n)
1	4		2	4

Opcode *of arithmetic instruction*

Instruction	**Opcode(b15-b11)**	**Mapped address(CAR)[in Hex]**
ADD	0 1010	50
SUB	0 1011	58
INC	0 0010	10
DEC	0 0011	18
MUL	0 0100	20
AND	0 0101	28
OR	0 0110	30

CMA	0 0111	38
CLA	0 1000	40

- ***Non-Arithmetic Microinstruction (b15- b0)***

All MRI Instructions are direct.

b15= 1

b15 b0

Arithmetic bit	opcode	Address for MRI inst.
1	4	11

<u>Opcode *of non-arithmetic instruction*</u>

Instruction	**Opcode(b15-b11)**	**Mapped address(CAR)[in Hex]**
LDA	1 0000	80
STA	1 0001	88
BUN	1 0010	90
BSA	1 0011	98
BZ	1 0100	A0
IN	1 0101	A8
OUT	1 0110	B0
HLT	1 0111	B8

<u>Microinstruction</u>

At Power on CAR = F8, PC = 000

Mapping of opcode to CAR

CAR[b7-b3] =Opcode CAR [b2-b0]= 000

b37 b0

Hardware control pin	CD(condition)	BR(branching)	CAR Address
25	3	2	8

Hardware control pin

b37 b13

E,L,I,RESET	E,L	E,L	E,L	L	E	E	L	L	abc	clk
PC	MAR	RAM	A,B,C,D	Cache	ROM	INR	OUTR	IR	ALU	

CD(condition)

CD(bits)	Condition	Flag	meaning
000	Always 1	U	Unconditional branching
001	A = 0	Z	Set when zero value in accumulator(A)
010	IN flag	R	Instruction IN works only when R=1
011	OUT flag	W	Instruction OUT works only when W=1
100	N flag	N	Set 1 if ALU output is negative(b15(A) =1)

BR(Branching)

00	If CD=1(true) CAR<- AD else CAR<- CAR+1	JUMP At AD Next
01	If CD=1(true) SBR<- CAR+1 ,CAR <- AD else CAR<- CAR+1	RET Next
10	CAR<- SBR	CALL AD
11	CAR[7-3]=IR[15-11], CAR[2-0]=0	MAP

<u>Arithmetic-microinstructions</u>

@50 ADD(A=A+ barrel shifted B)

B(E), BS(bo-b5 decode)	U	JMP	Next
A(E,L), ALU(001)	U	JMP	F8(Fetch)

@58 SUB (A=A- barrel shifted B)

B(E), BS(bo-b5 decode)	U	JMP	Next
A(E,L), ALU(010)	U	JMP	F8(Fetch)

@10 INC

A(E,L), ALU(011)	U	JMP	F8(Fetch)

@18 DEC

A(E,L), ALU(100)	U	JMP	F8(Fetch)

@20 MUL(C=C*D)

B(L),C(E)	U	JMP	Next
C(E),A(L)	U	JMP	Next
B(E),BS(0000)	U	JMP	Next
A(E,L),ALU(001)	U	JMP	Next
A(E),C(L)	U	JMP	Next
A(L),D(E)	U	JMP	@29
A(E),D(L),R	Z	JMP	@21
NOP	Z	JMP	F8(Fetch)

@28 AND (A= A && barrel shifted B)

B(E), BS(bo-b5 decode)	U	JMP	Next
A(E,L), ALU(101)	U	JMP	F8(Fetch)

@30 OR (A= A || barrel shifted B)

B(E), BS(bo-b5 decode)	U	JMP	Next
A(E,L), ALU(110)	U	JMP	F8(Fetch)

@38 CMA (A=~A)

A(E,L), ALU(111)	U	JMP	F8(Fetch)

@40 CLA(A=A && (~A) = 0)

A(E), C(L)	U	JMP	Next
A(E,L), ALU(111)	U	JMP	Next
A(E), B(L), BS(bo-b5(0000) Decode)	U	JMP	Next
A(L), C(E)	U	JMP	Next
A(A,E), ALU(101)	U	JMP	F8(Fetch)

<u>Non-Arithmetic-microinstructions</u>

@80 LDA

B(E),MAR(L)	U	JMP	NEXT
[MAR]->A(L)	U	JMP	F8(Fetch)

@88 STA

B(E),MAR(L)	U	JMP	NEXT
A->RAM	U	JMP	F8(Fetch)

@90 BUN

B(E),MAR(L)	U	JMP	NEXT
MAR(E), PC(L)	U	JMP	F8(Fetch)

@98 BSA

PC(E), IR(L)	U	JMP	Next
MAR(E), PC(L)	U	JMP	Next
IR->[MAR] , PC(I)	U	JMP	F8(Fetch)

@A0 BZ

B(E),MAR(L)	U	JMP	NEXT
NOP	Z	JMP	@A2
NOP	U	JMP	F8(Fetch)
MAR(E), PC(L)	U	JMP	F8(Fetch)

@A8 IN

NOP	R	JMP	@AA
NOP	U	JMP	F8(Fetch)
INR(E), A(L), PC(I)	U	JMP	F8(Fetch)

@B0 OUT

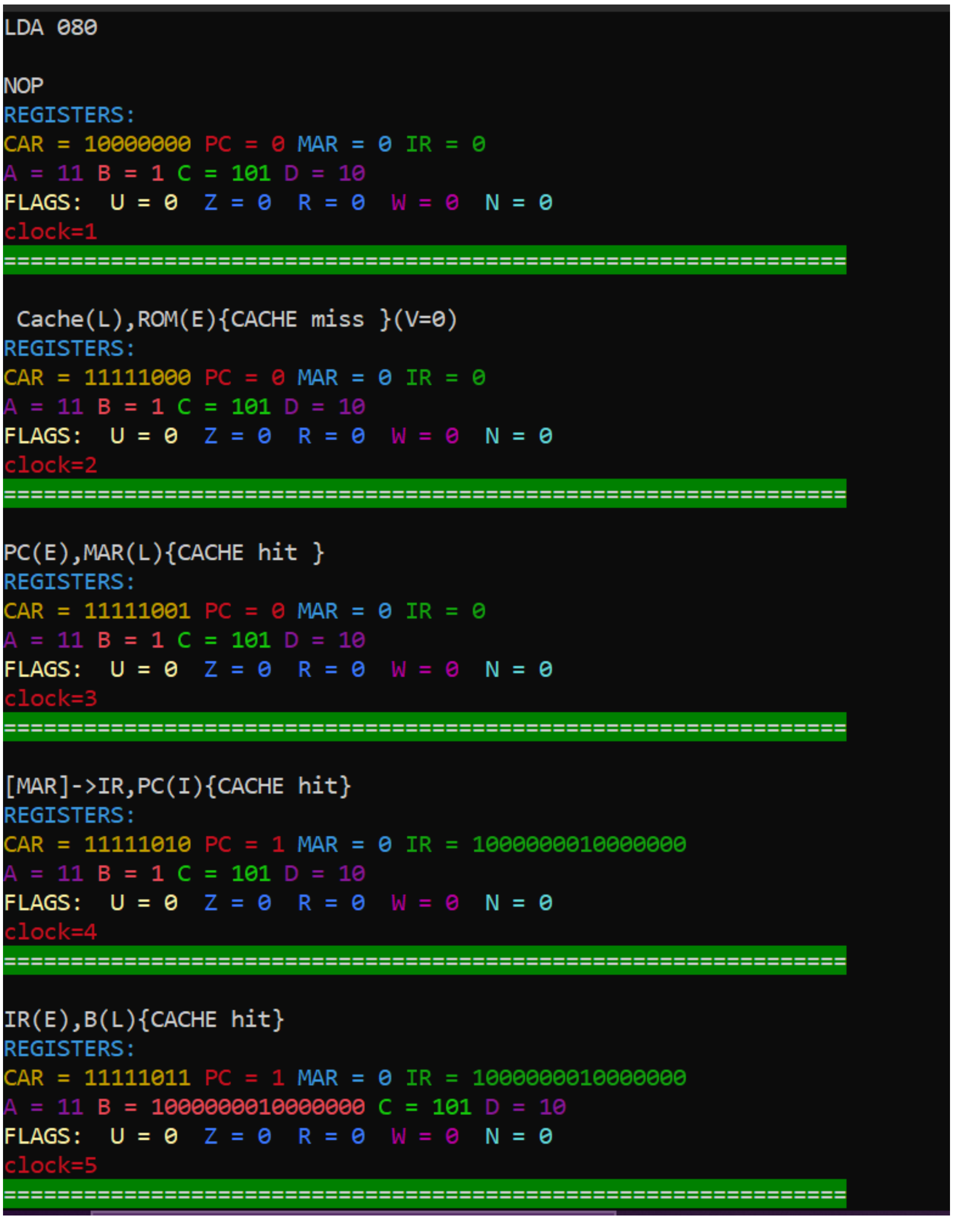
NOP	W	JMP	@B2
NOP	U	JMP	F8(Fetch)
A(L), OUTR(L), PC(I)	U	JMP	F8(Fetch)

@B8 HLT

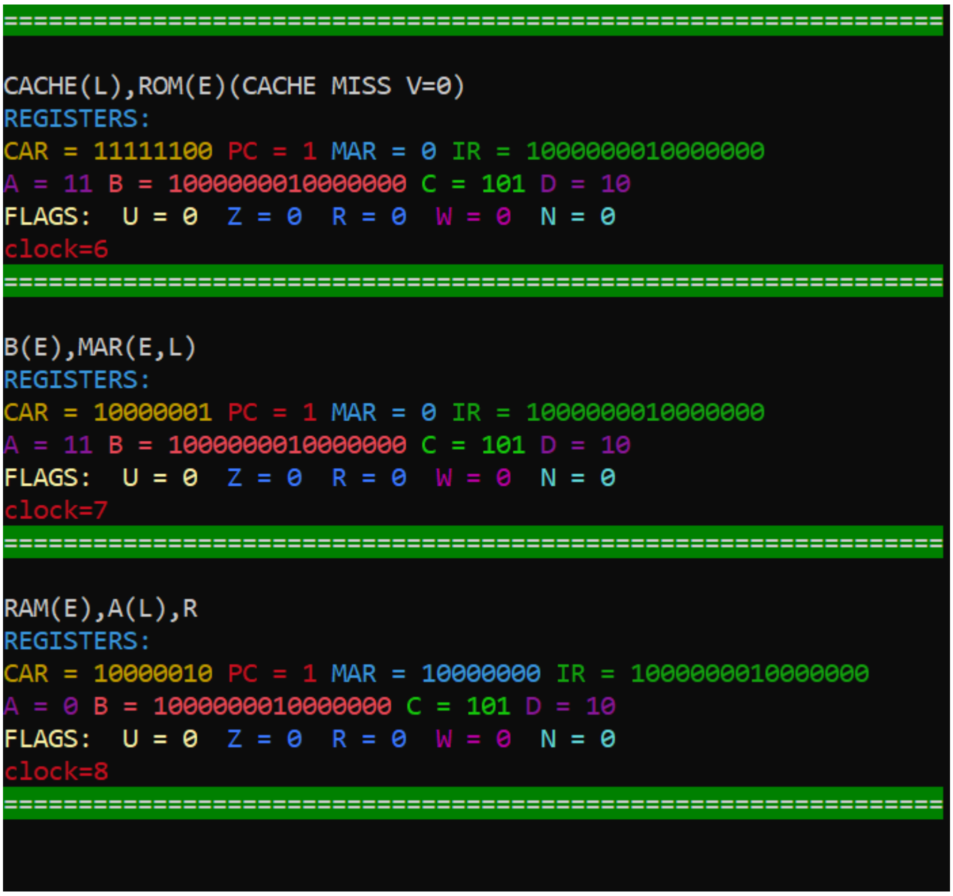
Clock disabled			

@F8 fetch (AT POWER ON.. CAR=F8)

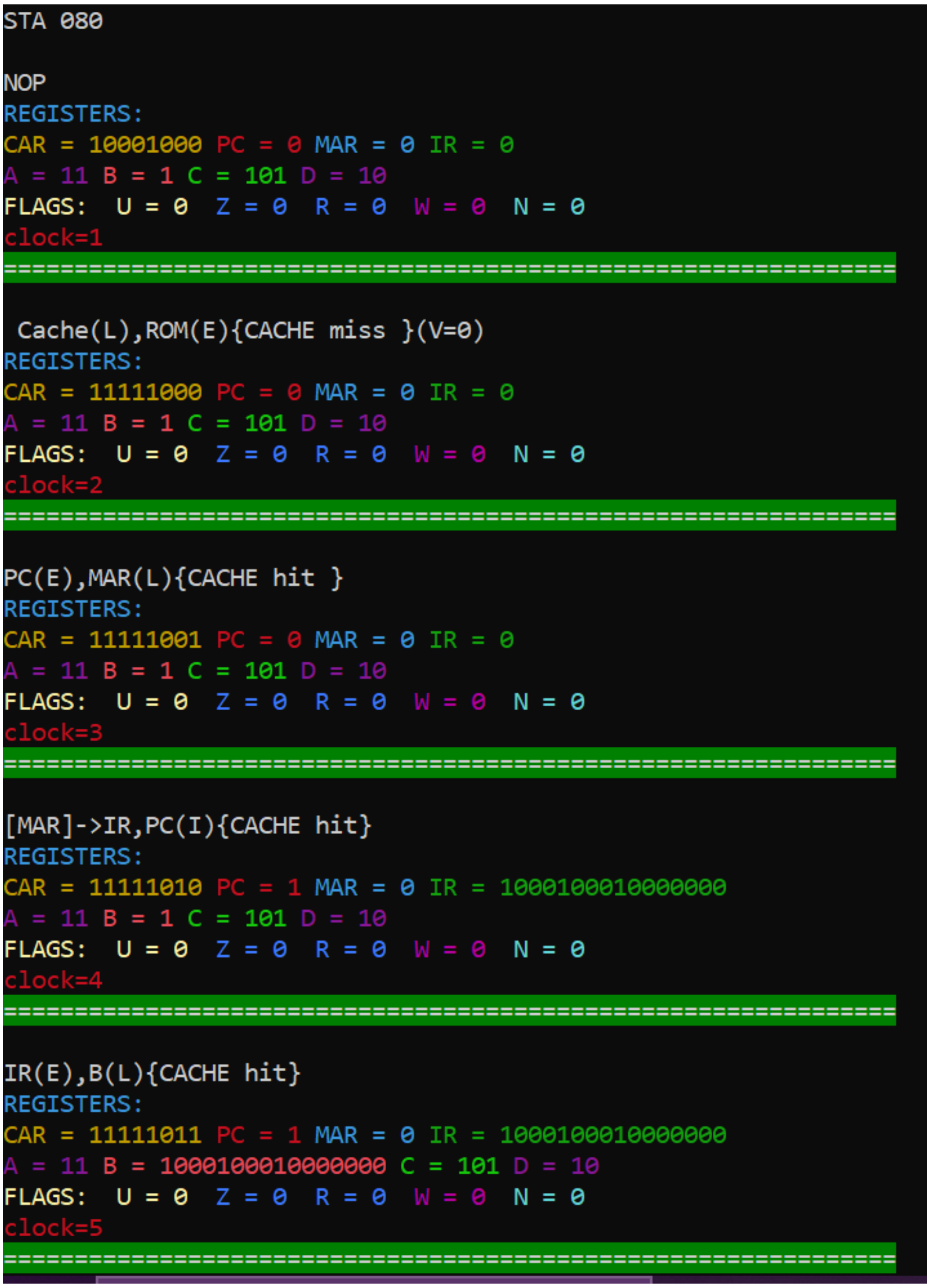
Cache(L),ROM(E){cache miss }(V=0)	U	JMP	NEXT
PC(E),MAR(L){cache hit }	U	JMP	NEXT
[MAR]->IR,PC(I){cache hit }	U	JMP	NEXT
IR(E),B(L){cache hit}	U	JMP	NEXT
Cache(L),ROM(E){catch miss }	U	MAP	……



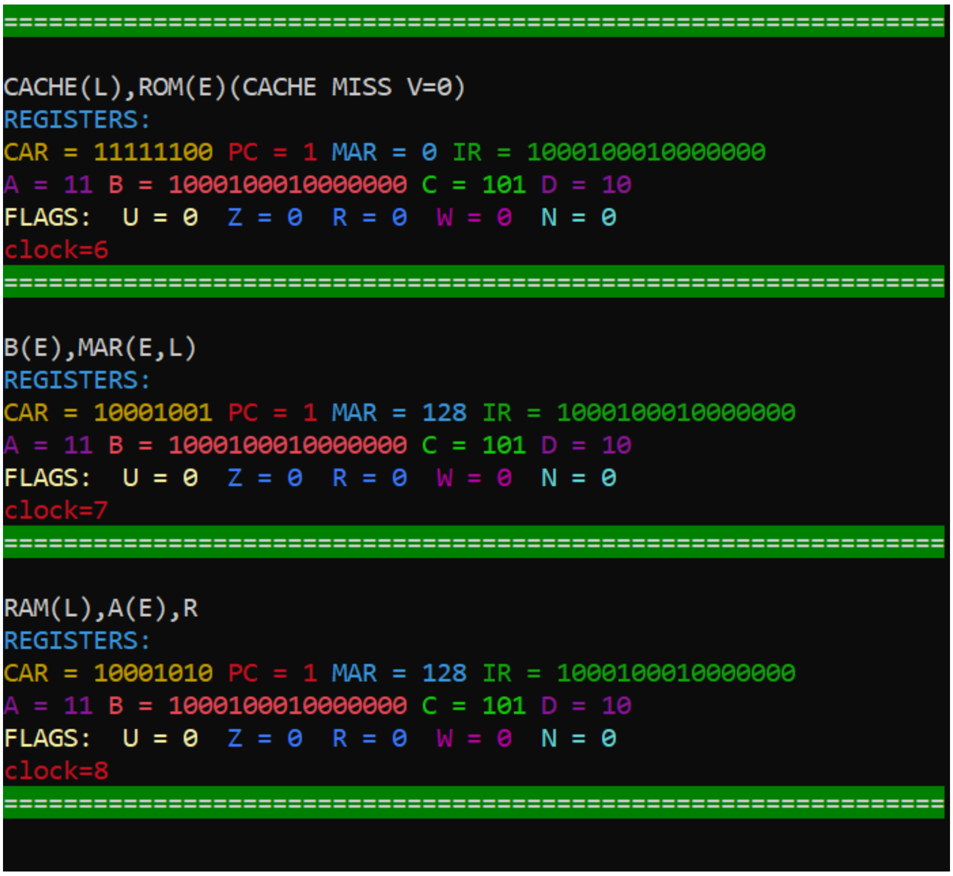
```
LDA 080

NOP
REGISTERS:
CAR = 10000000 PC = 0 MAR = 0 IR = 0
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=1
================================================================

 Cache(L),ROM(E){CACHE miss }(V=0)
REGISTERS:
CAR = 11111000 PC = 0 MAR = 0 IR = 0
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=2
================================================================

PC(E),MAR(L){CACHE hit }
REGISTERS:
CAR = 11111001 PC = 0 MAR = 0 IR = 0
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=3
================================================================

[MAR]->IR,PC(I){CACHE hit}
REGISTERS:
CAR = 11111010 PC = 1 MAR = 0 IR = 1000000010000000
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=4
================================================================

IR(E),B(L){CACHE hit}
REGISTERS:
CAR = 11111011 PC = 1 MAR = 0 IR = 1000000010000000
A = 11 B = 1000000010000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=5
================================================================
```



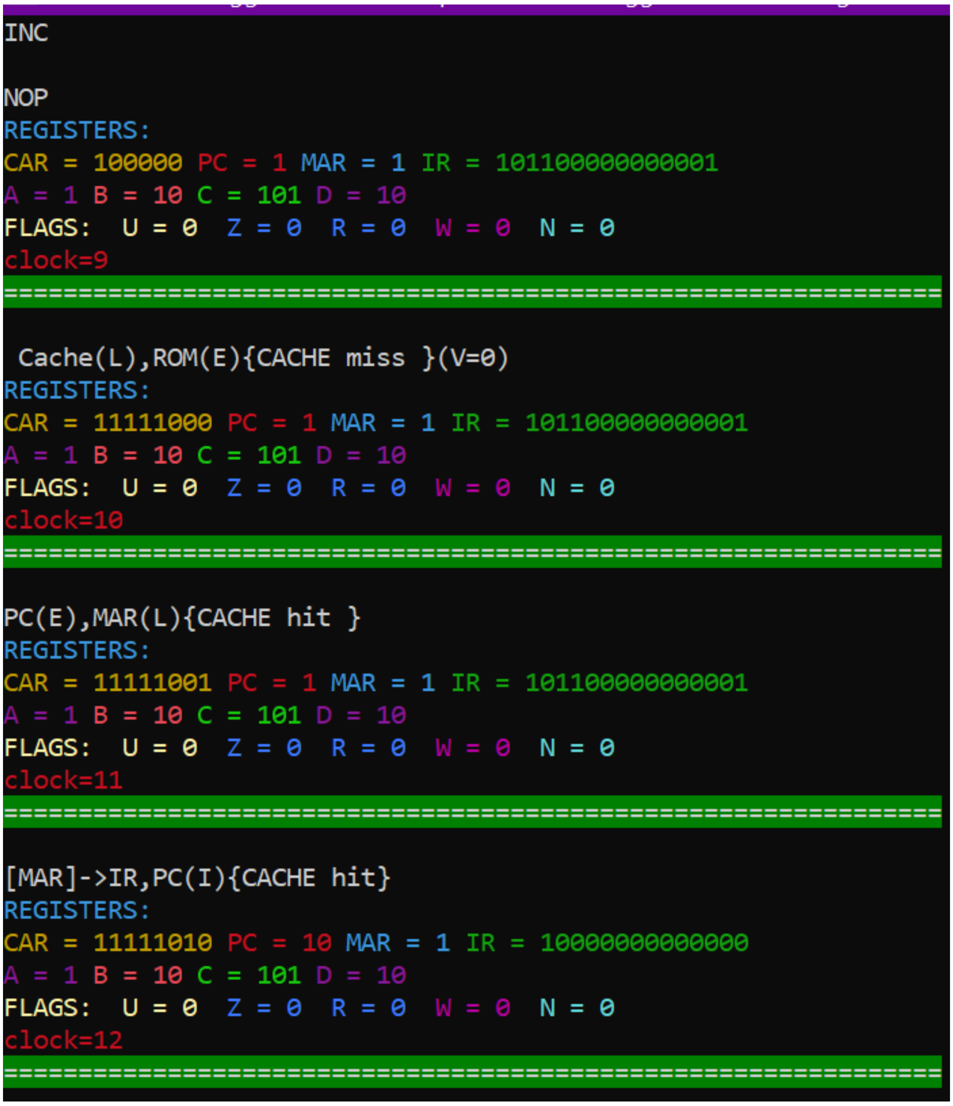
```
===============================================================

CACHE(L),ROM(E)(CACHE MISS V=0)
REGISTERS:
CAR = 11111100 PC = 1 MAR = 0 IR = 1000000010000000
A = 11 B = 1000000010000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=6
===============================================================

B(E),MAR(E,L)
REGISTERS:
CAR = 10000001 PC = 1 MAR = 0 IR = 1000000010000000
A = 11 B = 1000000010000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=7
===============================================================

RAM(E),A(L),R
REGISTERS:
CAR = 10000010 PC = 1 MAR = 10000000 IR = 1000000010000000
A = 0 B = 1000000010000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=8
===============================================================
```



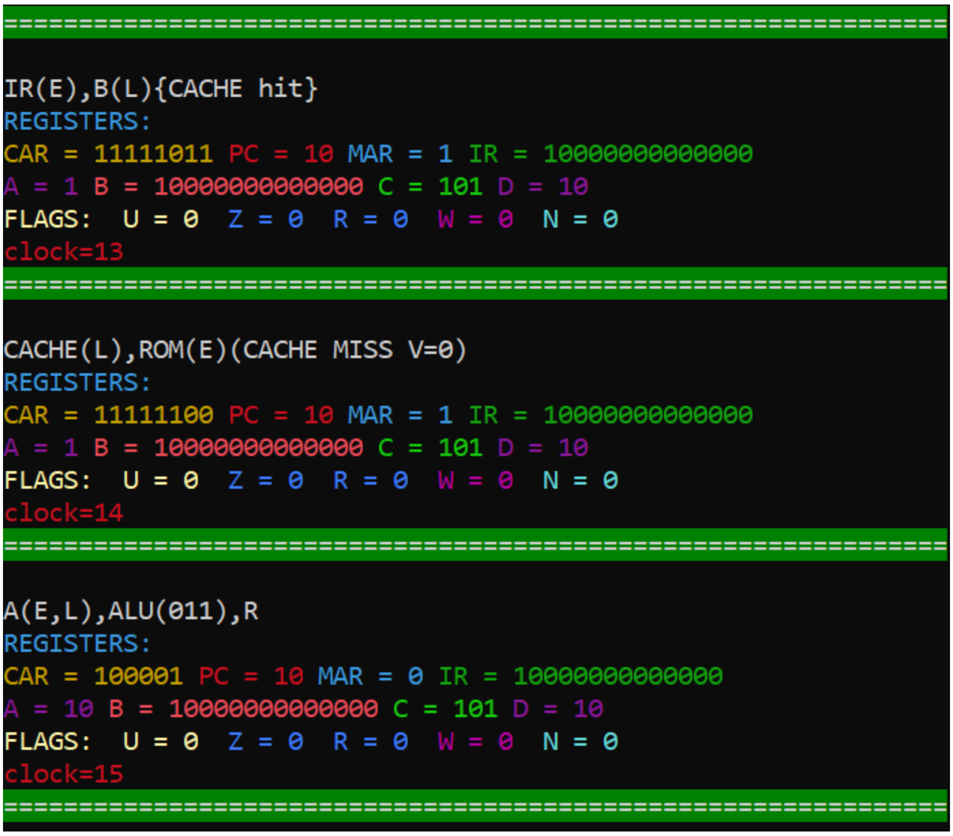
```
STA 080

NOP
REGISTERS:
CAR = 10001000 PC = 0 MAR = 0 IR = 0
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=1
===============================================================

 Cache(L),ROM(E){CACHE miss }(V=0)
REGISTERS:
CAR = 11111000 PC = 0 MAR = 0 IR = 0
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=2
===============================================================

PC(E),MAR(L){CACHE hit }
REGISTERS:
CAR = 11111001 PC = 0 MAR = 0 IR = 0
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=3
===============================================================

[MAR]->IR,PC(I){CACHE hit}
REGISTERS:
CAR = 11111010 PC = 1 MAR = 0 IR = 1000100010000000
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=4
===============================================================

IR(E),B(L){CACHE hit}
REGISTERS:
CAR = 11111011 PC = 1 MAR = 0 IR = 1000100010000000
A = 11 B = 1000100010000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=5
===============================================================
```



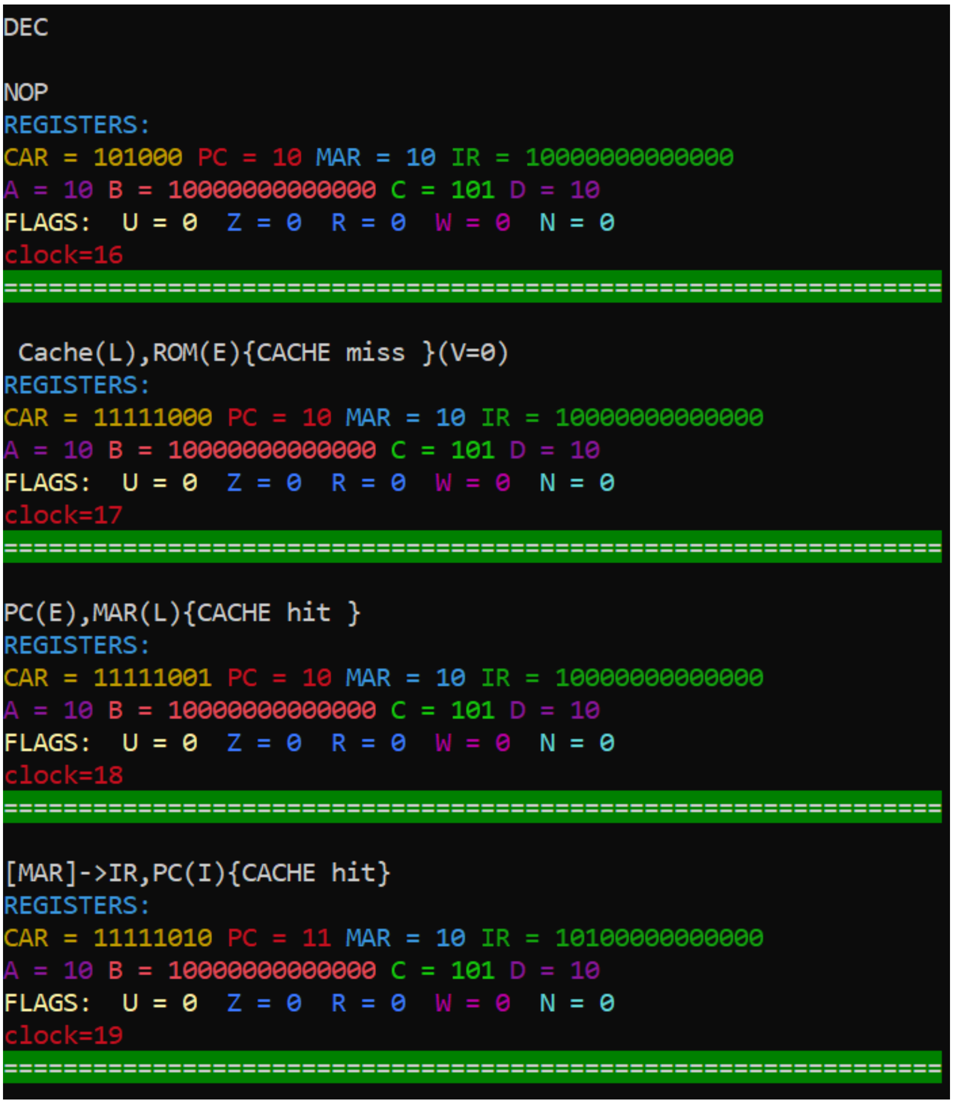
```
===============================================================

CACHE(L),ROM(E)(CACHE MISS V=0)
REGISTERS:
CAR = 11111100 PC = 1 MAR = 0 IR = 1000100010000000
A = 11 B = 1000100010000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=6
===============================================================

B(E),MAR(E,L)
REGISTERS:
CAR = 10001001 PC = 1 MAR = 128 IR = 1000100010000000
A = 11 B = 1000100010000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=7
===============================================================

RAM(L),A(E),R
REGISTERS:
CAR = 10001010 PC = 1 MAR = 128 IR = 1000100010000000
A = 11 B = 1000100010000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=8
===============================================================
```



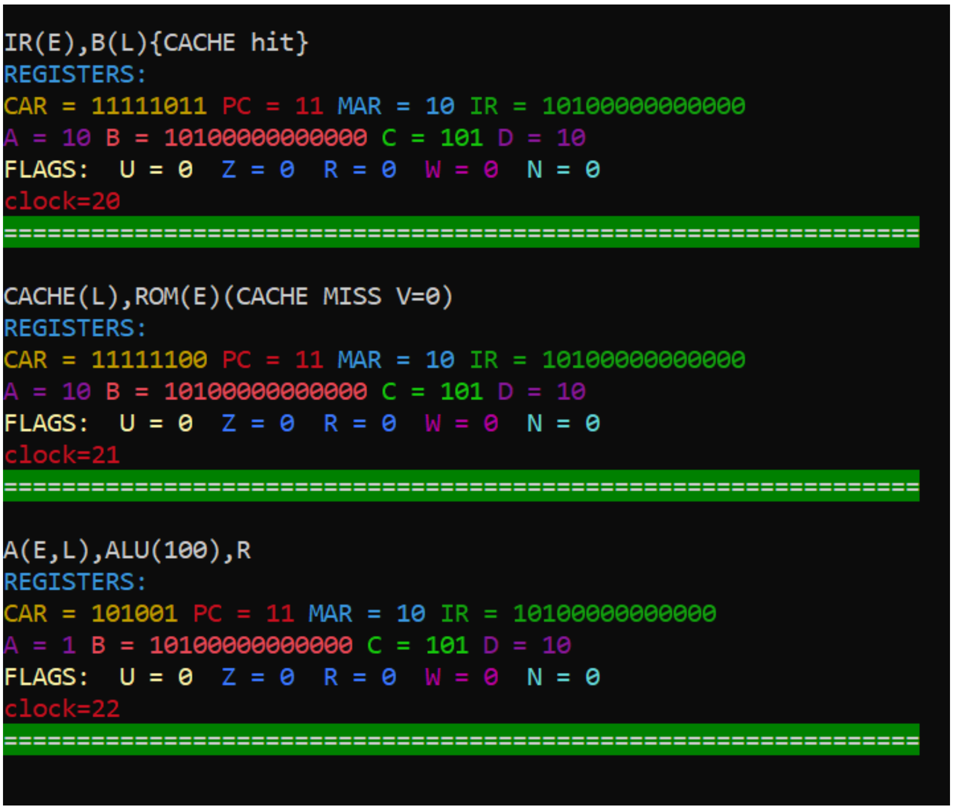
```
INC

NOP
REGISTERS:
CAR = 100000 PC = 1 MAR = 1 IR = 101100000000001
A = 1 B = 10 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=9
===============================================================

 Cache(L),ROM(E){CACHE miss }(V=0)
REGISTERS:
CAR = 11111000 PC = 1 MAR = 1 IR = 101100000000001
A = 1 B = 10 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=10
===============================================================

PC(E),MAR(L){CACHE hit }
REGISTERS:
CAR = 11111001 PC = 1 MAR = 1 IR = 101100000000001
A = 1 B = 10 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=11
===============================================================

[MAR]->IR,PC(I){CACHE hit}
REGISTERS:
CAR = 11111010 PC = 10 MAR = 1 IR = 10000000000000
A = 1 B = 10 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=12
===============================================================
```



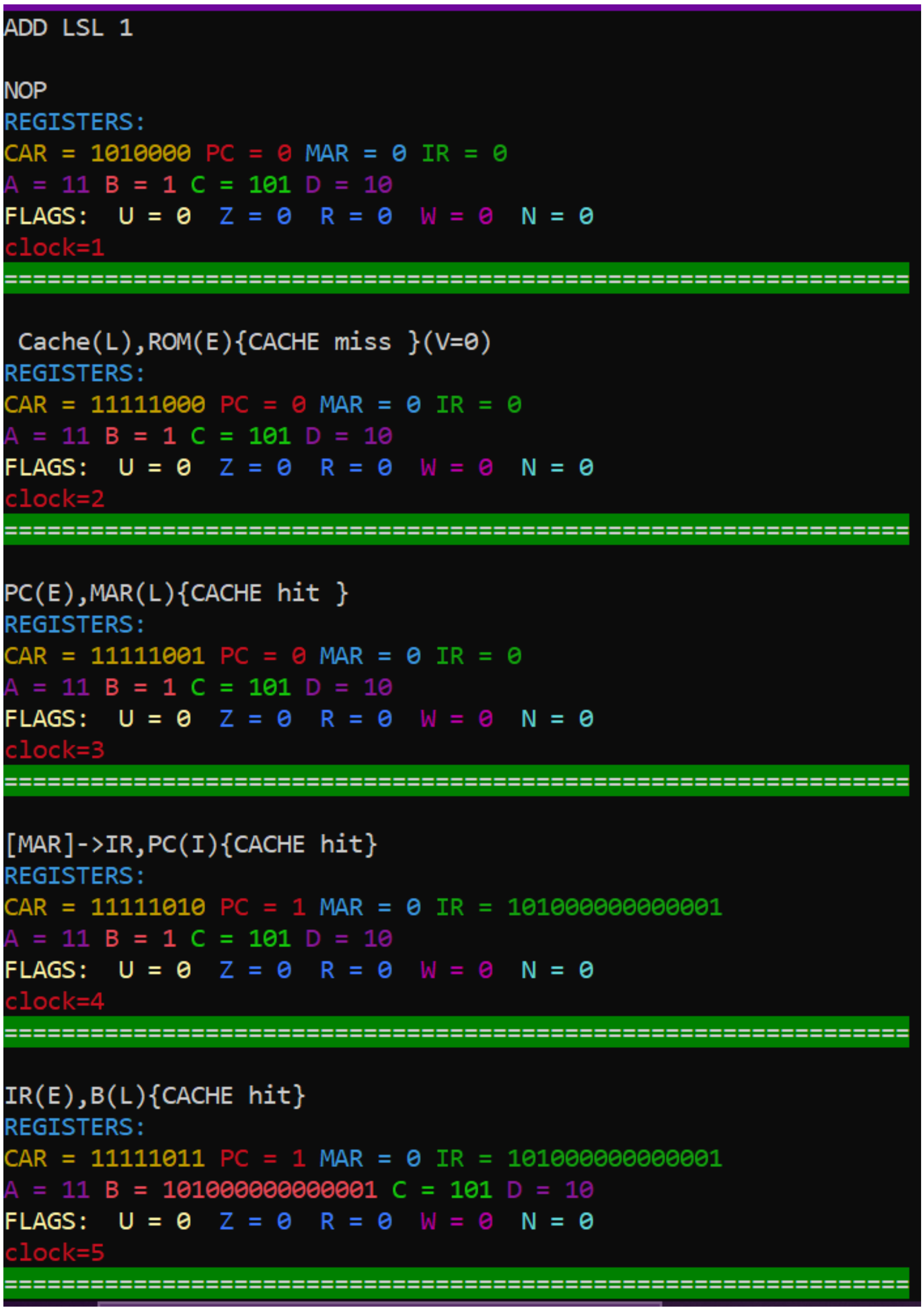
```
===============================================================

IR(E),B(L){CACHE hit}
REGISTERS:
CAR = 11111011 PC = 10 MAR = 1 IR = 10000000000000
A = 1 B = 10000000000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=13
===============================================================

CACHE(L),ROM(E)(CACHE MISS V=0)
REGISTERS:
CAR = 11111100 PC = 10 MAR = 1 IR = 10000000000000
A = 1 B = 10000000000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=14
===============================================================

A(E,L),ALU(011),R
REGISTERS:
CAR = 100001 PC = 10 MAR = 0 IR = 10000000000000
A = 10 B = 10000000000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=15
===============================================================
```



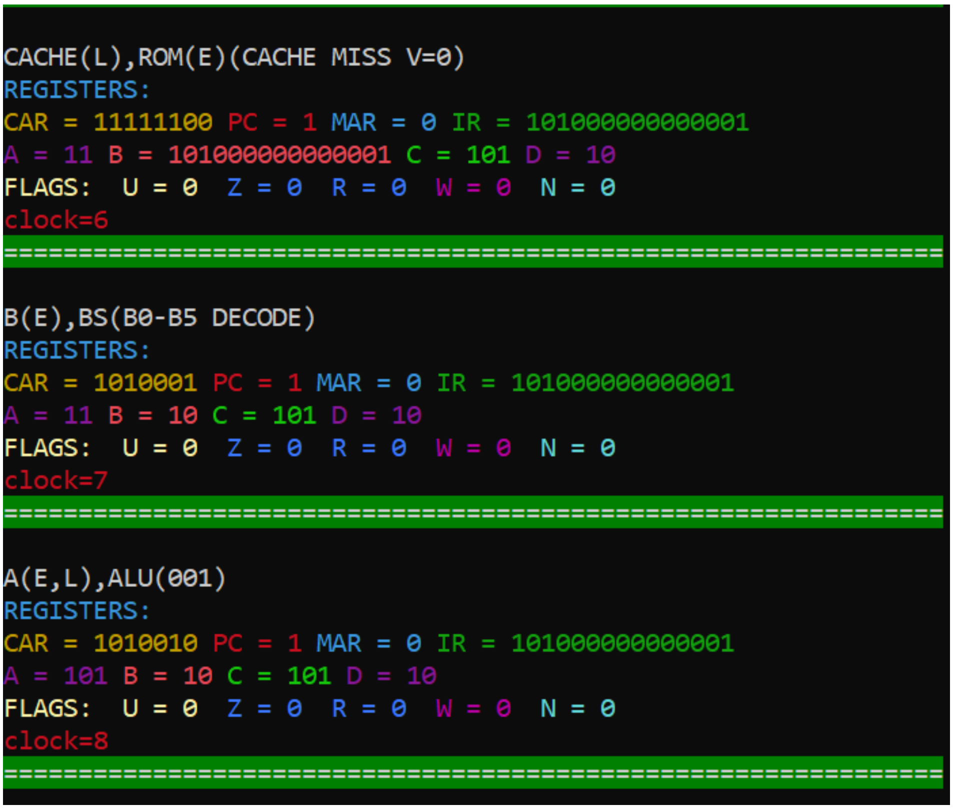
```
DEC

NOP
REGISTERS:
CAR = 101000 PC = 10 MAR = 10 IR = 10000000000000
A = 10 B = 10000000000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=16
===============================================================

 Cache(L),ROM(E){CACHE miss }(V=0)
REGISTERS:
CAR = 11111000 PC = 10 MAR = 10 IR = 10000000000000
A = 10 B = 10000000000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=17
===============================================================

PC(E),MAR(L){CACHE hit }
REGISTERS:
CAR = 11111001 PC = 10 MAR = 10 IR = 10000000000000
A = 10 B = 10000000000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=18
===============================================================

[MAR]->IR,PC(I){CACHE hit}
REGISTERS:
CAR = 11111010 PC = 11 MAR = 10 IR = 10100000000000
A = 10 B = 10000000000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=19
===============================================================
```



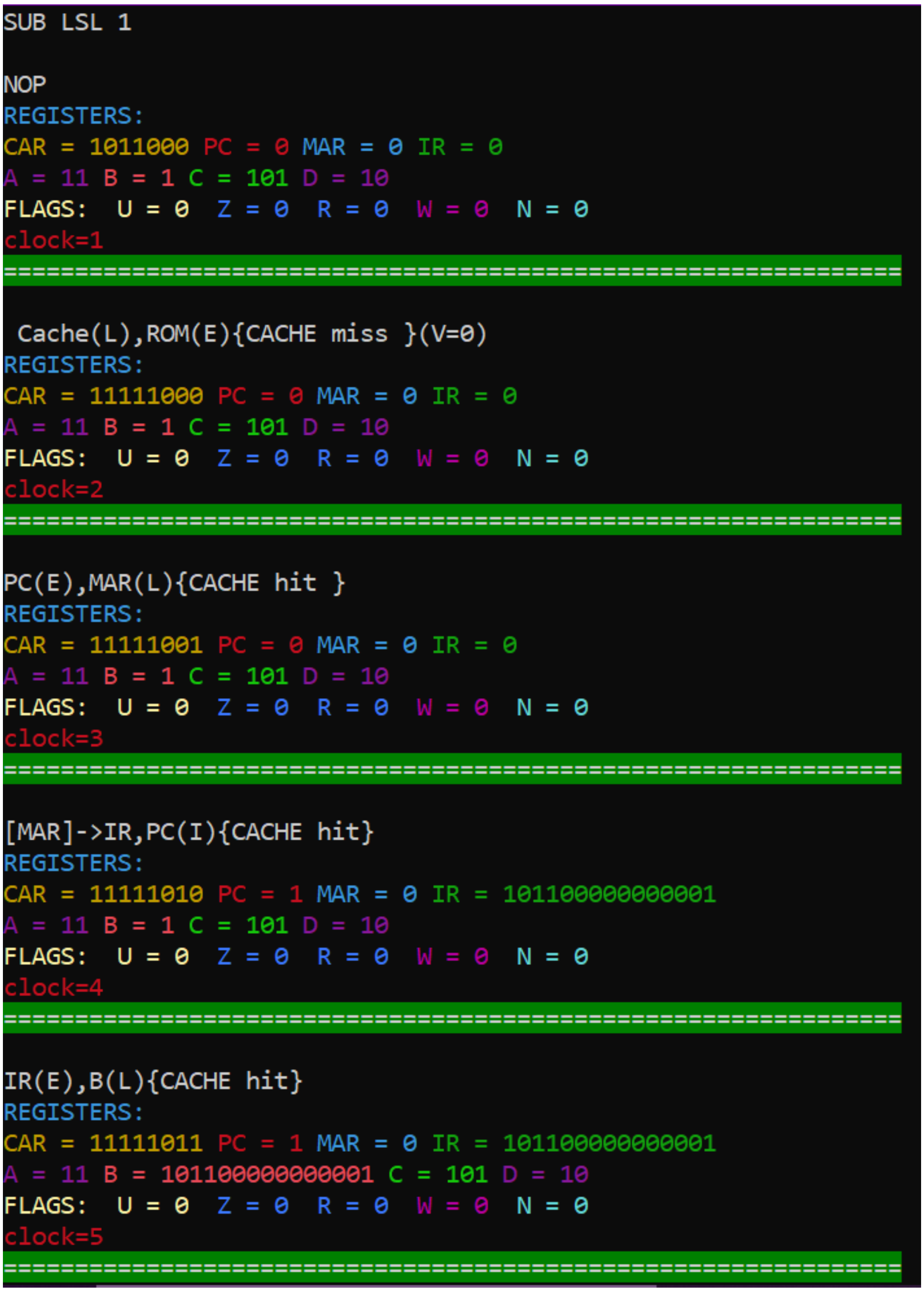
```
IR(E),B(L){CACHE hit}
REGISTERS:
CAR = 11111011 PC = 11 MAR = 10 IR = 10100000000000
A = 10 B = 10100000000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=20
===============================================================

CACHE(L),ROM(E)(CACHE MISS V=0)
REGISTERS:
CAR = 11111100 PC = 11 MAR = 10 IR = 10100000000000
A = 10 B = 10100000000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=21
===============================================================

A(E,L),ALU(100),R
REGISTERS:
CAR = 101001 PC = 11 MAR = 10 IR = 10100000000000
A = 1 B = 10100000000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=22
===============================================================
```



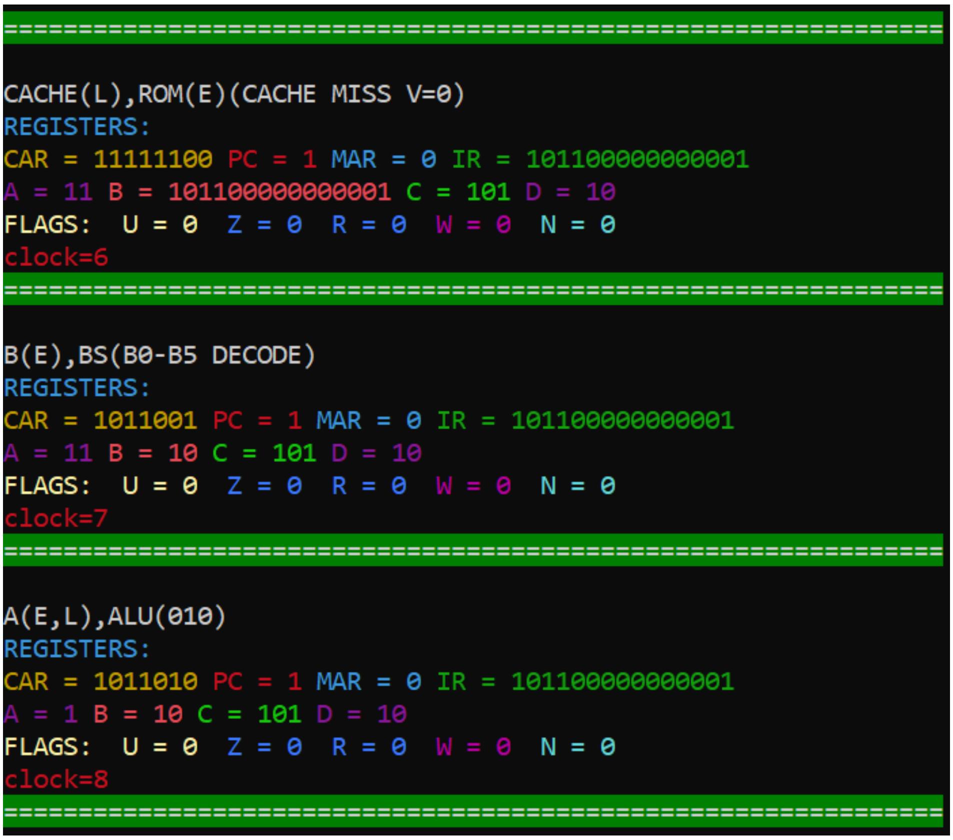
```
ADD LSL 1

NOP
REGISTERS:
CAR = 1010000 PC = 0 MAR = 0 IR = 0
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=1
===============================================================

 Cache(L),ROM(E){CACHE miss }(V=0)
REGISTERS:
CAR = 11111000 PC = 0 MAR = 0 IR = 0
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=2
===============================================================

PC(E),MAR(L){CACHE hit }
REGISTERS:
CAR = 11111001 PC = 0 MAR = 0 IR = 0
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=3
===============================================================

[MAR]->IR,PC(I){CACHE hit}
REGISTERS:
CAR = 11111010 PC = 1 MAR = 0 IR = 101000000000001
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=4
===============================================================

IR(E),B(L){CACHE hit}
REGISTERS:
CAR = 11111011 PC = 1 MAR = 0 IR = 101000000000001
A = 11 B = 101000000000001 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=5
===============================================================
```

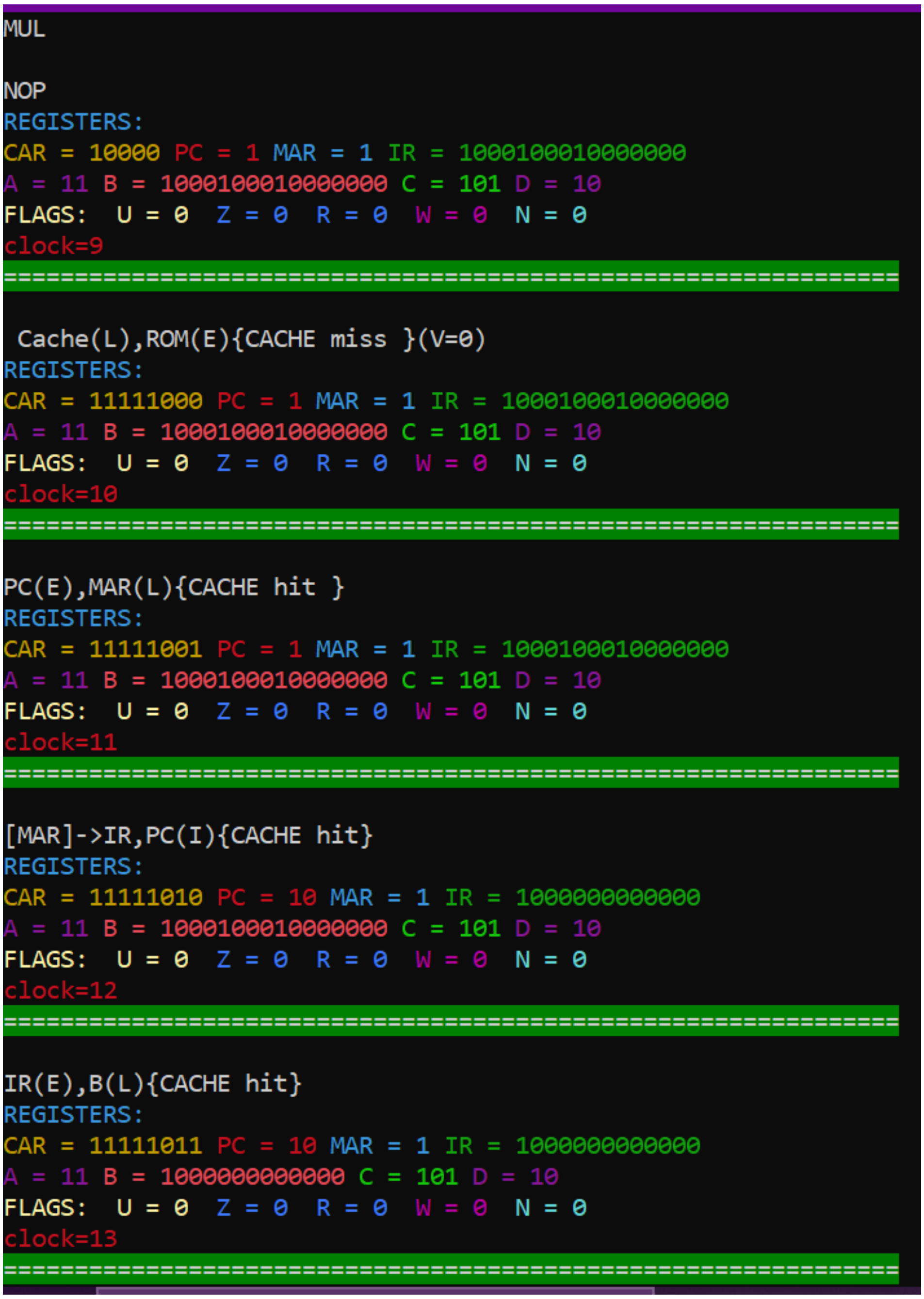


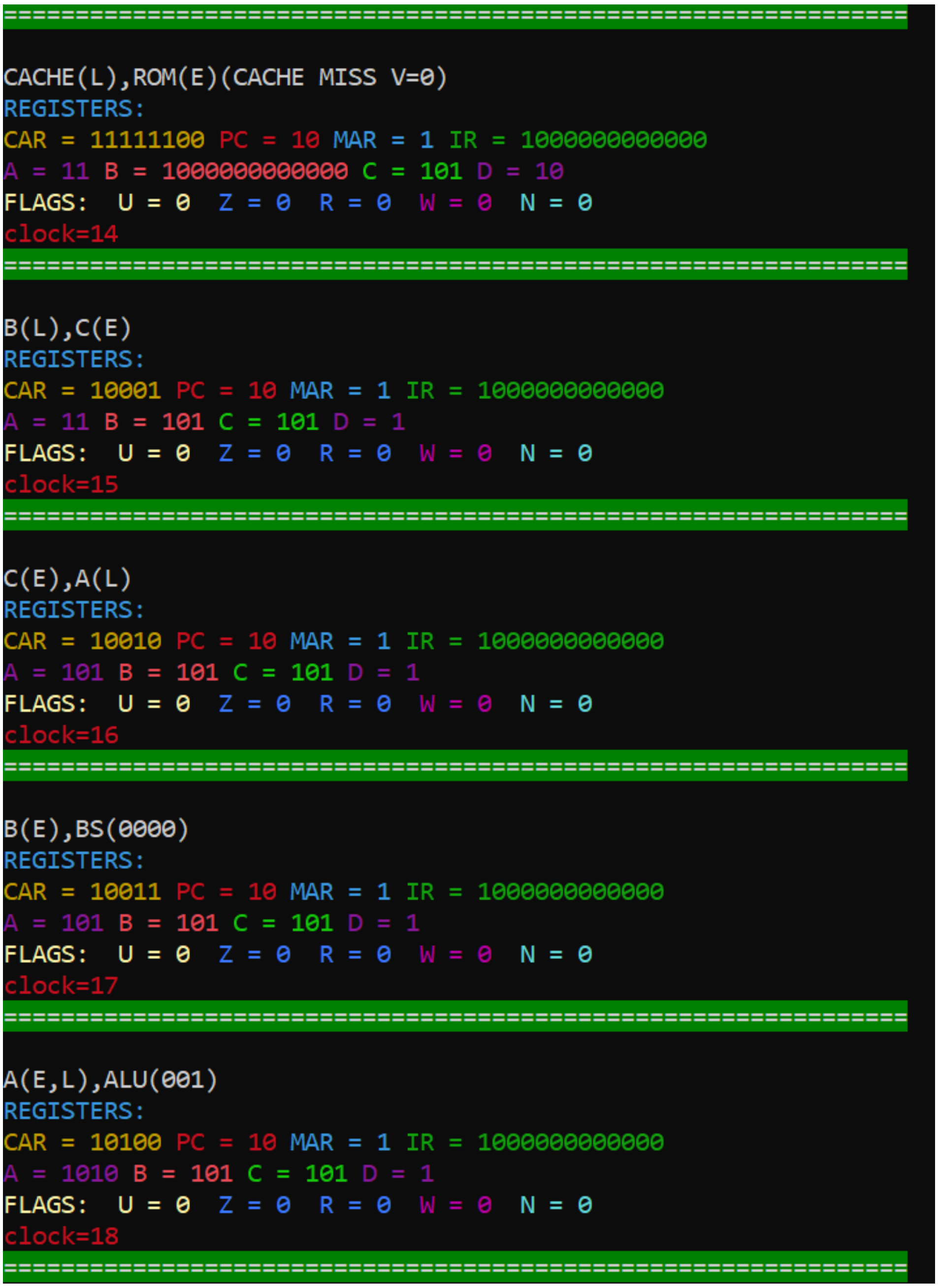
```
CACHE(L),ROM(E)(CACHE MISS V=0)
REGISTERS:
CAR = 11111100 PC = 1 MAR = 0 IR = 101000000000001
A = 11 B = 101000000000001 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=6
===============================================================

B(E),BS(B0-B5 DECODE)
REGISTERS:
CAR = 1010001 PC = 1 MAR = 0 IR = 101000000000001
A = 11 B = 10 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=7
===============================================================

A(E,L),ALU(001)
REGISTERS:
CAR = 1010010 PC = 1 MAR = 0 IR = 101000000000001
A = 101 B = 10 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=8
===============================================================
```



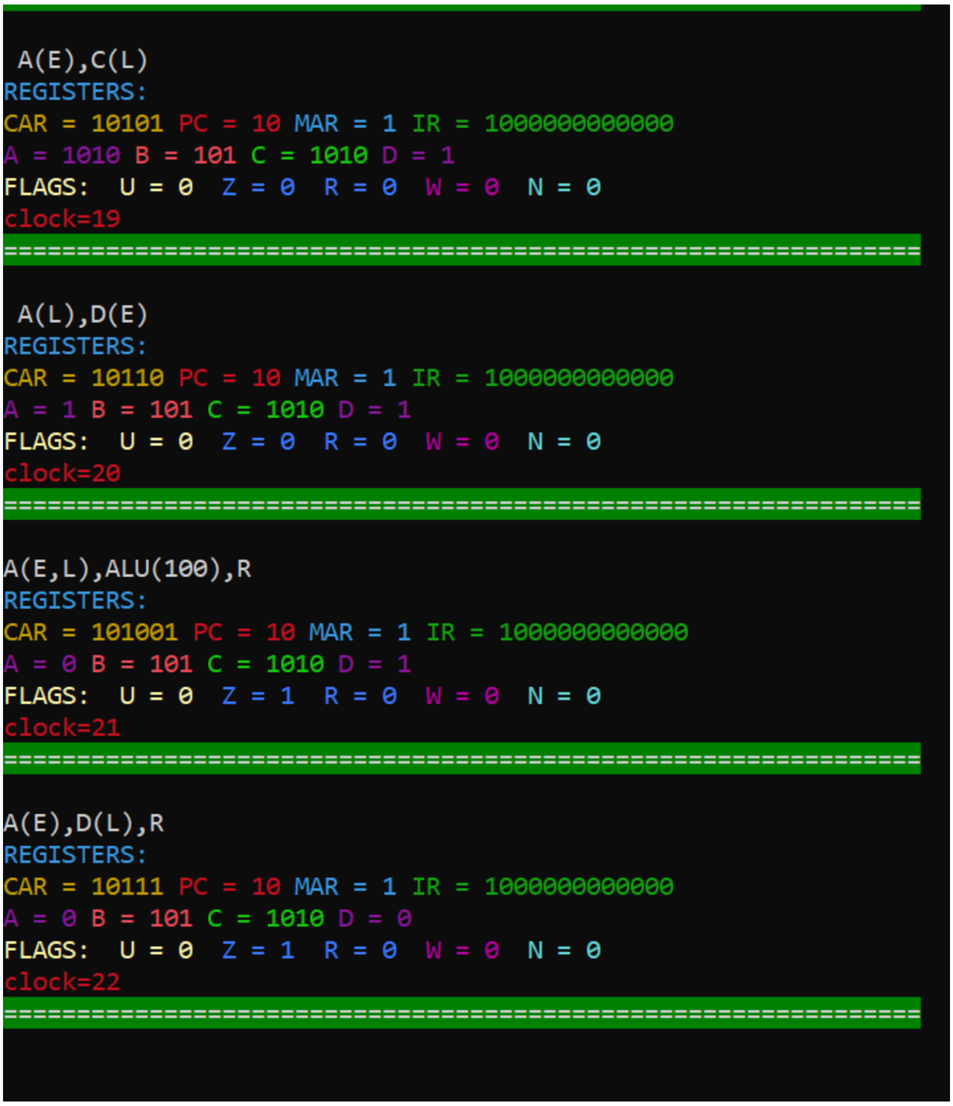
```
SUB LSL 1

NOP
REGISTERS:
CAR = 1011000 PC = 0 MAR = 0 IR = 0
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=1
================================================================

 Cache(L),ROM(E){CACHE miss }(V=0)
REGISTERS:
CAR = 11111000 PC = 0 MAR = 0 IR = 0
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=2
================================================================

PC(E),MAR(L){CACHE hit }
REGISTERS:
CAR = 11111001 PC = 0 MAR = 0 IR = 0
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=3
================================================================

[MAR]->IR,PC(I){CACHE hit}
REGISTERS:
CAR = 11111010 PC = 1 MAR = 0 IR = 101100000000001
A = 11 B = 1 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=4
================================================================

IR(E),B(L){CACHE hit}
REGISTERS:
CAR = 11111011 PC = 1 MAR = 0 IR = 101100000000001
A = 11 B = 101100000000001 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=5
================================================================
```


```
===============================================================

CACHE(L),ROM(E)(CACHE MISS V=0)
REGISTERS:
CAR = 11111100 PC = 1 MAR = 0 IR = 101100000000001
A = 11 B = 101100000000001 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=6
===============================================================

B(E),BS(B0-B5 DECODE)
REGISTERS:
CAR = 1011001 PC = 1 MAR = 0 IR = 101100000000001
A = 11 B = 10 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=7
===============================================================

A(E,L),ALU(010)
REGISTERS:
CAR = 1011010 PC = 1 MAR = 0 IR = 101100000000001
A = 1 B = 10 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=8
===============================================================
```


```
MUL

NOP
REGISTERS:
CAR = 10000 PC = 1 MAR = 1 IR = 1000100010000000
A = 11 B = 1000100010000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=9
==============================================================

 Cache(L),ROM(E){CACHE miss }(V=0)
REGISTERS:
CAR = 11111000 PC = 1 MAR = 1 IR = 1000100010000000
A = 11 B = 1000100010000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=10
==============================================================

PC(E),MAR(L){CACHE hit }
REGISTERS:
CAR = 11111001 PC = 1 MAR = 1 IR = 1000100010000000
A = 11 B = 1000100010000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=11
==============================================================

[MAR]->IR,PC(I){CACHE hit}
REGISTERS:
CAR = 11111010 PC = 10 MAR = 1 IR = 1000000000000
A = 11 B = 1000100010000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=12
==============================================================

IR(E),B(L){CACHE hit}
REGISTERS:
CAR = 11111011 PC = 10 MAR = 1 IR = 1000000000000
A = 11 B = 1000000000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=13
==============================================================
```



```
==============================================================

CACHE(L),ROM(E)(CACHE MISS V=0)
REGISTERS:
CAR = 11111100 PC = 10 MAR = 1 IR = 1000000000000
A = 11 B = 1000000000000 C = 101 D = 10
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=14
==============================================================

B(L),C(E)
REGISTERS:
CAR = 10001 PC = 10 MAR = 1 IR = 1000000000000
A = 11 B = 101 C = 101 D = 1
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=15
==============================================================

C(E),A(L)
REGISTERS:
CAR = 10010 PC = 10 MAR = 1 IR = 1000000000000
A = 101 B = 101 C = 101 D = 1
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=16
==============================================================

B(E),BS(0000)
REGISTERS:
CAR = 10011 PC = 10 MAR = 1 IR = 1000000000000
A = 101 B = 101 C = 101 D = 1
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=17
==============================================================

A(E,L),ALU(001)
REGISTERS:
CAR = 10100 PC = 10 MAR = 1 IR = 1000000000000
A = 1010 B = 101 C = 101 D = 1
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=18
==============================================================
```



```
 A(E),C(L)
REGISTERS:
CAR = 10101 PC = 10 MAR = 1 IR = 1000000000000
A = 1010 B = 101 C = 1010 D = 1
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=19
===============================================================

 A(L),D(E)
REGISTERS:
CAR = 10110 PC = 10 MAR = 1 IR = 1000000000000
A = 1 B = 101 C = 1010 D = 1
FLAGS:  U = 0  Z = 0  R = 0  W = 0  N = 0
clock=20
===============================================================

A(E,L),ALU(100),R
REGISTERS:
CAR = 101001 PC = 10 MAR = 1 IR = 1000000000000
A = 0 B = 101 C = 1010 D = 1
FLAGS:  U = 0  Z = 1  R = 0  W = 0  N = 0
clock=21
===============================================================

A(E),D(L),R
REGISTERS:
CAR = 10111 PC = 10 MAR = 1 IR = 1000000000000
A = 0 B = 101 C = 1010 D = 0
FLAGS:  U = 0  Z = 1  R = 0  W = 0  N = 0
clock=22
===============================================================
```