CS370 Operating Systems

Colorado State University
Yashwant K Malaiya
Fall 2016

Slides based on
- Text by Silberschatz, Galvin, Gagne
- Various sources

What do these terms mean?

- Operating Systems

- Virtual

- Concurrent

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Topics covered in this lecture

- Course Overview
- Expectations
- Introduction

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Course webpage

- All course materials will be on
  - the course webpage

    http://www.cs.colostate.edu/~cs370

  - canvas

- Schedule

- Lectures

- Assignments

- Announcements

- Grades will be posted on Canvas

- The course website and canvas are live now

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Contacting us

- Instructor

  Yashwant Malaiya

  Computer Science (CSB 364)

  Office Hours: 1-2 PM Monday, 3-4 PM Thursday

- GTA

  Rejina Basnet

  Office Hours in CSB 120: TBA, TBA

- UTAs: **Leon Ang Li, Sam Maxwell**

- All e-mail should be sent to cs370@cs.colostate.edu
- The subject should start as **CS370: …**

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Topics we will cover in CS 370

- Processes and Threads

- CPU Scheduling

- Process Synchronization and Deadlocks

- Memory Management

- File System interface and management

- Storage Management

- Virtualization

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Textbook

- Operating Systems Concepts, 9th edition

  Avi Silberschatz, Peter Galvin, and Greg Gagne

  Publisher - John Wiley & Sons, Inc.

  (The Dinosaur Book)

- May also use materials from other sources including
  - Andrew S Tanenbaum, Modern Operating Systems
  - Thomas Anderson and Michael Dahlin, Operating Systems Principles & Practice
  - S. Pallikara, R. Wakefield
  - Other sources

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- Topics that will be covered and the order in they will be covered

- Readings -chapters that I will cover

- May also see chapters mentions of other resources besides the textbook

- Schedule for when the assignments will be posted and when they are due
  - Subject to dynamic adjustment

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Grading breakdown

- Assignments: 30%
  - Programming & written
- Quizzes 10%
  - On-line, in-class
- Mid Term: 20%
- Project: 15%
- Final exam: 25%

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Grading Policy I

- Letter grades will be based on the following standard breakpoints:

  >= 90 is an A, >= 88 is an A-,

  >=86 is a B+, >=80 is a B, >=78 is a B-,

  >=76 is a C+, >=70 is a C,

  >=60 is a D, and <60 is an F.

- I will not cut higher than this, but I may cut lower.

- There will be no make-up exams
  - Except for documented
    - required university event
    - acceptable family or medical emergency

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Grading Policy II

- Plan: Every assignment will be posted about 2 weeks before the due date.
  - Every assignment will include information about how much it will count towards the course grade, and how it will be graded.
- Late submission penalty: 10%/day for the first 2 days and a ZERO thereafter.
- Detailed submission instructions posted on course website.
- Plan: Assignments will be graded within 2 weeks of submission

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What will Quizzes and Tests include?

- I will only ask questions about what I teach or ask you to study
  - If I didn't teach it, I won't ask from that portion
- If the concepts were covered in my lectures/slides/assignments
  - You should be able to answer the questions
- I will try to avoid questions about arcane aspects of some esoteric device controller

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Exams

- One mid-term (20%)
- The final exam is comprehensive, but more emphasis on the later part (25%)
- There will be 10-12 quizzes (in class or online) (10%)
  - we may convert some homework into on-line quizzes
- Programming/ writen assignments
  - 30% of your course grade
- If you walk into class more than 20 minutes late, there is an automatic 75% deduction on the quiz score.

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Term paper and poster session

- Group based
  - Logistics to be determined
- A poster session where you will describe your work
- The term paper is a group assignment
  - More details later
- Tentative topics (to be determined later)
  - Multi-core Architectures
  - Reliability/Security
  - ?

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Electronic devices in lecture room

- Permitted only in the last row, with the pledge that you will
  - not distract others
  - use it only for class related use
  - turn off wireless

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Be kind to everyone

- You will be courteous to fellow students, instructor and teaching assistants
  - Classroom, outside, discussion board
- Do not distract your peers
  - No chatting
  - No eating
  - No cellphone use

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Help me help you

- Surveys at the end of a class
- You will provide a list of
  - 2 concepts you followed clearly
  - 2 concepts you had problems keeping up
  - Problem areas for the majority of the class will be addressed in the next class

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Research

- Computer security
  - Vulnerability discovery
  - Risk evaluation
  - Impact of security breaches
  - Vulnerability markets
- Hardware and software
  - Testing & test effectiveness
  - Reliability and fault tolerance
- Results have been used by industry, researchers and educators

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About me

- Teaching
  - Computer Organization (CS270)
  - Computer Architecture (CS470)
  - Operating systems (CS370)
  - Fault tolerant computing (CS530)
- Professional
  - Organized international conferences on Microarchitecture, VLSI Design, Testing, Software Reliability
  - Computer Science Accreditation: national & international
  - Professional lectures

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EXPECTATIONS

- You are expected to attend all classes

- Assignments have to be done individually

- Expect to work at least 6-8 hours per week outside of class
  - Coding and reviewing material from class

- If you miss a lecture?
  - Add about 3 hours per missed lecture

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Expert view on How to fail this class?

- Believing that you can learn via osmosis

- Missing lectures
  - "If you don't have the discipline to show up, you will most likely not have the discipline to catch up"
  - Procrastinating
  - Get started on the assignments early

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Interactions

- You ca have discussions with me, the GTA, UTAs, and your peers
- But note
  - No code can be exchanged under any circumstances
  - No one takes over someone else's keyboard
  - No code may be copied and pasted from anywhere, unless provided by us
- Bumps are to be expected along the way
  - But you should get over this yourself
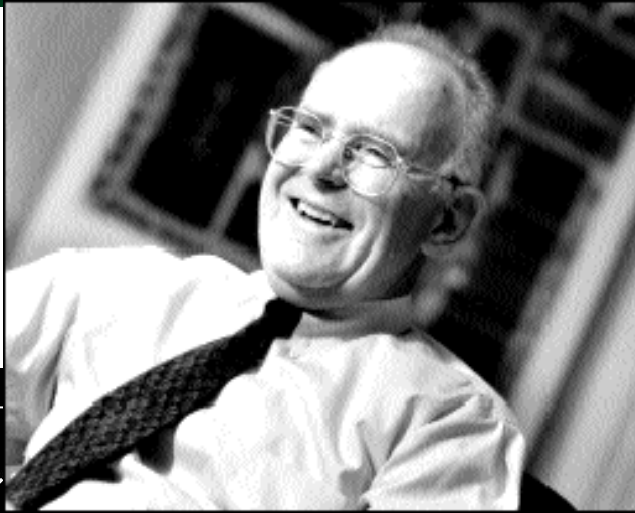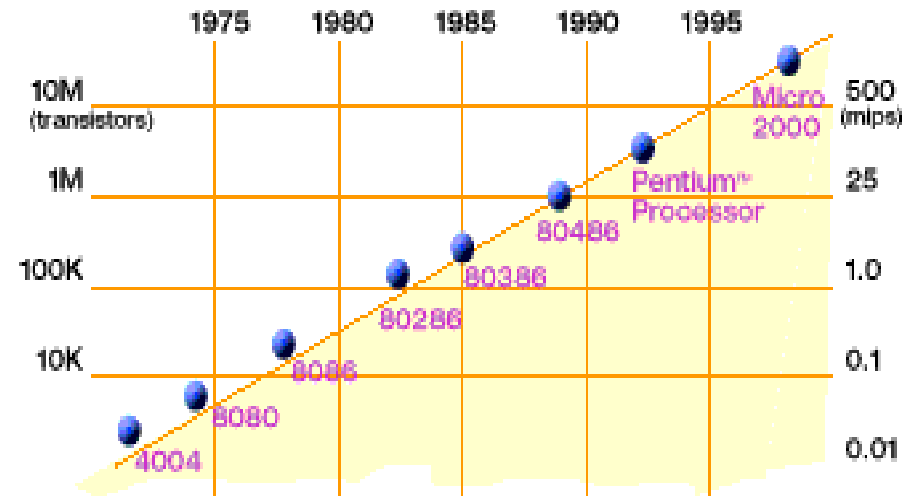 - It will help you with the next problem you encounter

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Operator …

Switchboard Operator

©UCB
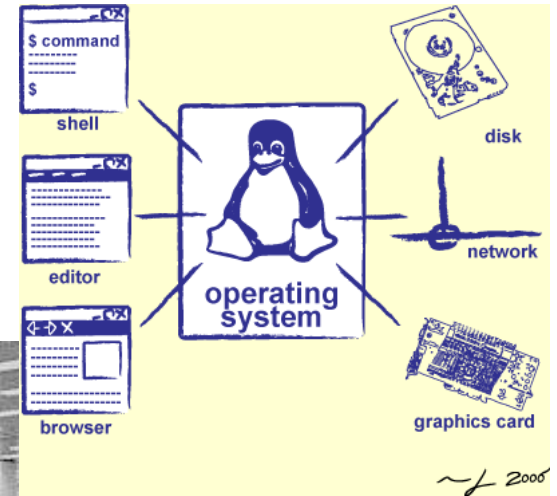
Computer Operators

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Technology Trends: Moore's Law

2X transistors/Chip Every 1.5 years
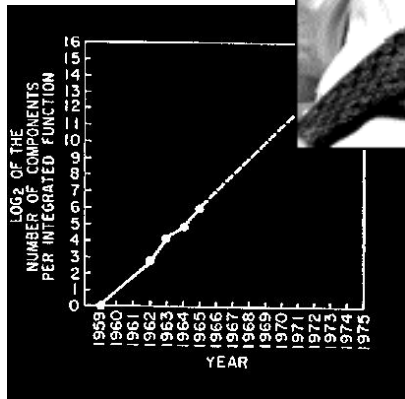
Called "Moore's Law"

Gordon Moore (co-founder of Intel) predicted in 1965 that the transistor density of semiconductor chips would double roughly every 18 months.

Microprocessors have become smaller, denser, and more powerful.

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Computer Performance Over Time

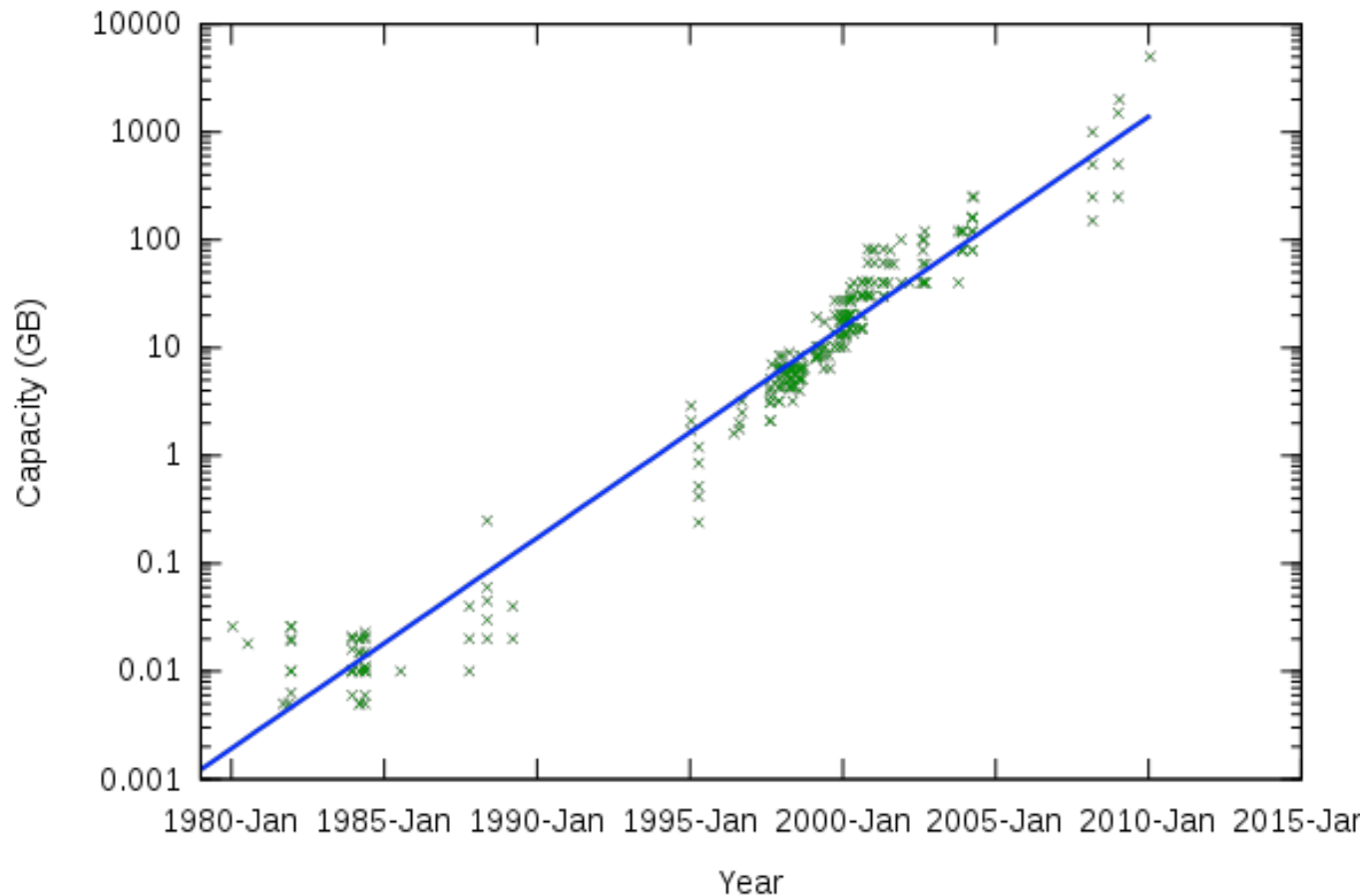|	1981	1997	2014	Factor (2014/1981)
Uniprocessor speed (MIPS)	1	200	2500	2.5K
CPUs per computer	1	1	10+	10+
Processor MIPS/$	$100K	$25	$0.20	500K
DRAM Capacity (MiB)/$	0.002	2	1K	500K
Disk Capacity (GiB)/$	0.003	7	25K	10M
Home Internet	300 bps	256 Kbps	20 Mbps	100K
Machine room network	10 Mbps (shared)	100 Mbps (switched)	10 Gbps (switched)	1000
Ratio of users to computers	100:1	1:1	1:several	100+

Anderson Dahlin 2014

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25

From David Culler

log (people per computer)

Number Crunching
Data Storage

productivity
interactive

streaming
information
to/from physical
world

year
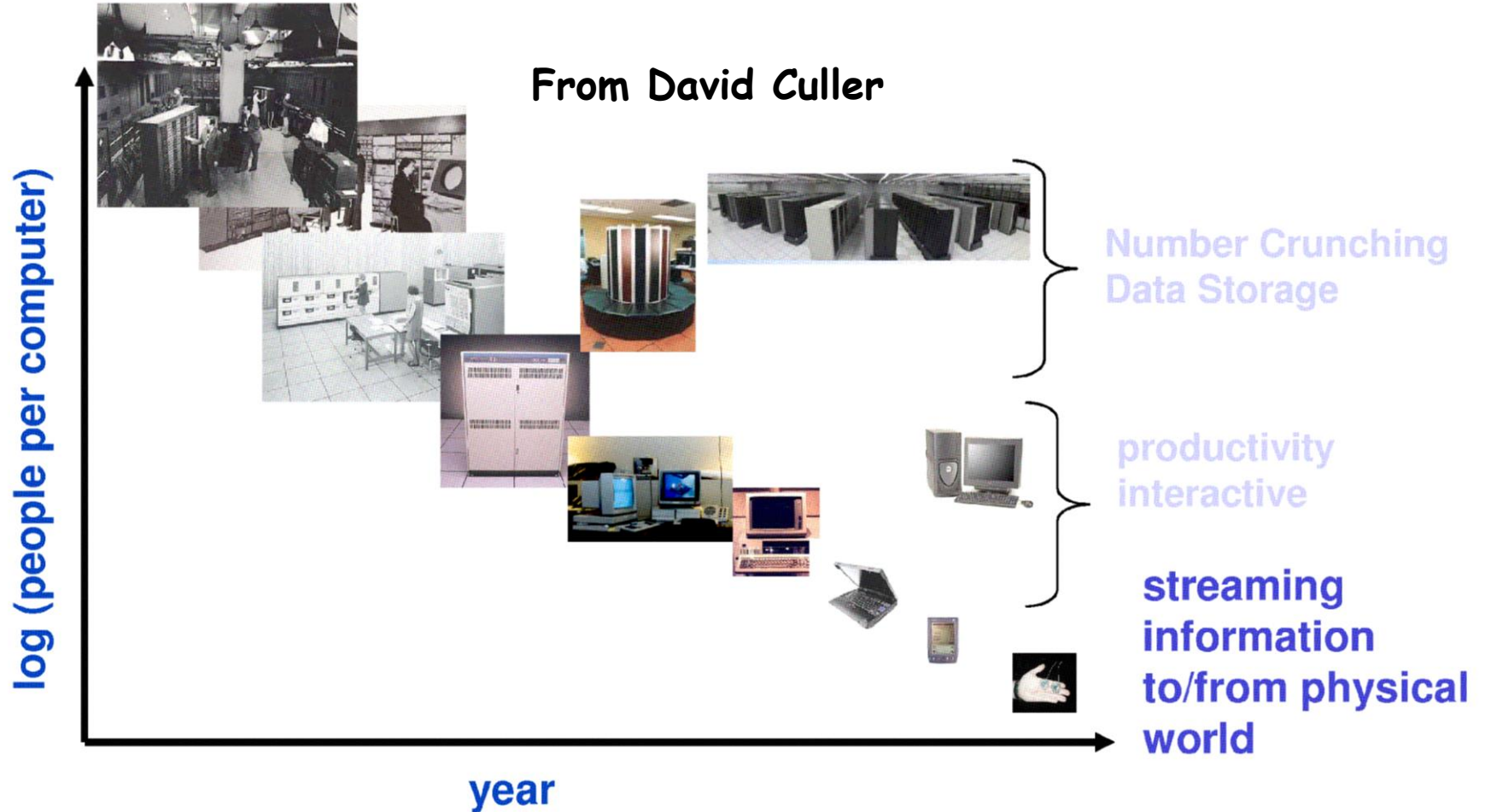
- Today: Multiple CPUs/person!
  - Approaching 100s?

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- *Retail* hard disk capacity in GB
  (source: http://www.digitaltonto.com/2011/our-emergent-digital-future/)

What is an Operating System?

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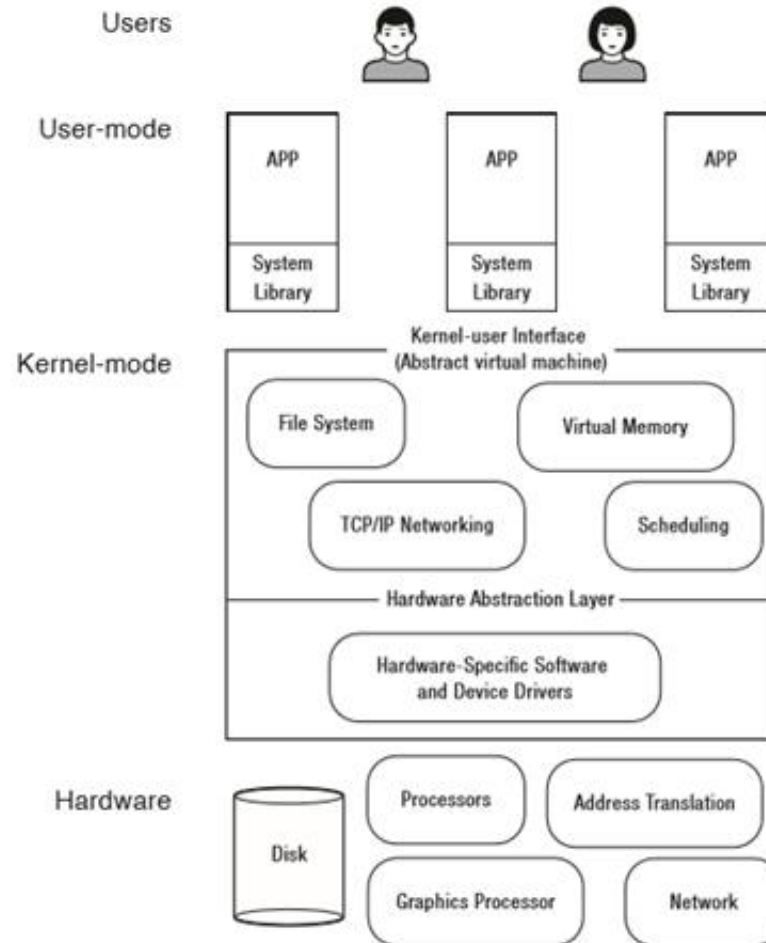
What is an Operating System?

- **Referee**
  - Manage sharing of resources, Protection, Isolation
   - Resource allocation, isolation, communication
- **Illusionist**
  - Provide clean, easy to use abstractions of physical resources
    - Infinite memory, dedicated machine
    - Higher level objects: files, users, messages
    - Masking limitations, virtualization
- **Glue**
  - Common services
    - Storage, Window system, Networking
    - Sharing, Authorization
    - Look and feel

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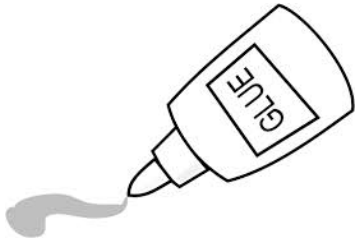
A Modern processor: SandyBridge
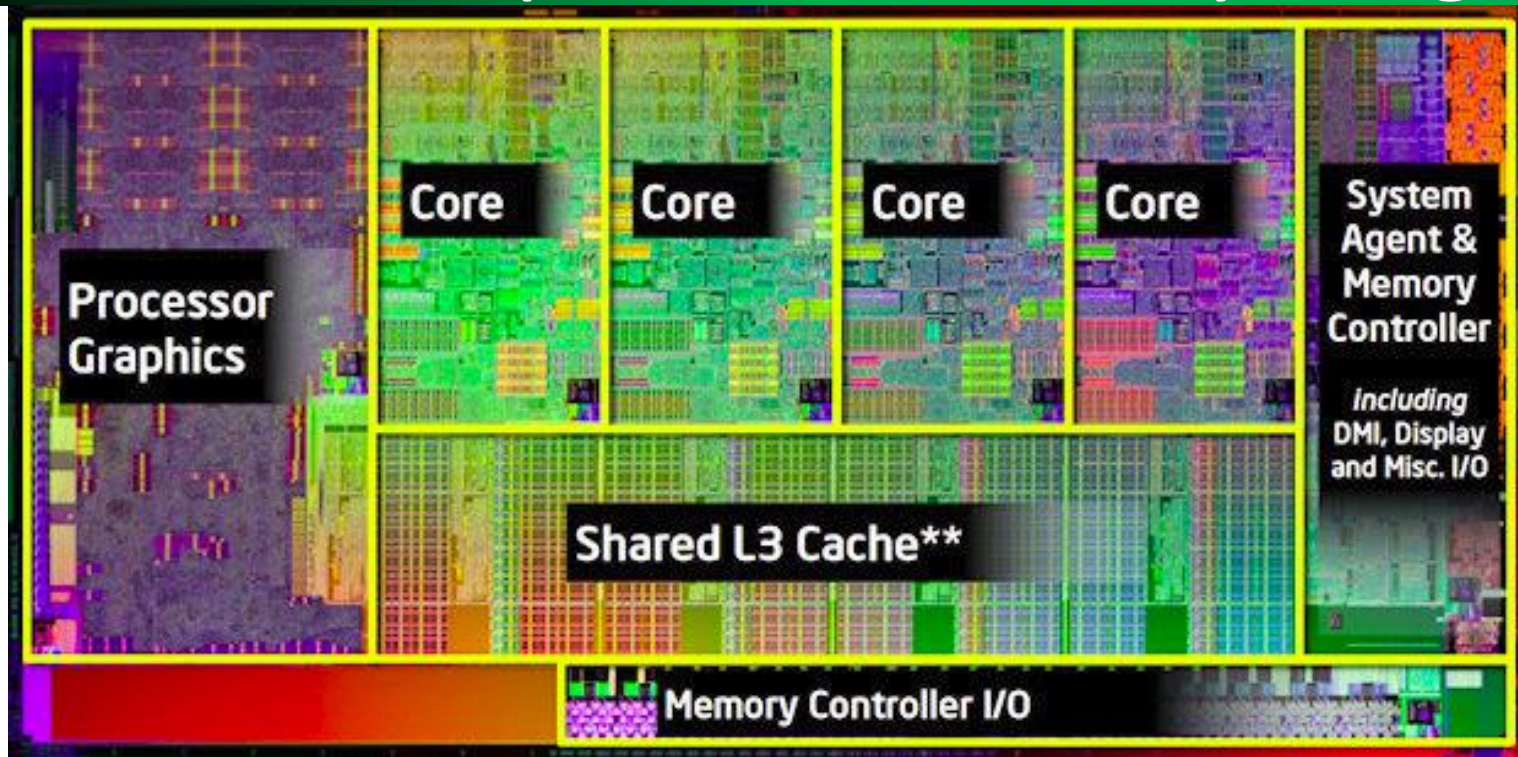
- Package: LGA 1155
  - 1155 pins
  - 95W design envelope
- Cache:
  - L1: 32K Inst, 32K Data (3 clock access)
  - L2: 256K (8 clock access)
  - Shared L3: 3MB – 20MB (not out yet)

- Transistor count:
  - 504 Million (2 cores, 3MB L3)
  - 2.27 Billion (8 cores, 20MB L3)
- Note that ring bus is on high metal layers – above the Shared L3 Cache

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Functionality comes with

SandyBridge I/O Configuration

Proc

Caches

Busses

Memory

adapters

Controllers

Networks

I/O Devices:

Disks
Displays
Keyboards

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