Unit I
PART-A

Q.No	Question	Text Book	Blooms Taxonomy level	CLO
1.	1. The _____ format is usually used to store data. **a) BCD** b) Decimal c) Hexadecimal d) Octal			
2.	A source program is usually in _____ a) Assembly language b) Machine level language **c) High-level language** d) Natural language			
3.	The small extremely fast, RAM's are called as _____ **a) Cache** b) Heaps c) Accumulators d) Stacks			
4.	_____ bus structure is usually used to connect I/O devices. **a) Single bus** b) Multiple bus c) Star bus d) Rambus			
5.	The Input devices can send information to the processor. **a) When the SIN status flag is set** b) When the data arrives regardless of the SIN flag c) Neither of the cases d) Either of the cases			

6.	The decoded instruction is stored in _____ **a) IR** b) PC c) Registers d) MDR			
7.	Which of the register/s of the processor is/are connected to Memory Bus? a) PC **b) MAR** c) IR d) Both PC and MAR			
8.	ISP stands for _____ **a) Instruction Set Processor** b) Information Standard Processing c) Interchange Standard Protocol d) Interrupt Service Procedure			
9.	The internal components of the processor are connected by _____ a) Processor intra-connectivity circuitry **b) Processor bus** c) Memory bus d) Rambus			
10.	The registers, ALU and the interconnection between them are collectively called as _____ a) process route b) information trail c) information path **d) data path**			
11.	An optimizing Compiler does _____ a) Better compilation of the given piece of code **b) Takes advantage of the type of processor and reduces its process time** c) Does better memory management d) None of the mentioned			

12.	. When Performing a looping operation, the instruction gets stored in the _____ a) Registers **b) Cache** c) System Heap d) System stack			
13.	To reduce the memory access time we generally make use of _____ a) Heaps b) Higher capacity RAM's c) SDRAM's **d) Cache's**			
14.	The time delay between two successive initiations of memory operation _____ a) Memory access time b) Memory search time **c) Memory cycle time** d) Instruction delay			
15.	During the execution of a program which gets initialized first? a) MDR b) IR **c) PC** d) MAR			
16.	The internal components of the processor are connected by _____ a)Processor intra-connectivity circuitry b)**Processor bus** c)Memory bus d) Rambus			

17.	In multiple Bus organisation, the registers are collectively placed and referred as _____ a) Set registers **b) Register file** c) Register Block d) Map registers			
18.	he ISA standard Buses are used to connect _____ a) RAM and processor b) GPU and processor c) **Harddisk and Processor** d) CD/DVD drives and Processor			
19.	An optimizing Compiler does _____ a) Better compilation of the given piece of code **b) Takes advantage of the type of processor and reduces its process time** c) Does better memory management d) None of the mentioned			
20.	When Performing a looping operation, the instruction gets stored in the _____ a) Registers **b) Cache** c) System Heap d) System stack			
21.	The circuit used to store one bit of data is called a) Registers b) Encoder c) Decoder **d) Flip flop**			

22.	The average time required to reach a storage location in memory and obtain its content is a) Turnaround time **b) Access time** c) Seek time d) Transfer time			
23.	The addressing mode used in the instruction ADD X,Y is a) Direct b) Indirect c) Absolute **d) index**			
24.	A stack organised computer uses instruction of **a) Zero addressing** b) One addressing c) Two addressing d) Three addressing			
25.	An n-bit microprocessor has a) n-bit program counter **b) n-bit instruction register** c) n-bit stack pointer d) n-bit address register			
26.	The register that keeps track of the instructions of a program in the memory a) Instruction Register **b) Program Counter** c) Index Register d) Accumulator			

27.	The BSA instruction is a) Branch and store accumulator **b) Branch and save return address** c) Branch and shift address d) Branch and show accumulator			
28.	The load instruction is used to designate a transfer from memory to a processor register known as **a) Accumulator** b) Instruction register c) Program counter d) Index register			
29.	Status bit is also called as a) Binary bit **b) Flag bit** c) Signed bit d) Unsigned bit			
30.	What is the content of Stack Pointer(SP)? a) Address of current instruction b) Address of next instruction **c) Address of top element of stack** d) Size of stack			
31.	In assembly language programming, the minimum number of operands required for an instruction is/are **a) Zero** b) One c) Two d) Three			

32.	In which addressing mode the operand is given explicitly in the instruction **a) Immediate** b) Register c) Direct d) Indirect			
33.	The ALU makes use of _____ to store the intermediate results. **a) Accumulators** b) Registers c) Heap d) Stack			
34.	The control unit controls other units by generating _____ a) Control signals **b) Timing signals** c) Transfer signals d) Command Signals			
35.	The instruction -> Add LOCA, R0 does _____ a) Adds the value of LOCA to R0 and stores in the temp register b) Adds the value of R0 to the address of LOCA **c) Adds the values of both LOCA and R0 and stores it in R0** d) Adds the value of LOCA with a value in accumulator and stores it in R0			
36.	The bus used to connect the monitor to the CPU is _____ a) PCI bus **b) SCSI bus** c) Memory bus d) Rambus			

37.	Add #45, when this instruction is executed the following happen/s _____ a) The processor raises an error and requests for one more operand **b) The value stored in memory location 45 is retrieved and one more operand is requested** c) The value 45 gets added to the value on the stack and is pushed onto the stack d) None of the mentioned			
38.	In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is _____ a) EA = 5+R1 b) EA = R1 c) EA = [R1] **d) EA = 5+[R1]**			
39.	The effective address of the following instruction is MUL 5(R1,R2). a) 5+R1+R2 b) 5+(R1*R2) **c) 5+[R1]+[R2]** d) 5*([R1]+[R2])			
40.	An 24 bit address generates an address space of _____ locations. a) 1024 b) 4096 c) 2^{48} **d) 16,777,216**			
41.	The type of memory assignment used in Intel processors is _____ **a) Little Endian** b) Big Endian c) Medium Endian d) None of the mentioned			

42.	RTN stands for _____ **a) Register Transfer Notation** b) Register Transmission Notation c) Regular Transmission Notation d) Regular Transfer Notation			
43.	The instruction, Add R1,R2,R3 in RTN is _____ a) R3=R1+R2+R3 b) R3<-[R1]+[R2]+[R3] c) R3=[R1]+[R2] **d) R3<-[R1]+[R2]**			
44.	The two phases of executing an instruction are _____ a) Instruction decoding and storage **b) Instruction fetch and instruction execution** c) Instruction execution and storage d) Instruction fetch and Instruction processing			
45.	When using Branching, the usual sequencing of the PC is altered. A new instruction is loaded which is called as _____ **a) Branch target** b) Loop target c) Forward target d) Jump instruction			
46.	_____ converts the programs written in assembly language into machine instructions. a) Machine compiler b) Interpreter **c) Assembler** d) Converter			

47.	The alternate way of writing the instruction, ADD #5,R1 is _____ a) ADD [5],[R1]; **b) ADDI 5,R1;** c) ADDIME 5,[R1]; d) There is no other way			
48.	_____ the most suitable data structure used to store the return addresses in the case of nested subroutines. a) Heap **b) Stack** c) Queue d) List			
49.	The system is notified of a read or write operation by _____ a) Appending an extra bit of the address b) Enabling the read or write bits of the devices c) Raising an appropriate interrupt signal **d) Sending a special signal along the BUS**			
50.	The method of synchronising the processor with the I/O device in which the device sends a signal when it is ready is? a) Exceptions b) Signal handling **c) Interrupts** d) DMA			

PART-B

Q.No	Question	Text book	Blooms Taxonomy Level	CLO

1.	Explain the various functional units of a computer.			
2.	Explain the various types of Memory System.			
3.	Explain the role of registers – PC, IR, MAR and MDR in processor.			
4.	What is a Bus? Explain Single and Multiple Bus Structure.			
5.	Explain Register Transfer Notation with examples.			
6.	Explain Assembly Language Notation with examples.			
7.	What are the different types of Instruction Format? Explain each with an example.			
8.	Differentiate RISC and CISC.			
9.	What are Assembler Directives? Give an example.			
10	Explain various Processor and CPU cores in ARM processor.			

PART-C

Q.No	Question	Text book	Blooms Taxonomy Level	CLO

1.	Explain Instruction Execution in Straight Line Sequencing and Branching.			
2.	Describe various Addressing Modes with suitable examples.			
3.	Explain basic I/O operations in detail.			
4.	Explain Memory location, memory addresses and memory operation in detail.			
5.	Define Microprocessor. Explain the evolution of Microprocessors in detail.			
6.	Explain Assembly Language Program with an example.			
7.	Explain ARM processor and Thumb instruction set in detail.			
8.	Explain Instruction encoding format for Load and Store instructions in ARM processor.			

UNIT-II

(MULTIPLE CHOICE QUESTIONS)

S.NO	QUESTION	BLOOMS LEVEL	CLO
1.	Which method/s of representation of numbers occupies large amount of memory than others ? **a) Sign-magnitude** b) 1′s compliment c) 2′s compliment d) Both a and b		
2.	Which representation is most efficient to perform arithmetic operations on the numbers ? a) Sign-magnitude b) 1′s compliment **c) 2′S compliment** d) None of the above		
3.	Which method of representation has two representations for ’0′ ? a) Sign-magnitude **b) 1′s compliment** c) 2′s compliment d) None of the above		
4.	When we perform subtraction on -7 and 1 the answer in 2′s compliment form is _____ . a) 1010 b) 1110 **c) 0110** d) 1000		
5.	When we perform subtraction on -7 and -5 the answer in 2′s compliment form is _____ . a) 11110 b) 1110 c) 1010 **d) 0010**		
6.	When we subtract -3 from 2, the answer in 2′s compliment form is _____ . a) 0001 b) 1101 **c) 0101** d) 1001		

7.	The processor keeps track of the results of its operations using a flags called _____ . **a) Conditional code flags** b) Test output flags c) Type flags d) Status flags		
8.	The register used to store the flags is called as _____ . a) Flag register **b) Status registers** c) Test register d) Log register		
9.	The Flag 'V' is set to 1 indicates that, **a) The operation is valid** b) The operation is validated c) The operation as resulted in an overflow d) Both a and c		
10.	In some pipelined systems, a different instruction is used to add to numbers which can affect the flags upon execution. That instruction is _____ . a) AddSetCC b) AddCC **c) Add++** d) SumSetCC		
11.	The most efficient method followed by computers to multiply two unsigned numbers is _____ . **a) Booth algorithm** b) Bit pair recording of multipliers c) Restoring algorithm d) Non restoring algorithm		
12.	For the addition of large integers most of the systems make use of _____ . a) Fast adders b) Full adders **c) Carry look-ahead adders** d) Ripple adder		

13.	In a normal n-bit adder , to find out if an overflow as occurred we make use of _____ . **a) And gate** b) Nand gate c) Nor gate d) Xor gate		
14.	In the implementation of a Multiplier circuit in the system we make use of _____ . a) Counter b) Flip flop **c) Shift register** d) Push down stack		
15.	When 1101 is used to divide 100010010 the remainder is _____ . a) 101 **b) 11** c) 0 d) 1		
16.	The logic operations are implemented using _____ circuits. a) Bridge b) Logical c) Combinatorial **d) Gate**		
17.	The carry generation function: ci + 1 = yici + xici + xiyi, is implemented in _____. a) Half adders **b) Full adders** c) Ripple adders d) Fast adders		
18.	The carry in the ripple adders,(which is true) a) Are generated at the beginning only. b) Must travel through the configuration. **c) Is generated at the end of each operation.** d) None of the above		
19.	In full adders the sum circuit is implemented using _____. a) And & or gates **b) NAND gate** c) XOR d) XNOR		

20.	The usual implementation of the carry circuit involves _____. **a) And and or gates** b) XOR c) NAND d) XNOR		
21.	**Problems in Multiplication** The product of 1101 & 1011 is a) 10001111 b) 10101010 **c) 11110000** d) 11001100		
22.	The product of -13 & 11 is a) 1100110011 **b) 1101110001** c) 1010101010 d) 1111111000		
23.	We make use of _____ circuits to implement multiplication. a) Flip flops b) Combinatorial **c) Fast adders** d) Carry look ahead		
24.	The multiplier is stored in _____. a) PC Register b) Shift register **c) Cache** d) IR		
25.	The _____ is used to co-ordinate the operation of the multiplier. **a) Controller** b) Coordinator c) Control sequencer d) Program Counter		
26.	The method used to reduce the maximum number of summands by half is _____. a) Fast multiplication **b) Bit-pair recording** c) Quick multiplication d) Carry Save Summand		

27.	The bits 1 & 1 are recorded as _____ in bit-pair recording. a) -1 **b) 0** c) +1 d) both a and b		
28.	The multiplier -6(11010) is recorded as, a) 0-1-2 b) 0-1+1-10 **c) -2-10** d) None of the above		
29.	The numbers written to the power of 10 in the representation of decimal numbers are called as _____. a) Height factors b) Size factors **c) Scale factors** d) Space Factors		
30.	If the decimal point is placed to the right of the first significant digit, then the number is called as _____. a) Orthogonal **b) Normalized** c) Determinate d) Diagonal		
31.	_____ constitute the representation of the floating number. a) Sign **b) Significant digits** c) Scale factor d) All of the above		
32.	The sign followed by the string of digits is called as _____. a) Significant b) Determinant **c) Mantissa** d) Exponent		
33.	) In Booth's algorithm, for Multiplier=1000 and Multiplicand=1100. How many number of cycles are required to get the correct multiplication result? a. 4 **b. 5** c. 3 d. 6		

34.	In Booth's algorithm, for Multiplier=100 and Multiplicand=1100. How many number of cycles are required to get the correct multiplication result? a. 4 b. 5 **c. 3** d. 6		
35.	In IEEE 32-bit representations, the mantissa of the fraction is said to occupy _____ bits. **a) 24** b) 23 c) 20 d) 16		
36.	The normalized representation of 0.0010110 * 2 ^ 9 is a) 0 10001000 0010110 b) 0 10000101 0110 **c) 0 10101010 1110** d) 0 11110100 11100		
37.	The 32 bit representation of the decimal number is called as ____. **a) Double-precision** b) Single-precision c) Extended format d) None of the above		
38.	In 32 bit representation the scale factor as a range of _____. **a) -128 to 127** b) -256 to 255 c) 0 to 255 d) -16 to 15		
39.	In double precision format the size of the mantissa is _____. a) 32 bit b) 52 bit **c) 64 bit** d) 72 bit		
40.	Which of the following is ordinary (average) multiplier in booth recoding multiplication? a. 01010101 b. 00001111 **c. 11001100** d. None of these		

41.	In booth recoding, M is multiplicand and -1 is booth recoded multiplier, then what will be the result of multiplication? a. 1's complement of M **b. 2's complement of M** c. M d. Right shift of M		
42.	In Booth's algorithm, if Q0=0 and Q-1=0 then it will perform which operation, **a. A=A-M** b. A=A+M c. Arithmetic right shift of A, Q and Q-1 d. A=M-A		
43.	In Booth's algorithm, if Q0=1 and Q-1=1 then it will perform which operation, a. A=A-M **b. A=A+M** c. Arithmetic right shift of A, Q and Q-1 d. A=M-A		
44.	In Booth's algorithm, if Q0=1 and Q-1=0 then it will perform which operation, a. A=A-M b. A=A+M **c. Arithmetic right shift of A, Q and Q-1** d. A=M-A		
45.	In Booth's algorithm, if Q0=0 and Q-1=1 then it will perform which operation, a. A=A-M b. A=A+M c. Arithmetic right shift of A, Q and Q-1 **d. A=M-A**		
46.	What version of multiplicand will be selected if consecutive multiplier bits are 00? **a. 0*M** b. +1*M c. -1*M d. 2*M		
47.	What version of multiplicand will be selected if consecutive multiplier bits are 01? a. 0*M **b. +1*M** c. -1*M d. -2*M		

48.	)What version of multiplicand will be selected if consecutive multiplier bits are 10? a. 0*M b. +1*M c. -1*M **d. 0*M**		
49.	Which of the following is good multiplier in booth recoding multiplication? a. 01010101 **b. 00001111** c. 11001100 d. None of these		
50.	Which of the following is worst case multiplier in booth recoding multiplication? **a. 01010101** b. 00001111 c. 11001100 d. None of these		

PART B
2 Marks with answers

S.NO	QUESTION	BLOOMS LEVEL	CLO
1	1. Differentiate between restoring and non-restoring division		
2	**2** Explain the design of a four bits carry look ahead adder circuit		
3	**3** Add +5 and -9 using 2's compliment method		
4	**4** Given Booth's algorithm to multiply two binary numbers, explain the working of the algorithm with an example.		
5	**5** Explain with figure the design of a 4-bit carry look ahead adder		
6	**6** With figure explain circuit arrangements for binary division.		
7	**7** IEEE standard for floating point numbers, explain.		
8	**8** Design 4 bit carry look ahead logic and explain how it is faster them 4 bit ripple adder		

9	**9** Multiply 14 x - 8 using Booth's algorithm		
10	**10** Explain normalization, excess - exponent and special values with respect to IEEE floating point representation		

PART C
12 Marks (Only Question)

S.NO	QUESTION	BLOOMS LEVEL	CLO
1	**1** Discuss in detail Multiplication of positive numbers with Problem Solving		
2	**2** Explain in detail Signed operand multiplication with Problem solving		
3	**3** Explain in detail about Fast multiplication- Bit pair recoding of Multipliers , Problem Solving		
4	**4** Explain in detail about Carry Save Addition of summands, Problem Solving		
5	**5** Discuss in detail about Integer division – Restoring Division with Solving Problems		
6	**6** Explain in detail Non Restoring Division with Solving Problems		
7	**7** Discuss in detail about Floating point numbers and operations with **Solving Problems**		

8	**8** Explain in detail Addition and subtraction of Signed numbers with Problem solving		
9	**9** Discuss in detail about Design of fast adders, Ripple carry adder and Carry look ahead adder		

Unit III

PART-A

Q.No	Question		
1.	The general purpose registers are combined into a block called as _____. **a) Register bank** b) Register Case c) Register file d) None of the above		
2.	In _____ technology, the implementation of the register file is by using an array of memory locations. **a) VLSI** b) ANSI c) ISA d) ASCI		
3.	In a three BUS architecture, how many input and output ports are there ? a) 2 output and 2 input **b) 1 output and 2 input** c) 2 output and 1 input d) 1 output and 1 input		
4.	The main advantage of multiple bus organization over single bus is, a) Reduction in the number of cycles for execution b) Increase in size of the registers **c) Better Connectivity** d) None of these		
5.	CISC stands for, a) Complete Instruction Sequential Compilation b) Computer Integrated Sequential Compiler **c) Complex Instruction Set Computer** d) Complex Instruction Sequential Compilation		
6.	. If the instruction Add R1,R2,R3 is executed in a system which is pipelined, then the value of S is (Where S is term of the Basic performance equation) a) 3 **b) ~2** c) ~1 d) 6		
7.	In multiple BUS organisation _____ is used to select any of the BUSes for input into ALU. **a) MUX** b) DE-MUX c) En-CDS d) None of the above		

8.	_____ are the different type/s of generating control signals. a) Micro-programmed b) Hardwired c) Micro-instruction **d) Both a and b**		
9.	The type of control signal are generated based on, a) contents of the step counter b) Contents of IR c) Contents of condition flags d) All of the above		
10.	What does the hardwired control generator consist of ? a) Decoder/encoder b) Condition codes c) Control step counter d) All of the above		
11.	What does the end instruction do ? **a) It ends the generation of a signal** b) It ends the complete generation process c) It starts a new instruction fetch cycle and resets the counter d) It is used to shift the control to the processor		
12.	What does the RUN signal do ? a) It causes the termination of a signal b) It causes a particular signal to perform its operation **c) It causes a particular signal to end** d) It increments the step counter by one		
13.	The benefit of using hardwired approach is a) It is cost effective b) It is highly efficient **c) It is very reliable** d) It increases the speed of operation		
14.	The disadvantage/s of the hardwired approach is a) It is less flexible b) It cannot be used for complex instructions **c) It is costly** d) Both a and b		
15.	In micro-programmed approach, the signals are generated by _____. **a) Machine instructions** b) System programs c) Utility tools d) None of the above		

16.	A word whose individual bits represent a control signal is _____. a) Command word **b) Control word** c) Co-ordination word d) Generation word		
17.	A sequence of control words corresponding to a control sequence is called _____. **a) Micro routine** b) Micro function c) Micro procedure d) None of the above		
18.	. Individual control words of the micro routine are called as _____. a) Micro task b) Micro operation **c) Micro instruction** d) Micro command		
19.	The special memory used to store the micro routines of a computer is _____. a) Control table **b) Control store** c) Control mart d) Control shop		
20.	To read the control words sequentially _____ is used. a) PC **b) IR** c) UPC d) None of the above		

PART-B

Q.No	Question	Text book	Blooms Taxonomy Level
21.	_____ have been developed specifically for pipelined systems. a) Utility software **b) Speed up utilities** c) Optimizing compilers d) None of the mentioned		
22.	The pipelining process is also called as _____. a) Superscalar operation b) Assembly line operation **c) Von neumann cycle** d) None of the mentioned		

23.	The fetch and execution cycles are interleaved with the help of _____. a) Modification in processor architecture **b) Clock** c) Special unit d) Control unit		
24.	Each stage in pipelining should be completed within ____ cycle. a) 1 b) 2 c) 3 **d) 4**		
25.	If a unit completes its task before the allotted time period, then a) It'll perform some other task in the remaining time b) Its time gets reallocated to different task **c) It'll remain idle for the remaining time** d) None of the mentioned		
26.	To increase the speed of memory access in pipelining, we make use of _____. a) Special memory locations **b) Special purpose registers** c) Cache d) Buffers		
27.	The periods of time when the unit is idle is called as _____. a) Stalls b) Bubbles c) Hazards **d) Both a and b**		
28.	The contention for the usage of a hardware device is called as _____. **a) Structural hazard** b) Stalk c) Deadlock d) None of the mentioned		
29.	Any condition that causes a processor to stall is called as _____. **a) Hazard** b) Page fault c) System error d) None of the above		
30.	The periods of time when the unit is idle is called as _____. **a) Stalls** b) Bubbles c) Hazards **d) Both a and b**		

PART-C

Q.No	Question	Text book	Bloom s Taxon omy Level
31.	**Various Hazards** i) The contention for the usage of a hardware device is called as _____. **a) Structural hazard** b) Stalk c) Deadlock d) None of the above ii) The situation where in the data of operands are not available is called _____. **a) Data hazard** b) Stock c) Deadlock d) Structural hazard iii) The stalling of the processor due to the unavailability of the instructions is called as ____. **a) Control hazard** b) Structural hazard c) Input hazard d) None of the above iv) The time lost due to branch instruction is often referred to as _____. a) Latency b) Delay **c) Branch penalty** d) None of the above		
32.	Algorithm used in Concurrency: i) The algorithm followed in most of the systems to perform out of order execution is _____. **a) Tomasulo algorithm** b) Score carding c) Reader-writer algorithm d) None of the above ii). The problem where process concurrency becomes an issue is called as _____. a) Philosophers problem b) Bakery problem **c) Bankers problem** d) Reader-writer problem		

33.	Bus Structure: i) Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle time of the bus was reduced to 125 nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus? (A) 1 Megabyte/sec (B) 4 Megabytes/sec (C) 8 Megabytes/sec **(D) 2 Megabytes/sec** **ii)** The communication between the components in a microcomputer takes place via the address and (A) I/O bus **(B) Data bus** (C) Address bus (D) Control lines		
34.	**Micro Programmed Control** **i)** A microprogram sequencer **(A) generates the address of next micro instruction to be executed.** (B) generates the control signals to execute a microinstruction. (C) sequentially averages all microinstructions in the control memory. (D) enables the efficient handling of a micro program subroutine. ii) The operation executed on data stored in registers is called (A) Macro-operation **(B) Micro-operation** (C) Bit-operation (D) Byte-operation		
35.	Hard Wired Control i) Hardwired control unit uses ____to interpret an instruction **a) Special Program** b) Special micro c) fixed logic d) instruction register ii) While designing hardwired control unit factor to be considered a) amount of hardware used b) Speed of operation c) cost of design **d) all of the above**		

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FACULTY OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

QUESTION BANK

DEGREE / BRANCH: B Tech/CSE/AIML

III SEMESTER

18CSC203J-COMPUTER ORGANIZATION AND ARCHITECTURE

Regulation–2018

AcademicYear -2021-2022

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

Ramapuram Campus, Bharathi Salai, Ramapuram, Chennai-600089

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

QUESTION BANK

SUBJECT : 18CSC203J-COMPUTER ORGANIZATION AND ARCHITECTURE

SEM/YEAR:III/II

Course Outcomes

CO1: *Identify the computer hardware and how software interacts with computer hardware*
CO2: *Apply Boolean algebra as related to designing computer logic, through simple combinational and sequential logic circuits*
CO3: *Analyze the detailed operation of Basic Processing units and the performance of Pipelining*
CO4: *Analyze concepts of parallelism and multi-core processors*
CO5: *Identify the memory technologies, input-output systems and evaluate the performance of memory system*
CO6: *Identify the computer hardware, software and its interactions*

UNIT IV			
Parallelism- Need, types of Parallelism- applications of Parallelism- Parallelism in Software- Instruction level parallelism- Data level parallelism- Challenges in parallel processing- Architectures of Parallel Systems - Flynn's classification- SISD,SIMD - MIMD, MISD - Hardware multithreading- Coarse Grain parallelism, Fine Grain parallelism - Uni-processor and Multiprocessors- Multi-core processors- Memory in Multiprocessor Systems- Cache Coherency in Multiprocessor Systems- MESI protocol for Multiprocessor Systems.			
PART-A (Multiple Choice Questions)			
Q. No	**Questions**	**Course Outcome**	**Competence BT Level**
1	Identify how the potential parallelism among instructions is exploited _____ a. Pipelining b. Scalability c. Supervision d. Compatibility **Answer:** a. Pipelining	*CO4*	BT1
2	Comparing with pipelining the performance becomes potentially greater since the clock cycle _____ a. increases b. decreases c. stabilizes	*CO4*	BT2

	d. none of the above **Answer:** b. decreases		
3	Find out the processor whose technique is to allow multiple instructions to be issued in every pipeline stage. a. single-issue processors b. dual -issue processors c. multiple- issue processors d. no-issue processor **Answer:** c. multiple- issue processors	*CO4*	BT1
4	Estimate what multiple issue processors try to exploit in a large amount ? a. data level parallelism b. task level parallelism c. bit level parallelism d. instruction level parallelism **Answer:** d. instruction level parallelism	*CO4*	BT4
5	An approach to implement a multiple issue processor where the decisions are made by the compiler before execution is understood as a _____ a. static multiple issue b. dynamic multiple issue c. speculation d. loop delay **Answer:** a. static multiple issue	*CO4*	BT2
6	Parallelism achieved by performing the same operation on independent data is defined as _____ a. data level parallelism b. task level parallelism c. bit level parallelism d. instruction level parallelism **Answer:** a. data level parallelism	*CO4*	BT1
7	Who identified the way of classifying systems with parallel processing capability? a. Alan Turing b. Flynn c. John Von Neumann d. Frederick P. Brooks **Answer:** b. Flynn	*CO4*	BT1
8	Which of the following category does uniprocessors fall under? a. SISD b. SIMD	*CO4*	BT1

	c. MISD d. MIMD **Answer:** a. SISD		
9	In a Symmetric multiprocessor (SMP), the memory access time to any region of memory is validated _____ a. differently for each processor. b. uniquely for each processor. c. approximately same for each processor d. statically for each processor **Answer:** c. approximately same for each processor	*CO4*	BT5
10	The memory access time to different regions of memory may differ for a _____ a. SMP b. NUMA c. Uniprocessor d. Vector processor **Answer:** b. NUMA	*CO4*	BT4
11	MIMD may be identified as _____ a. shared memory multiprocessors b. distributed memory multiprocessors c. both a and b d. either a or b **Answer:** d. either a or b	*CO4*	BT2
12	Hardware multithreading increases utilization of a processor by switching to another thread when _____ a. one thread is running b. one thread is stalled c. multiple threads are running d. multiple threads are stalled **Answer:** b. one thread is stalled	*CO4*	BT2
13	A thread includes _____ a. program counter, register state and stack b. only program counter and register states c. only register , states and stack d. only program counter and stack **Answer:** a. program counter, register state and stack	*CO4*	BT1
14	What does a process switch usually invoke? a. operating system and the thread switch b. operating system or the thread switch c. operating system but not the thread switch	*CO4*	BT2

	d. operating system and functional unit **Answer:** c. operating system but not the thread switch		
15	Determine what the processor must be able to do, to make fine grained multithreading practical. a. stall threads on every clock cycle b. switch threads on every cache miss c. stall threads on every cache miss d. switch threads on every clock cycle **Answer:** d. switch threads on every clock cycle	*CO4*	BT3
16	Identify of the following is an advantage of fine-grained multithreading? a. it can increase the throughput b. it can hide the throughput losses that arise from short and long stalls c. it can reduce the throughput losses that arise from short and long stalls d. all of the above **Answer:** b. it can hide the throughput losses that arise from short and long stalls	*CO4*	BT1
17	Choose the primary disadvantage of fine-grained multithreading. a. it slows down the execution of multiple threads b. it speeds up the execution of individual threads c. it slows down the execution of individual threads d. it speeds up the execution of multiple threads **Answer:** c. it slows down the execution of individual threads	*CO4*	BT3
18	Coarse-grained multithreading approach switches threads only on costly stalls such as_____ a. last-level cache hits b. capacity misses c. conflict misses d. last-level cache misses **Answer:** d. last-level cache misses	*CO4*	BT1
19	When a processor with coarse-grained multithreading issues instructions from a single thread and a stall occurs, the pipeline must be _____ a. emptied b. frozen c. either a or b d. both a and b **Answer:** c. either a or b	*CO4*	BT1
20	What is coarse-grained multithreading more useful for? a. reducing the throughput losses	*CO4*	BT1

	b. reducing the penalty of high-cost stall c. reducing the penalty of low-cost stall d. all of the above **Answer:** b. reducing the penalty of high-cost stall		
21	Simultaneous multithreading (SMT) is a variation on hardware multithreading that uses resources of multiple issue and dynamically scheduled pipelined processor to exploit_____ a. thread-level parallelism b. instruction- level parallelism c. either a or b d. both a and b **Answer:** d. both a and b	*CO4*	BT1
22	Simultaneous multithreading helps to determine _____ a. lower the cost of multithreading b. decreases processor utilization c. manage the cache misses d. none of the above **Answer:** a. lower the cost of multithreading	*CO4*	BT3
23	In the superscalar without hardware multithreading support, the use of issue slots is limited by a lack of _____ a. thread-level parallelism b. instruction- level parallelism c. either a or b d. both a and b **Answer:** b. instruction- level parallelism	*CO4*	BT2
24	What type of major stall can leave the entire processor idle, in the superscalar working without the hardware multithreading support? a. instruction cache miss b. instruction cache hit c. both a and b d. either a or b **Answer:** a. instruction cache miss	*CO4*	BT4
25	What is the collection of independent uniprocessors interconnected together identified as? a. instruction stream b. control unit c. cluster d. NUMA **Answer:** c. cluster	*CO4*	BT1
26	Identify which system is responsible for execution of active processes	*CO4*	BT1

	and allocating resources in both SMP and uniprocessor cases? a. information system b. database system c. knowledge-based system d. operating system **Answer:** d. operating system		
27	Validate how all the processors share accesses to I/O devices in SMP. a. through same channel b. through different channel c. either a or b d. both a and b **Answer:** c. either a and b	*CO4*	BT5
28	Choose which of the following can be considered as an advantage of SMP over uniprocessor? a. availability b. reliability c. maintainability d. serviceability **Answer:** a. availability	*CO4*	BT3
29	Find out the main drawback for bus organization? a. simplicity b. reliability c. performance d. flexibility **Answer:** c. performance	*CO4*	BT1
30	Choose which of the following is disadvantage of multiprocessor systems? a. multiprocessor system is quite expensive b. all the processors in the multiprocessor system share the memory. c. an integrated operating system is required in multiprocessor systems. d. all of the above **Answer:** d. all of the above	*CO4*	BT3
31	Determine which is used to improve performance and reduce the number of bus accesses when equipped with each processor. a. DMA controller b. cache memory c. clocks d. none of the above **Answer:** b. cache memory	*CO4*	BT3
32	Relate to a problem that will occur when a word is altered in one cache	*CO4*	BT2

	and it could conceivably invalidate a word in another cache. a. cache miss b. cache hit c. cache coherence d. stall **Answer:** c. cache coherence		
33	What is defined as the process of coordinating the behavior of two or more processes which may be running on different processors. a. synchronization b. memory management c. fault tolerance d. simultaneous concurrent processing **Answer:** a. synchronization	*CO4*	BT1
34	Choose which of the following offers the programmer a single physical address space across all processes. a. distributed memory multiprocessor b. shared memory multiprocessor c. homogeneous multiprocessor system d. heterogeneous multiprocessor system **Answer:** b. shared memory multiprocessor	*CO4*	BT3
35	A multiprocessor in which the latency to a word in memory does not depend on which processor requests the access is termed as_____ a. distributed memory access b. non uniform memory access c. uniform memory access d. none of the above **Answer:** c. uniform memory access	*CO4*	BT1
36	Which of the following challenges does NUMA machines support when compared to UMA? a. ability for scaling to larger sizes. b. lower latency to nearby memory. c. either a or b d. both a and b **Answer:** d. both a and b	*CO4*	BT2
37	A _____ is a synchronization device that allows access to data to only one processor at a time. a. lock b. power cable c. coprocessor d. none of the above **Answer:** a. lock	*CO4*	BT1

38	_____ defines what values can be returned by a read. a. consistency b. coherence c. reliability d. latency **Answer:** b. coherence	*CO4*	BT1
39	_____ determines when a written value will be returned by a read. a. reliability b. coherence c. consistency d. latency **Answer:** c. consistency	*CO4*	BT3
40	The approach to ensure that all writes to the same location are seen in the same order is termed as _____ a. synchronization b. cache coherence c. latency d. write serialization **Answer:** d. write serialization	*CO4*	BT1
41	Select which schemes are provided by the cache coherent multiprocessor on shared data items? a. migration b. replication c. both a and b d. either a or b **Answer:** c. both a and b	*CO4*	BT1
42	When a data item can be moved to a local cache and used there in a transparent fashion it is termed as _____ a. migration b. replication c. synchronization d. serialization **Answer:** a. migration	*CO4*	BT1
43	In a cache coherent multiprocessor, migration helps to reduce_____ a. latency b. bandwidth c. both a and b d. either a or b **Answer:** c. both a and b	*CO4*	BT4

44	When a private data is cached, its location is migrated to the cache and it helps in _____ a. increasing the average access time as well as the memory bandwidth required b. reducing the average access time as well as the memory bandwidth not required c. reducing the average access time as well as the memory bandwidth required d. increasing the average access time as well as the memory bandwidth not required **Answer:** c. reducing the average access time as well as the memory bandwidth required	*CO4*	BT4
45	SISD means _____ a. Single Information Single Design b. Single Instruction Single Data c. Single Instruction Single Design d. Single Information Single Document **Answer:** b. Single Instruction Single Data	*CO4*	BT1
46	One of the protocols under the snooping method which is used to enforce coherence by ensuring that a processor has exclusive access to a data item before it writes the item is referred as_____ a. write update protocol b. directory protocol c. write invalidate protocol d. write broadcast protocol **Answer:** c. write invalidate protocol	*CO4*	BT1
47	Select which protocol under the snoopy approach enables multiple writers as well as multiple readers? a. write update protocol b. directory protocol c. write invalidate protocol d. none of the above **Answer:** a. write update protocol	*CO4*	BT3
48	Determine what lead to the development of MESI protocol? a. cache size b. cache coherency c. bus snooping d. number of caches **Answer:** b. cache coherency	*CO4*	BT3
49	What does MESI stand for? a. modified exclusive state invalid b. modified exclusive shared invalid	*CO4*	BT1

	c. modified exclusive system input d. modified embedded shared invalid **Answer:** b. modified exclusive shared invalid		
50	Alternative way of a snooping-based coherence protocol, is defined as _____ a. write invalidate protocol b. directory protocol c. write update protocol d. write broadcast protocol **Answer:** b. directory protocol	*CO4*	BT1
	PART B (4 Marks)		
1	Define instruction level parallelism. Instruction-level parallelism (ILP) is a measure of how many of the operations in a computer program can be performed simultaneously. The potential overlap among instructions is called instruction level parallelism.	CO4	BT1
2	List the limitations in instruction level parallelism: 1.True data dependency; 2. Procedural dependency; 3. Resource conflicts; 4. Output dependency; 5. Antidependency.	CO4	BT2
3	Outline the categories of computer systems under Flynn. Single instruction, single data (SISD) stream Single instruction, multiple data (SIMD) stream: Multiple instruction, single data (MISD) stream: Multiple instruction, multiple data (MIMD) stream	CO4	BT1
4	Quote the functions of SMID. A single machine instruction controls the simultaneous execution of a number of processing elements on a lockstep basis. Each processing element has an associated data memory, so that instructions are executed on different sets of data by different processors.	CO4	BT1
5	Highlight aboout a Multicore processor. A multicore processor, also known as a chip multiprocessor, combines two or more processor units (called cores) on a single piece of silicon (called a die).	CO4	BT1
6	What is Cache Coherence? When multiple caches exist, there is a need for a cache-Coherence scheme to avoid access to invalid data. Cache coherency may be addressed with software-based techniques. In the case where the cache contains stale data, the cached copy may be invalidated and reread from memory when needed again.	CO4	BT1

7	Define Coarse-grained multithreading. A version of hardware multithreading that implies switching between threads only after significant events, such as a last-level cache miss.	CO4	BT1
8	Paraphrase on MESI? To provide cache consistency on an SMP, the data cache often supports a protocol known as MESI(modified/exclusive/shared/invalid)	CO4	BT2
9	What is Fine Grained Multithreading? switches between threads on each instruction, resulting in interleaved execution of multiple threads.	CO4	BT1
10	Express what is Data-level parallelism? Data-level parallelism specifically subword parallelism, offers a simple path to higher performance for programs that are intensive in arithmetic operations for either integer or floating-point data.	CO4	BT2
PART C (12 Marks)			
1	Illustrate with neat sketches about Instruction level and Data level parallelism.	CO4	BT4
2	Discuss in detail about Flynn's Classification.	CO4	BT4
3	Elaborate about Hardware Multithreading	CO4	BT4
4	Articulate the key features of the MESI protocol.	CO4	BT3
5	Compare and contrast Uniprocessor and Multiprocessor system and explain them in detail	CO4	BT2
6.	Highlight about the Hardware performance issues that led to the development of multicore computers	CO4	BT4
7.	Compare and contrast about SISD,SIMD,MIMD,MISD	CO4	BT2
8.	Summarize in detail about Cache Coherence.	CO4	BT4
9.	Compare Coarse grained and Fine grained Multithreading and explain them in detail.	CO4	BT2
10.	Discuss about MESI protocol for Multiprocessor Systems	CO4	BT4

Note:

1. **BT Level –** Blooms Taxonomy Level
2. **CO – Course Outcomes**

BT1 –Remember BT2 – Understand BT3 – Apply BT4 – Analyze BT5 – Evaluate BT6 – Create

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FACULTY OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF
COMPUTER SCIENCE AND ENGINEERING

RAMAPURAM

SRM
INSTITUTE OF SCIENCE & TECHNOLOGY
(Deemed to be University u/s 3 of UGC Act, 1956)

QUESTION BANK

DEGREE / BRANCH: B Tech/CSE and all specializations

(AIML, BDA, IOT, CS)

III SEMESTER
18CSC203J-COMPUTER ORGANIZATION AND ARCHITECTURE

Regulation–2018

Academic Year -2021-2022

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

Ramapuram Campus, Bharathi Salai, Ramapuram, Chennai-600089

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

QUESTION BANK

SUBJECT CODE : 18CSC203J

SUBJECT NAME : COMPUTER ORGANIZATION AND ARCHITECTURE

SEM/YEAR:III/II

Course Outcomes

CO1: *Identify the computer hardware and how software interacts with computer hardware*

CO2: *Apply Boolean algebra as related to designing computer logic, through simple combinational and sequential logic circuits*

CO3: *Analyze the detailed operation of Basic Processing units and the performance of Pipelining*

CO4: *Analyze concepts of parallelism and multi-core processors*

CO5: *Identify the memory technologies, input-output systems and evaluate the performance of memory system*

CO6: *Identify the computer hardware, software and its interactions*

UNIT V			
Memory systems -Basic Concepts, Memory hierarchy- Memory technologies, RAM, Semiconductor RAM-ROM,Types, Speed,size cost- Cache memory, Mapping Functions- Replacement Algorithms, Problem Solving-Virtual Memory, Performance considerations of various memories- Input Output Organization, Need for Input output devices- Memory mapped IO, Program controlled IO- Interrupts-Hardware, Enabling and Disabling Interrupts, Handling multiple Devices			
PART-A (Multiple Choice Questions)			
Q. No	**Questions**	**Course Outcome**	**Competence BT Level**

1	Which of the following is the smallest entity of memory? (a) Block **(b) Cell** (c) Instance (d) Set	CO5	BT2
2	The primary memory (also called main memory) of a personal computer consists of (a) RAM only (b) ROM only **(c) both RAM and ROM** (d) Cache memory	CO5	BT1
3	The Boot sector files of the system are stored in which computer memory? (a) RAM **(b) ROM** (c) Cache (d) Register	CO5	BT2
4	Which of the following statements are not correct about the main memory of a computer? (a) In main memory, data gets lost when power is switched off. (b) Main memory is faster than secondary memory but slower than registers. (c) They are made up of semiconductors. **(d) SRAM is used in Main memory**	CO5	BT2

5	What is the full form of RAM? (a) Read Access Memory **(b) Random Access Memory** (c) Readable Access Memory (d) Random Accumulator Memory	CO5	BT1
6	RAM is _ _ _ _ _ _ and _ _ _ _ _. **(a) volatile, temporary** (b) non-volatile, temporary (c) volatile, permanent (d) non-volatile, permanent	CO5	BT3
7	Which of the following memory is non-volatile? (a) RAM **(b) ROM** (c) Cache (d) ROM and Cache	CO5	BT2
8	Which of the following is the lowest in the computer memory hierarchy? (a) Cache (b) RAM **(c) Secondary memory** (d) CPU registers	CO5	BT2
9	Which of the following has the fastest speed in the computer memory hierarchy? (a) Cache **(b) Register in CPU**	CO5	BT1

	(c) Main memory (d) Disk cache		
10	Which memory acts as a buffer between CPU and main memory? (a) RAM (b) ROM **(c) Cache** (d) Storage	CO5	BT2
11	Which of the following statements are not correct about cache memory? (a) Cache memory is used to store data temporarily. (b) It holds that data and program which has to be executed within a short period of time. **(c) It needs frequent refreshing** (d) It consumes less access time as compared to the Main memory	CO5	BT2
12	In which type of ROM, data can be erased by ultraviolet light and then reprogrammed by the user or manufacturer? (a) PROM (b) **EPROM** (c) EEPROM (d) Both a and b	CO5	BT1
13	Primary storage is . . . . . as compared to secondary storage. (a) Slow and inexpensive (b) Fast and inexpensive	CO5	BT2

	(c) Fast and expensive (d) Slow and expensive		
14	Which of the following statements is not true about secondary memory (auxiliary memory)? (a) Secondary memory is non-volatile in nature and slower than primary memories. **(b) It is a faster memory device** (c) Data is permanently stored even if power is switched off. (d) Computers may run without secondary memory. (e) It is also known as backup memory.	CO5	BT2
15	Virtual memory is an (a) Extremely large memory (b) Extremely large secondary memory **(c) Illusion of an extremely large memory** (d) A type of memory used in supercomputers.	CO5	BT2
16	Whenever the data is not found in the cache memory it is called as _____ a) HIT **b) MISS** c) FOUND d) ERROR	CO5	BT2
17	When the data at a location in cache is different from the data located in the main memory, the cache is called _____ a) Unique **b) Inconsistent** c) Variable	CO5	BT2

	d) Fault		
18	Which of the following is not a write policy to avoid Cache Coherence? a) Write through **b) Write within** c) Write back d) Buffered write	CO5	BT2
19	In _____ mapping, the data can be mapped anywhere in the Cache Memory. **a) Associative** b) Direct c) Set Associative d) Indirect	CO5	BT2
20	The transfer between CPU and Cache is _____ a) Block transfer **b) Word transfer** c) Set transfer d) Associative transfer	CO5	BT2
21	LRU stands for _____ a) Low Rate Usage b) Least Rate Usage **c) Least Recently Used** d) Low Required Usage	CO5	BT1
22	The binary address issued to data or instructions are called as _____ a) Physical address b) Location	CO5	BT1

	c) Relocatable address **d) Logical address**		
23	Which of the following is not the main aim of virtual memory organization? a) To provide effective memory access **b) To provide permanent backup** c) To improve the execution of the program d) To provide better memory transfer	CO5	BT1
24	TLB is a _____ a) Permanent memory b) Larger memory **c) Small cache** d) Interface used for I/O devices	CO5	BT1
25	Which of the following is used for detecting and correcting errors? a) ACC b) BCC **c) ECC** d) TLB	CO5	BT1
26	In a 3.5 inch(diameter) capacity magnetic disk, There are an average of _____sectors per track a) 200 b) 300 **c) 400** d) 500	CO5	BT2
27	Which of the following is the time required to move the read/write head to the proper track? a) Track time b) Fetch time **c) Seek time** d) Disk time	CO5	BT1
28	ROM stores a small _____ program that can read and write main memory locations	CO5	BT1

	a) monitor b) snooping c) writer d) sub-routine		
29	In memory design, an approach to implement a narrow bus that is much faster is _____ **a) Rambus** b) internal bus c) Memory bus d) multi bus	CO5	BT1
30	After the completion of the DMA transfer, the processor is notified by _____ a) Acknowledge signal **b) Interrupt signa**l c) WMFC signal d) None of the mentioned	CO5	BT1
31	How is a privilege exception dealt with? **a) The program is halted and the system switches into supervisor mode and restarts the program execution** b) The Program is stopped and removed from the queue c) The system switches the mode and starts the execution of a new process d) The system switches mode and runs the debugger	CO5	BT1
32	The instructions which can be run only supervisor mode are? a) Non-privileged instructions b) System instructions **c) Privileged instructions** d) Exception instructions	CO5	BT2
33	The two facilities provided by the debugger is _____ a) Trace points b) Break points c) Compile **d) Both Trace and Break points**	CO5	BT2
34	If during the execution of an instruction an exception is raised then _____	CO5	BT2

	a) The instruction is executed and the exception is handled **b) The instruction is halted and the exception is handled** c) The processor completes the execution and saves the data and then handle the exception d) None of the mentioned		
35	Interrupts initiated by an instruction is called as _____ a) Internal **b) External** c) Hardware d) Software	CO5	BT2
36	In memory-mapped I/O _____ **a) The I/O devices and the memory share the same address space** b) The I/O devices have a separate address space c) The memory and I/O devices have an associated address space d) A part of the memory is specifically set aside for the I/O operation	CO5	BT3
37	The advantage of I/O mapped devices to memory mapped is _____ a) The former offers faster transfer of data b) The devices connected using I/O mapping have a bigger buffer space **c) The devices have to deal with fewer address lines** d) No advantage as such	CO5	BT2
38	The system is notified of a read or write operation by _____ a) Appending an extra bit of the address b) Enabling the read or write bits of the devices c) Raising an appropriate interrupt signal **d) Sending a special signal along the BUS**	CO5	BT2
39	To overcome the lag in the operating speeds of the I/O device and the processor we use _____ a) Buffer spaces **b) Status flags** c) Interrupt signals d) Exceptions	CO5	BT1
40	The method which offers higher speeds of I/O transfers is _____ a) Interrupts b) Memory mapping	CO5	BT2

	c) Program-controlled I/O **d) DMA**		
41	The method of synchronizing the processor with the I/O device in which the device sends a signal when it is ready is? a) Exceptions b) Signal handling **c) Interrupts** d) DMA	CO5	BT2
42	The process wherein the processor constantly checks the status flags is called as _____ **a) Polling** b) Inspection c) Reviewing d) Echoing	CO5	BT2
43	How can the processor ignore other interrupts when it is servicing one _____ a) By turning off the interrupt request line b) By disabling the devices from sending the interrupts c) BY using edge-triggered request lines **d) All of the mentioned**	CO5	BT1
44	CPU as two modes privileged and non-privileged. In order to change the mode from privileged to non-privileged. a) A hardware interrupt is needed **b) A software interrupt is needed** c) Either hardware or software interrupt is needed d) A non-privileged instruction (which does not generate an interrupt)is needed	CO5	BT2
45	An interrupt that can be temporarily ignored is _____ a) Vectored interrupt b) Non-maskable interrupt **c) Maskable interrupt** d) High priority interrupt	CO5	BT1
46	The time between the receiver of an interrupt and its service is _____ a) Interrupt delay **b) Interrupt latency**	CO5	BT2

	c) Cycle time d) Switching time		
47	When the process is returned after an interrupt service _____ should be loaded again. i) Register contents ii) Condition codes iii) Stack contents iv) Return addresses a) i, iv b) ii, iii and iv c) iii, iv **d) i, ii**	CO5	BT2
48	The signal sent to the device from the processor to the device after receiving an interrupt is _____ **a) Interrupt-acknowledge** b) Return signal c) Service signal d) Permission signal	CO5	BT2
49	The return address from the interrupt-service routine is stored on the _____. a) System heap b) Processor register **c) Processor stack** d) Memory	CO5	BT1
50	The interrupt-request line is a part of the _____. a) Data line **b) Control line** c) Address line d) None of the mentioned	CO5	BT2
	PART B (4 Marks)		
1	Write on address spaces in I/o Devices with a neat diagram.	CO5	BT1
2	Treatment of an interrupt-service routine is very similar to that of a subroutine –Justify the above statement	CO5	BT3

3	Does Saving and restoring registers involve memory transfers? Is the statement true or false .explain in brief your answer?	CO5	BT2
4	What are the steps to be done to reduce interrupt latency?	CO5	BT2
5	Write short notes Delay, latency and interrupt latency.	CO5	BT2
6	Define hardware interrupt.	CO5	BT1
7	Draw a diagram for enabling and disabling of interrupts?	CO5	BT2
8	Explain on privilege exception?	CO5	BT2
9	Explain about speed size cost?	CO5	BT2
PART C (12 Marks)			
1	Write on privilege exception and draw a diagram to justify your answer and explain it.	CO5	BT2
2	Difference between handling I/O interrupt-request and handling exceptions due to errors and brief on it.	CO5	BT2
3	Discuss in detail about the Control unit which performs these transfers is a part of the I/O devices**.**	CO5	BT2
4	Draw and explain DMA bus attribution .Converse on your answer with your own example	CO5	BT3
5	Draw a diagram with master and slave for your synchronous bus and describe on it**.**	CO5	BT3