SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

Ramapuram Campus, Bharathi Salai, Ramapuram, Chennai - 600089

FACULTY OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

QUESTION BANK

DEGREE / BRANCH: B Tech/CSE/AIML

III SEMESTER

18CSC203J-COMPUTER ORGANIZATION AND ARCHITECTURE

Regulation–2018

AcademicYear -2021-2022

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

Ramapuram Campus, Bharathi Salai, Ramapuram, Chennai-600089

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

QUESTION BANK

SUBJECT : 18CSC203J-COMPUTER ORGANIZATION AND ARCHITECTURE

SEM/YEAR:III/II

Course Outcomes

CO1: *Identify the computer hardware and how software interacts with computer hardware*
CO2: *Apply Boolean algebra as related to designing computer logic, through simple combinational and sequential logic circuits*
CO3: *Analyze the detailed operation of Basic Processing units and the performance of Pipelining*
CO4: *Analyze concepts of parallelism and multi-core processors*
CO5: *Identify the memory technologies, input-output systems and evaluate the performance of memory system*
CO6: *Identify the computer hardware, software and its interactions*

UNIT IV			
Parallelism- Need, types of Parallelism- applications of Parallelism- Parallelism in Software- Instruction level parallelism- Data level parallelism- Challenges in parallel processing- Architectures of Parallel Systems - Flynn's classification- SISD,SIMD - MIMD, MISD - Hardware multithreading- Coarse Grain parallelism, Fine Grain parallelism - Uni-processor and Multiprocessors- Multi-core processors- Memory in Multiprocessor Systems- Cache Coherency in Multiprocessor Systems- MESI protocol for Multiprocessor Systems.			
PART-A (Multiple Choice Questions)			
Q. No	**Questions**	**Course Outcome**	**Competence BT Level**
1	Identify how the potential parallelism among instructions is exploited _____ a. Pipelining b. Scalability c. Supervision d. Compatibility **Answer:** a. Pipelining	*CO4*	BT1
2	Comparing with pipelining the performance becomes potentially greater since the clock cycle _____ a. increases b. decreases c. stabilizes	*CO4*	BT2

	d. none of the above **Answer:** b. decreases		
3	Find out the processor whose technique is to allow multiple instructions to be issued in every pipeline stage. a. single-issue processors b. dual -issue processors c. multiple- issue processors d. no-issue processor **Answer:** c. multiple- issue processors	*CO4*	BT1
4	Estimate what multiple issue processors try to exploit in a large amount ? a. data level parallelism b. task level parallelism c. bit level parallelism d. instruction level parallelism **Answer:** d. instruction level parallelism	*CO4*	BT4
5	An approach to implement a multiple issue processor where the decisions are made by the compiler before execution is understood as a _____ a. static multiple issue b. dynamic multiple issue c. speculation d. loop delay **Answer:** a. static multiple issue	*CO4*	BT2
6	Parallelism achieved by performing the same operation on independent data is defined as _____ a. data level parallelism b. task level parallelism c. bit level parallelism d. instruction level parallelism **Answer:** a. data level parallelism	*CO4*	BT1
7	Who identified the way of classifying systems with parallel processing capability? a. Alan Turing b. Flynn c. John Von Neumann d. Frederick P. Brooks **Answer:** b. Flynn	*CO4*	BT1
8	Which of the following category does uniprocessors fall under? a. SISD b. SIMD	*CO4*	BT1

	c. MISD d. MIMD **Answer:** a. SISD		
9	In a Symmetric multiprocessor (SMP), the memory access time to any region of memory is validated _____ a. differently for each processor. b. uniquely for each processor. c. approximately same for each processor d. statically for each processor **Answer:** c. approximately same for each processor	*CO4*	BT5
10	The memory access time to different regions of memory may differ for a _____ a. SMP b. NUMA c. Uniprocessor d. Vector processor **Answer:** b. NUMA	*CO4*	BT4
11	MIMD may be identified as _____ a. shared memory multiprocessors b. distributed memory multiprocessors c. both a and b d. either a or b **Answer:** d. either a or b	*CO4*	BT2
12	Hardware multithreading increases utilization of a processor by switching to another thread when _____ a. one thread is running b. one thread is stalled c. multiple threads are running d. multiple threads are stalled **Answer:** b. one thread is stalled	*CO4*	BT2
13	A thread includes _____ a. program counter, register state and stack b. only program counter and register states c. only register , states and stack d. only program counter and stack **Answer:** a. program counter, register state and stack	*CO4*	BT1
14	What does a process switch usually invoke? a. operating system and the thread switch b. operating system or the thread switch c. operating system but not the thread switch	*CO4*	BT2

	d. operating system and functional unit **Answer:** c. operating system but not the thread switch		
15	Determine what the processor must be able to do, to make fine grained multithreading practical. a. stall threads on every clock cycle b. switch threads on every cache miss c. stall threads on every cache miss d. switch threads on every clock cycle **Answer:** d. switch threads on every clock cycle	*CO4*	BT3
16	Identify of the following is an advantage of fine-grained multithreading? a. it can increase the throughput b. it can hide the throughput losses that arise from short and long stalls c. it can reduce the throughput losses that arise from short and long stalls d. all of the above **Answer:** b. it can hide the throughput losses that arise from short and long stalls	*CO4*	BT1
17	Choose the primary disadvantage of fine-grained multithreading. a. it slows down the execution of multiple threads b. it speeds up the execution of individual threads c. it slows down the execution of individual threads d. it speeds up the execution of multiple threads **Answer:** c. it slows down the execution of individual threads	*CO4*	BT3
18	Coarse-grained multithreading approach switches threads only on costly stalls such as_____ a. last-level cache hits b. capacity misses c. conflict misses d. last-level cache misses **Answer:** d. last-level cache misses	*CO4*	BT1
19	When a processor with coarse-grained multithreading issues instructions from a single thread and a stall occurs, the pipeline must be _____ a. emptied b. frozen c. either a or b d. both a and b **Answer:** c. either a or b	*CO4*	BT1
20	What is coarse-grained multithreading more useful for? a. reducing the throughput losses	*CO4*	BT1

	b. reducing the penalty of high-cost stall c. reducing the penalty of low-cost stall d. all of the above **Answer:** b. reducing the penalty of high-cost stall		
21	Simultaneous multithreading (SMT) is a variation on hardware multithreading that uses resources of multiple issue and dynamically scheduled pipelined processor to exploit_____ a. thread-level parallelism b. instruction- level parallelism c. either a or b d. both a and b **Answer:** d. both a and b	*CO4*	BT1
22	Simultaneous multithreading helps to determine _____ a. lower the cost of multithreading b. decreases processor utilization c. manage the cache misses d. none of the above **Answer:** a. lower the cost of multithreading	*CO4*	BT3
23	In the superscalar without hardware multithreading support, the use of issue slots is limited by a lack of _____ a. thread-level parallelism b. instruction- level parallelism c. either a or b d. both a and b **Answer:** b. instruction- level parallelism	*CO4*	BT2
24	What type of major stall can leave the entire processor idle, in the superscalar working without the hardware multithreading support? a. instruction cache miss b. instruction cache hit c. both a and b d. either a or b **Answer:** a. instruction cache miss	*CO4*	BT4
25	What is the collection of independent uniprocessors interconnected together identified as? a. instruction stream b. control unit c. cluster d. NUMA **Answer:** c. cluster	*CO4*	BT1
26	Identify which system is responsible for execution of active processes	*CO4*	BT1

	and allocating resources in both SMP and uniprocessor cases? a. information system b. database system c. knowledge-based system d. operating system **Answer:** d. operating system		
27	Validate how all the processors share accesses to I/O devices in SMP. a. through same channel b. through different channel c. either a or b d. both a and b **Answer:** c. either a and b	*CO4*	BT5
28	Choose which of the following can be considered as an advantage of SMP over uniprocessor? a. availability b. reliability c. maintainability d. serviceability **Answer:** a. availability	*CO4*	BT3
29	Find out the main drawback for bus organization? a. simplicity b. reliability c. performance d. flexibility **Answer:** c. performance	*CO4*	BT1
30	Choose which of the following is disadvantage of multiprocessor systems? a. multiprocessor system is quite expensive b. all the processors in the multiprocessor system share the memory. c. an integrated operating system is required in multiprocessor systems. d. all of the above **Answer:** d. all of the above	*CO4*	BT3
31	Determine which is used to improve performance and reduce the number of bus accesses when equipped with each processor. a. DMA controller b. cache memory c. clocks d. none of the above **Answer:** b. cache memory	*CO4*	BT3
32	Relate to a problem that will occur when a word is altered in one cache	*CO4*	BT2

	and it could conceivably invalidate a word in another cache. a. cache miss b. cache hit c. cache coherence d. stall **Answer:** c. cache coherence		
33	What is defined as the process of coordinating the behavior of two or more processes which may be running on different processors. a. synchronization b. memory management c. fault tolerance d. simultaneous concurrent processing **Answer:** a. synchronization	*CO4*	BT1
34	Choose which of the following offers the programmer a single physical address space across all processes. a. distributed memory multiprocessor b. shared memory multiprocessor c. homogeneous multiprocessor system d. heterogeneous multiprocessor system **Answer:** b. shared memory multiprocessor	*CO4*	BT3
35	A multiprocessor in which the latency to a word in memory does not depend on which processor requests the access is termed as_____ a. distributed memory access b. non uniform memory access c. uniform memory access d. none of the above **Answer:** c. uniform memory access	*CO4*	BT1
36	Which of the following challenges does NUMA machines support when compared to UMA? a. ability for scaling to larger sizes. b. lower latency to nearby memory. c. either a or b d. both a and b **Answer:** d. both a and b	*CO4*	BT2
37	A _____ is a synchronization device that allows access to data to only one processor at a time. a. lock b. power cable c. coprocessor d. none of the above **Answer:** a. lock	*CO4*	BT1

38	_____ defines what values can be returned by a read. a. consistency b. coherence c. reliability d. latency **Answer:** b. coherence	*CO4*	BT1
39	_____ determines when a written value will be returned by a read. a. reliability b. coherence c. consistency d. latency **Answer:** c. consistency	*CO4*	BT3
40	The approach to ensure that all writes to the same location are seen in the same order is termed as _____ a. synchronization b. cache coherence c. latency d. write serialization **Answer:** d. write serialization	*CO4*	BT1
41	Select which schemes are provided by the cache coherent multiprocessor on shared data items? a. migration b. replication c. both a and b d. either a or b **Answer:** c. both a and b	*CO4*	BT1
42	When a data item can be moved to a local cache and used there in a transparent fashion it is termed as _____ a. migration b. replication c. synchronization d. serialization **Answer:** a. migration	*CO4*	BT1
43	In a cache coherent multiprocessor, migration helps to reduce_____ a. latency b. bandwidth c. both a and b d. either a or b **Answer:** c. both a and b	*CO4*	BT4

44	When a private data is cached, its location is migrated to the cache and it helps in _____ a. increasing the average access time as well as the memory bandwidth required b. reducing the average access time as well as the memory bandwidth not required c. reducing the average access time as well as the memory bandwidth required d. increasing the average access time as well as the memory bandwidth not required **Answer:** c. reducing the average access time as well as the memory bandwidth required	*CO4*	BT4
45	SISD means _____ a. Single Information Single Design b. Single Instruction Single Data c. Single Instruction Single Design d. Single Information Single Document **Answer:** b. Single Instruction Single Data	*CO4*	BT1
46	One of the protocols under the snooping method which is used to enforce coherence by ensuring that a processor has exclusive access to a data item before it writes the item is referred as_____ a. write update protocol b. directory protocol c. write invalidate protocol d. write broadcast protocol **Answer:** c. write invalidate protocol	*CO4*	BT1
47	Select which protocol under the snoopy approach enables multiple writers as well as multiple readers? a. write update protocol b. directory protocol c. write invalidate protocol d. none of the above **Answer:** a. write update protocol	*CO4*	BT3
48	Determine what lead to the development of MESI protocol? a. cache size b. cache coherency c. bus snooping d. number of caches **Answer:** b. cache coherency	*CO4*	BT3
49	What does MESI stand for? a. modified exclusive state invalid b. modified exclusive shared invalid	*CO4*	BT1

	c. modified exclusive system input d. modified embedded shared invalid **Answer:** b. modified exclusive shared invalid		
50	Alternative way of a snooping-based coherence protocol, is defined as _____ a. write invalidate protocol b. directory protocol c. write update protocol d. write broadcast protocol **Answer:** b. directory protocol	*CO4*	BT1
	PART B (4 Marks)		
1	Define instruction level parallelism. Instruction-level parallelism (ILP) is a measure of how many of the operations in a computer program can be performed simultaneously. The potential overlap among instructions is called instruction level parallelism.	CO4	BT1
2	List the limitations in instruction level parallelism: 1.True data dependency; 2. Procedural dependency; 3. Resource conflicts; 4. Output dependency; 5. Antidependency.	CO4	BT2
3	Outline the categories of computer systems under Flynn. Single instruction, single data (SISD) stream Single instruction, multiple data (SIMD) stream: Multiple instruction, single data (MISD) stream: Multiple instruction, multiple data (MIMD) stream	CO4	BT1
4	Quote the functions of SMID. A single machine instruction controls the simultaneous execution of a number of processing elements on a lockstep basis. Each processing element has an associated data memory, so that instructions are executed on different sets of data by different processors.	CO4	BT1
5	Highlight aboout a Multicore processor. A multicore processor, also known as a chip multiprocessor, combines two or more processor units (called cores) on a single piece of silicon (called a die).	CO4	BT1
6	What is Cache Coherence? When multiple caches exist, there is a need for a cache-Coherence scheme to avoid access to invalid data. Cache coherency may be addressed with software-based techniques. In the case where the cache contains stale data, the cached copy may be invalidated and reread from memory when needed again.	CO4	BT1

7	Define Coarse-grained multithreading. A version of hardware multithreading that implies switching between threads only after significant events, such as a last-level cache miss.	CO4	BT1
8	Paraphrase on MESI? To provide cache consistency on an SMP, the data cache often supports a protocol known as MESI(modified/exclusive/shared/invalid)	CO4	BT2
9	What is Fine Grained Multithreading? switches between threads on each instruction, resulting in interleaved execution of multiple threads.	CO4	BT1
10	Express what is Data-level parallelism? Data-level parallelism specifically subword parallelism, offers a simple path to higher performance for programs that are intensive in arithmetic operations for either integer or floating-point data.	CO4	BT2
PART C (12 Marks)			
1	Illustrate with neat sketches about Instruction level and Data level parallelism.	CO4	BT4
2	Discuss in detail about Flynn's Classification.	CO4	BT4
3	Elaborate about Hardware Multithreading	CO4	BT4
4	Articulate the key features of the MESI protocol.	CO4	BT3
5	Compare and contrast Uniprocessor and Multiprocessor system and explain them in detail	CO4	BT2
6.	Highlight about the Hardware performance issues that led to the development of multicore computers	CO4	BT4
7.	Compare and contrast about SISD,SIMD,MIMD,MISD	CO4	BT2
8.	Summarize in detail about Cache Coherence.	CO4	BT4
9.	Compare Coarse grained and Fine grained Multithreading and explain them in detail.	CO4	BT2
10.	Discuss about MESI protocol for Multiprocessor Systems	CO4	BT4

Note:

1. **BT Level –** Blooms Taxonomy Level
2. **CO – Course Outcomes**

BT1 –Remember BT2 – Understand BT3 – Apply BT4 – Analyze BT5 – Evaluate BT6 – Create