## SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

Ramapuram Campus, Bharathi Salai, Ramapuram, Chennai - 600089

### **FACULTY OF ENGINEERING AND TECHNOLOGY**

# DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING



## **QUESTION BANK**

**DEGREE / BRANCH: B Tech/CSE and all specializations** 

(AIML, BDA, IOT, CS)

III SEMESTER

18CSC203J-COMPUTER ORGANIZATION AND ARCHITECTURE

Regulation-2018

Academic Year -2021-2022

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# DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

#### **QUESTION BANK**

SUBJECT CODE : 18CSC203J

SUBJECT NAME : COMPUTER ORGANIZATION AND ARCHITECTURE

SEM/YEAR:III/II

**Course Outcomes** 

**CO1:** Identify the computer hardware and how software interacts with computer hardware

CO2: Apply Boolean algebra as related to designing computer logic, through simple combinational and sequential logic circuits

CO3: Analyze the detailed operation of Basic Processing units and the performance of

Pipelining

CO4: Analyze concepts of parallelism and multi-core processors

CO5: Identify the memory technologies, input-output systems and evaluate the performance of memory

system

CO6: Identify the computer hardware, software and its interactions

### UNIT V

Memory systems -Basic Concepts, Memory hierarchy- Memory technologies, RAM, Semiconductor RAM-ROM, Types, Speed, size cost- Cache memory, Mapping Functions- Replacement Algorithms, Problem Solving-Virtual Memory, Performance considerations of various memories- Input Output Organization, Need for Input output devices- Memory mapped IO, Program controlled IO- Interrupts-Hardware, Enabling and Disabling Interrupts, Handling multiple Devices

	PART-A (Multiple Choice Questions)		
Q.	Questions		Competence
No		Outcome	BT Level

1	Which of the following is the smallest entity of memory?  (a) Block  (b) Cell  (c) Instance  (d) Set	CO5	BT2
2	The primary memory (also called main memory) of a personal computer consists of  (a) RAM only (b) ROM only (c) both RAM and ROM (d) Cache memory	CO5	вті
3	The Boot sector files of the system are stored in which computer memory?  (a) RAM  (b) ROM  (c) Cache  (d) Register	CO5	BT2
4	Which of the following statements are not correct about the main memory of a computer?  (a) In main memory, data gets lost when power is switched off.  (b) Main memory is faster than secondary memory but slower than registers.  (c) They are made up of semiconductors.  (d) SRAM is used in Main memory	CO5	BT2

5			
	What is the full form of RAM?		
	(a) Read Access Memory		
	(b) Random Access Memory	CO5	BT1
	(c) Readable Access Memory		
	(d) Random Accumulator Memory		
6	RAM is and		
	(a) volatile, temporary		
	(b) non-volatile, temporary	CO5	BT3
	(c) volatile, permanent	003	<b>D</b> 13
	(d) non-volatile, permanent		
7	Which of the following memory is non-volatile?		
	(a) RAM		
	(b) ROM	CO5	BT2
	(c) Cache		
	(d) ROM and Cache		
8	Which of the following is the lowest in the computer memory hierarchy?		
	(a) Cache		
	(b) RAM	CO5	BT2
	(c) Secondary memory (d) CPU registers		
	(d) CFO legisters		
9	Which of the following has the fastest speed in the computer memory hierarchy?		
	(a) Cache	CO5	BT1
	(b) Register in CPU		

	(c) Main memory	1	
	(d) Disk cache		
10	Which memory acts as a buffer between CPU and main memory?		
	(a) RAM		
	(b) ROM	CO5	BT2
	(c) Cache		
	(d) Storage		
11	Which of the following statements are not correct about cache memory?		
	(a) Cache memory is used to store data temporarily.		
	(b) It holds that data and program which has to be executed within a short period of time.	CO5	BT2
	(c) It needs frequent refreshing		
	(d) It consumes less access time as compared to the Main memory		
12	In which type of ROM, data can be erased by ultraviolet light and then reprogrammed by the user or manufacturer?		
	(a) PROM		
	(b) EPROM	CO5	BT1
	(c) EEPROM		
	(d) Both a and b		
13	Primary storage is as compared to secondary storage.		
	(a) Slow and inexpensive	CO5	BT2
	(b) Fast and inexpensive		
	(d) It consumes less access time as compared to the Main memory  In which type of ROM, data can be erased by ultraviolet light and then reprogrammed by the user or manufacturer?  (a) PROM  (b) EPROM  (c) EEPROM  (d) Both a and b  Primary storage is as compared to secondary storage.  (a) Slow and inexpensive		

(c) Fast and expensive		
(d) Slow and expensive		
Which of the following statements is not true about secondary memory (auxiliary memory)?		
(a) Secondary memory is non-volatile in nature and slower than primary memories.		
(b) It is a faster memory device	CO5	BT2
(c) Data is permanently stored even if power is switched off.		
(d) Computers may run without secondary memory.		
(e) It is also known as backup memory.		
Virtual memory is an		
(a) Extremely large memory		
(b) Extremely large secondary memory	CO5	BT2
(c) Illusion of an extremely large memory		
(d) A type of memory used in supercomputers.		
Whenever the data is not found in the cache memory it is called as		
a) HIT		
b) MISS	CO5	BT2
c) FOUND	003	D12
d) ERROR		
When the data at a location in cache is different from the data located in the main memory, the cache is called		
a) Unique	CO5	BT2
b) Inconsistent		
c) Variable		
	Which of the following statements is not true about secondary memory (auxiliary memory)?  (a) Secondary memory is non-volatile in nature and slower than primary memories.  (b) It is a faster memory device  (c) Data is permanently stored even if power is switched off.  (d) Computers may run without secondary memory.  (e) It is also known as backup memory.  Virtual memory is an  (a) Extremely large memory  (b) Extremely large secondary memory  (c) Illusion of an extremely large memory  (d) A type of memory used in supercomputers.  Whenever the data is not found in the cache memory it is called as  a) HIT  b) MISS  c) FOUND  d) ERROR  When the data at a location in cache is different from the data located in the main memory, the cache is called  a) Unique  b) Inconsistent	(d) Slow and expensive  Which of the following statements is not true about secondary memory (auxiliary memory)?  (a) Secondary memory is non-volatile in nature and slower than primary memories.  (b) It is a faster memory device  (c) Data is permanently stored even if power is switched off.  (d) Computers may run without secondary memory.  (e) It is also known as backup memory.  Virtual memory is an  (a) Extremely large memory  (b) Extremely large secondary memory  (c) Illusion of an extremely large memory  (d) A type of memory used in supercomputers.  Whenever the data is not found in the cache memory it is called as

	d) Fault		
18	Which of the following is not a write policy to avoid Cache Coherence?  a) Write through  b) Write within  c) Write back  d) Buffered write	CO5	BT2
19	In mapping, the data can be mapped anywhere in the Cache Memory.  a) Associative b) Direct c) Set Associative d) Indirect	CO5	BT2
20	The transfer between CPU and Cache is  a) Block transfer  b) Word transfer  c) Set transfer  d) Associative transfer	CO5	BT2
21	LRU stands for a) Low Rate Usage b) Least Rate Usage c) Least Recently Used d) Low Required Usage	CO5	BT1
22	The binary address issued to data or instructions are called as  a) Physical address b) Location	CO5	BT1

	c) Relocatable address		
	d) Logical address		
23	Which of the following is not the main aim of virtual memory organization?		
	a) To provide effective memory access		
	b) To provide permanent backup	CO5	BT1
	c) To improve the execution of the program		
	d) To provide better memory transfer		
24	TLB is a		
	a) Permanent memory		
	b) Larger memory		
	c) Small cache	CO5	BT1
	d) Interface used for I/O devices		
25	Which of the following is used for detecting and correcting errors?		
	a) ACC		
	b) BCC	CO5	BT1
	c) ECC		
	d) TLB		
26	In a 3.5 inch(diameter) capacity magnetic disk, There are an average of		
	sectors per track		
	a) 200		
	b) 300	CO5	BT2
	c) 400		
	d) 500		
27	Which of the following is the time required to move the read/write head to the		
	proper track?		
	a) Track time		
	b) Fetch time	CO5	BT1
	c) Seek time		
	d) Disk time		
28	ROM stores a small program that can read and write main memory		
	locations	CO5	BT1

		1	
	a) monitor		
	b) snooping		
	c) writer		
	d) sub-routine		
29	In memory design, an approach to implement a narrow bus that is much faster		
	is		
	a) Rambus	CO5	DT1
	b) internal bus	CO5	BT1
	c) Memory bus		
	d) multi bus		
30	After the completion of the DMA transfer, the processor is notified by		
	a) Acknowledge signal		
	b) Interrupt signal	CO5	BT1
	c) WMFC signal		
	d) None of the mentioned		
31	How is a privilege exception dealt with?		
	a) The program is halted and the system switches into supervisor mode		
	and restarts the program execution		
	b) The Program is stopped and removed from the queue	CO5	BT1
	c) The system switches the mode and starts the execution of a new process		
	d) The system switches mode and runs the debugger		
32	The instructions which can be run only supervisor mode are?		
	a) Non-privileged instructions		
	b) System instructions	CO5	BT2
	c) Privileged instructions		
	d) Exception instructions		
33	The two facilities provided by the debugger is		
	a) Trace points		
	b) Break points	CO5	BT2
	c) Compile		212
	d) Both Trace and Break points		
34	If during the execution of an instruction an exception is raised then		
		CO5	BT2

	a) The instruction is executed and the exception is handled		
	b) The instruction is halted and the exception is handled		
	c) The processor completes the execution and saves the data and then handle		
	the exception		
	d) None of the mentioned		
35	Interrupts initiated by an instruction is called as		
	a) Internal		
	b) External	CO5	BT2
	c) Hardware		
	d) Software		
36	In memory-mapped I/O		
	a) The I/O devices and the memory share the same address space		
	b) The I/O devices have a separate address space	CO5	ВТ3
	c) The memory and I/O devices have an associated address space		
	d) A part of the memory is specifically set aside for the I/O operation		
37	The advantage of I/O mapped devices to memory mapped is		
	a) The former offers faster transfer of data		
	b) The devices connected using I/O mapping have a bigger buffer space	CO5	BT2
	c) The devices have to deal with fewer address lines		
	d) No advantage as such		
38	The system is notified of a read or write operation by		
	a) Appending an extra bit of the address		
	b) Enabling the read or write bits of the devices	CO5	BT2
	c) Raising an appropriate interrupt signal		
	d) Sending a special signal along the BUS		
39	To overcome the lag in the operating speeds of the I/O device and the processor		
	we use		
	a) Buffer spaces	COF	DTI
	b) Status flags	CO5	BT1
	c) Interrupt signals		
	d) Exceptions		
40	The method which offers higher speeds of I/O transfers is		
	a) Interrupts	CO5	BT2
	b) Memory mapping		

	c) Program-controlled I/O		
	d) DMA		
41	The method of synchronizing the processor with the I/O device in which the		
	device sends a signal when it is ready is?		
	a) Exceptions		
	b) Signal handling	CO5	BT2
	c) Interrupts		
	d) DMA		
42	The process wherein the processor constantly checks the status flags is called as		
	a) Polling		
	b) Inspection	CO5	BT2
	c) Reviewing		
	d) Echoing		
43	How can the processor ignore other interrupts when it is servicing one		
	a) By turning off the interrupt request line		
	b) By disabling the devices from sending the interrupts	CO5	BT1
	c) BY using edge-triggered request lines		
	d) All of the mentioned		
44	CPU as two modes privileged and non-privileged. In order to change the mode		
	from privileged to non-privileged.		
	a) A hardware interrupt is needed		
	b) A software interrupt is needed	CO5	BT2
	c) Either hardware or software interrupt is needed		
	d) A non-privileged instruction (which does not generate an interrupt)is needed		
45	An interrupt that can be temporarily ignored is		
	a) Vectored interrupt		
	b) Non-maskable interrupt	CO5	BT1
	c) Maskable interrupt		
	d) High priority interrupt		
46	The time between the receiver of an interrupt and its service is		
	a) Interrupt delay	CO5	BT2
	b) Interrupt latency		

a) i, iv b) ii, iii and iv c) iii, iv d) i, ii  The signal sent to the device from the processor to the device after receiving an interrupt is		c) Cycle time		
again. i) Register contents ii) Condition codes iii) Stack contents iv) Return addresses  CO5 BT2  a) i, iv b) ii, iii and iv c) iii, iv d) i, ii  48 The signal sent to the device from the processor to the device after receiving an interrupt is		d) Switching time		
i) Register contents ii) Condition codes iii) Stack contents iv) Return addresses  a) i, iv b) ii, iii and iv c) iii, iv d) i, ii  48 The signal sent to the device from the processor to the device after receiving an interrupt is a) Interrupt-acknowledge b) Return signal c) Service signal d) Permission signal  49 The return address from the interrupt-service routine is stored on the a) System heap b) Processor register c) Processor stack d) Memory  50 The interrupt-request line is a part of the a) Data line b) Control line c) Address line d) None of the mentioned  PART B (4 Marks)  1 Write on address spaces in I/o Devices with a neat diagram. COS BTI CO	47	When the process is returned after an interrupt service should be loaded		
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b) ii, iii and iv c) iii, iv d) i, ii  The signal sent to the device from the processor to the device after receiving an interrupt is		a) i, iv		
c) iii, iv d) i, ii  The signal sent to the device from the processor to the device after receiving an interrupt is				
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The return address from the interrupt-service routine is stored on the  a) System heap b) Processor register c) Processor stack d) Memory  50 The interrupt-request line is a part of the a) Data line b) Control line c) Address line d) None of the mentioned  PART B (4 Marks)  1 Write on address spaces in I/o Devices with a neat diagram.  CO5 BT1  Treatment of an interrupt-service routine is very similar to that of a subroutine		c) Service signal		
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The interrupt-request line is a part of the  a) Data line  b) Control line c) Address line d) None of the mentioned  PART B (4 Marks)  Write on address spaces in I/o Devices with a neat diagram.  CO5  BT1  Treatment of an interrupt-service routine is very similar to that of a subroutine		c) Processor stack		
a) Data line b) Control line c) Address line d) None of the mentioned  PART B (4 Marks)  Write on address spaces in I/o Devices with a neat diagram.  Treatment of an interrupt-service routine is very similar to that of a subroutine  COS BT3		d) Memory		
b) Control line c) Address line d) None of the mentioned  PART B (4 Marks)  Write on address spaces in I/o Devices with a neat diagram.  Treatment of an interrupt-service routine is very similar to that of a subroutine  COS BT3	50	The interrupt-request line is a part of the		
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PART B (4 Marks)  1 Write on address spaces in I/o Devices with a neat diagram.  CO5 BT1  Treatment of an interrupt-service routine is very similar to that of a subroutine		c) Address line		
<ul> <li>Write on address spaces in I/o Devices with a neat diagram.</li> <li>Treatment of an interrupt-service routine is very similar to that of a subroutine</li> </ul>		d) None of the mentioned		
2 Treatment of an interrupt-service routine is very similar to that of a subroutine		PART B (4 Marks)		
COS BT3	1		CO5	BT1
–Justify the above statement	2		CO5	ВТ3

3	Does Saving and restoring registers involve memory transfers? Is the statement true or false .explain in brief your answer?	CO5	BT2
4	What are the steps to be done to reduce interrupt latency?	CO5	BT2
5	Write short notes Delay, latency and interrupt latency.	CO5	BT2
6	Define hardware interrupt.	CO5	BT1
7	Draw a diagram for enabling and disabling of interrupts?	CO5	BT2
8	Explain on privilege exception?	CO5	BT2
9	Explain about speed size cost?	CO5	BT2
	PART C (12 Marks)		
1	Write on privilege exception and draw a diagram to justify your answer and explain it.	CO5	BT2
2	Difference between handling I/O interrupt-request and handling exceptions due to errors and brief on it.	CO5	BT2
3	Discuss in detail about the Control unit which performs these transfers is a part of the I/O devices.	CO5	BT2
4	Draw and explain DMA bus attribution .Converse on your answer with your own example	CO5	ВТ3
5	Draw a diagram with master and slave for your synchronous bus and describe on it.	CO5	BT3