Unit III - Combinational Logic Circuits

Part – B (4 marks)

1. Obtain the SOP term for the given function F= $\Sigma_{A,B,C}$ (0,2,3,5,7). Convert the obtained SOP form to POS form?
2. Obtain the reduced logical expression using K-map method for the given minterms. F(A,B,C,D) = Σ(3,7,11,12,13,14,15)
3. Explain the working of 8:1 Multiplexer with suitable truth table, equations and diagram.
4. Implement the following function using 8:1 MUX

$\boldsymbol{f(A,B,C,D) = \sum_m(0,2,4,6,8,10,12,14)}$

5. Implement the following Boolean function with the help of 4:1 Mux. f(A,B,C,D) = ΠM(1,2,4,7,11,13,15).
6. What is multiplexer? Draw logic diagram for 4 line to 1 line multiplexer.
7. Implement the following Boolean function using 8:1 Mux: F(A,B,C,D)=Σm(0,1,3,4,8,9,15)
8. Obtain the design of the given function using suitable multiplexer F= Σm(0,2,5,7).
9. Draw the circuit to implement a four-bit binary adder- subtractor using mode selection control input
10. Describe the application of multiplexer and demultiplexer
11. Describe the application of encoder and decoder
12. Difference between decoder and encoder
13. Implement the full subtractor with the help of 2:4 decoder.
14. Outline the characteristics of a priority encoder and how it differs from a regular encoder?
15. Design a half subtractor using only basic gates
16. Design a half adder using only basic gates
17. Implementation the full-subtractor using two half-subtractors.
18. Design a 4-bit Carry Propagation–Look-Ahead Carry generator
19. Implement the following function using PLA F1=∑m(1,2,4,6)
20. Show how a full order can be converted to a full subtractor with the addition of an inverter circuit.
21. Design a 1- bit magnitude comparator .
22. Design a 8x4 PROM with 3 input and 4 output lines
23. Write difference between a PAL & PLA.
24. Draw logic diagram of 1 to 2 line de-mux. Explain its action with truth table.

25. Compare RAM and ROM.
26. Implement the following using a suitable PROM F = ∑m (2,1,0)
27. Draw the picture of complete ALU circuit.
28. Compare Behavioral style in VHDL with Dataflow style in VHDL.
29. Define gate level modelling and data flow modelling in VHDL?
30. What are the various modelling technique in HDL?
31. Explain the behavioural modelling and data flow modelling?

Part – C (12 marks)

1. Determine the sum of product for the following Boolean expression using quine McCluskey method. F (A,B,C,D) = ∑ m (2,6,8,9,10,11,14,15)
2. Determine the sum of product for the following Boolean expression using quine McCluskey method. F (A,B,C,D) = ∑ m (1,7,9,10,12,13,15) +d (0,2,4)
3. Implement the following Boolean function using an 8:1 multiplexer considering D as the input and A,B,C as selection lines : F(A, B, C, D) = AB'+BD+B'CD'
4. Design a full adder using 4X1 multiplexer; also write its truth table and logical diagram.
5. Design a full adder circuit using Demultiplexer
6. Design an Octal to Binary Encoder
7. Design a 3*8 decoder and explain its operation as a minterm generator.
8. Design a 3 bit magnitude comparator using gates
9. Draw the logic diagram of a 4 bit carry look ahead adder and explain how this adder is advantageous over the ripple carry adder
10. Analyze the principle and design of Parallel binary adder with diagrams
11. Describe about multiplexer and Simplify the following function using 8x1 Mux F= ∑m (0,1,3,4,8,9,15)
12. Realize the function F(w, x, y, z)= Σ (1,4,6,7,8,9,10,11,15) using 8 to 1 Multiplexer.
13. Derive the circuit that implements an 8-to-3 binary encoder with neat diagram.
14. Demonstrate on a 2-bit magnitude comparator with three outputs: A>B, A=B and A
15. Discuss about the purpose of decoder and Implement a full adder and full subtractor using decoder.
16. Discuss about the design of 4-bit BCD adder with neat diagram and mention how many adders are used in the BCD circuit.
17. With necessary diagrams, explain in detail about the working of a 4-bit look ahead carry

adder. Also mention its advantages over conventional adder.

18. Design the Logic diagram of 2-bit magnitude comparator with relevant truth table and K Map reduction.
19. Discuss the working of 8 to 3 line binary encoder with truth table, equations and neat circuit diagram.
20. With neat diagram and truth table, explain the working of 4:2 line binary encoder.