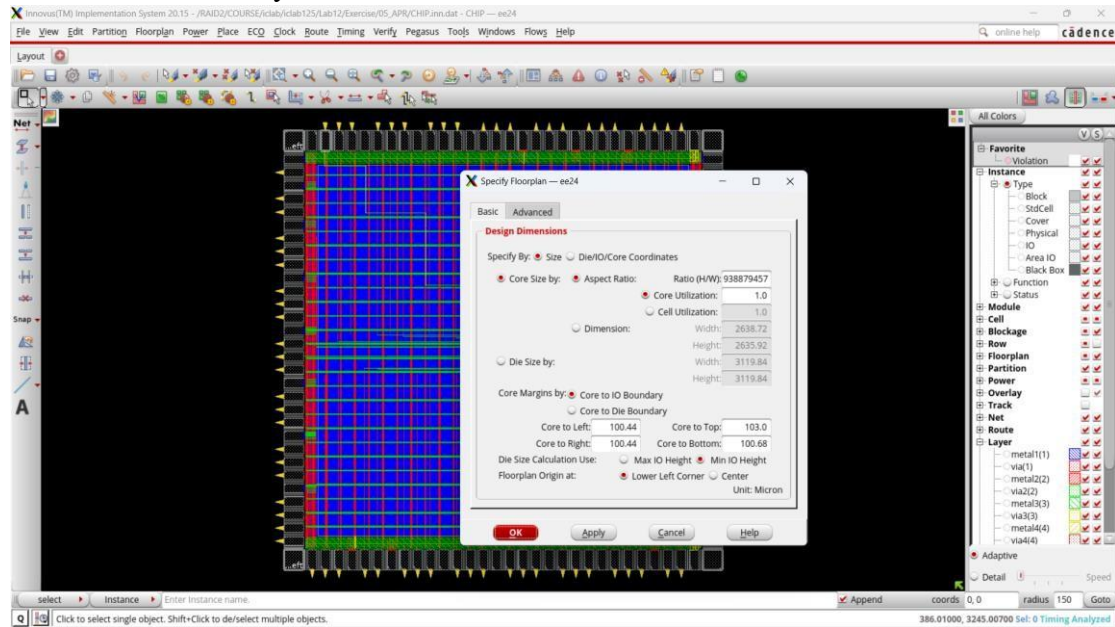


ICLAB LAB12 Report

國際半導體學院碩一

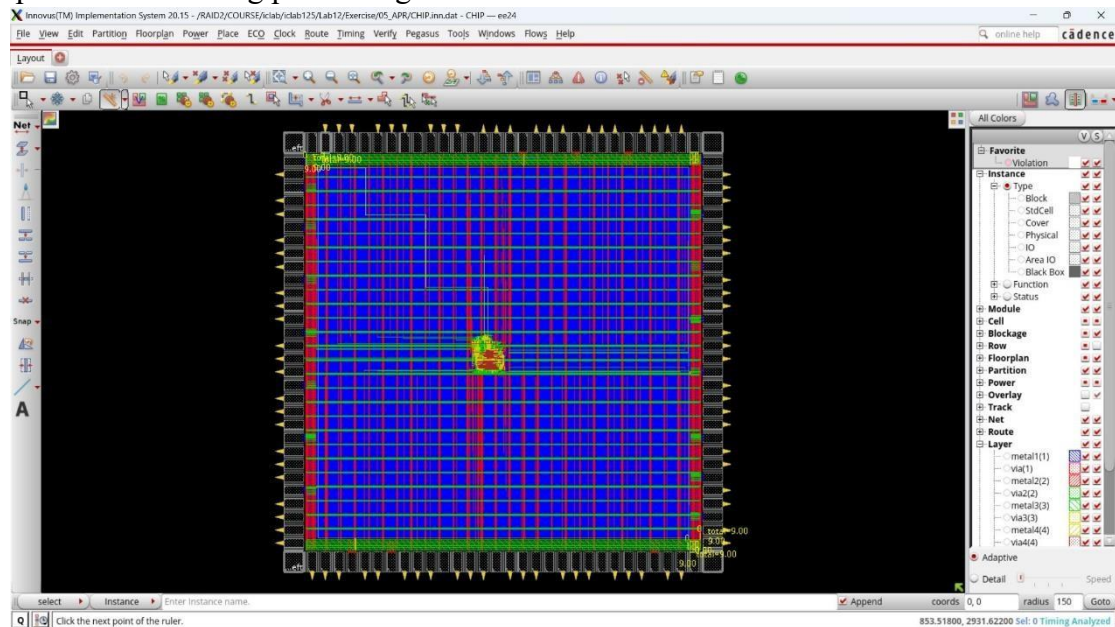
ICLAB 帳號：iclab125 學號：313591021 姓名：沈佳瞳

1.Core to IO boundary

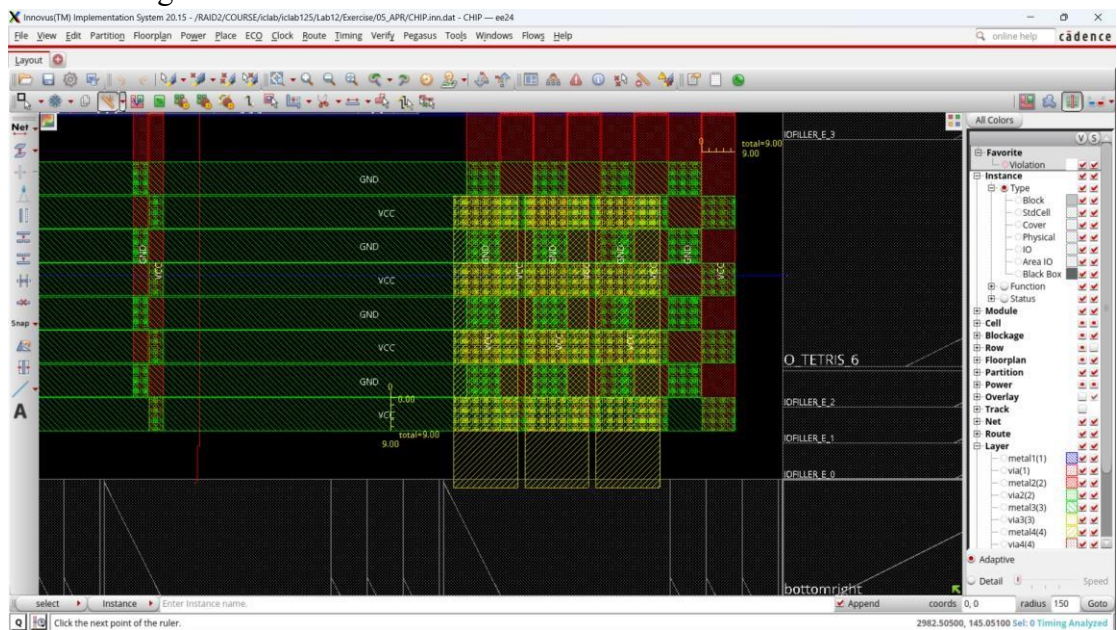
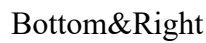


2.Core Ring

4pairs & interleaving power ring



Top&Left



3. Post-Route setup time analysis

Quick connect...

RAI02\COURSE\iclab125\Lab12\Exercise05_APR\

Name	Size (KB)	Last modified	Owner
cadence		2024-11-18 20:31	iclab012
Celric		2024-11-18 20:31	iclab012
CHP_forgoan.inm.dat		2024-12-05 19:06	iclab012
CHP_xanofautem.inm		2024-12-05 19:09	iclab012
CHP_placement.inm		2024-12-05 19:02	iclab012
CHP_postCTS.inm.dat		2024-12-05 19:07	iclab012
CHP_postRattem.inm		2024-12-05 19:17	iclab012
CHP_powerplan.inm.dat		2024-12-05 19:01	iclab012
CHP_pwrCTS.inm.dat		2024-12-05 19:05	iclab012
cmf		2024-12-05 18:44	iclab012
D6S		2024-12-05 19:06	iclab012
endxlogr		2024-12-05 19:15	iclab012
l0vermap		2024-11-18 20:31	iclab012
LEF		2024-11-18 20:31	iclab012
LIB		2024-11-18 20:31	iclab012
lhc		2024-11-18 20:31	iclab012
timingreports		2024-12-05 19:17	iclab012
01_combine	1	2024-11-18 20:31	iclab012
01_setup	1	2024-12-05 18:44	iclab012
01_clean_up	1	2024-11-18 20:31	iclab012
CHP_CCDT.spec	2	2024-12-05 19:06	iclab012
CHP_cm.rpt	1	2024-12-05 19:09	iclab012
CHP_cm.rpt.pdf	1	2024-12-05 19:01	iclab012
CHP_drc.rpt	1	2024-12-05 19:09	iclab012
CHP_drc.rpt.pdf	1	2024-12-05 19:00	iclab012
01_globals	135	2024-12-05 18:55	iclab012
CHP_01e	7	2024-12-05 18:41	iclab012
CHP_01d	16	2024-12-05 18:41	iclab012
CHP_01d.pdf	1	2024-12-04 20:27	iclab012
CHP_forgoan.inm	1	2024-12-05 18:56	iclab012
CHP_mnm.view	1	2024-12-05 18:55	iclab012
CHP_nxofautem	1	2024-12-05 19:09	iclab012
CHP_placement.inm	1	2024-12-05 19:02	iclab012
CHP_postCTS.inm	1	2024-12-05 19:07	iclab012
CHP_postRattem	1	2024-12-05 19:17	iclab012

Remote monitoring

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```

Total number of fetched objects 1362
AIE_INFO: Total number of nets for which stage creation was skipped for all views 0
AIE_INFO-610: Total number of nets in the design is 1340, 0.4 percent of the nets selected for SI analysis
End delay calculation. (MWM=2588.94 CPU=00:00:00 REAL=00:00:00)
End delay calculation (fullDC). (MWM=2588.94 CPU=00:00:00 REAL=00:00:00)
** Done Building Timing Graph (cpu=00:00:01.4 real=00:00:01.0 totSessionCpu=01:23 mem=2588.9M)

-----
timeDesign Summary
-----

Setup views included:
av_func_mode_max

-----
| Setup mode | all | reg2reg | default |
|-----|-----|-----|-----|
| MNS (ns): | 13.897 | 31.282 | 13.897 |
| TNS (ns): | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 595 | 247 | 366 |
|-----|-----|-----|-----|

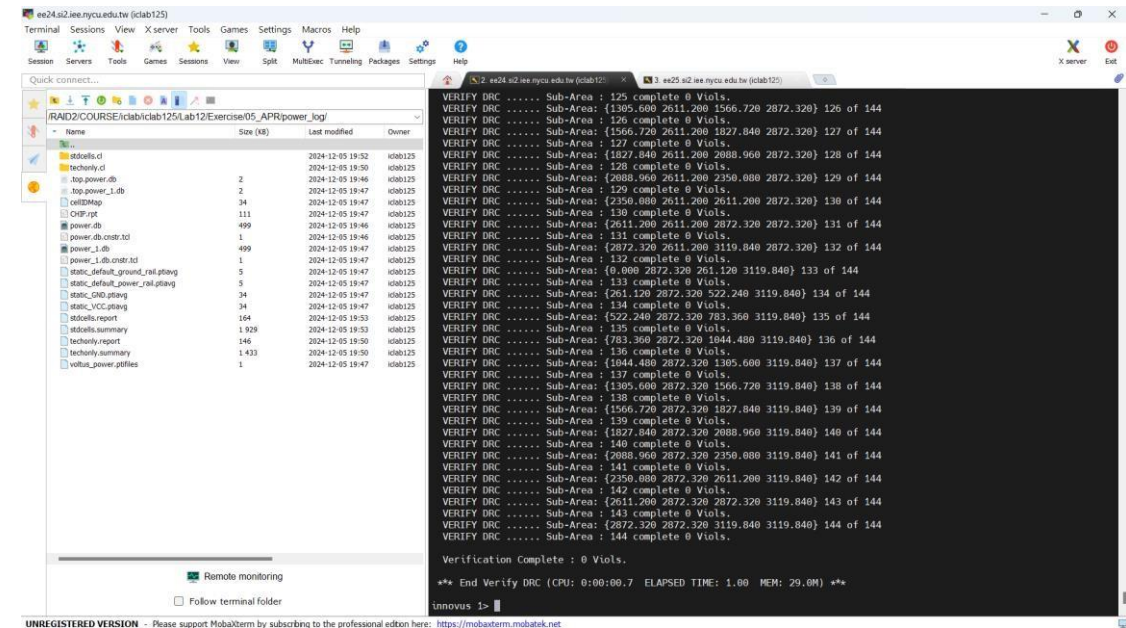
-----
| DRVs | Real | Total | |
|---|---|---|---|
| Nr nets(terms) | Worst Vio | Nr nets(terms) |
|-----|-----|-----|
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_fanin | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0.000 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
|-----|-----|-----|

Density: 0.551%
Total number of glitch violations: 0
Reported timing to dir timingReports
Total CPU time: 7.02 sec
Total Real Time: 10.9 sec
Total Memory Usage: 2604,214844 Mbytes
Reset AIE Options
** timeDesign #1 [finish] : cpu/real = 0:00:07.0/0:00:09.7 (0.7), totSession cpu/real = 0:01:23.2/0:06:07.2 (0.2), me
m = 2604.2M
innovus 5>
  
```

4. Post-Route hold time analysis

The screenshot displays the Mobatek testbench environment. On the left, a file explorer shows the project structure for 'RND2COURSElab125Lab12Exercise05_APR'. The central terminal window shows the command 'run' being executed. The right-hand console window provides detailed simulation results, including a summary of fetched objects, timing reports, and resource usage statistics. The console output indicates that the simulation completed successfully, with a total CPU time of 1.03 seconds and a total memory usage of 2561.33984 Mbytes.

5.DRC result



Terminal Sessions View X server Tools Games Settings Macros Help

Quick connect...

RAID2\COURSE\iclab125\Lab12\Exercise05_APR\power_log\

Name	Size (KB)	Last modified	Owner
dbcells.d	1	2024-12-05 19:52	iclab125
techonly.d	1	2024-12-05 19:50	iclab125
top.power.db	2	2024-12-05 19:46	iclab125
top.power_1.db	2	2024-12-05 19:47	iclab125
cellMap	34	2024-12-05 19:47	iclab125
chip.rpt	111	2024-12-05 19:47	iclab125
power.db	499	2024-12-05 19:46	iclab125
power.db.csr.tcl	1	2024-12-05 19:46	iclab125
power_1.db	499	2024-12-05 19:47	iclab125
power_1.db.csr.tcl	1	2024-12-05 19:47	iclab125
static_default_ground_rail.plg	5	2024-12-05 19:47	iclab125
static_default_power_rail.plg	1	2024-12-05 19:47	iclab125
static_GND.plg	34	2024-12-05 19:47	iclab125
static_VCC.plg	34	2024-12-05 19:47	iclab125
stdcells.report	164	2024-12-05 19:53	iclab125
stdcells.summary	1,929	2024-12-05 19:53	iclab125
techonly.report	146	2024-12-05 19:50	iclab125
techonly.summary	1,433	2024-12-05 19:50	iclab125
volut_power.ptfiles	1	2024-12-05 19:47	iclab125

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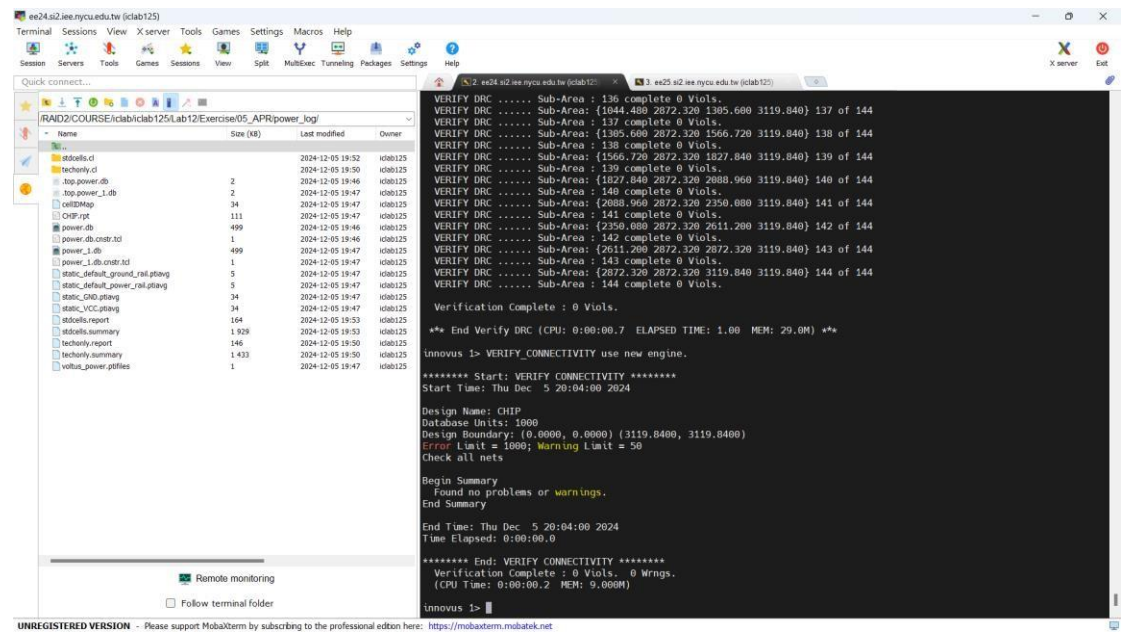
```
VERIFY DRC ..... Sub-Area : 125 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1395.600 2611.200 1566.720 2872.320} 126 of 144
VERIFY DRC ..... Sub-Area : 126 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1566.720 2611.200 1827.840 2872.320} 127 of 144
VERIFY DRC ..... Sub-Area : 127 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1827.840 2611.200 2088.960 2872.320} 128 of 144
VERIFY DRC ..... Sub-Area : 128 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2088.960 2611.200 2350.080 2872.320} 129 of 144
VERIFY DRC ..... Sub-Area : 129 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2350.080 2611.200 2611.200 2872.320} 130 of 144
VERIFY DRC ..... Sub-Area : 130 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2611.200 2611.200 2872.320 2872.320} 131 of 144
VERIFY DRC ..... Sub-Area : 131 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2872.320 2611.200 3119.840 2872.320} 132 of 144
VERIFY DRC ..... Sub-Area : 132 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {0.000 2872.320 261.120 3119.840} 133 of 144
VERIFY DRC ..... Sub-Area : 133 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {261.120 2872.320 522.240 3119.840} 134 of 144
VERIFY DRC ..... Sub-Area : 134 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {522.240 2872.320 783.360 3119.840} 135 of 144
VERIFY DRC ..... Sub-Area : 135 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {783.360 2872.320 1044.480 3119.840} 136 of 144
VERIFY DRC ..... Sub-Area : 136 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1044.480 2872.320 1305.600 3119.840} 137 of 144
VERIFY DRC ..... Sub-Area : 137 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1305.600 2872.320 1566.720 3119.840} 138 of 144
VERIFY DRC ..... Sub-Area : 138 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1566.720 2872.320 1827.840 3119.840} 139 of 144
VERIFY DRC ..... Sub-Area : 139 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1827.840 2872.320 2088.960 3119.840} 140 of 144
VERIFY DRC ..... Sub-Area : 140 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2088.960 2872.320 2350.080 3119.840} 141 of 144
VERIFY DRC ..... Sub-Area : 141 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2350.080 2872.320 2611.200 3119.840} 142 of 144
VERIFY DRC ..... Sub-Area : 142 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2611.200 2872.320 2872.320 3119.840} 143 of 144
VERIFY DRC ..... Sub-Area : 143 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2872.320 2872.320 3119.840 3119.840} 144 of 144
VERIFY DRC ..... Sub-Area : 144 complete 0 Viols.

Verification Complete : 0 Viols.

** End Verify DRC (CPU: 0:00:00.7 ELAPSED TIME: 1.00 MEM: 29.0M) **

innovus >
```

6.LVSResult



Terminal Sessions View X server Tools Games Settings Macros Help

Quick connect...

RAID2\COURSE\iclab125\Lab12\Exercise05_APR\power_log\

Name	Size (KB)	Last modified	Owner
dbcells.d	1	2024-12-05 19:52	iclab125
techonly.d	1	2024-12-05 19:50	iclab125
top.power.db	2	2024-12-05 19:46	iclab125
top.power_1.db	2	2024-12-05 19:47	iclab125
cellMap	34	2024-12-05 19:47	iclab125
chip.rpt	111	2024-12-05 19:47	iclab125
power.db	499	2024-12-05 19:46	iclab125
power.db.csr.tcl	1	2024-12-05 19:46	iclab125
power_1.db	499	2024-12-05 19:47	iclab125
power_1.db.csr.tcl	1	2024-12-05 19:47	iclab125
static_default_ground_rail.plg	5	2024-12-05 19:47	iclab125
static_default_power_rail.plg	1	2024-12-05 19:47	iclab125
static_GND.plg	34	2024-12-05 19:47	iclab125
static_VCC.plg	34	2024-12-05 19:47	iclab125
stdcells.report	164	2024-12-05 19:53	iclab125
stdcells.summary	1,929	2024-12-05 19:53	iclab125
techonly.report	146	2024-12-05 19:50	iclab125
techonly.summary	1,433	2024-12-05 19:50	iclab125
volut_power.ptfiles	1	2024-12-05 19:47	iclab125

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```
VERIFY DRC ..... Sub-Area : 136 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1044.480 2872.320 1305.600 3119.840} 137 of 144
VERIFY DRC ..... Sub-Area : 137 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1305.600 2872.320 1566.720 3119.840} 138 of 144
VERIFY DRC ..... Sub-Area : 138 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1566.720 2872.320 1827.840 3119.840} 139 of 144
VERIFY DRC ..... Sub-Area : 139 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {1827.840 2872.320 2088.960 3119.840} 140 of 144
VERIFY DRC ..... Sub-Area : 140 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2088.960 2872.320 2350.080 3119.840} 141 of 144
VERIFY DRC ..... Sub-Area : 141 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2350.080 2872.320 2611.200 3119.840} 142 of 144
VERIFY DRC ..... Sub-Area : 142 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2611.200 2872.320 2872.320 3119.840} 143 of 144
VERIFY DRC ..... Sub-Area : 143 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {2872.320 2872.320 3119.840 3119.840} 144 of 144
VERIFY DRC ..... Sub-Area : 144 complete 0 Viols.

Verification Complete : 0 Viols.

** End Verify DRC (CPU: 0:00:00.7 ELAPSED TIME: 1.00 MEM: 29.0M) **

innovus > VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Thu Dec 5 20:04:00 2024

Design Name: CHIP
Database Units: 10000
Design Boundary: (0.0000, 0.0000) (3119.8400, 3119.8400)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
Found no problems or warnings.
End Summary

End Time: Thu Dec 5 20:04:00 2024
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols., 0 Wrngs.
(CPU Time: 0:00:00.2 MEM: 9.000M)

innovus >
```

7. Post Layout simulation result

Quick connect...

RAID2/COURSE/iclab125/Lab12/Exercise05_APR/

File Name Size (KB) Last modified Owner

- codebase 2024-11-18 20:31 klab12
- CeH2C 2024-11-18 20:31 klab12
- CHIP.inn.dat 2024-12-05 19:28 klab12
- CHIP_floorplan.inn.dat 2024-12-05 18:56 klab12
- CHIP_nanoRoute.inn.dat 2024-12-05 19:24 klab12
- CHIP_nanoRouteinn.dat 2024-12-05 19:09 klab12
- CHIP_placement.inn.dat 2024-12-05 19:02 klab12
- CHIP_postCTS.inn.dat 2024-12-05 19:07 klab12
- CHIP_postRoute.inn.dat 2024-12-05 19:27 klab12
- CHIP_postRouteinn.dat 2024-12-05 19:17 klab12
- CHIP_powerplan.inn.dat 2024-12-05 19:01 klab12
- CHIP_preCTS.inn.dat 2024-12-05 19:05 klab12
- cmd 2024-12-05 18:44 klab12
- D6S 2024-12-05 19:06 klab12
- extLogDir 2024-12-05 19:26 klab12
- layermap 2024-11-18 20:31 klab12
- LEF 2024-11-18 20:31 klab12
- LIB 2024-11-18 20:31 klab12
- RC 2024-11-18 20:31 klab12
- timingReports 2024-12-05 19:26 klab12
- timing_file_3795.tf.gz 82 2024-12-05 19:22 klab12
- 00_combine 2024-11-18 20:31 klab12
- 01_senv 2024-12-05 18:44 klab12
- 09_clean_up 2024-11-18 20:31 klab12
- CHIP.CCOP.rpt 2 2024-12-05 19:06 klab12
- CHIP.com.rpt 1 2024-12-05 19:28 klab12
- CHIP.com.rpt.oid 1 2024-12-05 19:23 klab12
- CHIP.def 1 2024-12-05 19:32 klab12
- CHIP.drc.rpt 1 2024-12-05 19:28 klab12
- CHIP.drc.rpt.oid 1 2024-12-05 19:23 klab12
- CHIP_globals 135 2024-12-05 18:55 klab12
- CHIP.inn 1 2024-12-05 19:28 klab12
- CHIP.is 7 2024-12-05 18:41 klab12
- CHIP.sdc 16 2024-12-05 18:41 klab12
- CHIP.sdf 1,507 2024-12-05 19:29 klab12

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```
No. 968 PASS
No. 969 PASS
No. 970 PASS
No. 971 PASS
No. 972 PASS
No. 973 PASS
No. 974 PASS
No. 975 PASS
No. 976 PASS
No. 977 PASS
No. 978 PASS
No. 979 PASS
No. 980 PASS
No. 981 PASS
No. 982 PASS
No. 983 PASS
No. 984 PASS
No. 985 PASS
No. 986 PASS
No. 987 PASS
No. 988 PASS
No. 989 PASS
No. 990 PASS
No. 991 PASS
No. 992 PASS
No. 993 PASS
No. 994 PASS
No. 995 PASS
No. 996 PASS
No. 997 PASS
No. 998 PASS
No. 999 PASS
*****
Congratulations!
*****
execution cycles = 84824
clock period = 48,000,000ns
*****
$finish called from file "PATTERN.V", line 26.
$finish at simulation time 4461420000
*****
VCS Simulation Report
Time: 4461420000 ps
CPU Time: 6.920 seconds; Data structure size: 0.6Mb
Thu Dec 5 19:39:25 2024
CPU time: 1.254 seconds to compile + .350 seconds to elab + .649 seconds to link + 6.908 seconds in simulation
19:39 iclab125@ee24:/Lab12/Exercise06_POST.js
```

8. Power result

Quick connect...

RAID2/COURSE/iclab125/Lab12/Exercise05_APR/

File Name Size (KB) Last modified Owner

- CHIP_postCTS.inn.dat 2024-12-05 19:07 klab12
- CHIP_postRoute.inn.dat 2024-12-05 19:27 klab12
- CHIP_postRouteinn.dat 2024-12-05 19:17 klab12
- CHIP_powerplan.inn.dat 2024-12-05 19:01 klab12
- CHIP_preCTS.inn.dat 2024-12-05 19:05 klab12
- cmd 2024-12-05 18:44 klab12
- D6S 2024-12-05 19:06 klab12
- extLogDir 2024-12-05 19:26 klab12
- layermap 2024-11-18 20:31 klab12
- LEF 2024-11-18 20:31 klab12
- LIB 2024-11-18 20:31 klab12
- power_log 2024-12-05 18:40 klab12
- RC 2024-11-18 20:31 klab12
- timingReports 2024-12-05 19:26 klab12
- 00_combine 2024-11-18 20:31 klab12
- 01_senv 2024-12-05 18:44 klab12
- 09_clean_up 2024-11-18 20:31 klab12
- CHIP.CCOP.rpt 2 2024-12-05 19:06 klab12
- CHIP.com.rpt 1 2024-12-05 19:28 klab12
- CHIP.com.rpt.oid 1 2024-12-05 19:23 klab12
- CHIP.def 1 2024-12-05 19:32 klab12
- CHIP.drc.rpt 1 2024-12-05 19:28 klab12
- CHIP.drc.rpt.oid 1 2024-12-05 19:23 klab12
- CHIP_globals 135 2024-12-05 18:55 klab12
- CHIP.inn 1 2024-12-05 19:28 klab12
- CHIP.is 7 2024-12-05 18:41 klab12
- CHIP.sdc 16 2024-12-05 18:41 klab12
- CHIP.sdf 1,507 2024-12-05 19:29 klab12
- CHIP.v 2024-12-05 19:29 klab12
- CHIP_uts.sdc 1 2024-12-04 20:27 klab12
- CHIP_floorplan.inn 1 2024-12-05 18:56 klab12
- CHIP_inn.inn 1 2024-12-05 18:55 klab12
- CHIP_nanoRoute.inn 1 2024-12-05 19:24 klab12
- CHIP_nanoRouteinn 1 2024-12-05 19:09 klab12
- CHIP_placement.inn 1 2024-12-05 19:02 klab12
- CHIP_postCTS.inn 1 2024-12-05 19:07 klab12

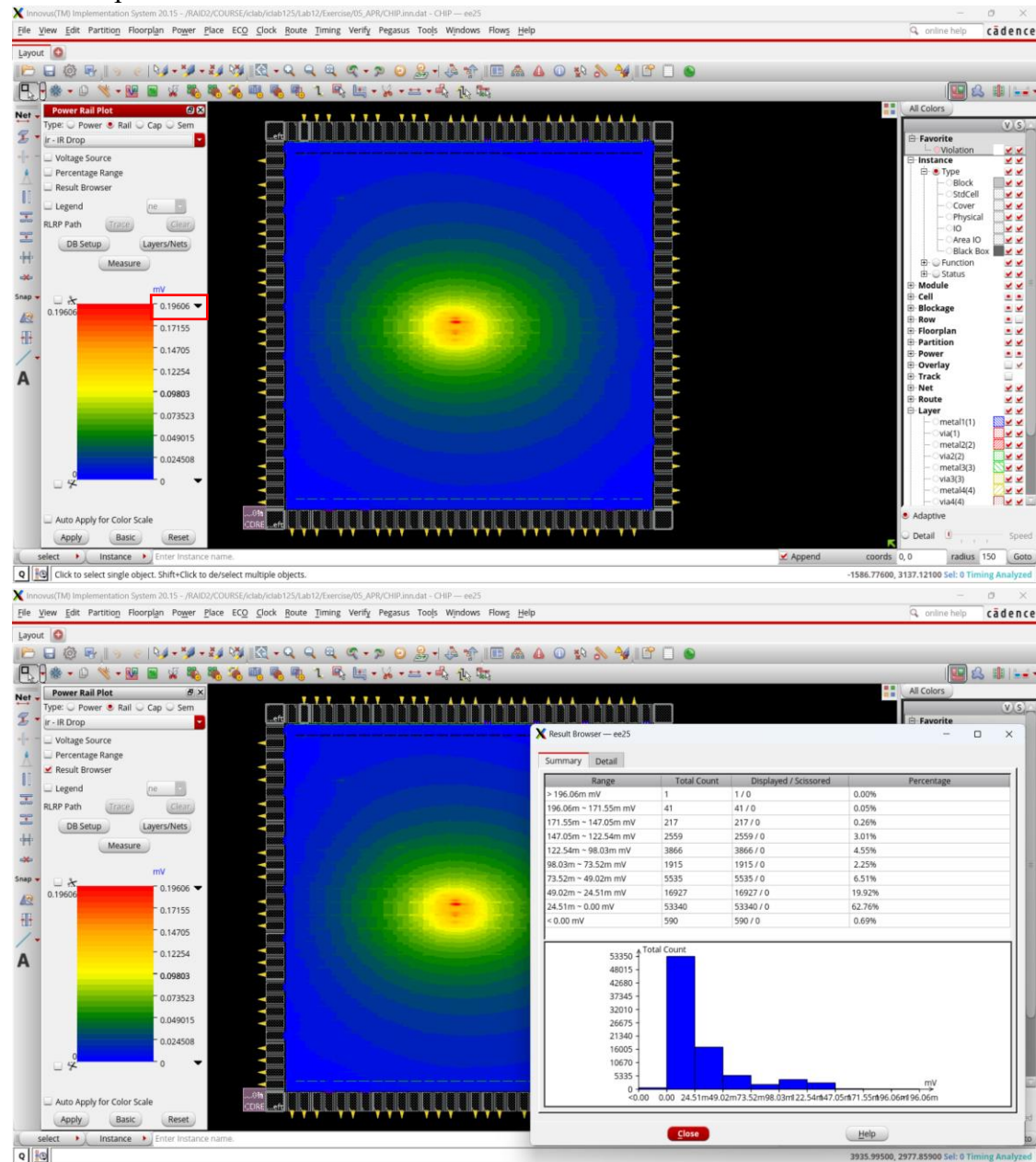
Remote monitoring

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```
2024-Dec-05 19:47:41 (2024-Dec-05 11:47:41 GMT): 20%
2024-Dec-05 19:47:41 (2024-Dec-05 11:47:41 GMT): 30%
2024-Dec-05 19:47:41 (2024-Dec-05 11:47:41 GMT): 40%
... Calculating internal and Leakage power
2024-Dec-05 19:47:41 (2024-Dec-05 11:47:41 GMT): 50%
2024-Dec-05 19:47:41 (2024-Dec-05 11:47:41 GMT): 60%
2024-Dec-05 19:47:41 (2024-Dec-05 11:47:41 GMT): 70%
2024-Dec-05 19:47:41 (2024-Dec-05 11:47:41 GMT): 80%
2024-Dec-05 19:47:41 (2024-Dec-05 11:47:41 GMT): 90%
2024-Dec-05 19:47:41 (2024-Dec-05 11:47:41 GMT): 98%
Finished Calculating power
2024-Dec-05 19:47:41 (2024-Dec-05 11:47:41 GMT)
Ended Power Computation: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=1669.91MB/3750.05MB/2013.74MB)
Begin Processing User Attributes
Ended Processing User Attributes: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=1669.91MB/3750.05MB/2013.74MB)
Ended Power Analysis: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=1669.91MB/3750.05MB/2013.74MB)
Begin Boundary Leakage Calculation
Ended Boundary Leakage Calculation: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=1669.91MB/3750.05MB/2013.74MB)
Begin Static Power Report Generation
32 instances have no static power
Total Power
-----
Total Internal Power: 1.11900314 45.7749%
Total Switching Power: 1.31632968 53.8084%
Total Leakage Power: 0.01019549 0.4168%
Total Power: 2.44632032
-----
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=1669.93MB/3750.05MB/2013.74MB)
Begin Creating Binary Database
Ended Creating Binary Database: (cpu=0:00:00, real=0:00:00, mem(process/total/peak)=2184.23MB/4520.47MB/2184.23MB)
Output file is power_log/CHIP.rpt
```


9. IR Drop result



降低 IR drop 的方法：

IR drop 是指電流流經步線網路造成的電壓損耗。我將 chip 設計為正方形，放置了 12 組 core power pads，平均分布在 chip 的四個邊，避免 power 走線過長。最終 IR drop 小於 0.2mV。