ICLAB LAB12 Report

國際半導體學院碩一

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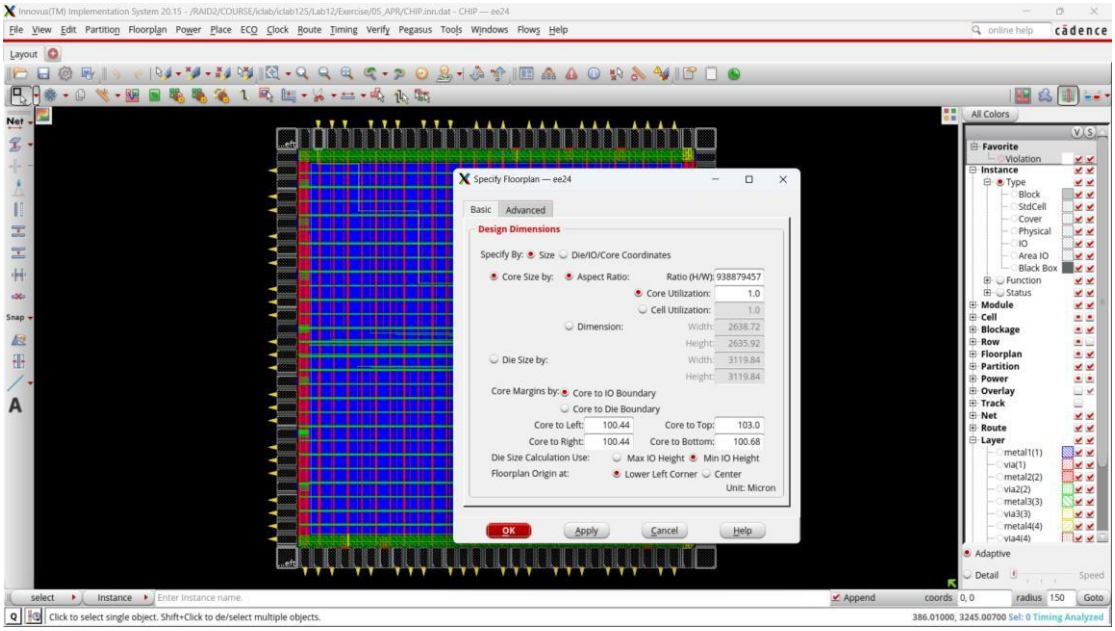
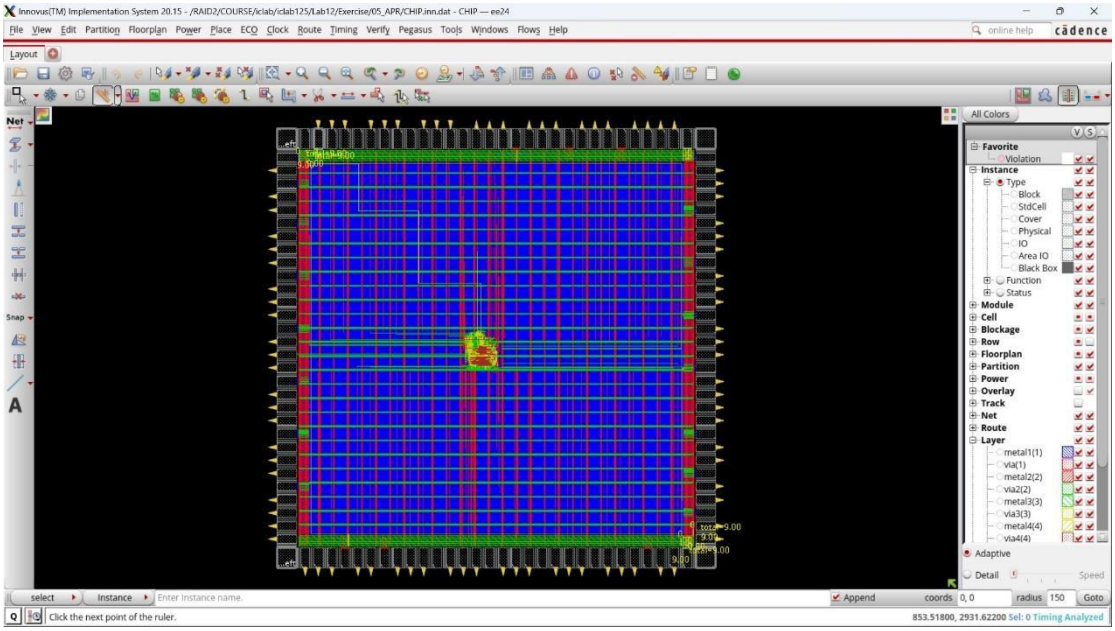
1.Core to IO boundary

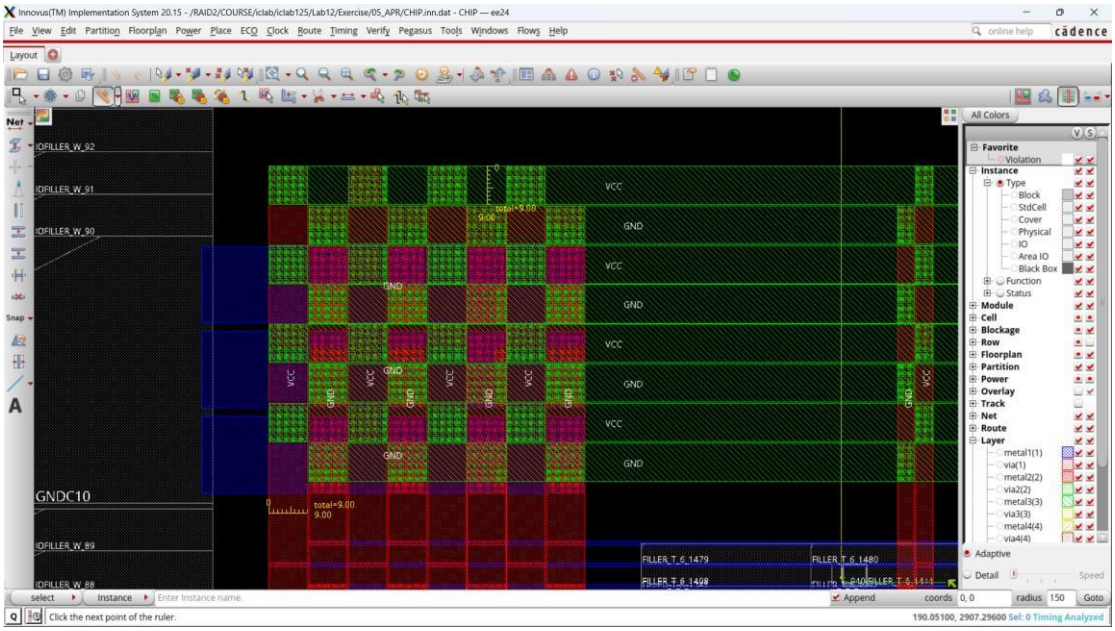


2.Core Ring

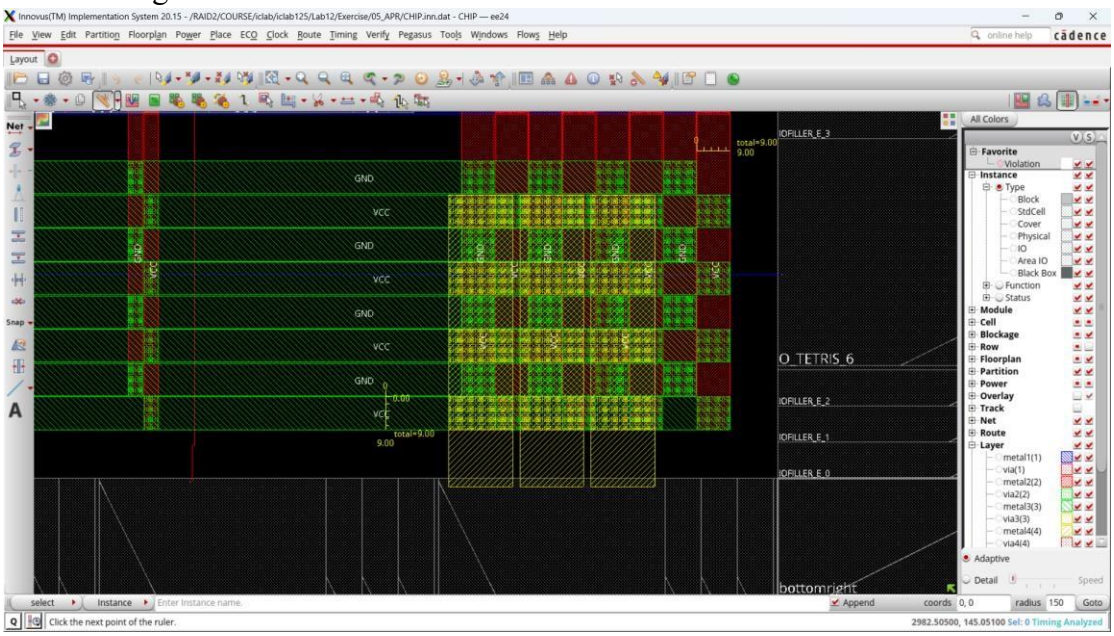
4pairs &interleaving power ring



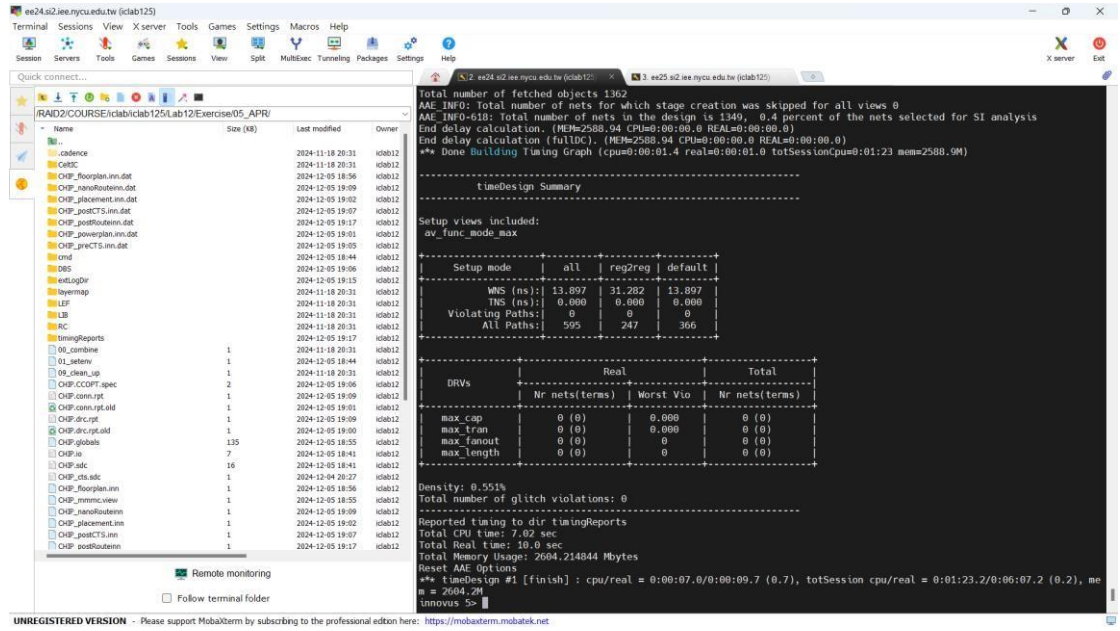
Top&Left



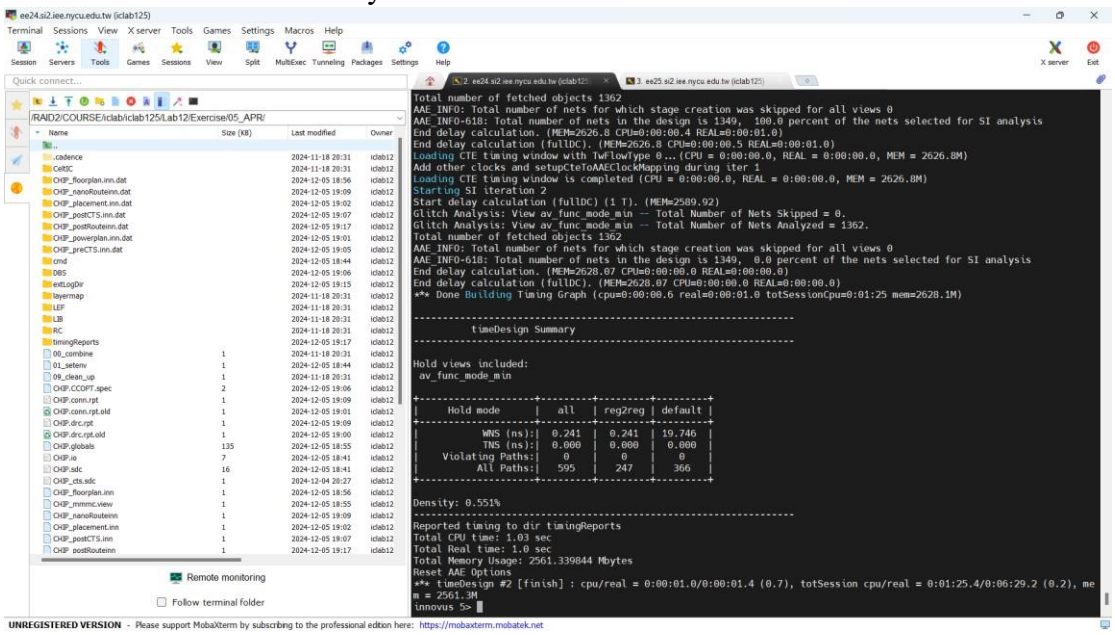
Bottom&Right



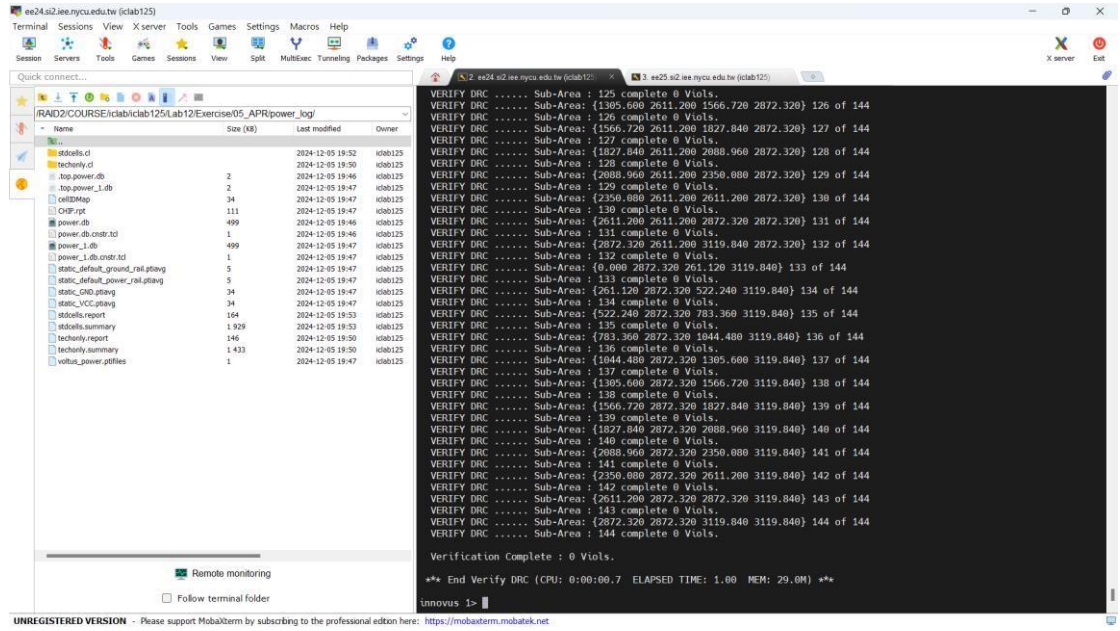
3.Post-Route setup time analysis



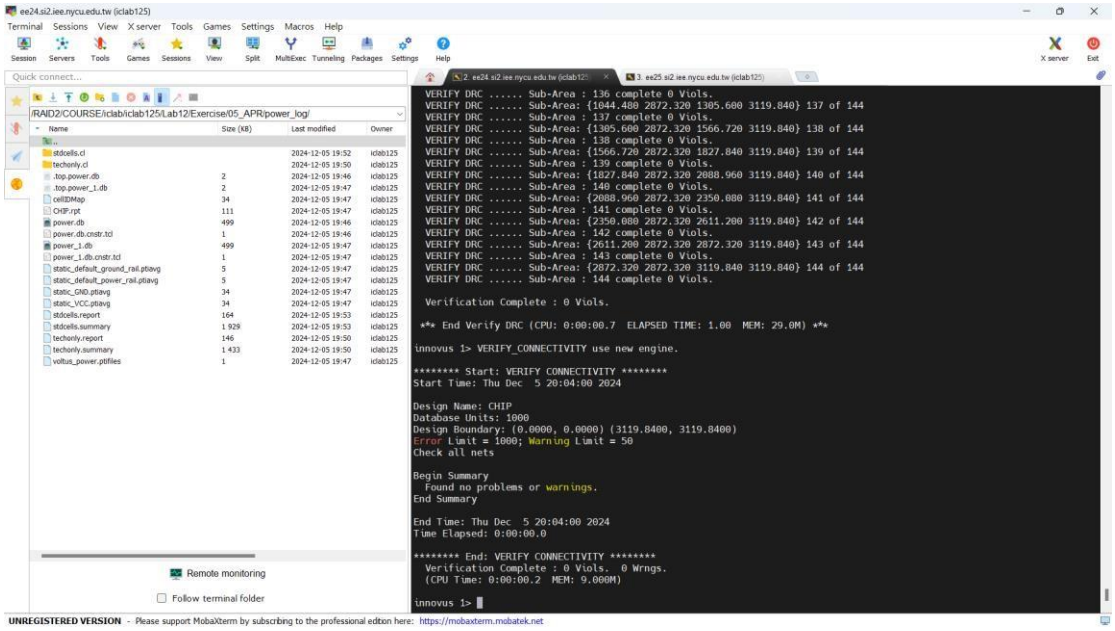
4. Post-Route hold time analysis



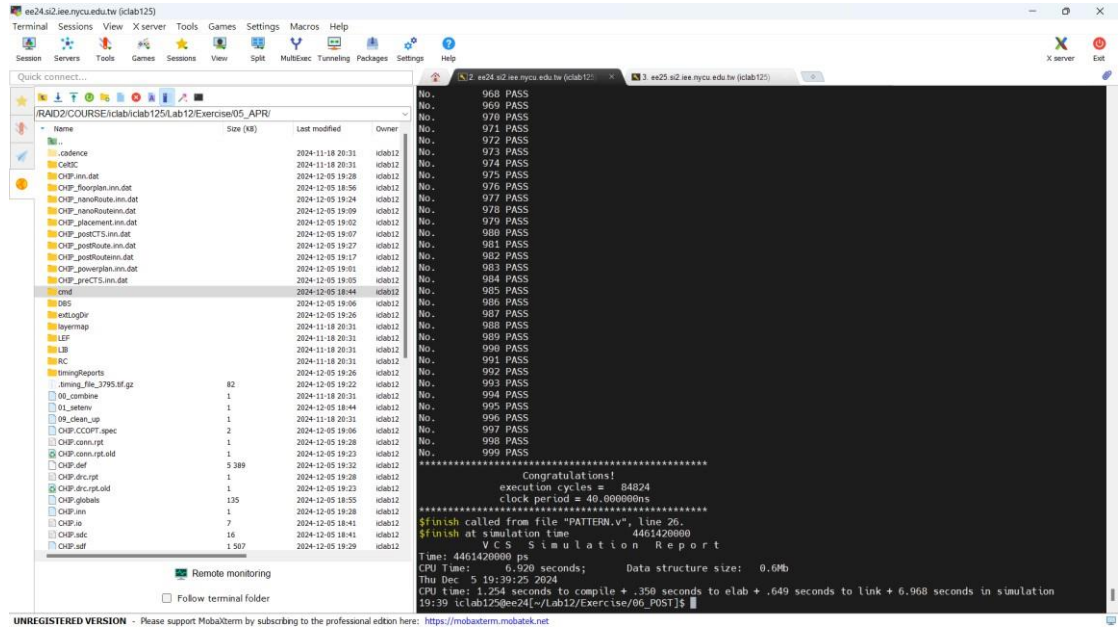
5.DRC result



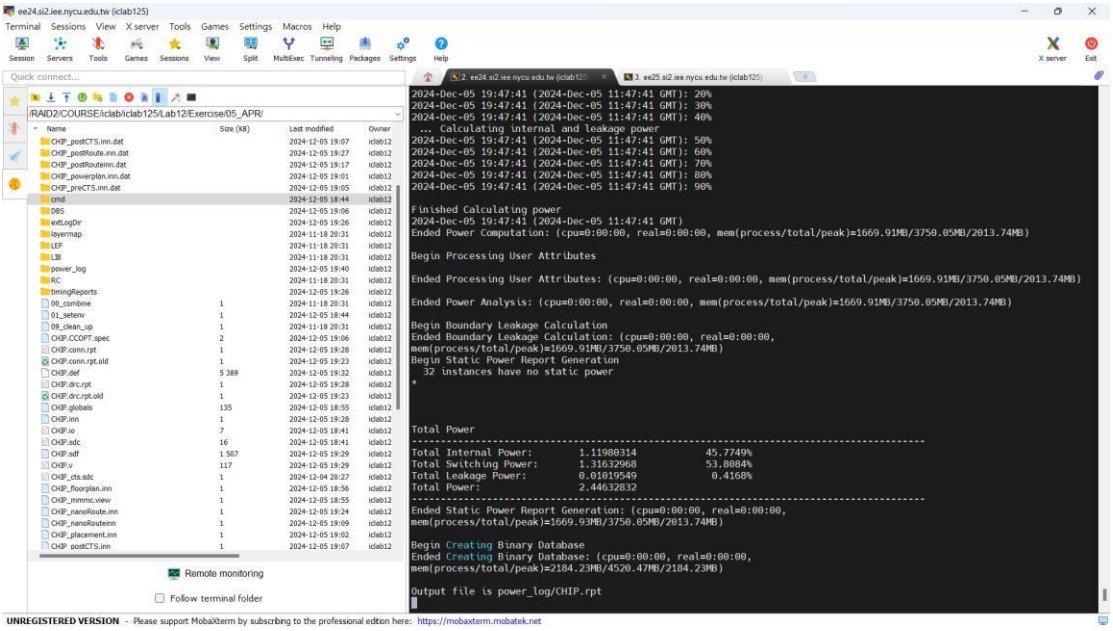
6.LVSResult



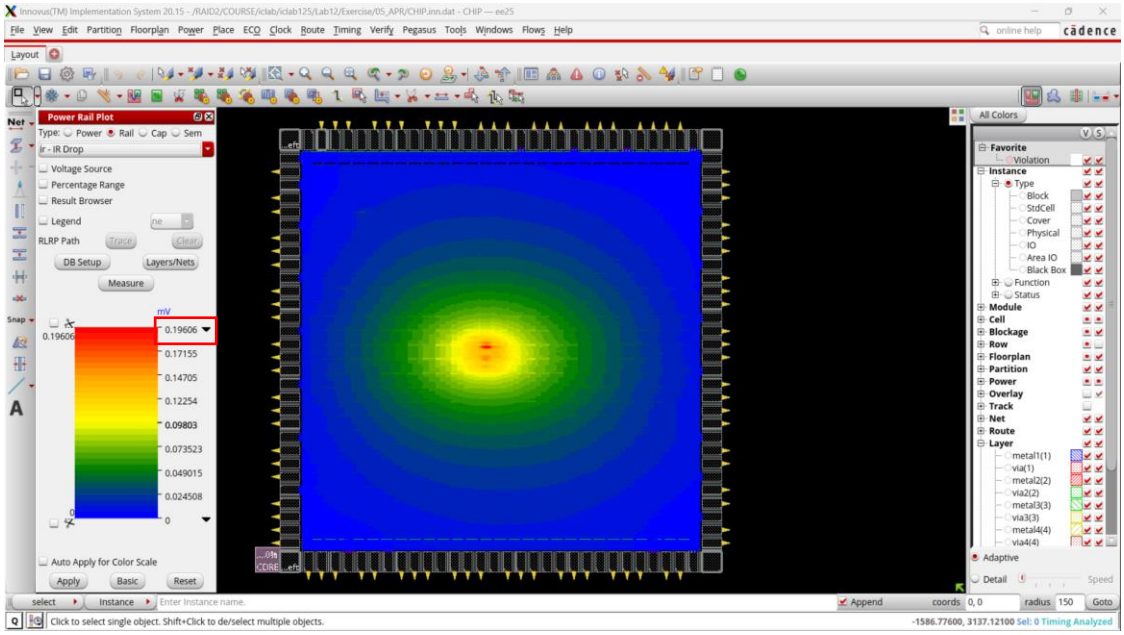
7.Post Layout simulation result

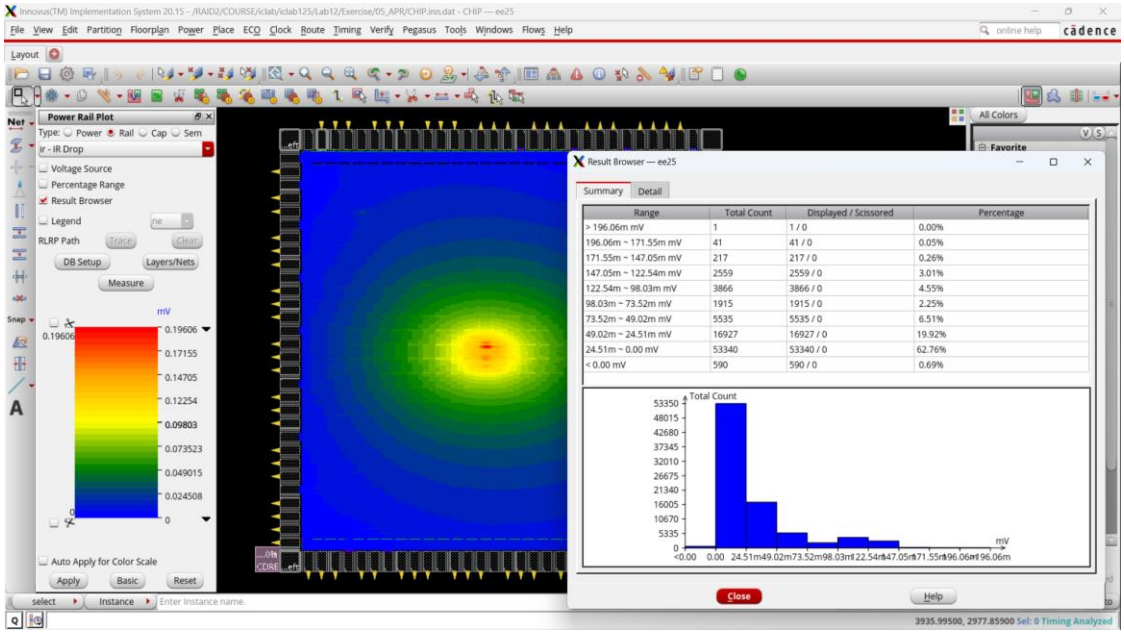


8.Power result



9.IR Drop result





降低 IR drop 的方法：

IR drop 是指電流流經步線網路造成的電壓損耗。我將 chip 設計為正方形，放置了 12 組 core power pads，平均分布在 chip 的四個邊，避免 power 走線過長。最終 IR drop 小於 0.2mV。