*Design Guide*

# Type 2BP UWB Module

## Hardware Design Guide - Rev. D

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# About This Document

This document provides details on how to design the schematic and layout for Type 2BP module, as well as perform ToF calibration and AoA PDOA calibration.

For Module specification refer to Type 2BP Datasheet.

# Audience & Purpose

This Application Note targets hardware developers, using Type 2BP module.

# Document Conventions

**Table 1** describes the document conventions.

**Table 1: Document Conventions**

| Conventions | Description |
|---|---|
|  | **Warning Note**<br>Indicates very important note. Users are strongly recommended to review. |
|  | **Info Note**<br>Intended for informational purposes. Users should review. |
|  | **Menu Reference**<br>Indicates menu navigation instructions.<br>**Example**: Insert➔Tables➔Quick Tables➔Save Selection to Gallery |
|  | **External Hyperlink**<br>This symbol indicates a hyperlink to an external document or website.<br>**Example**: Type 2BP Product Page<br>Click on the text to open the external link. |
|  | **Internal Hyperlink**<br>This symbol indicates a hyperlink within the document.<br>**Example**: Module Introduction<br>Click on the text to open the link. |
| `Console input/output or code snippet` | **Console I/O or Code Snippet**<br>This text ***Style*** denotes console input/output or a code snippet. |
| `# Console I/O comment`<br>`// Code snippet comment` | **Console I/O or Code Snippet Comment**<br>This text ***Style*** denotes a console input/output or code snippet comment.<br>• Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output.<br>• Code Snippet comment (preceded by "//") may exist in the original code. |

# 1 Module Introduction

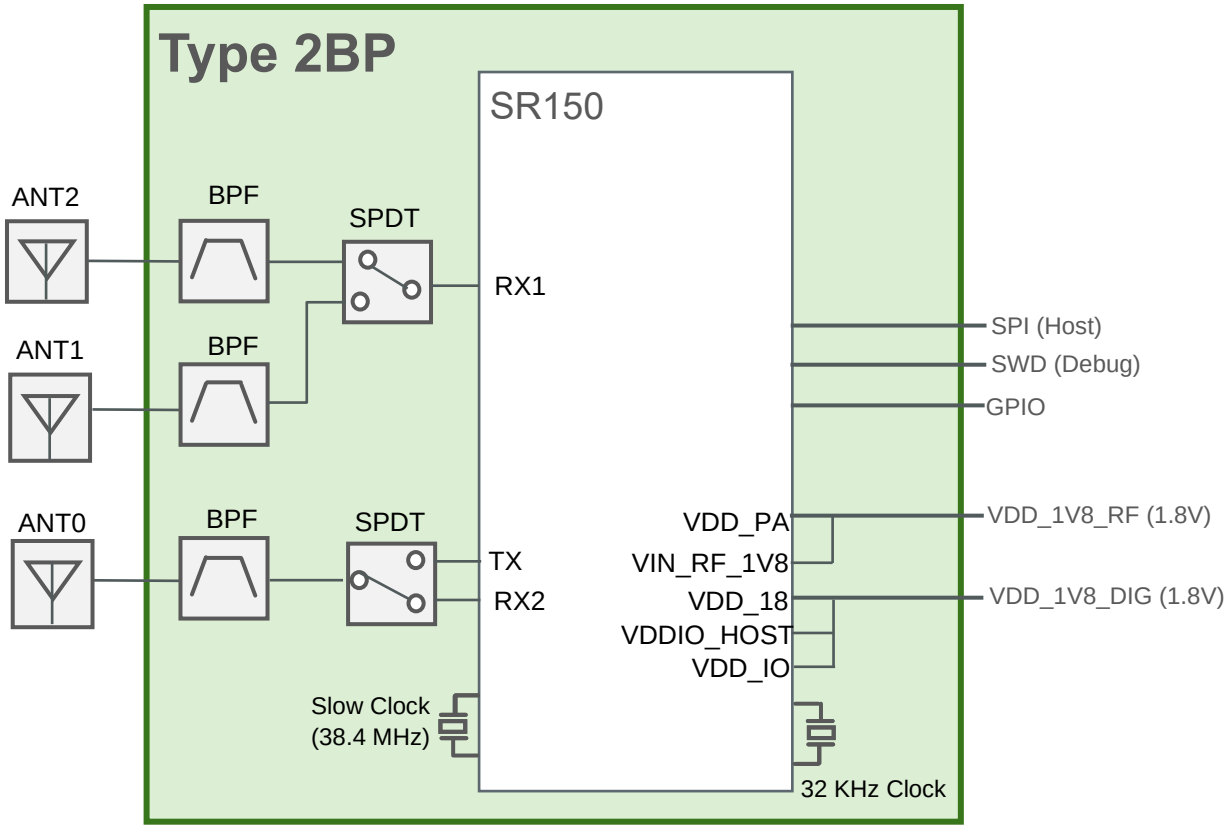
## 1.1 Type 2BP Introduction

- Main IC: NXP / SR150
- Compliant with IEEE802.15.4z HRP PHY
- Supports SHF UWB bands, Ch5 and 9.
- Supports 62.4MHz,124.8 MHz and 249.6 MHz PRF mode.
- Data rates of 6.81 Mbps, 7.8 Mbps, 27.2 Mbps and 31.2 Mbps.
- Complies with FCC&ETSI UWB spectral masks
- Supports 2-way ranging (DS-TWR) and one way ranging (TDoA)
- Supports 2D and 3D Angle of Arrival (AoA) measurement
- Surface mount type 6.6 x 5.8 mm (Typical), H = 1.2 mm (Maximum)

## 1.2 Block Diagram

**Figure 1** shows the block diagram.

**Figure 1: Module Internal Block Diagram**

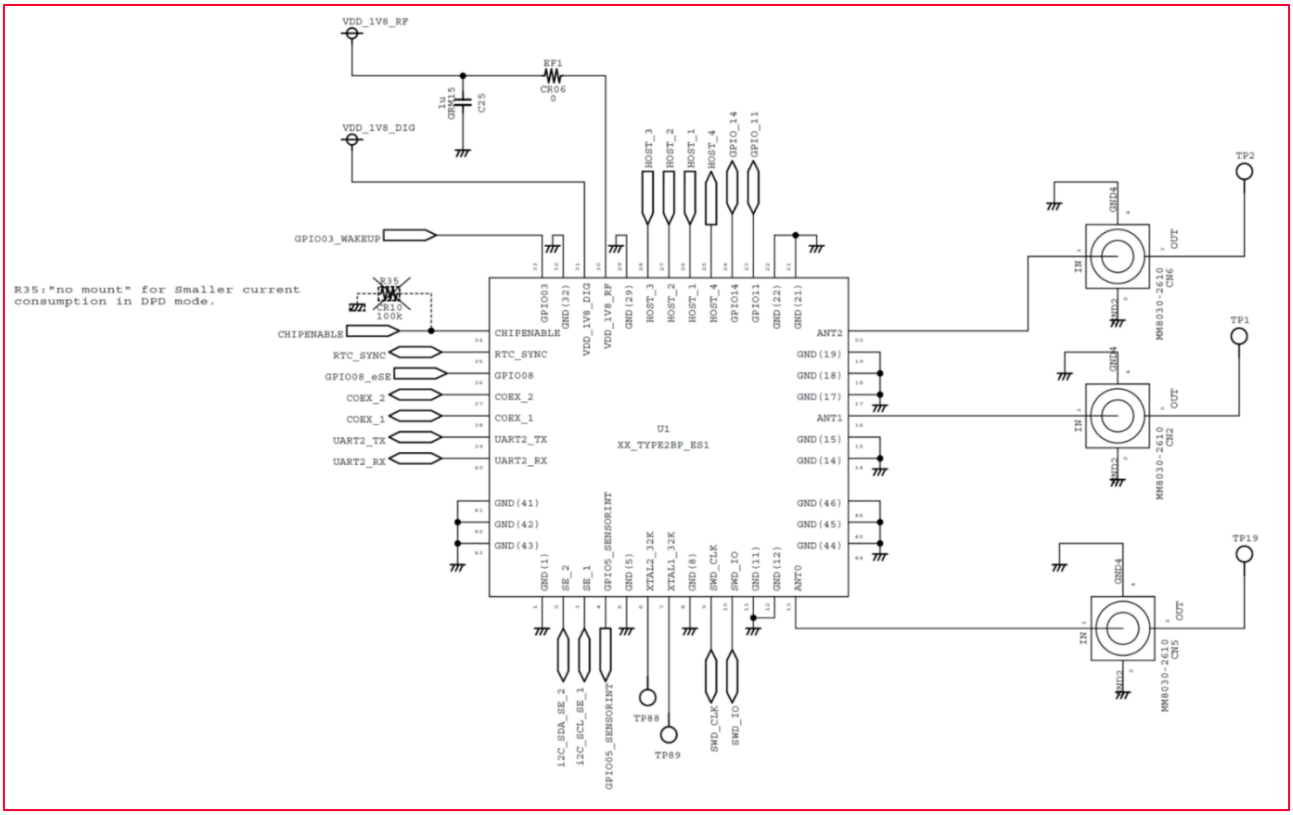


# 2 Circuit

## 2.1 Reference Schematic

**Figure 2** shows the reference circuit of Type 2BP module.

**Figure 2: Reference Circuit**




- C25, GRM155B31C105MA12 or higher value is recommended. Place as close to PIN30: VDD_1V8_RF as possible.
- EF1, 0Ω resistor is fine. But it is recommended to reserve a series component pad for Ferrite bead in case of any noise issue.
- R35, 100 kΩ pull down resistor might cause ~10 µA current consumption when the module is in DPD mode on SDK03.13.05. For power sensitive application, R35 can be removed.

On Murata EVK, RF switch connector PN is MM8030-2610.

Following Prove cables are recommended:

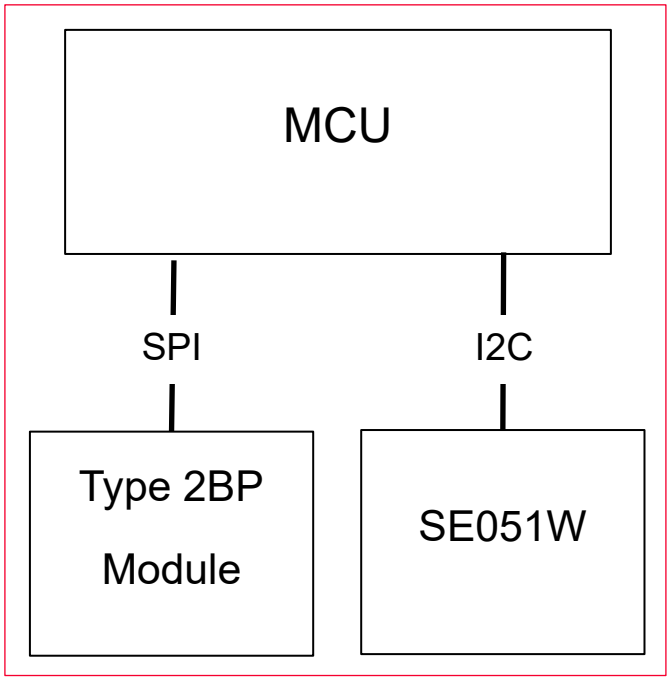
- MXHQ87WJ3000 (300 mm) or,
- MXHQ87WJ1000 (100 mm)

## 2.2 Secure Element Connection

In SR150 context, the secure element is not directly connected to the UWB chipset. MCU is doing the bridge and is handling the SE051W access. When secure element access is needed for UWB session, MCU communicates with SE051W and sends back the data to the UWB chipset.

**Figure 3** shows the SR150/SE051W system view.

**Figure 3: SR150/SE051W System View**




For the detail of SE051W, please contact NXP.

## 2.3 SR150 Interface

The connections described in **Table 2** are needed for communication between host and SR150 based UWB module via SPI bus. SR150 IO voltage is 1.8V, it may be required voltage level shift IC depend on host side voltage. Refer **Figure 4** and **Figure 5** for different I/O voltage examples.

**Table 2: HOST Connections**

| Module PIN Name | Functionality | HW Connection When Used | HW Connection When NOT Used |
|---|---|---|---|
| Host_1 | SCK (Serial input Clock) | HOST | Must be connected |
| Host_2 | NSS (Not Slave Select) | HOST | Must be connected |
| Host_3 | MOSI (Master Out Slave In) Data input. | HOST | Must be connected |
| Host_4 | MISO (Master In Slave Out) Data output. | HOST | Must be connected |
| GPIO05_SENSORINT | IRQ sent to the Host to let it know data are available for read. | HOST | Must be connected |
| CHIPENABLE | connection for the HOST to disable/enable the chip. | HOST | Must be connected |
| GPIO03_SYNC | SPI Rx Handshake from Host to SR150. | HOST | Must be connected |

**Figure 4** shows the interface connection for 1.8V MCU IO Voltage.

**Figure 4: Type 2BP Interface Connection - 1.8V MCU IO Voltage Case**

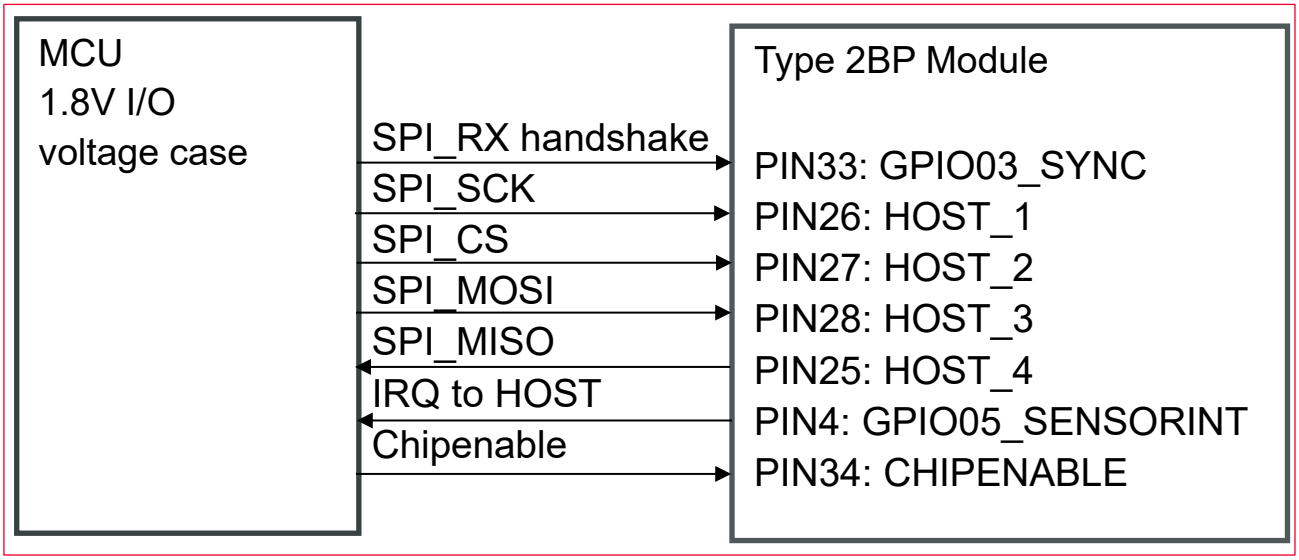
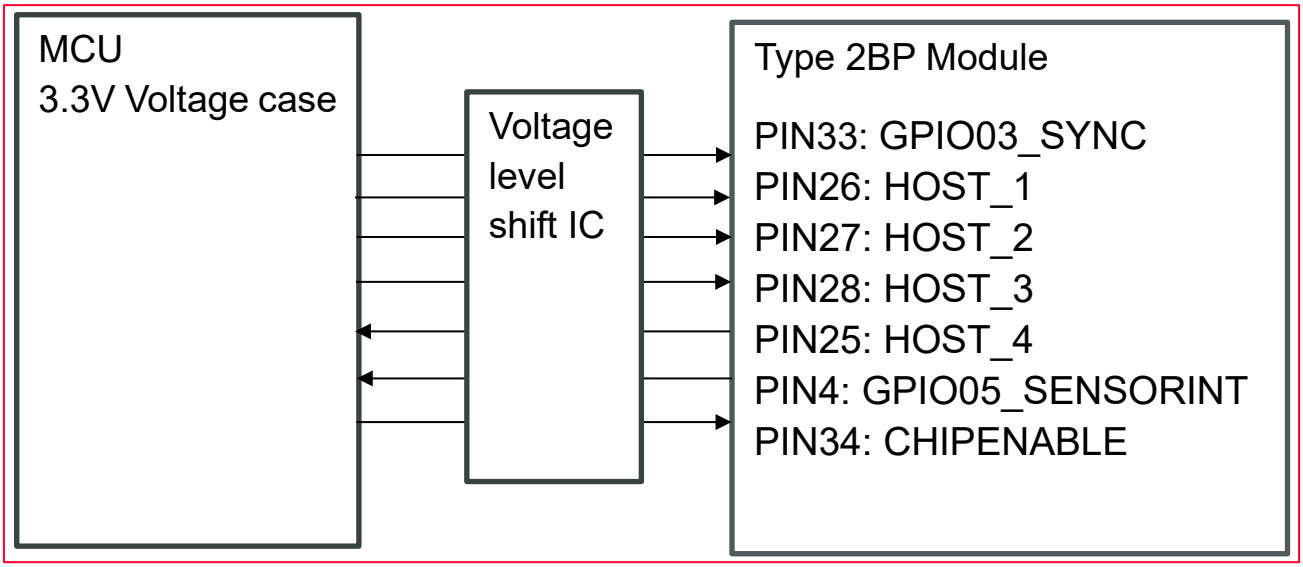



**Figure 5** shows the interface connection for 3.3V MCU IO voltage case.

**Figure 5: Type 2BP Interface Connection - 3.3V MCU IO Voltage Case**




# 3 Layout

## 3.1 RF Trace

RF trace line should be 50 Ω. There should be enough GND via along with Antenna line. RF matching components may be required depending on the Antenna. It is recommended to route same length for RF lines from module to 3 antennas.

For the details of Murata EVK Antenna, please refer to Antenna Design Guide and EVK Design file (brd/dxf file).

## 3.2 Power Line

It is recommended to have an additional 1 µF de-coupling capacitor as close to PIN 30: VDD_1V8_RF line as possible.

It is also recommended to have series 0 Ω resistor to reserve rand pattern in case any noise issue.

# 4 Tx Power, X'tal Calibration

Tx power and X'tal trim value are calibrated and stored to OTP (One-time programable) memory of SR150 chipset before the shipment from Murata's Module production factory. Please note that Tx power is calibrated to meet datasheet spec at Module antenna terminal. (calibrated at Module Bottom Pad).

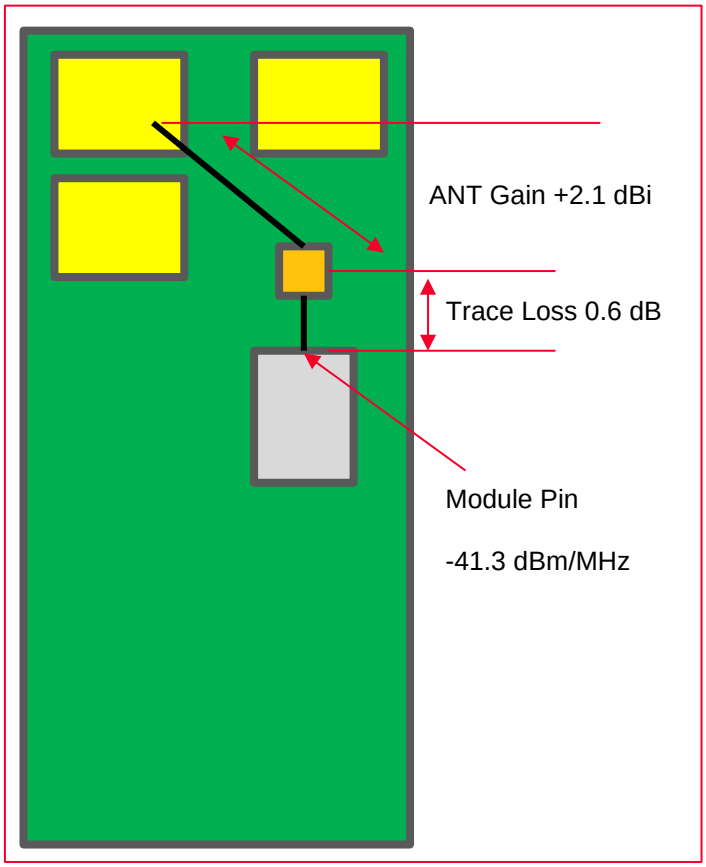
## 4.1 Tx Power

TX Power calibration value is stored in the OTP memory.

- Target TX Power is < -41.3 dBm/MHz at module pin at room temperature.
- Please apply your antenna gain and trace loss to set TX Power.
- Value in OTP + (antenna gain - trace loss + 0.5) x 4
- Example
  - Value in OTP: 30
  - Antenna gain: +2.1 dBi
  - Trace loss: 0.6 dB
  - 30 + (2.1 - 0.6 + 0.5) x 4 = 30 + (2) x 4 = 30 + 8 = 38

You can NOT increase TX Power even if your antenna gain is minus value.

**Figure 6: Example on Module EVK for Tx Power Concept**




# 5 Calibration on Final Product

To achieve good accuracy of distance measurement and AoA performance, calibration with final product is necessary. In this document, only an overview of calibration flow is available. Please refer to the document which is indicated as reference in this guide.

## 5.1 ToF (Antenna Delay) Calibration

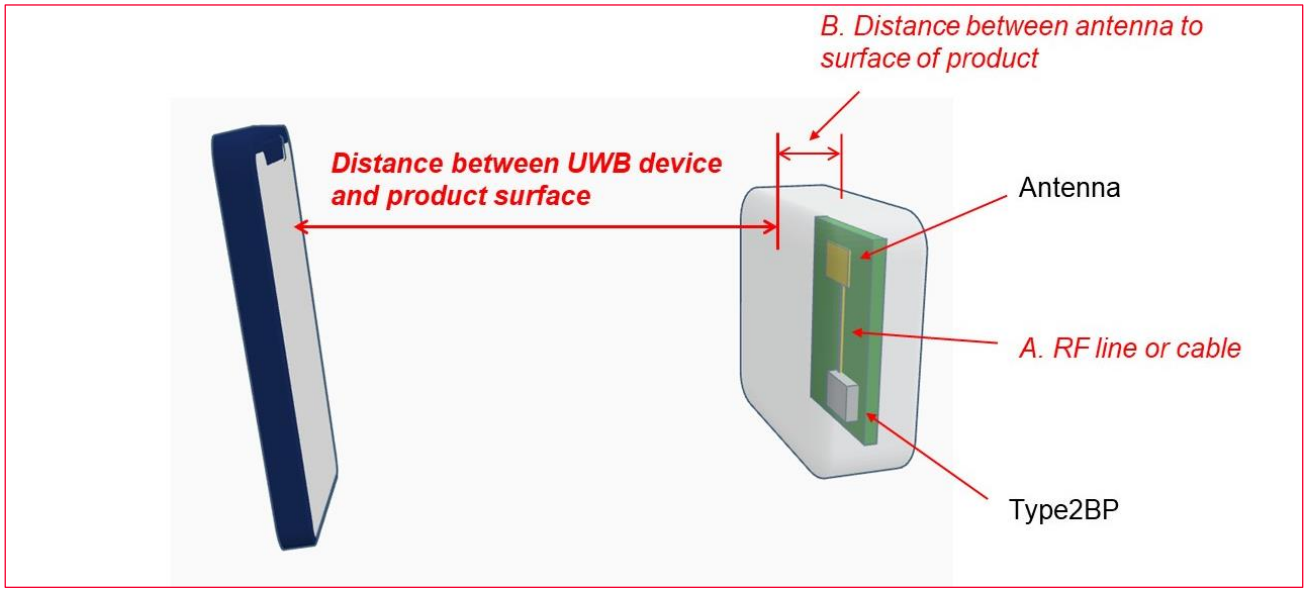
UWB ToF (Time of flight) ranging technology enabling “cm” range accuracy in LOS condition.

In FiRa standard, ±10 cm in LOS condition, 95% success rate are defined as reference ranging ability.

To have better accuracy of ranging distance as user experience, it is recommended to calibrate “distance between final product to product is accurate as user expected”.

An example is shown in **Figure 7**.

**Figure 7: Example of Distance Definition**

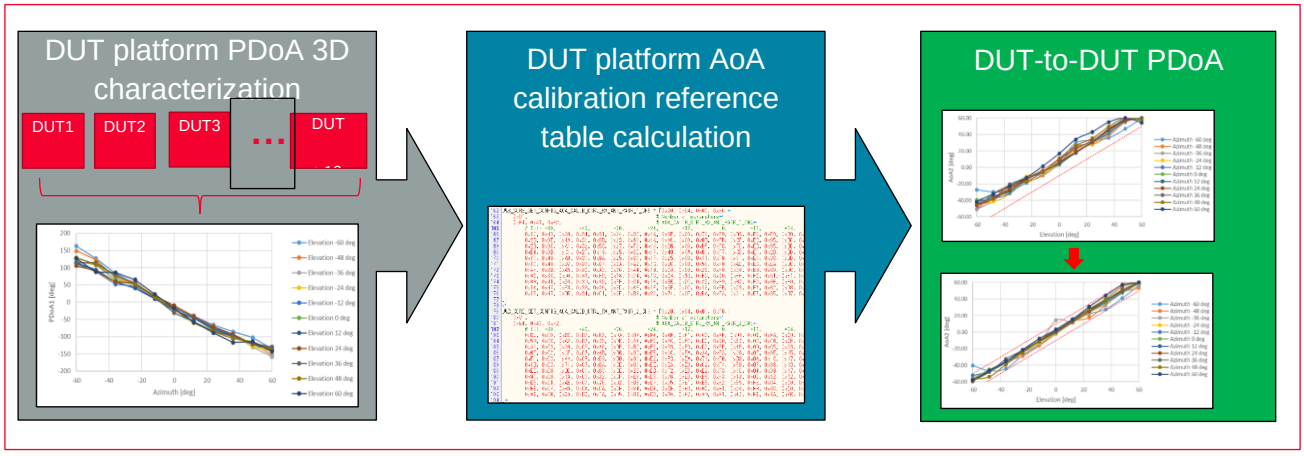



- For end user experience, it may be expected to output “measured distance” as “distance between UWB device and product surface”.
- In case, electrical length of A (RF line or cable) and B (Antenna to product surface) should be deducted by electrical length calibration. To do this calibration, please refer to ToF (Antenna delay) Calibration Guide.

## 5.2 3D PDoA, AoA Calibration

**Figure 8** shows 3 flows of 3D AoA calibration and DUT to DUT PDoA Calibration.

**Figure 8: 3D AoA, PDOA Calibration Flow**



### 5.2.1 PDoA 3D Characterization Measurement

Please refer to AoA Calibration Guide for the detailed process.

### 5.2.2 AoA Calibration Table Calculation

After you get PDoA data on the DUT (i.e. product), please share the result with Murata. Murata will ask NXP to generate an AoA calibration reference table send back to you.

### 5.2.3 Unit to Unit Variation Calibration for AoA Fine Tuning (Optional)

In general, AoA calibration table which was generated in Section 5.2.2 will work for all of product.

To achieve better AoA accuracy, there is an option to do individual AoA calibration with final product.

This is assumed to be performed in the test process of final product.

Please refer to Factory Calibration Guide for details.

# Revision History

| Revision | Date | Author | Change Description |
|---|---|---|---|
| A | Apr 4, 2022 | | Initial release |
| B | Oct 4, 2022 | | Updated for EVB Rev 4.0 design |
| C | May 11, 2023 | | Updated for EVB Rev 4.1 design |
| D | Mar 18, 2024 | | Document format changed |