RCLK00 EQU 01H ;RISING CLOCK SIGNAL FOR ALL

RCLK01 EQU 02H ;COUNTER WILL BE STORED IN

RCLK02 EQU 04H ;ONE BYTE LOCATION WE WILL

RCLK03 EQU 08H ;AND THAT LOCATION WITH RCLKxx

RCLK04 EQU 10H ;TO CHECK IF RISING EDGE IS

RCLK05 EQU 20H ;DETECTED AT CLK INPUT OF

RCLK06 EQU 40H ;COUNTER xx

RCLK07 EQU 80H

CTR\_HANDLER:

MOV A,CTR\_PREV\_CLK

MOV CTR\_PREV\_CLK,CTR\_CLK

CPL A

ANL A,CTR\_CLK

MOV R7,A ; STORE RISING CLOCK PULSES IN R7

CT00\_CHK:

MOV A,CTR\_RESET

JNB CT00R,CT00\_UPDATE

CLR A

MOV DPTR,#CTC00H

MOVX @DPTR,A

INC DPTR

MOVX @DPTR,A

MOV A,CTR\_DONE

CLR CT00D

MOV CTR\_DONE,A

SJMP CT01\_CHK

CT00\_UPDATE:

MOV A,CTR\_DONE

JB CT00D,CT01\_CHK

MOV A,R7

ANL A,#RCLK00

JZ CT01\_CHK

MOV DPTR,#CTC00L

MOVX A,@DPTR

ADD A,#01H

MOVX @DPTR,A

MOV DPTR,#CTC00H

MOVX A,@DPTR

ADDC A,#00H

MOVX @DPTR,A

CT00\_DONE:

MOV DPTR,#CTS00L

MOVX A,@DPTR

MOV R1,A

MOV DPTR,#CTC00L

MOVX A,@DPTR

CLR C

SUBB A,R1

MOV DPTR,#CTS00H

MOVX A,@DPTR

MOV R1,A

MOV DPTR,#CTC00H

MOVX A,@DPTR

SUBB A,R1

JC CT01\_CHK

MOV A,CTR\_DONE

SETB CT00D

MOV CTR\_DONE,A