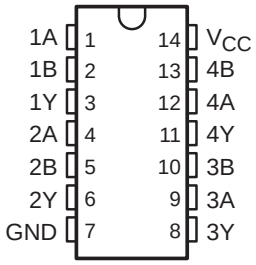
SN54HCT32, SN74HCT32
QUADRUPLE 2-INPUT POSITIVE-OR GATES

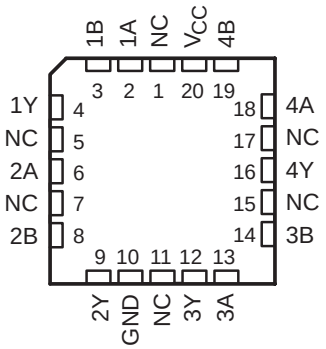
SCLS064E – NOVEMBER 1988 – REVISED AUGUST 2003

- **Operating Voltage Range of 4.5 V to 5.5 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I_{CC}**
- **Typical t_{pd} = 13 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Inputs Are TTL-Voltage Compatible**

SN54HCT32 . . . J OR W PACKAGE
SN74HCT32 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HCT32 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HCT32 devices contain four independent 2-input OR gates. They perform the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = A + B$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HCT32N	SN74HCT32N
	SOIC – D	Tube of 50	SN74HCT32D	HCT32
		Reel of 2500	SN74HCT32DR	
		Reel of 250	SN74HCT32DT	
	SOP – NS	Reel of 2000	SN74HCT32NSR	HCT32
	SSOP – DB	Reel of 2000	SN74HCT32DBR	HT32
	TSSOP – PW	Tube of 90	SN74HCT32PW	HT32
		Reel of 2000	SN74HCT32PWR	
		Reel of 250	SN74HCT32PWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HCT32J	SNJ54HCT32J
	CFP – W	Tube of 150	SNJ54HCT32W	SNJ54HCT32W
	LCCC – FK	Tube of 55	SNJ54HCT32FK	SNJ54HCT32FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	**B**	**Y**
H	X	H
X	H	H
L	L	L

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HCT32			SN74HCT32			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8			0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time				500			500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT32		SN74HCT32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –4 mA		3.98	4.3		3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA			0.17	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		5.5 V			2		40		20	µA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

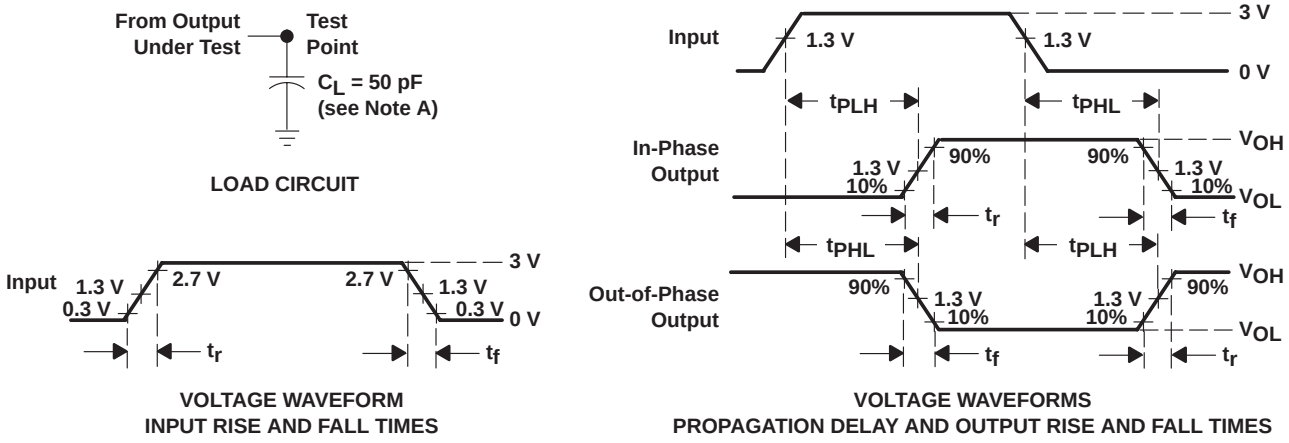
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT32		SN74HCT32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V		15	24		35		30	ns
			5.5 V		13	22		32		27	
t_t		Y	4.5 V		9	15		22		19	ns
			5.5 V		8	14		20		17	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms