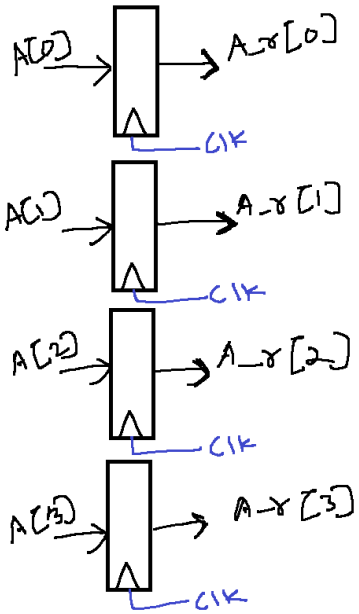
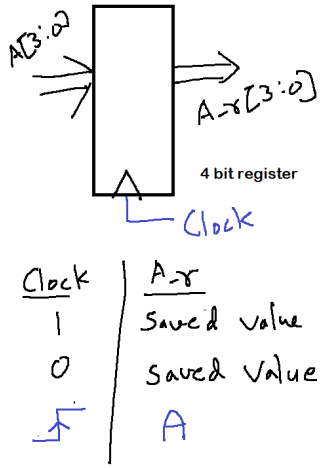
Register





- An example of a 4 **bit positive edge triggered** register

The default register type **for this course**

- A register is simply a bundle of individual D flip flops(of the same edge type)
- In this example, I have an input 4-bit bus A(with individual bits A[3],A[2],A[1],A[0])
- At the output of register, we have signal A_r
- As seen in the truth table, when clock transitions 0->1 (positive edge), A_r samples A. Else it holds previously captured value of A(keep state)
- In **Digital**, besides Clock signal(C), you have enalble en signal. When en=1, the truth table here applies. Else if en=0**, A_r keeps on holding state.**