Project Proposal - All Digital PLL Synchronizer

ECE298A - TinyTapeout Project

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1. **Project Overview**
    a. What is a digital PLL Synchronizer?
        - A digital PLL (Phase Locked Loop) synchronizer is a clock that aligns the phase of a clock with a reference clock.
        - Theyre often used in communication receivers and (our application) chip deskewing

    b. Usefulness?
        - This will ensure on chip timing is reliable
        - Can be fabbed as a reusable IP block

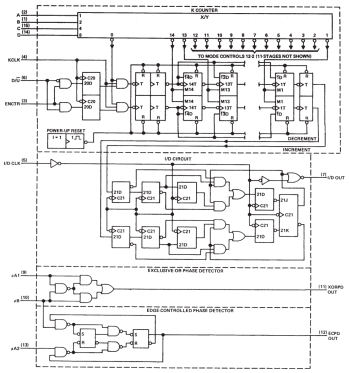
2. **Objectives**
    a. Implement first order digital PLL Synchronizer using Verilog

    b. Verify functionality with CocoTB python scripts

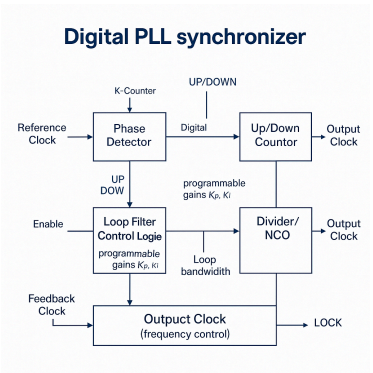
    c. Synthesize for TinyTapeout

    d. Demonstrate created PLL can lock onto a reference signal, maintain phase alignment, read fuzzy signals and produced realigned phases

3. **Block Diagram**



[1]



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4. **Project Timeline**
    a. *Week 3 (Sept 17):* Built/tested counter in Verilog.

    b. *Week 4 (Sept 24):* Proposal submitted; counter working.

    c. *Weeks 5–6 (Oct 1–8):* Implement and test phase detector + divider.

    d. *Week 8 (Oct 22):* Sub-block evaluation.

    e. *Weeks 9–10 (Oct 29–Nov 5):* Full PLL integration, synthesis with OpenLane.

    f. *Week 11 (Nov 12):* System integration milestone.

g. *Weeks 12–13 (Nov 19–26):* Final verification + documentation.

h. *Dec 3:* Submission.

5. **Design Details**
   a. *Counter:* Up/Down counter coded in Verilog and tested with CocoTB - Done

   b. *Phase Detector:* Output Up/Down pulses depending on lead/lag of input

   c. *Loop filter:* Accumulates corrections to smooth jitter of incoming signal

   d. *Divider/NCO:* Generates controlled clock output

   e. *Lock detector:* Monitors stable phase alignment

6. **Tools and Verification**
   a. *Coding:* Verilog will be used (Synthesizeable to TinyTapeout)

   b. *Verification:* CocoTB testbenches in Python

   c. *Synthesis & Layout:* OpenLane

   d. *Version control:* Github actions for CI

7. **Expected Outcome**
   a. A working PLL synchronizer block fitting within 1 TinyTapeout file

   b. *Demo:* PLL locks onto a reference clock in simulation

   c. Ready for Fab via TinyTapeout

8. **References**

[1] Texas Instruments, *SN54/74LS297 Digital Phase-Locked-Loop Filters Datasheet*, SDLS155, Rev. March 1988. [Online]. Available: https://www.ti.com/lit/ds/symlink/sn74ls297.pdf

[2] Texas Instruments, *Digital Phase-Locked Loop Design Using SN54/74LS297*, Application Report SDLA005B, Mar. 1997. [Online]. Available: https://www.ti.com/lit/an/sdla005b/sdla005b.pdf

[3] Artificially generated image by ChatGPT after receiving the following prompt: “Can you create a low-level block diagram of a digital PLL synchronizer that is to be made on a tile, on a chip”