ASCII CODE

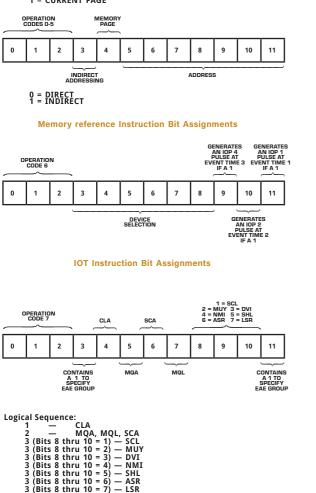
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EAE Microinstruction Bit Assignments

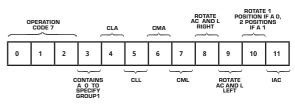
Character	Code	Characte	Code
A B C D E F G H I J K L M N O P Q R S T U V W X Y Z O 1 2 3 4 5 6 7 8 9	301 302 303 304 305 306 307 310 311 312 313 314 315 316 317 320 321 322 323 324 325 326 327 330 331 331 342 325 326 327 330 321 322 323 324 325 326 327 330 327 330 327 330 321 322 323 324 325 326 327 330 327 330 327 330 327 330 321 322 323 324 325 326 327 330 327 328 329 320 327 330 327 328 329 320 327 330 327 330 327 328 329 320 321 320 327 327 330 327 328 329 320 327 327 328 329 320 320 327 327 327 327 327 327 327 327	! " # \$ % & . ()) * + , / / / / / / / / / / / / / / / / / /	215 240 DE 375
	Rim Loader Low Speed)	Rim Loade (High Speed	
7756. 7757. 7760. 7761. 7763. 7763. 7764. 7765. 7766. 7767. 7770. 7771. 7772.	6031 5357 6036 7106 7006 7510 5357 7006 6031 5367 6034 7420 3776	7756/ 60 7757/ 60 7750/ 53 7761/ 60 7762/ 711 7763/ 70 7764/ 75 7766/ 70 77770/ 50 7771/ 60 7771/ 60 7771/ 40 7771/ 744 7771/ 33 7771/ 35	11 57 57 66 66 60 67 74 67 67 67 76 76



Mnemoni	c Code	Operation	Time (µsec.
		BASIC INSTRUCTIONS	
AND TAD ISZ DCA JMS JMP IOT OPR	0000 1000 2000 3000 4000 5000 6000 7000	logical AND 2's complement add increment and skip if zero deposit and clear AC jump to subroutine jump in/out transfer operate	3 3 3 3 1.5 4.25 1.5
GROUP	1 OPEF	RATE MICROINSTRUCTIONS	(1 CYCLE)
NOP CLA CLL CMA CML RAR RAL RTR RTL	7000 7200 7100 7040 7020 7010 7004 7012 7006 7001	no operation clear AC clear link complement AC complement link rotate AC and link right one rotate AC and link left one rotate AC and link left wo rotate AC and link left two increment AC	Sequence 1 1 2 2 4 4 4 4 3
GROUP	2 OPE	RATE MICROINSTRUCTIONS	(1 CYCLE)
SMA SZA SPA SNA SNL SZL SKP OSR HLT CLA	7500 7440 7510 7450 7420 7430 7410 7404 7402 7600	skip on minus AC skip on zero AC skip on plus AC skip on non zero AC skip on non-zero link skip on zero link skip on zero link skip unconditionally inclusive OR, switch register whalts the program clear AC	Sequence 1 1 1 1 1 1 1 with AC 3 3

	COMBI	NED OPERATE MICROINSTF	RUCTIONS	Mnemo	onic Code	Operation	Time (µsec.)
CIA	7041	samulament and insumment A	Sequence C 2, 3	TELETYPE KEYBOARD/READER			
LAS	7604	complement and increment A load AC with switch registe	r 2, 3	KSF	6031	skip if keyboard/reader flag = 1	4.25
STL GLK	7120 7204	set link (to 1) get link (put link in AC bit	1, 2	ксс	6032	clear AC and keyboard/reader flag	4.25
CLA CLL	7201	clear AC and link set AC = 1	1 1, 3	KRS	6034	read keyboard/reader buffer, static	4.25
CLA CMA CLL RAR CLL RAL CLL RTL	7110 7104 7106	set AC = — 1 shift positive number one r shift positive number one I clear link, rotate 2 left	eft 1, 4 1, 4	KRB	6036	Clear AC, read keyboard buffer clear keyboard flag	4.25
CLL RTR SZA CLA	7640	clear link, rotate 2 right skip if AC = 0, then clear AC			TE	ELETYPE TELEPRINTER/PUNCH	
SZA SNL SNA CLA		skip if AC = 0, or link is 1, o skip if AC ≠ 0, then clear AC	1, 2	TSF	6041	skip if teleprinter/punch flag = 1	4.25
SMA CLA		skip if $AC < 0$, then clear AC		TCF	6042	clear teleprinter/punch flag	4.25
SMA SZA SMA SNL	7520	skip if AC ≤ 0 skip if AC < 0 or line is 1, or		TPC	6044	load teleprinter/punch buffer, select and punch	4.25
SPA SNA SPA SZL SPA CLA SNA SZL	7530 7710	skip if AC > 0 skip if AC ≥ 0 and if the link skip if AC ≥ 0, then clear AC skip if AC ≠ 0 and link = 0		TLS	6046	load teleprinter/punch buffer, select and punch, and clear teleprinter/punch flag	4.25
0.0022	•		-	HIGH	SPEED	PERFORATED TAPE READER 1	YPE PR8/I
Mnemo	nic Code	e Operation	Time (µsec.)	RSF	6011	skip if reader flag = 1	4.25
mileino		MICROINSTRUCTIONS TYPE	-	RRB	6012	read reader buffer, and clear flag	4.25
				RFC	6014	clear flag and buffer and	4.25
DVI NMI	7407 7411	divide normalize	5.2 — 7.8			fetch character	
SHL	7411	shift left	1.5 + 0.25n				
ASR LSR	7415 7417	arithmetic shift right logical shift right	3.0 + 0.25n 3.0 + 0.25n 3.0 + 0.25n	HIGH	H SPEED	PERFORATED TAPE PUNCH T	YPE PP8/I
MQL	7421	load AC into MQ, clear AC	3.0 + 0.25n 1.5	PSF	6021	skip if punch flag = 1	4.25
MUY	7405	multiply	4.8 — 7.2	PCF	6022	clear flag and buffer	4.25
MQA CAM SCA	7501 7621 7441	inclusive OR, MQ with AC clear AC and MQ read SC into AC	1.5 1.5	PPC	6024	load buffer, and punch character	4.25
CLA SCL	7601 7403	clear AC load the step counter	1.5 1.5 3.0	PLS	6026	clear flag and buffer; load and punch	4.25
					DECTAP	E AND CONTROL TYPE TU56/	TC08
		IOT MICROINSTRUCTIONS					
		io i miorionio morno		DTRA	6761	read status register A	4.25
		PROGRAM INTERRUPT		DTCA	6762	clear status register A	4.25
				DTXA DTSF	6764 6771	load status register A	4.25 4.25
ION	6001	turn interrupt on	1.5	DTRB	6772	skip on flags read status register B	4.25
IOF	6001	turn interrupt off	1.5	DTLB	6774	load status register B	4.25
	EX	TENDED MEMORY TYPE N	IC8/I		RANDO	M ACCESS DISC FILE TYPE D	F32D
CDF	62n1 62n2	change to data field n	1.5 1.5	DCMA	6601	clear disk memory	4.25
CIF RDF RIF	62n4 6224	change to instruction field n read data field into AC 6-8 read instruction field into AC	1.5	DMAR	6603	address register, & disk flags load disk memory address register & read	4.25
RMF RIB	6244 6234	restore memory field read interrupt buffer	1.5 1.5	DMAW	6605	load disk memory address register and write	4.25

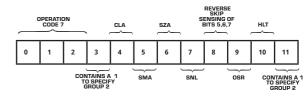
DCEA	6611	clear disk extended address register and memory address extension	4.25
DSAC	6612	skip on address confirmed flag	4.25
DEAL	6615	load disk extended address and memory address extension	4.25
DEAC	6616	read disk extended address register	4.25
DFSE	6621	skip on zero error flag	4.25
DFSC	6622	skip on data completion flag	4.25
DMAC	6626	read disk memory address register	4.25



- Logical Sequences: 1 CLA, CLL 2 CMA, CML

 - 3 IAC 4 RAR. RAL, RTR, RTL

Group 1 Operate Instruction Bit Assignments



Logical Sequences:

- 1 (Bit 8 is Zero) Either SMA or SZA or SNL 1 (Bit 8 is Zero) Both SMA and SZA and SNL
 - 2 CLA 3 — OSR. HLT

Group 2 Operate Instruction Bit Assignments