EESM6000C SoC Lab

FIR Filter Design and Verification Report

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1. Introduction

This report documents the design and verification process of a Finite Impulse Response (FIR) filter. The FIR filter is a crucial digital signal processing component, and its implementation involves multiple steps, including the design of the compute engine, addition of AXI bus interfaces, development of a testbench, and optimization for robustness and performance.

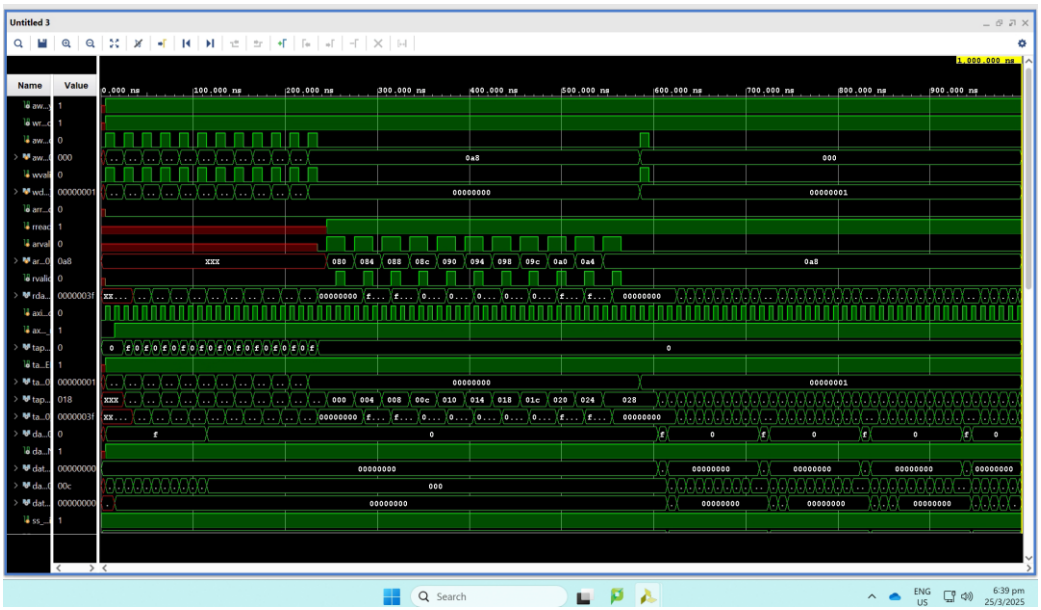
2. Design Specification

- Data Width: 32-bit integer.
- Tap Number: 11.
- Data Number: To be determined based on the size of the data file.
- Interfaces:
  - AXI-Lite: For configuration data.
  - AXI-Stream: For input stream (Xn) and output stream (Yn).
- Computational Resources:
  - Utilize one multiplier and one adder, with multiplication and addition running in separate pipeline cycles.
  - Do not use DSP, adhering to the Xilinx directive (use_dsp = "no").
  - Implement shift registers with SRAM (Shift_RAM, size = 10 DW).
  - Implement tap coefficients with SRAM (Tap_RAM = 11 DW), initialized by AXI-Lite write.

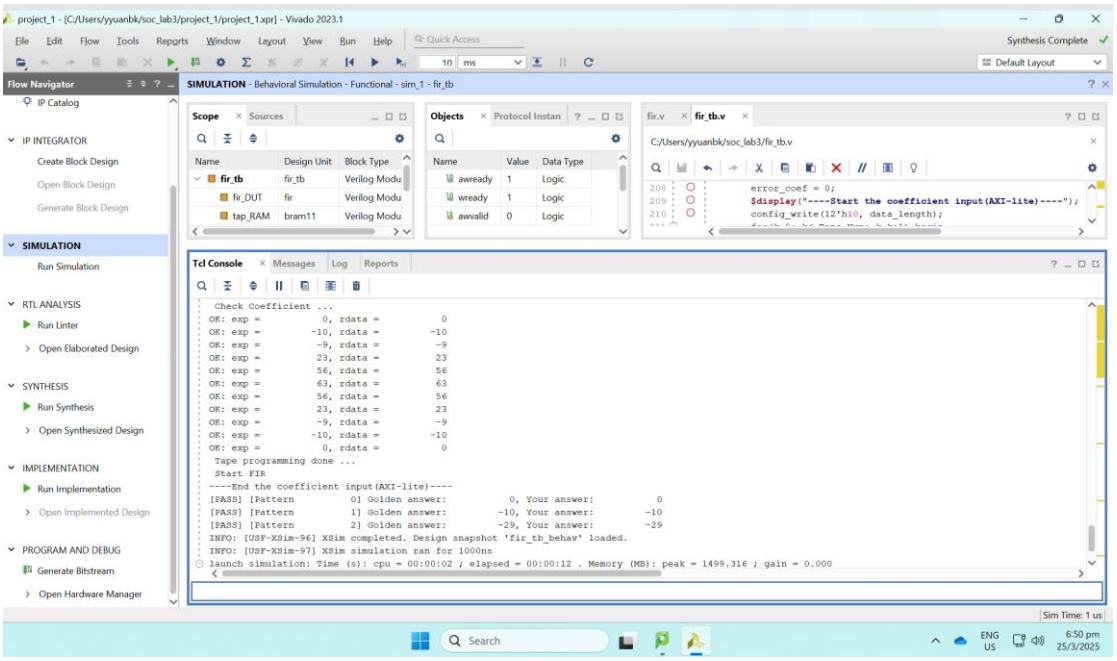
3. Verification

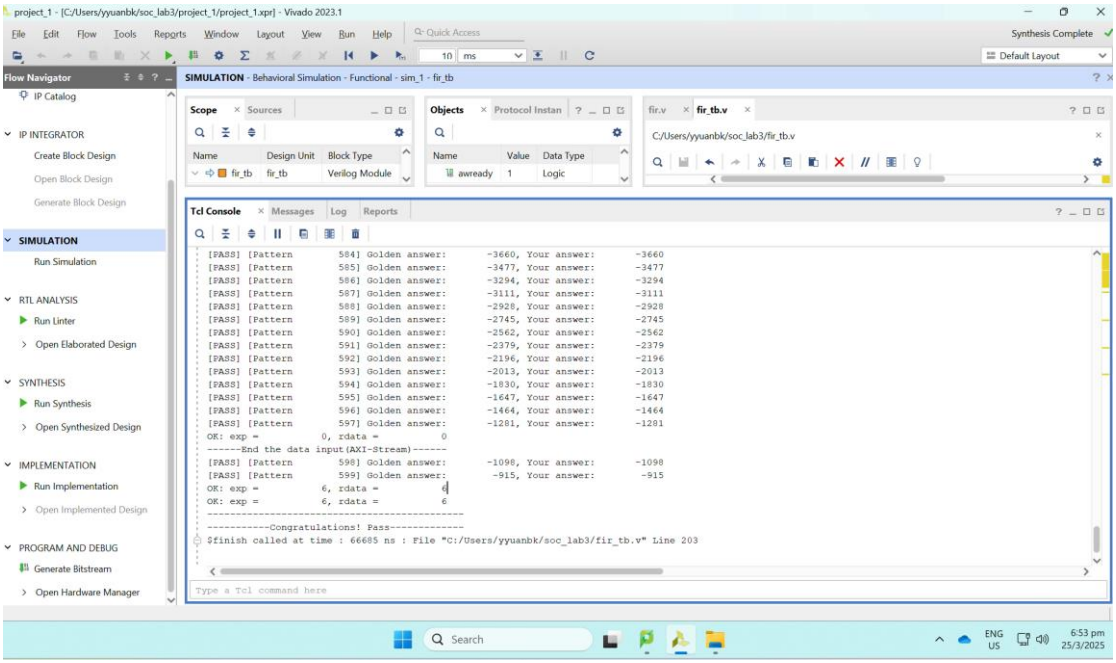
The testbench is designed to simulate the FIR filter's operation using the provided test dataset (samples_triangular_wave.dat for input and out_gold.dat for expected output). It performs multiple iterations of the test sequence, ensuring consistent and accurate results. The testbench includes mechanisms to compare the generated Yn output with the golden data, and report any discrepancies.

- Simulation Results:
  - The simulation waveform captures key signals, including configuration writes, ap_start, ap_done, Xn stream-in, and Yn stream-out.



- The results demonstrate the correct functionality of the FIR filter, with accurate data processing and proper handling of AXI protocols.





4. Conclusion

This report presents the comprehensive design and verification of an FIR filter, adhering to the provided specifications and utilizing AXI interfaces for efficient data management. The testbench effectively validates the design's functionality, and performance metrics offers valuable insights for further optimization. Future work may focus on implementing the suggested improvements to enhance the design's robustness and speed, ultimately leading to a more efficient and reliable FIR filter solution.