## 计算机组成原理与系统结构

## 第七章作业

1. A DMA module is transferring characters to memory using cycle stealing, from a device transmitting at 9600 bps. The processor is fetching instructions at the rate of 1 million instructions per second (1 MIPS). By how much will the processor be slowed down due to the DMA activity? (默认字长为1B)

**设备传输率为9600b/s；**

**周期窃取方式处理一个字节数据需要窃取一个总线周期，故**

**1s内，需要窃取9600/8 = 1200次总线周期；**

**处理器以1 MIPS的速度获取指令，由于窃取，速度会减慢1200 IPS，**

**或 1200 IPS / 1 MIPS = 0.12%**

1. A 32-bit computer has two selector channels and one multiplexor channel. Each selector channel supports two magnetic disk and two magnetic tape units. The multiplexor channel has two line printers, two card readers, and 10 VDT terminals connected to it. Assume the following transfer rates:

Disk drive           800KB/s

Magnetic tape drive  200KB/s

Line printer          6.6KB/s

Card reader          1.2KB/s

VDT                 1KB/s

Estimate the maxium aggregate I/O transfer rate in this system.

**虽然选择通道能连接多个设备，但在某一时间只能选择一台设备传输数据。故两个选择通道均连接到磁盘时，I/O速率最大；**

**多路转换通道可以同时与两个打印机、两个卡片读取器、十个VDT通信，故最大总I/O传输速率为**

**2 \* 800KB/s + 2 \* 6.6KB/s + 2 \* 1.2KB/s + 10 \* 1KB/s = 1625.6 KB/s**

1. Assume some I/O device send information to CPU with the maximum frequency of 4000 times per second, while the executing time of the corresponding interrupt handler routine is 40μs. Can this I/O device adopt Interrupt driven mode to work? And why?

**I/O设备发送数据的最大频率是4000次/秒，因此**

**最小平均数据发送间隔为 1 / 4000 = 0.25 ms = 250 μs**

**而中断处理时间是40μs，40μs < 250μs，可以采用中断驱动方式工作。**

1. Assume that a disk uses 32-bit word as the data transmission unit with transferring rate of 1MB/s, and CPU clock cycles is 50MHz. Please answer the following questions:
2. In programmed mode, suppose that it takes 100 clock cycles to finish required operation. Please calculate the ratio of time that CPU uses for I/O inquiring (assume that there is enough inquiring operation to avoid data loss).
3. In Interrupt driven mode, the time consumption (including handling interrupt) for each transferring process is 80 clock cycles. Please calculate the ratio of time that CPU takes for data transferring of disk.
4. In DMA mode, assume that it takes 1000 clock cycles to start DMA, and 500 clock cycles to post-process when the DMA finished. If the length of the average transmission data is 4 KB, how much is the ratio of time that CPU use to finish I/O operation when disk working？Ignore the bus-request time of DMA.
5. **字传输速率 1 MB/s / 32bits = 256K words/s；**

**CPU进行I/O等待的100个时钟周期内**

**传输的字 256K words/s \* 100 / 50MHz = 0.5 words**

**因此I/O时间比例为 50%。**

1. **80个时钟周期内传输的字 256K words/s \* 80 / 50MHz = 0.4 words**

**因此I/O时间比例为 40%。**

1. **块传输速率 1 MB/s / 4KB = 256 blocks/s**

**CPU等待DMA的1000+500个时钟周期内**

**传输的块 256 blocks/s \* 1500 / 50MHz = 0.0075 words**

**因此I/O时间比例为 0.75%。**