## 计算机组成原理与系统结构

## 第四章作业

1. **Problem 4.1**

**A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.**

Block address length : log 4K = 12 bits

Set address length : log (64/4) = 4 bits

Tag address length : Block length – Set length = 8 bits

Word address length : log 128 = 7 bits

|  |  |  |
| --- | --- | --- |
| Tag | Set | Word |
| 8 | 4 | 7 |

**Problem 4.2**

**A two-way set-associative cache has lines of 16 bytes and a total size of 8 Kbytes. The 64-Mbyte main memory is byte addressable. Show the format of the main memory addresses.**

Number of lines : 8Kbytes / 16bytes = 512

Set address length : log (512/2) = 8 bits

Number of blocks : 64Mbytes / 16bytes = 2^22

Block address length : log 2^22 = 22 bits

Tag address length : Block length – Set length = 14 bits

Word address length : log 16 = 4 bits

|  |  |  |
| --- | --- | --- |
| Tag | Set | Word |
| 14 | 8 | 4 |

**Problem 4.3**

**For the hexadecimal main memory addresses 0x333333, 0x777777, 0xDDDDDD, show the following information, in hexadecimal format:**

**a. Tag, Line, and Word values for a direct-mapped cache. (4.10)**

**b. Tag and Word values for an associative cache. (4.12)**

**c. Tag, Set, and Word values for a two-way set-associative cache. (4.15)**

|  |  |  |  |
| --- | --- | --- | --- |
|  | 0x333333 | 0x777777 | 0xDDDDDD |
| a.Tag/Line/Word | 33/CCC/3 | 77/DDD/3 | DD/3777/1 |
| b.Tag/Word | CCCCC/3 | DDDDD/3 | 377777/1 |
| c.Tag/Set/Word | 66/CCC/3 | EE/DDD/3 | 1BB/1777/1 |

**Problem 4.4**

**List the following values:**

**a. For the direct cache example of Figure 4.10: address length, number of addressable units, block size, number of blocks in main memory, number of lines in cache, size of tag**

**b. For the associative cache example of Figure 4.12: address length, number of addressable units, block size, number of blocks in main memory, number of lines in cache, size of tag**

**c. For the two-way set-associative cache example of Figure 4.15: address length, number of addressable units, block size, number of blocks in main memory, number of lines in set, number of sets, number of lines in cache, size of tag**

|  |  |  |  |
| --- | --- | --- | --- |
|  | a. Direct | b. Associative | c. Set-associative |
| Address length | 24 | 24 | 24 |
| Number of addressable units | 2^24 | 2^24 | 2^24 |
| Block size | 4 | 4 | 4 |
| Number of blocks in main memory | 2^22 | 2^22 | 2^22 |
| Number of lines in cache | 2^14 | 2^14 | 2^14 |
| Size of tag | 8 | 22 | 9 |
| Number of lines in set | / | / | 2 |
| Number of sets | / | / | 2^13 |

1. **For the address sequence: 1  2  3  4  1  2  3  4 1  2  3  4, draw and compute the hit ratio of 3-line cache using FIFO & LRU; which methods can be used to improve the hit ratio?**

FIFO:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 2 | 3 | 4 | 1 | 2 | 3 | 4 | 1 | 2 | 3 | 4 |
| 1 | 1 | 1 | 4 | 4 | 4 | 3 | 3 | 3 | 2 | 2 | 2 |
|  | 2 | 2 | 2 | 1 | 1 | 1 | 4 | 4 | 4 | 3 | 3 |
|  |  | 3 | 3 | 3 | 2 | 2 | 2 | 1 | 1 | 1 | 4 |

Hit times : 0 Hit ratio : 0

LRU:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 2 | 3 | 4 | 1 | 2 | 3 | 4 | 1 | 2 | 3 | 4 |
| 1 | 1 | 1 | 4 | 4 | 4 | 3 | 3 | 3 | 2 | 2 | 2 |
|  | 2 | 2 | 2 | 1 | 1 | 1 | 4 | 4 | 4 | 3 | 3 |
|  |  | 3 | 3 | 3 | 2 | 2 | 2 | 1 | 1 | 1 | 4 |

Hit times : 0 Hit ratio : 0

To improve the hit ratio, we can use random replacement or increase the cache capacity.

1. **Consider a machine with Cache-main memory system structure. Its main memory has 8 blocks(0-7) which block size is 4 words, and its Cache has 4 lines(0-3) and adapts a organization of 2-way set associative with LRU replacement algorithm, require:**

**1) show the structure of main memory address**

**2) show the corresponding relationship of main memory block number and Cache line number**

**3) Supposed initial Cache status is empty, for the address sequence: 1 2 4 1 3 7 0 1 2 5 4 6 4 7 2. List the assigned addresses of cache lines after each visit.**

**4) Given the hit ratio of Cache after above steps.**

1) Block address length : log 8 = 3 bits

Set address length : log (4/2) = 1 bits

Tag address length : Block length – Set length = 2 bits

Word address length : log 4 = 2 bits

|  |  |  |
| --- | --- | --- |
| Tag | Set | Word |
| 2 | 1 | 2 |

2) Set 0 (Line 0 and Line 1 in Cache) is corresponding to Block 0 (000), Block 2 (010), Block 4 (100), Block 6 (110) in main memory.

Set 1 (Line 2 and Line 3 in Cache) is corresponding to Block 1 (001), Block 3 (011), Block 5 (101), Block 7 (111) in main memory.

3)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 1 | 2 | 4 | 1 | 3 | 7 | 0 | 1 | 2 | 5 | 4 | 6 | 4 | 7 | 2 |
| Set 0 |  | 2 | 2 | 2 | 2 | 2 | 0 | 0 | 0 | 0 | 4 | 4 | 4 | 4 | 4 |
|  |  | 4 | 4 | 4 | 4 | 4 | 4 | 2 | 2 | 2 | 6 | 6 | 6 | 2 |
| Set 1 | 1 | 1 | 1 | 1 | 1 | 7 | 7 | 7 | 7 | 5 | 5 | 5 | 5 | 5 | 5 |
|  |  |  |  | 3 | 3 | 3 | 1 | 1 | 1 | 1 | 1 | 1 | 7 | 7 |

4) Hit times : 2

Hit ratio : 2/15