1. Description

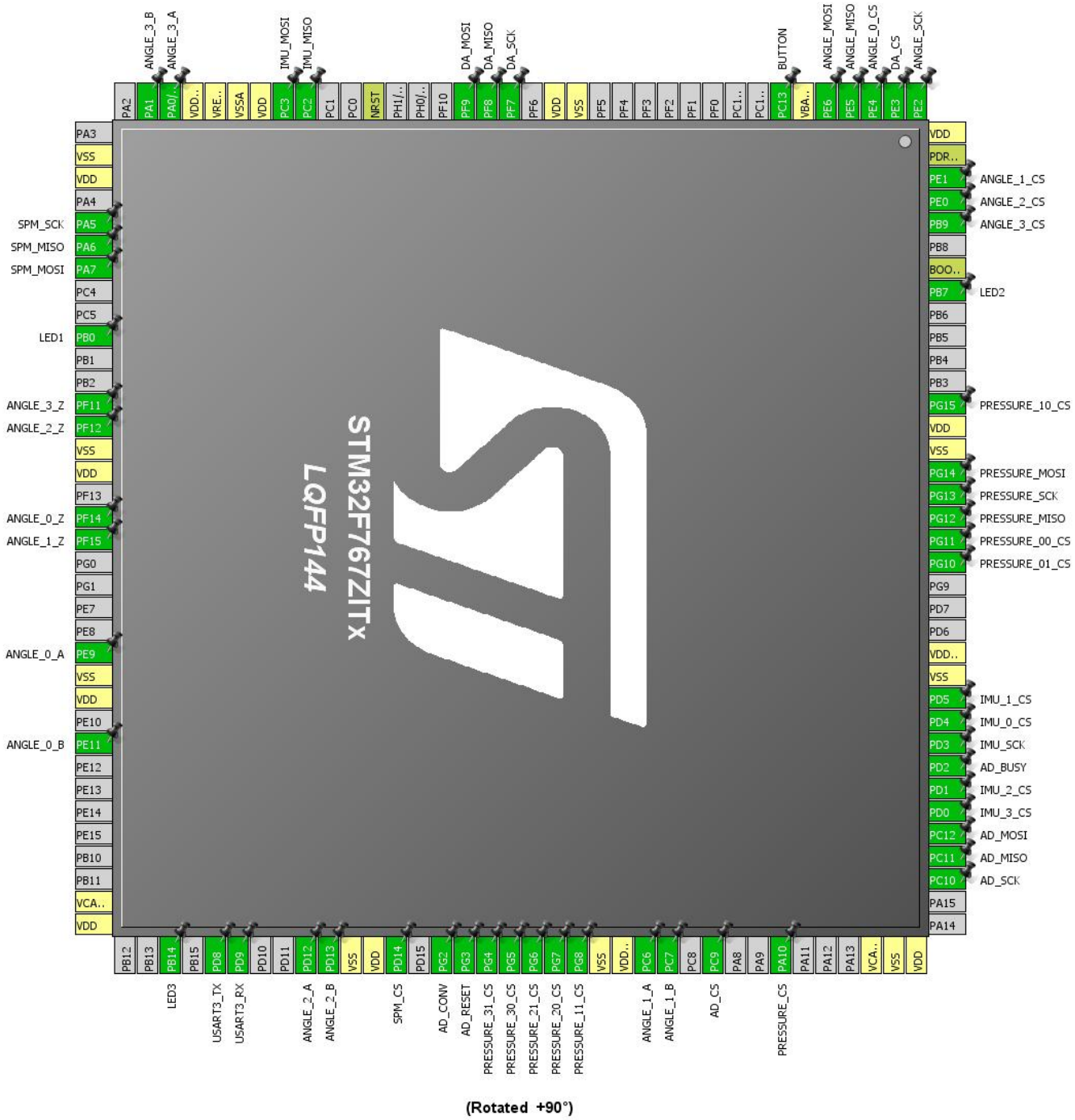
1.1. Project

Project Name	F7_Ethercat_RTOS
Board Name	F7_Ethercat_RTOS
Generated with:	STM32CubeMX 4.25.0
Date	04/19/2018

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

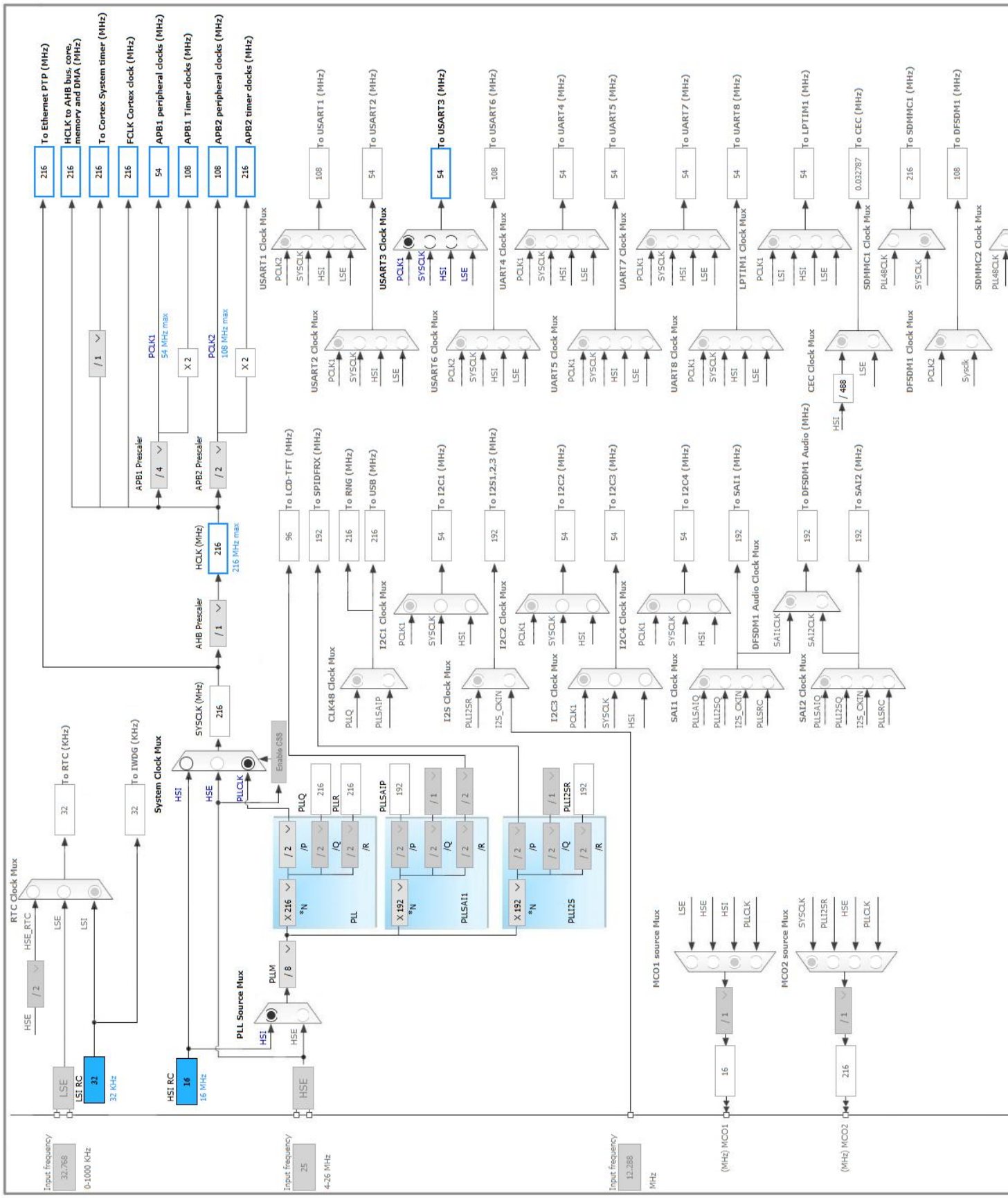
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SPI4_SCK	ANGLE_SCK
2	PE3 *	I/O	GPIO_Output	DA_CS
3	PE4 *	I/O	GPIO_Output	ANGLE_0_CS
4	PE5	I/O	SPI4_MISO	ANGLE_MISO
5	PE6	I/O	SPI4_MOSI	ANGLE_MOSI
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	BUTTON
16	VSS	Power		
17	VDD	Power		
19	PF7	I/O	SPI5_SCK	DA_SCK
20	PF8	I/O	SPI5_MISO	DA_MISO
21	PF9	I/O	SPI5_MOSI	DA_MOSI
25	NRST	Reset		
28	PC2	I/O	SPI2_MISO	IMU_MISO
29	PC3	I/O	SPI2_MOSI	IMU_MOSI
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	TIM5_CH1	ANGLE_3_A
35	PA1	I/O	TIM5_CH2	ANGLE_3_B
38	VSS	Power		
39	VDD	Power		
41	PA5	I/O	SPI1_SCK	SPM_SCK
42	PA6	I/O	SPI1_MISO	SPM_MISO
43	PA7	I/O	SPI1_MOSI	SPM_MOSI
46	PB0 *	I/O	GPIO_Output	LED1
49	PF11	I/O	GPIO_EXTI11	ANGLE_3_Z
50	PF12	I/O	GPIO_EXTI12	ANGLE_2_Z
51	VSS	Power		
52	VDD	Power		
54	PF14	I/O	GPIO_EXTI14	ANGLE_0_Z
55	PF15	I/O	GPIO_EXTI15	ANGLE_1_Z
60	PE9	I/O	TIM1_CH1	ANGLE_0_A
61	VSS	Power		
62	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
64	PE11	I/O	TIM1_CH2	ANGLE_0_B
71	VCAP_1	Power		
72	VDD	Power		
75	PB14 *	I/O	GPIO_Output	LED3
77	PD8	I/O	USART3_TX	
78	PD9	I/O	USART3_RX	
81	PD12	I/O	TIM4_CH1	ANGLE_2_A
82	PD13	I/O	TIM4_CH2	ANGLE_2_B
83	VSS	Power		
84	VDD	Power		
85	PD14 *	I/O	GPIO_Output	SPM_CS
87	PG2 *	I/O	GPIO_Output	AD_CONV
88	PG3 *	I/O	GPIO_Output	AD_RESET
89	PG4 *	I/O	GPIO_Output	PRESSURE_31_CS
90	PG5 *	I/O	GPIO_Output	PRESSURE_30_CS
91	PG6 *	I/O	GPIO_Output	PRESSURE_21_CS
92	PG7 *	I/O	GPIO_Output	PRESSURE_20_CS
93	PG8 *	I/O	GPIO_Output	PRESSURE_11_CS
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	TIM3_CH1	ANGLE_1_A
97	PC7	I/O	TIM3_CH2	ANGLE_1_B
99	PC9 *	I/O	GPIO_Output	AD_CS
102	PA10 *	I/O	GPIO_Output	PRESSURE_CS
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
111	PC10	I/O	SPI3_SCK	AD_SCK
112	PC11	I/O	SPI3_MISO	AD_MISO
113	PC12	I/O	SPI3_MOSI	AD_MOSI
114	PD0 *	I/O	GPIO_Output	IMU_3_CS
115	PD1 *	I/O	GPIO_Output	IMU_2_CS
116	PD2	I/O	GPIO_EXTI2	AD_BUSY
117	PD3	I/O	SPI2_SCK	IMU_SCK
118	PD4 *	I/O	GPIO_Output	IMU_0_CS
119	PD5 *	I/O	GPIO_Output	IMU_1_CS
120	VSS	Power		
121	VDDSDMMC	Power		
125	PG10 *	I/O	GPIO_Output	PRESSURE_01_CS

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
126	PG11 *	I/O	GPIO_Output	PRESSURE_00_CS
127	PG12	I/O	SPI6_MISO	PRESSURE_MISO
128	PG13	I/O	SPI6_SCK	PRESSURE_SCK
129	PG14	I/O	SPI6_MOSI	PRESSURE_MOSI
130	VSS	Power		
131	VDD	Power		
132	PG15 *	I/O	GPIO_Output	PRESSURE_10_CS
137	PB7 *	I/O	GPIO_Output	LED2
138	BOOT0	Boot		
140	PB9 *	I/O	GPIO_Output	ANGLE_3_CS
141	PE0 *	I/O	GPIO_Output	ANGLE_2_CS
142	PE1 *	I/O	GPIO_Output	ANGLE_1_CS
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. SPI1

Mode: Full-Duplex Master

5.1.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**54.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.2. SPI2

Mode: Full-Duplex Master

5.2.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**6.75 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

5.3. SPI3

Mode: Full-Duplex Master

5.3.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**6.75 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.4. SPI4

Mode: Full-Duplex Master

5.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**128 ***
Baud Rate	**843.75 KBits/s ***
Clock Polarity (CPOL)	**High ***

Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

5.5. SPI5

Mode: Full-Duplex Master

5.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**13.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

5.6. SPI6

Mode: Full-Duplex Master

5.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**128 ***

Baud Rate	**843.75 KBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

5.7. SYS

Timebase Source: TIM10

5.8. TIM1

Combined Channels: Encoder Mode

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xffff ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**6 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division

Input Filter	**6 ***

5.9. TIM2

Clock Source : Internal Clock

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**107 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0xffffffff ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

5.10. TIM3

Combined Channels: Encoder Mode

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct

Prescaler Division Ratio	No division
Input Filter	**6 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**6 ***

5.11. TIM4

Combined Channels: Encoder Mode

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**6 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**6 ***

5.12. TIM5

Combined Channels: Encoder Mode

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0x0000FFFF ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**6 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**6 ***

5.13. USART3

Mode: Asynchronous

5.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	**921600 ***
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.14. FREERTOS

mode: Enabled

5.14.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	**Static ***

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.14.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled

xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	SPM_SCK
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	SPM_MISO
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	SPM_MOSI
SPI2	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	IMU_MISO
	PC3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	IMU_MOSI
	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	IMU_SCK
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	AD_SCK
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	AD_MISO
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	AD_MOSI
SPI4	PE2	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	ANGLE_SCK
	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	ANGLE_MISO
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	ANGLE_MOSI
SPI5	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	DA_SCK
	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	DA_MISO
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	DA_MOSI
SPI6	PG12	SPI6_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	PRESSURE_MISO

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PG13	SPI6_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	PRESSURE_SCK
	PG14	SPI6_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	PRESSURE_MOSI
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ANGLE_0_A
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ANGLE_0_B
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ANGLE_1_A
	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ANGLE_1_B
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ANGLE_2_A
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ANGLE_2_B
TIM5	PA0/WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ANGLE_3_A
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ANGLE_3_B
USART3	PD8	USART3_TX	Alternate Function Push Pull	**Pull-up ***	**Very High ***	
	PD9	USART3_RX	Alternate Function Push Pull	**Pull-up ***	**Very High ***	
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DA_CS
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ANGLE_0_CS
	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	BUTTON
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PF11	GPIO_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ANGLE_3_Z
	PF12	GPIO_EXTI12	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ANGLE_2_Z
	PF14	GPIO_EXTI14	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ANGLE_0_Z
	PF15	GPIO_EXTI15	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ANGLE_1_Z
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPM_CS
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AD_CONV
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AD_RESET
	PG4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PRESSURE_31_CS
	PG5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PRESSURE_30_CS
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PRESSURE_21_CS
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PRESSURE_20_CS
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PRESSURE_11_CS
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AD_CS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PRESSURE_CS
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_3_CS
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_2_CS
	PD2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	AD_BUSY
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_0_CS
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_1_CS
	PG10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PRESSURE_01_CS
	PG11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PRESSURE_00_CS
	PG15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PRESSURE_10_CS
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ANGLE_3_CS
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ANGLE_2_CS
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ANGLE_1_CS

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART3_RX	DMA1_Stream1	Peripheral To Memory	**High ***
USART3_TX	DMA1_Stream4	Memory To Peripheral	**Medium ***
SPI3_RX	DMA1_Stream0	Peripheral To Memory	**High ***
SPI3_TX	DMA1_Stream5	Memory To Peripheral	**High ***
SPI6_RX	DMA2_Stream6	Peripheral To Memory	Low
SPI6_TX	DMA2_Stream5	Memory To Peripheral	Low

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_TX: DMA1_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI3_RX: DMA1_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

SPI3_TX: DMA1_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

SPI6_RX: DMA2_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

SPI6_TX: DMA2_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
EXTI line2 interrupt	true	5	0
DMA1 stream0 global interrupt	true	5	0
DMA1 stream1 global interrupt	true	5	0
DMA1 stream4 global interrupt	true	5	0
DMA1 stream5 global interrupt	true	5	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
SPI1 global interrupt	true	6	0
USART3 global interrupt	true	15	0
EXTI line[15:10] interrupts	true	6	0
DMA2 stream5 global interrupt	true	5	0
DMA2 stream6 global interrupt	true	5	0
SPI5 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
SPI2 global interrupt	unused		
TIM5 global interrupt	unused		
SPI3 global interrupt	unused		
FPU global interrupt	unused		
SPI4 global interrupt	unused		
SPI6 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	029041_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	F7_Ethercat_RTOS
Project Folder	C:\Users\40207\OneDrive\OneDriveDocumentation\STM32WorkSpaceOnedrive\
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F7 V1.11.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report