

Timer 1 Operation

Timer1 is one of five modules available inside the PIC32 microcontroller.

There are three special function registers that control most Timer1 functions. They are:

- **TMR1**, which contains the 16-bit counter value
- **T1CON**, which controls the activation and operating mode of the timer
- **PR1**, which controls the periodic reset of the timer.

The timer counter (TMR1) is incremented every clock cycle until its value matches the value in the periodic reset register (PR1). The timer clock source frequency is reduced by a prescale ratio (TCKPS). Assuming that the timer clock source is internal PBCLK (Peripheral Bus clock) and the timer clock prescale (TCKPS) is 1:256, the timer counter is incremented at a frequency of $f_{pb}/256$.

Timer 1 Details

The 16-bit Timer1 peripheral can operate as

- a synchronous timer using internal or external clock sources
- a gated timer using internal clock source and external clock pin
- an asynchronous timer using an external asynchronous clock source

The Timer1 module is disabled and powered off when the ON bit (T1CON[15]) = 0, thus providing maximum power savings. Updates to the T1CON register should only be performed when the timer module is disabled, ON bit (T1CON[15]) = 0.

All timer registers come in four forms, each at a separate address. Using, T1CON as an example:

T1CON	sets or clears all bits when assigned
T1CONCLR	clears selected bits
T1CONSET	sets selected bits
T1CONINV	toggles (inverts) selected bits

Example

```
T1CON = 0x30; // sets bits [5:4] and clears all others
T1CONSET = 0x8000; // sets bit [15], leaves all others unchanged
```

Synchronous Internal Timer

In this mode, the timer clock source is the internal PBCLK (Peripheral Bus Clock), TCS (TxCON[1]) = 0. Clock synchronization is not required, therefore the Timer1 Synchronization bit, TSYNC (T1CON[2]), is ignored. The TMR1 Count register increments on every PBCLK clock cycle when the timer clock prescale (TCKPS) is 1:1.

Timer1 generates a timer match event after the TMR1 Count register matches the PR1 Period register value (mid-clock cycle on the falling edge), then resets to 0x0000 on the next PBCLK clock cycle.

For clock prescale = N (other than 1:1), the timer operates at a clock rate = PBCLK/N and the TMRx Count register increments on every Nth PBCLK clock.

The following steps should be performed to properly configure the Timer1 peripheral for Timer mode operation.

1. Clear ON control bit (T1CON[15]) = 0 to disable timer.
2. Configure TCKPS control bits (T1CON[5:4]) to select desired timer clock prescale.
3. Set TCS control bit (T1CON[1]) = 0 to select the internal PBCLK clock source.
4. Clear TMR1 register.
5. Load PR1 register with desired 16-bit match value.
6. Set ON control bit = 1 to enable Timer.

Examples

Here is the essential code to initialize and start timer1, using a prescale of 1:256.

```
T1CON = 0x30 // Stop and Init Timer (with prescale 1:256)
TMR1 = 0x0; // Clear timer register
PR1 = 0xFFFF; // Load period register
T1CONSET = 0x8000; // Start Timer
```

Here is a complete project, using the PIC32 Starter Kit

[Timer Hardware](#): blink LED1 using an internal timer.

Peripheral Library Macros

The peripheral library contains macros for common timer operations. A close inspection of the macros below shows that they mostly hide the details of register names. You still need to know what configuration bits to set.

```
#define OpenTimer1(config, period)    (TMR1 = 0, PR1 = (period), T1CON = (config))
#define CloseTimer1()    (mT1IntEnable(0), T1CON = 0)
#define ReadTimer1()    (TMR1)
#define WriteTimer1(value)    TMR1 = ((value))
#define ReadPeriod1()    (PR1)
#define WritePeriod1(value)    PR1 = ((value))
```

See [timer.h](#) for more details.

Timer 1 Control register (T1CON)

15	14	13	12	11	10	9	8
ON	FRZ	SIDL	TMWDIS	TMWIP	--	--	--
7	6	5	4	3	2	1	0
TGATE	--	TCKPS[1:0]		--	TSYNC	TCS	--

where

- bit 15 **ON**: Timer On bit
 1 = Timer is enabled
 0 = Timer is disabled
- bit 14 **FRZ**: Freeze in Debug Exception Mode bit
 1 = Freeze operation when CPU is in Debug Exception mode
 0 = Continue operation when CPU is in Debug Exception mode
- bit 13 **SIDL**: Stop in Idle Mode bit
 1 = Discontinue operation when device enters Idle mode

	0 = Continue operation in Idle mode
bit 12	TMWDIS: Asynchronous Timer Write Disable bit
	In Asynchronous Timer mode:
	1 = Writes to asynchronous TMR1 are ignored until pending write operation completes
	0 = Back-to-back writes are enabled (legacy asynchronous timer functionality)
	In Synchronous Timer mode:
	This bit has no effect.
bit 11	TMWIP: Asynchronous Timer Write in Progress bit
	In Asynchronous Timer mode:
	1 = Asynchronous write to TMR1 register in progress
	0 = Asynchronous write to TMR1 register complete
	In Synchronous Timer mode:
	This bit is read as '0'.
bit 10-8	Unimplemented: Read as '0'
bit 7	TGATE: Gated Time Accumulation Enable bit
	When TCS = 1:
	This bit is ignored and read '0'.
	When TCS = 0:
	1 = Gated time accumulation is enabled
	0 = Gated time accumulation is disabled
bit 6	Unimplemented: Read as '0'
bit 5-4	TCKPS[1:0]: Timer Input Clock prescaler Select bits
	11 = 1:256 prescale value
	10 = 1:64 prescale value
	01 = 1:8 prescale value
	00 = 1:1 prescale value
bit 3	Unimplemented: Read as '0'
bit 2	TSYNC: Timer External Clock Input Synchronization Selection bit
	When TCS = 1:
	1 = External clock input is synchronized
	0 = External clock input is not synchronized
	When TCS = 0:
	This bit is ignored and read '0'.
bit 1	TCS: Timer Clock Source Select bit
	1 = External clock from T1CKI pin
	0 = Internal peripheral clock
bit 0	Unimplemented: Read as '0'

References

[*PIC32MX Family Data Sheet*](#), Microchip Technology, 2008.

[*PIC32 Peripheral Libraries for MPLAB C32 Compiler*](#), Microchip Technology, 2007.

Maintained by [John Loomis](#), last updated *17 November 2012*