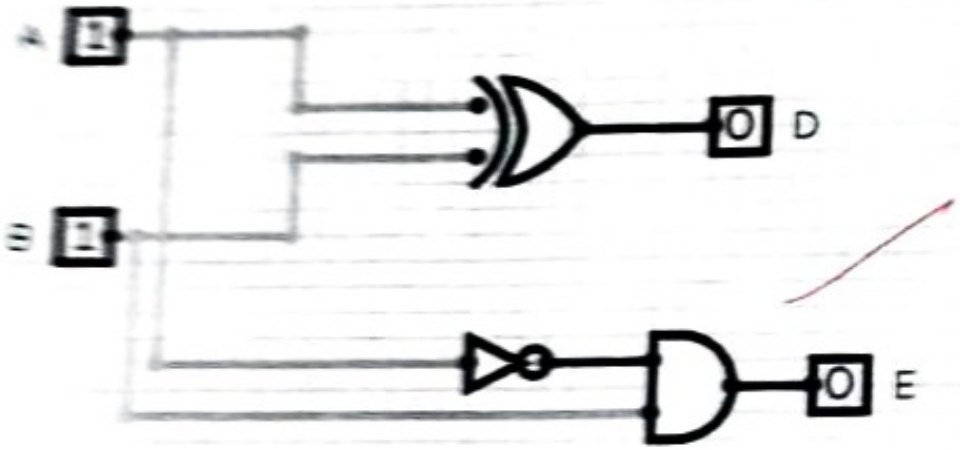
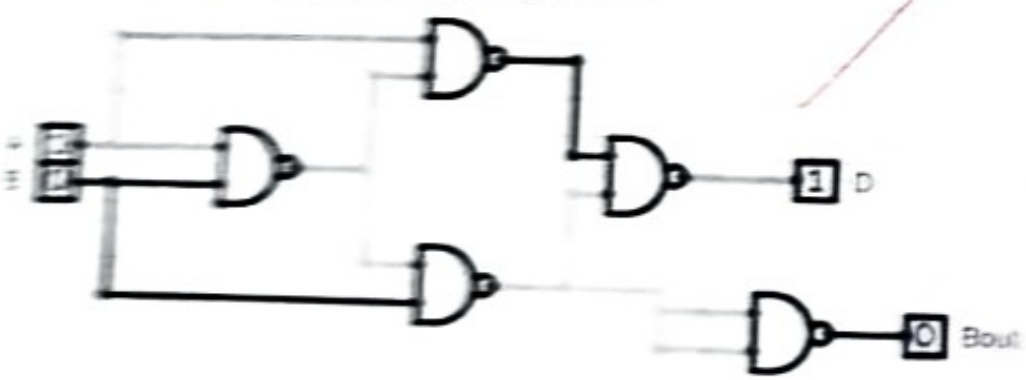
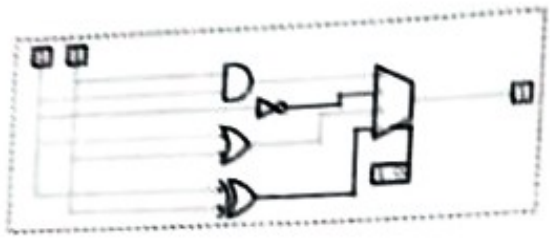
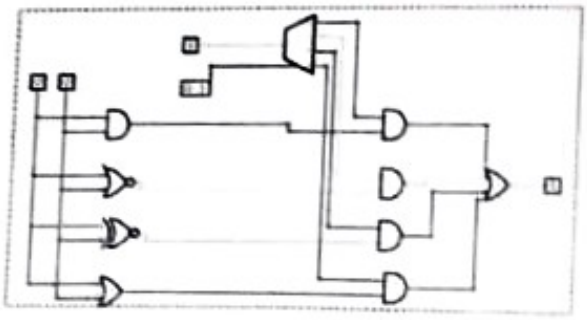
HALF SUBTRACTOR USING BASIC GATES

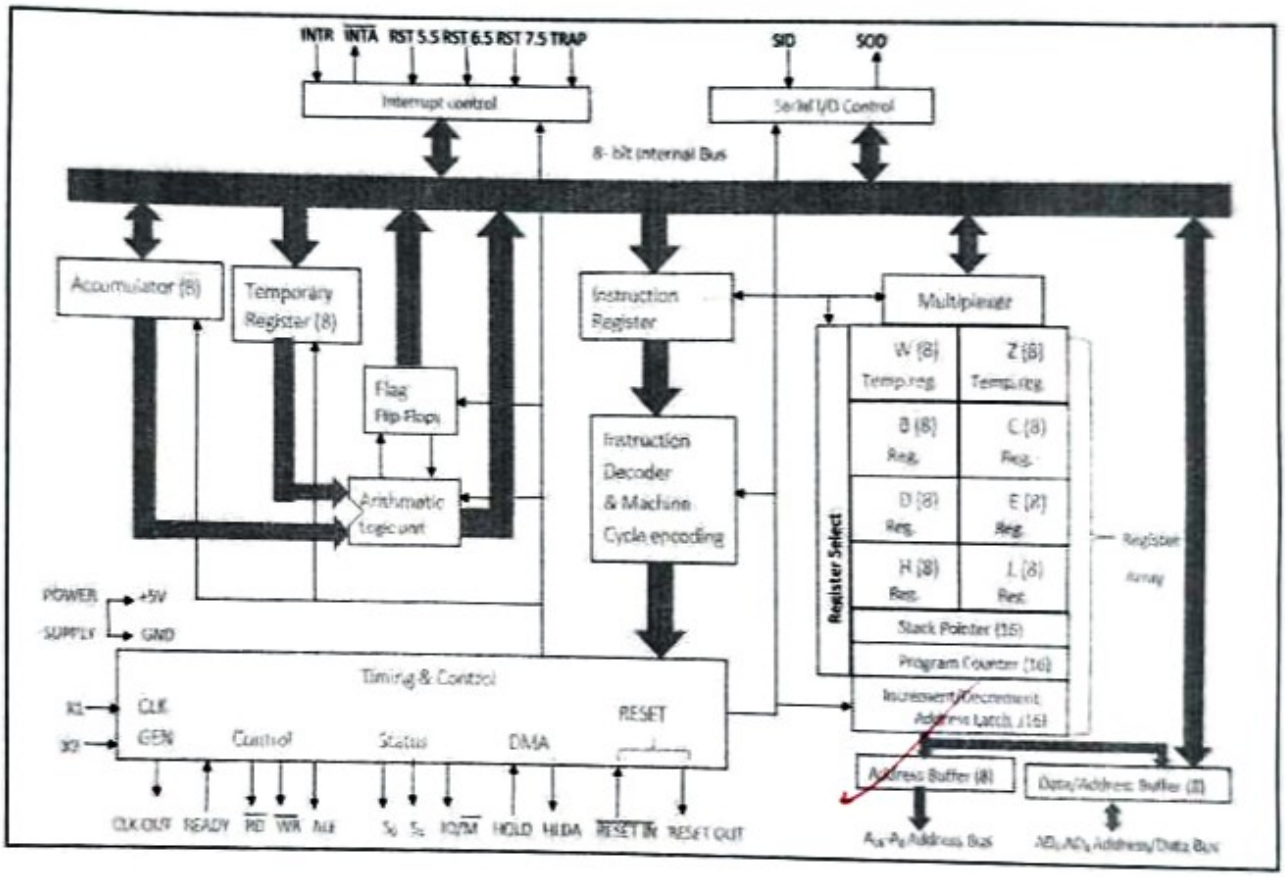


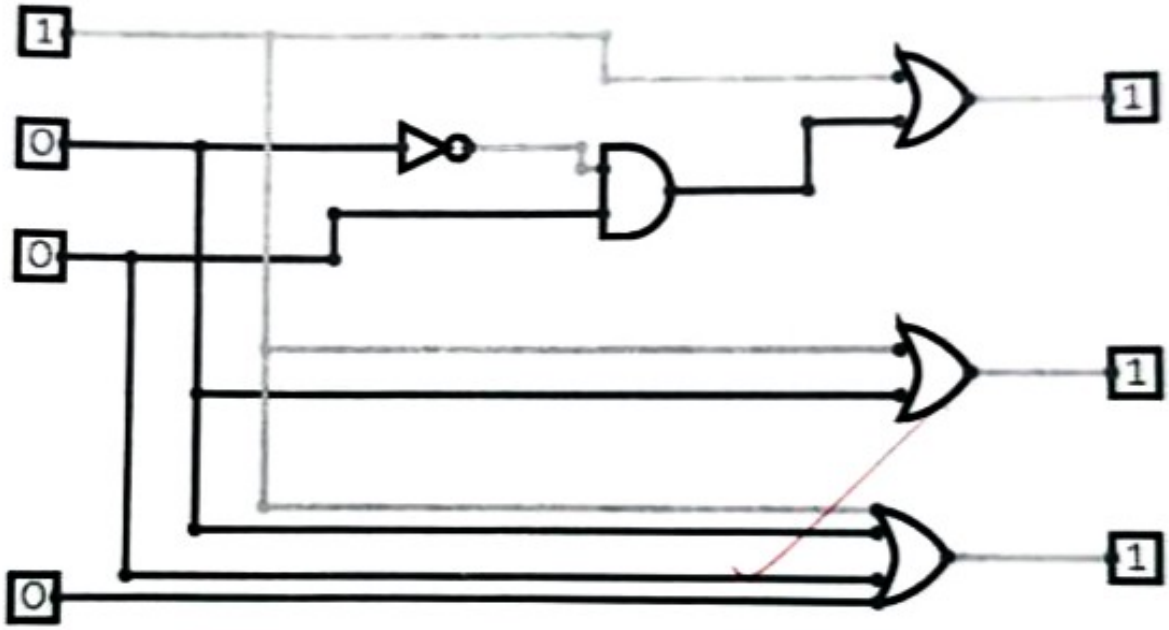
HALF SUBTRACTOR USING UNIVERSAL GATE








INTR
INTA
RST 5.5
RST 6.5
RST 7.5
TRAP
SID
SOD
Interrupt control
Serial I/O Control
8- bit internal Bus
Accumulator (8)
Temporary Register (8)
Flag Flip-Flops
Arithmetic Logic unit
Instruction Register
Instruction Decoder & Machine Cycle encoding
Multiplexer
W (8) Temp. reg
Z (8) Temp. reg
B (8) Reg.
C (8) Reg.
D (8) Reg.
E (8) Reg.
H (8) Reg.
L (8) Reg.
Register Select
Register Array
Stack Pointer (16)
Program Counter (16)
Address Buffer (8)
Data/Address Buffer (8)
POWER SUPPLY
+5V
GND
Timing & Control
CLK GEN
Control
Status
DMA
RESET
CLK OUT
READY
RD
WR
ALE
HOLD
HLDA
RESET IN
RESET OUT



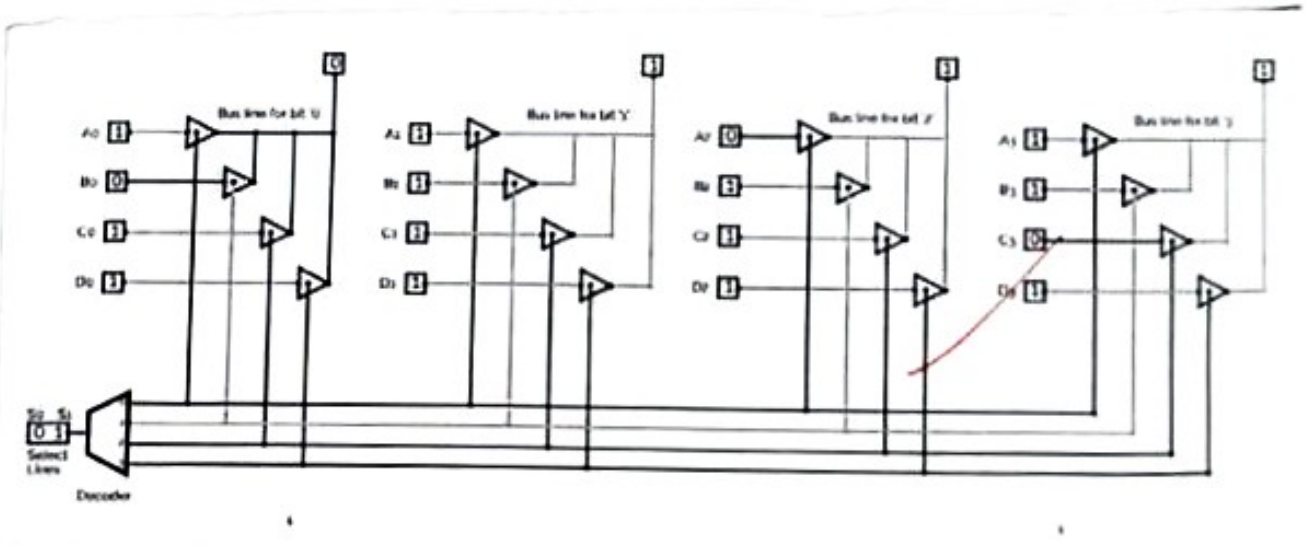
Truth table

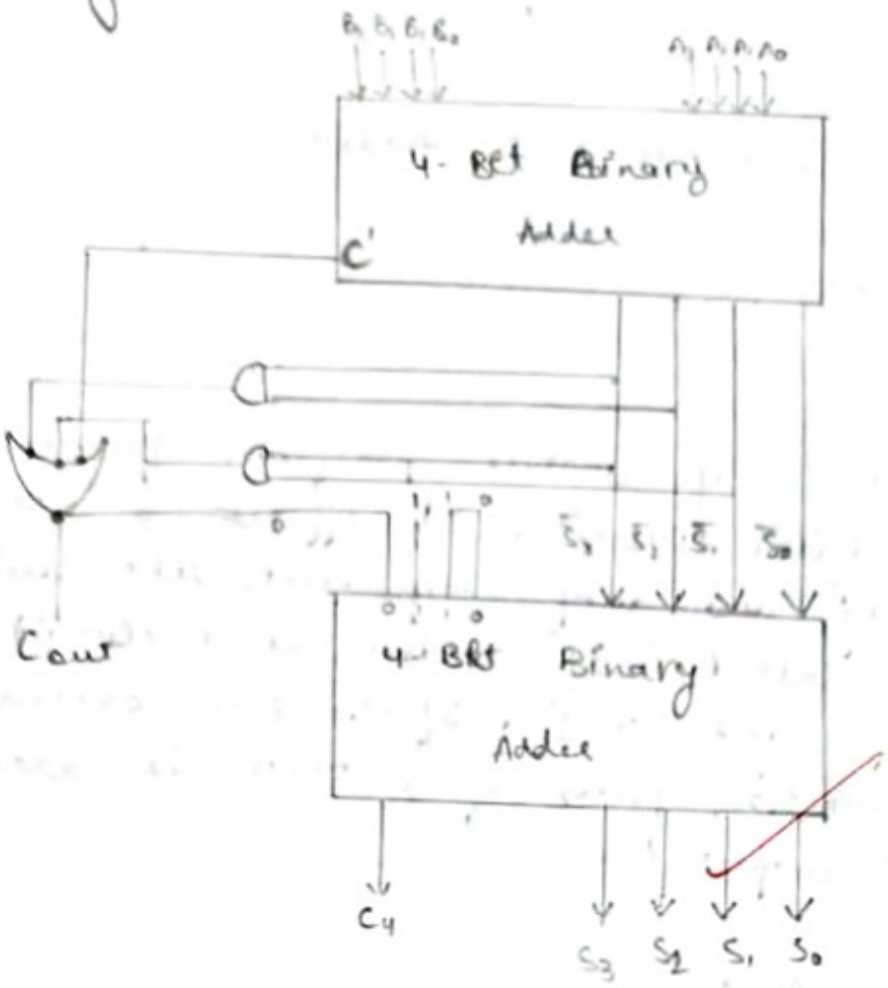
Enable		Decoder output	Enabled Register	Bus output
S_1	S_0	(Y_0, Y_1, Y_2, Y_3)		$(O_4, O_3, O_2, O_1, O_0)$
0	0	$Y_0 = 1$	R_0	A_4, A_3, A_2, A_1, A_0
0	1	$Y_1 = 1$	R_1	B_4, B_3, B_2, B_1, B_0
1	0	$Y_2 = 1$	R_2	C_4, C_3, C_2, C_1, C_0
1	1	$Y_3 = 1$	R_3	D_4, D_3, D_2, D_1, D_0

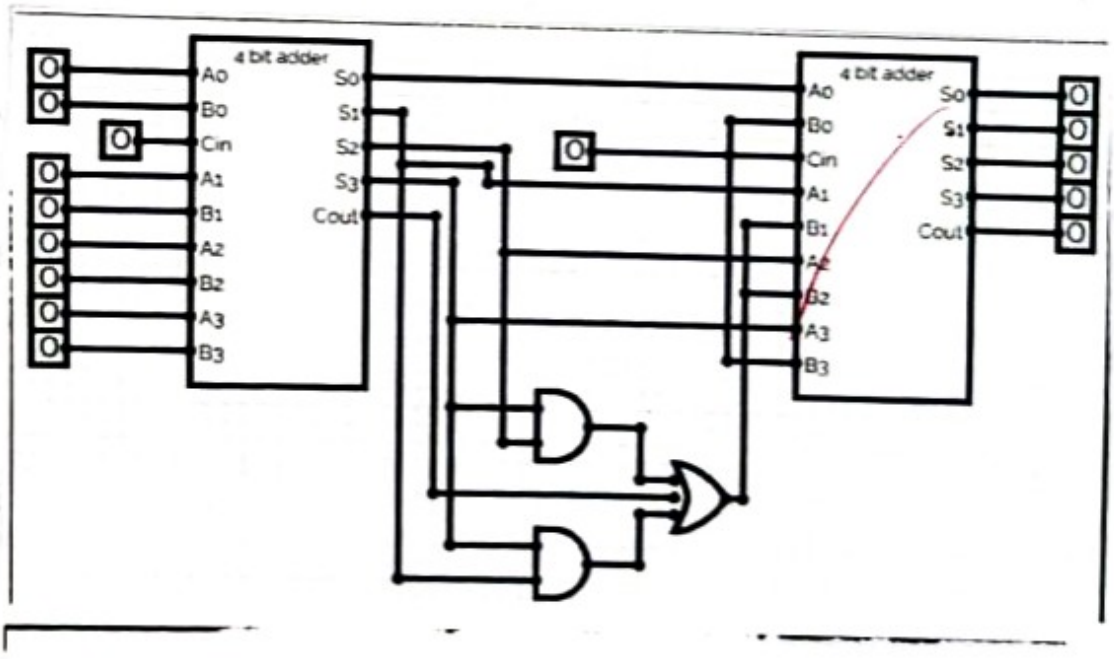
From the table above we can directly write the expression

$Y_0 = \bar{S}_1 \bar{S}_0$, $Y_1 = \bar{S}_1 S_0$, $Y_2 = S_1 \bar{S}_0$

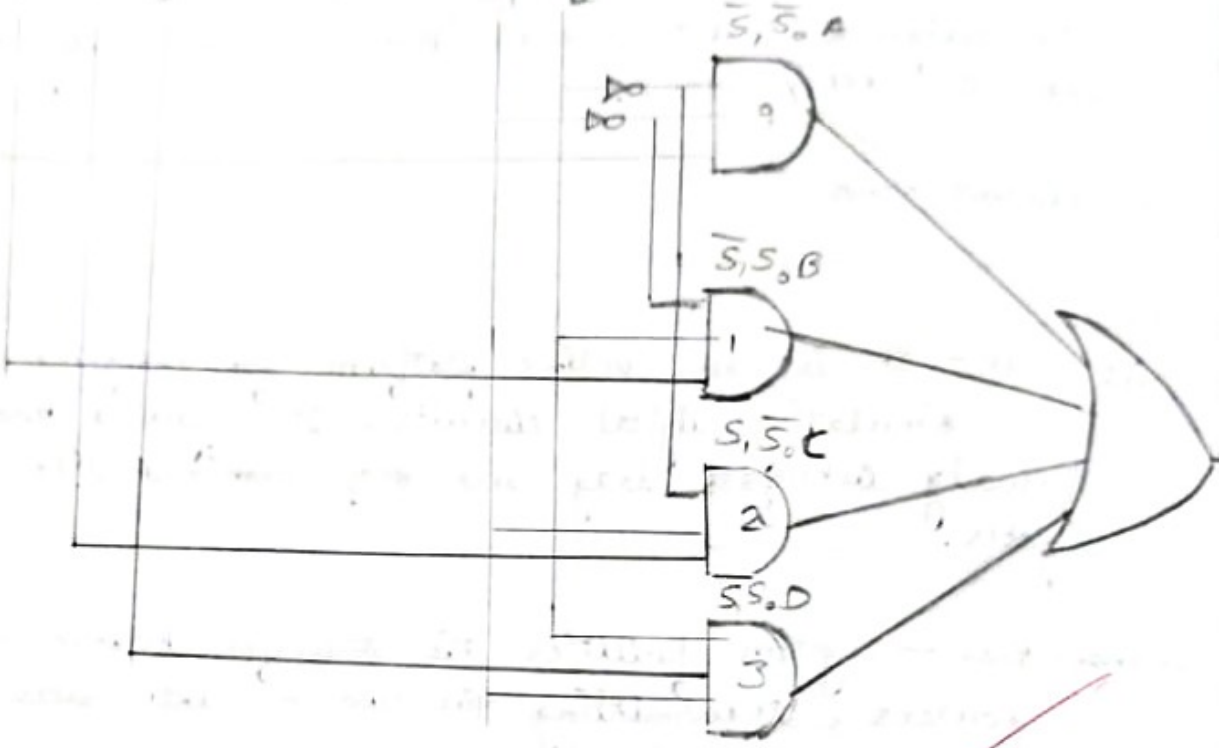
$Y_3 = S_1 S_0$

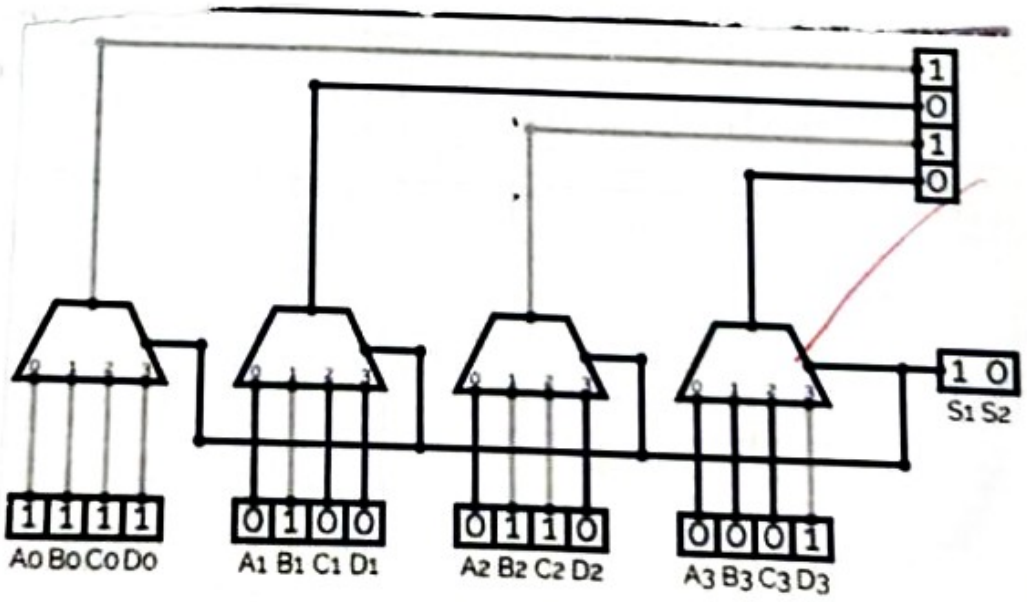


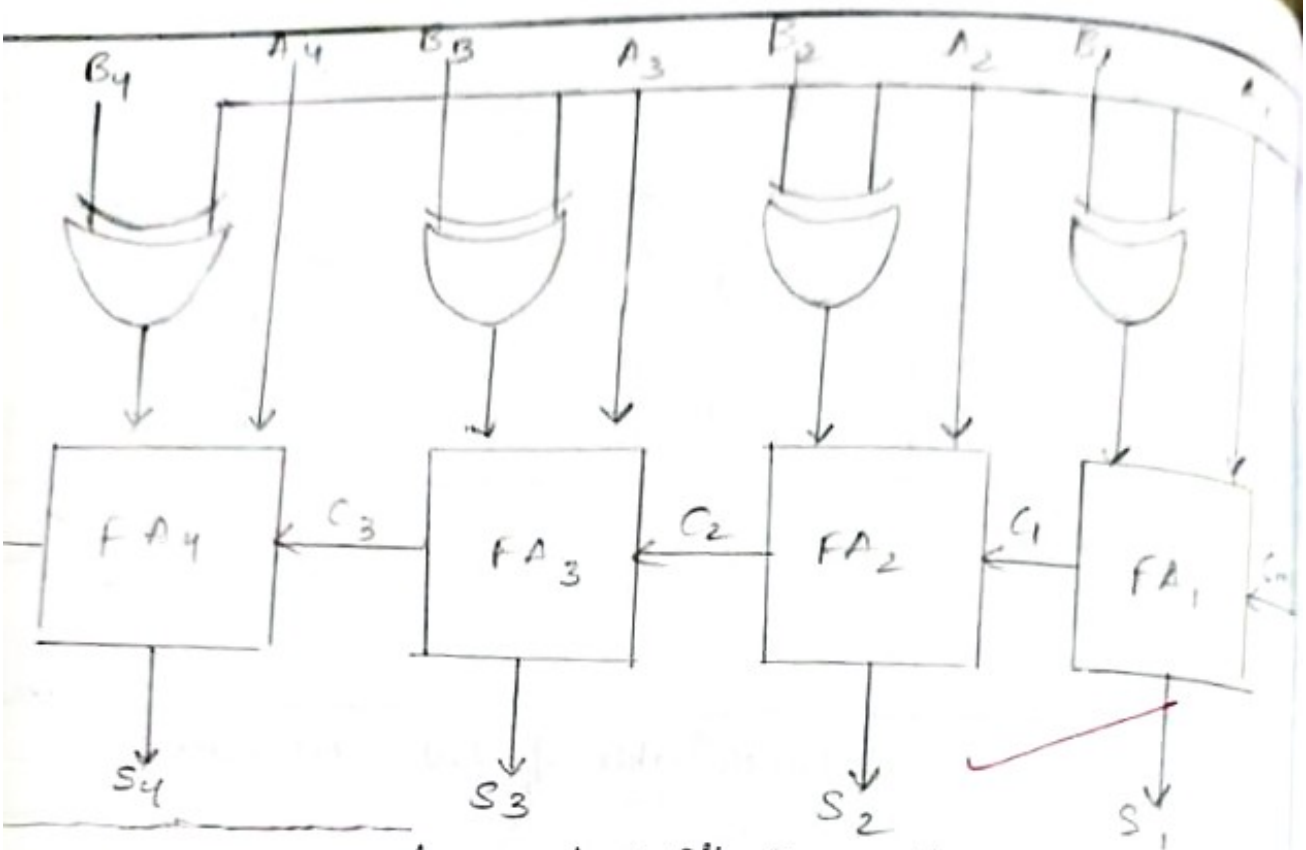




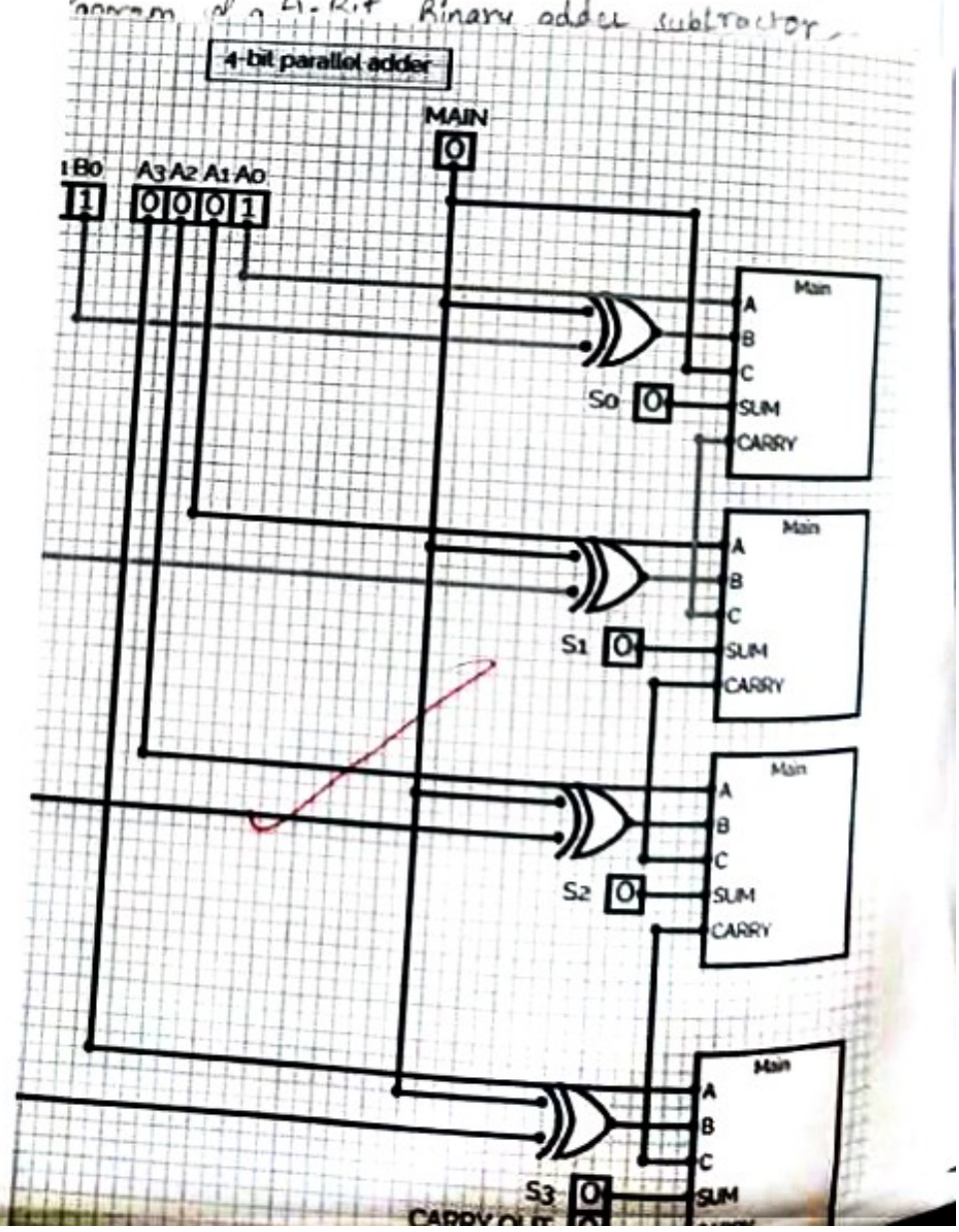
4-Bit BCD Adder



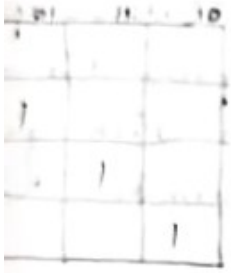




Program of 4-Bit Binary adder subtractor

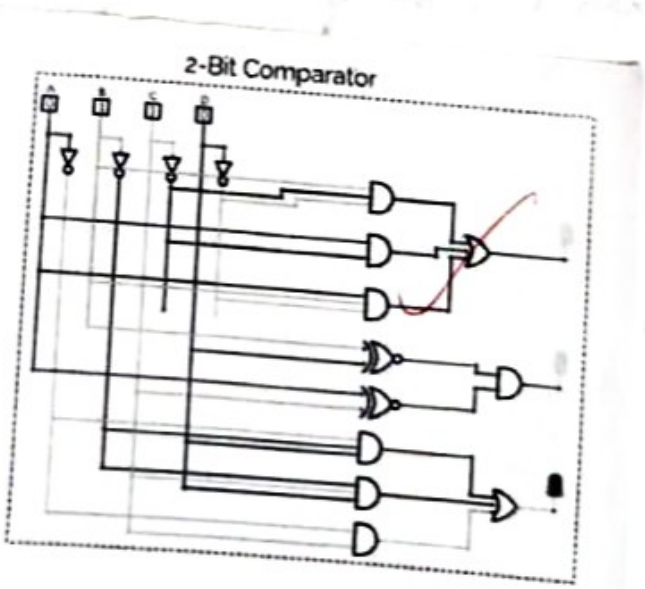


$A>B \Rightarrow A_1\bar{B_1} + A_0\bar{B_1}\bar{B_0} + A_1A_0\bar{B_0}$

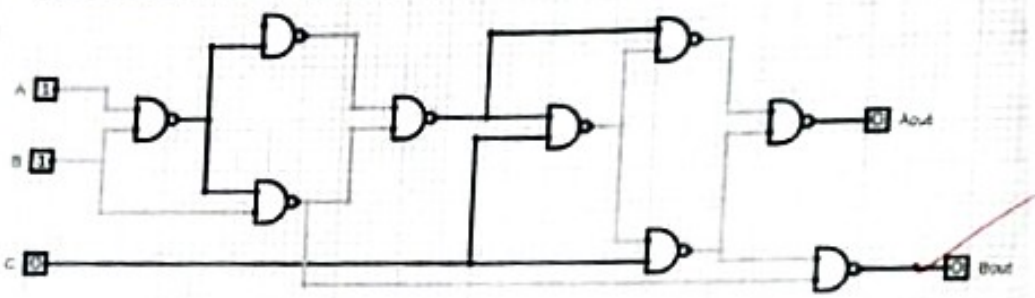


$A=B \Rightarrow (A_1 \cdot B_1)(A_0 \cdot B_0)$

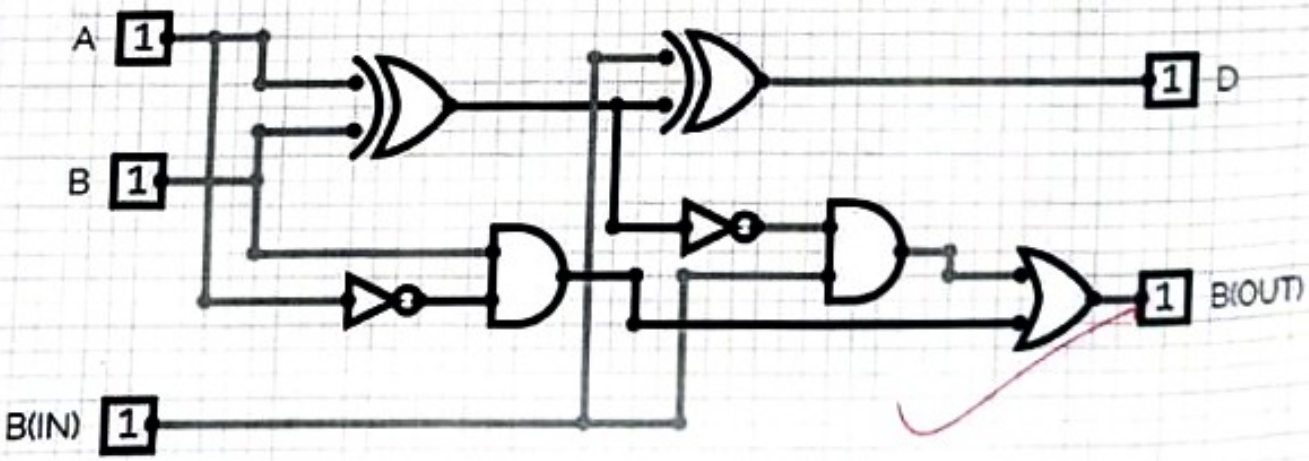
$A<B \Rightarrow \bar{A}_1B_1 + \bar{A}_1\bar{A}_0B_0 + \bar{A}_0B_1B_0$



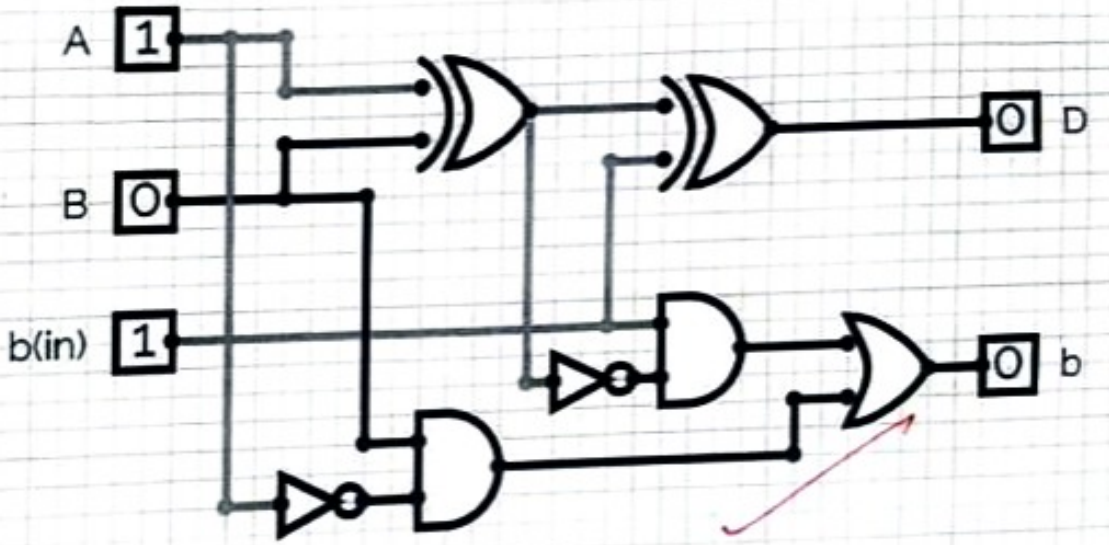
FULL SUBTRACTOR USING UNIVERSAL GATE(NAND GATE)



FULL SUBTRACTOR USING BASIC GATES

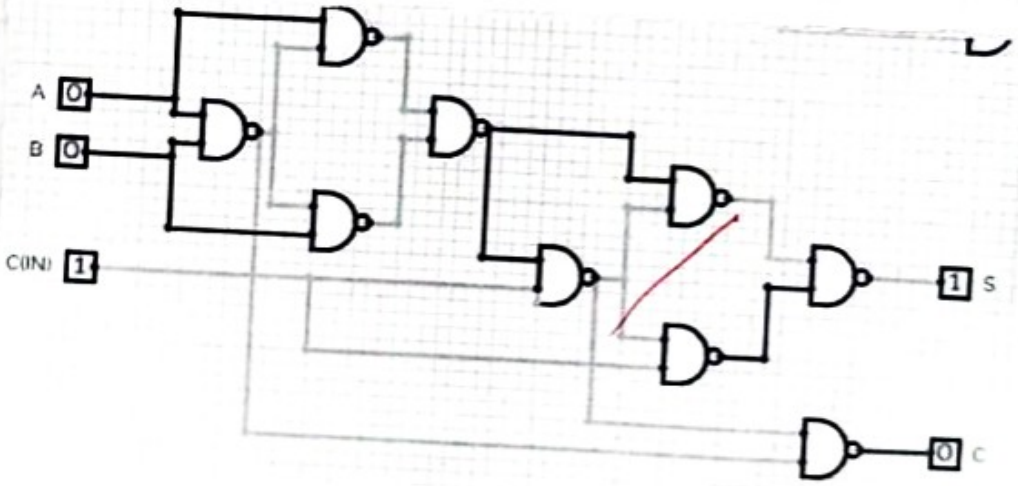


FULL SUBTRACTOR USING 2 HALF SUBTRACTOR AND AN OR GATE

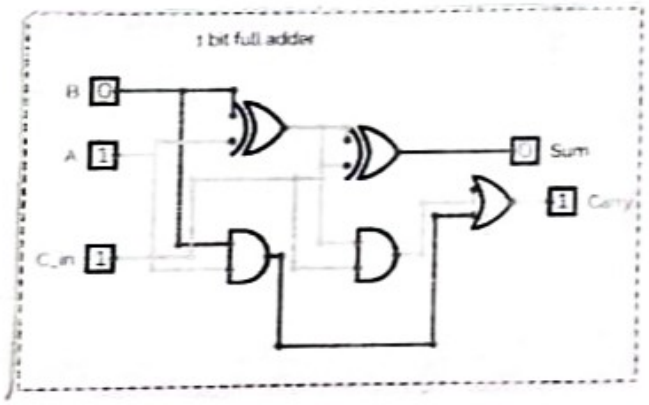


Input			Output	
A	B	C_{IN}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth table of Full-adder.



1 BIT FULL ADDER USING TWO HALF ADDER



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