为什么Java程序员也需要了解CPU

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关于我

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- 2010年6月加入淘宝
- 曾经淘宝Hadoop&Hive研发 组Leader
- 目前专注分布式实时计算
- Hive Contributor
- 自由、开源软件热爱者



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什么是volatile?





下面哪个程序跑得更快?

```
private static long value;

public static void increment() {
    while (value < 100000000L) {
      value++;
    }
}</pre>
```

```
private static volatile long value;
public static void increment() {
   while (value < 100000000L) {
     value++;
   }
}</pre>
```

如果换成AtomicLong呢?



下面哪个程序跑得更快?

```
AtomicIntegerFieldUpdater state = ...

public void lock() {
   while(state.getAndSet(true)) {}; //spin
}
```

```
AtomicIntegerFieldUpdater state= ...
public void lock() {
   while (true) {
     while(state.get()) {}; //spin
     if(!state.getAndSet(true))
        return;
   }
}
```

如果换成多线程呢?



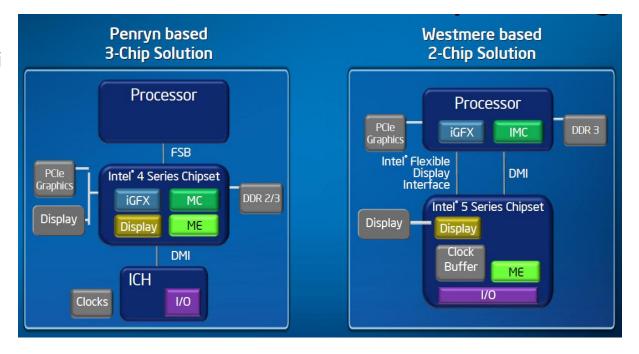
Intel 十年计划:Tick-Tock

Intel® Core® Microarchitecture		Intel® Microarchitecture codename Nehalem		Future Intel® Microarchitecture
Мегот	Penryn	Nehalem	Westmere	Sandy Bridge
NEW Microarchitecture 65nm	NEW Process Technology 45nm	NEW Microarchitecture 45nm	NEW Process Technology 32nm	NEW Microarchitecture 32nm
тоск	TICK	тоск	TICK	тоск
	1 -		Forecast	



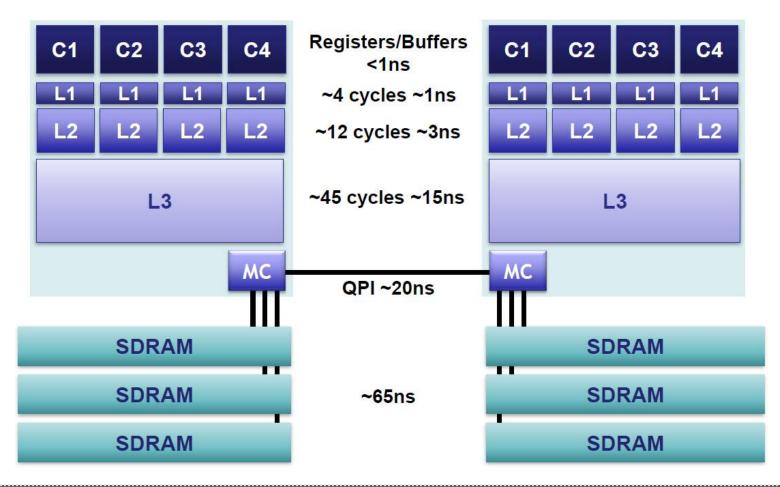
CPU微架构变革

- Hyper-threading
- 32KB L1d 与32KB L1i
- 256KB L2 Cache
- 4–12 MB L3 cache
- QPI 代替FSB
- PCI E和DMI整合入 处理器, 北桥消失
- 支持 2/3通道DDR3



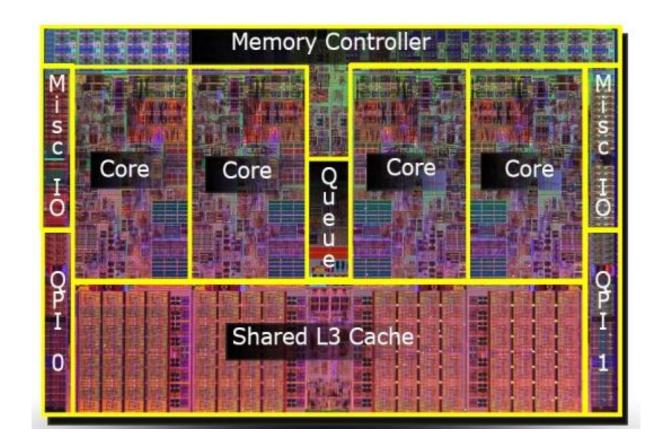


现代CPU微架构



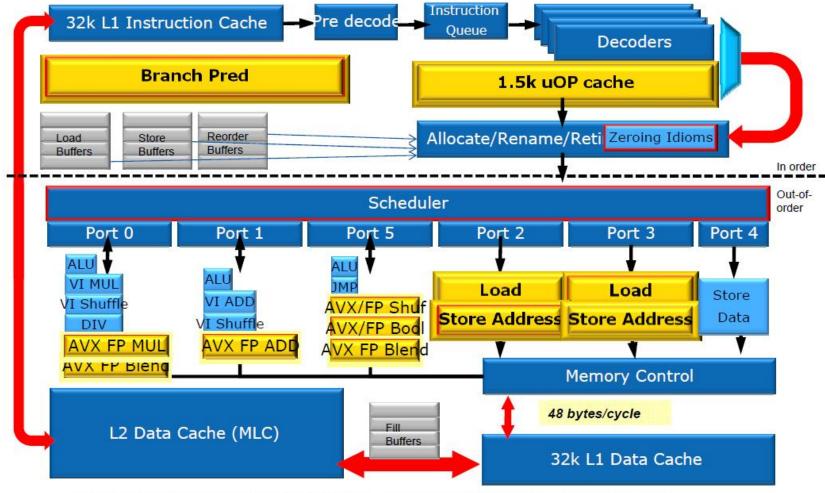


Intel Nehalem 排布





Intel Sandy Bridge



Sandy Bridge - Intel® Next Generation Microarchitecture

AVX= Intel® Advanced Vector Extensions (Intel® AVX)



下面哪个程序跑得更快?

```
private static long[][] longs;

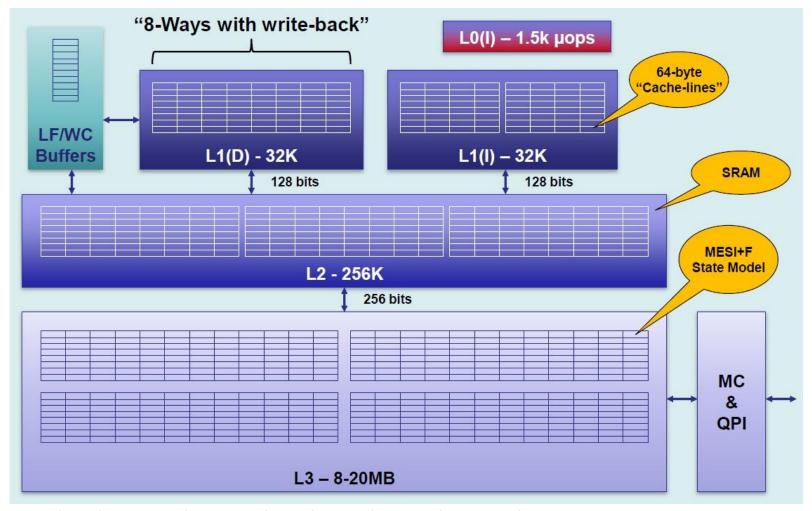
for (int i = 0; i < DIMENSION_1; i++) {
    for (int j = 0; j < DIMENSION_2; j++) {
        sum += longs[i][j];
     }
}</pre>
```

```
private static long[][] longs;

for (int j = 0; j < DIMENSION_2; j++) {
    for (int i = 0; i < DIMENSION_1; i++){
        sum += longs[i][j];
    }
}</pre>
```



CPU Cache



cat /sys/devices/system/cpu/cpu0/cache/index0/*



Cache Coherence & MESI协议

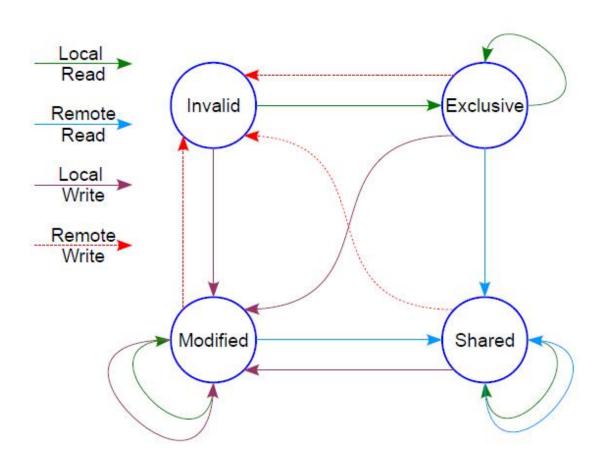
M: 修改

• E:独占

S:共享

• |:失效

发音: messy



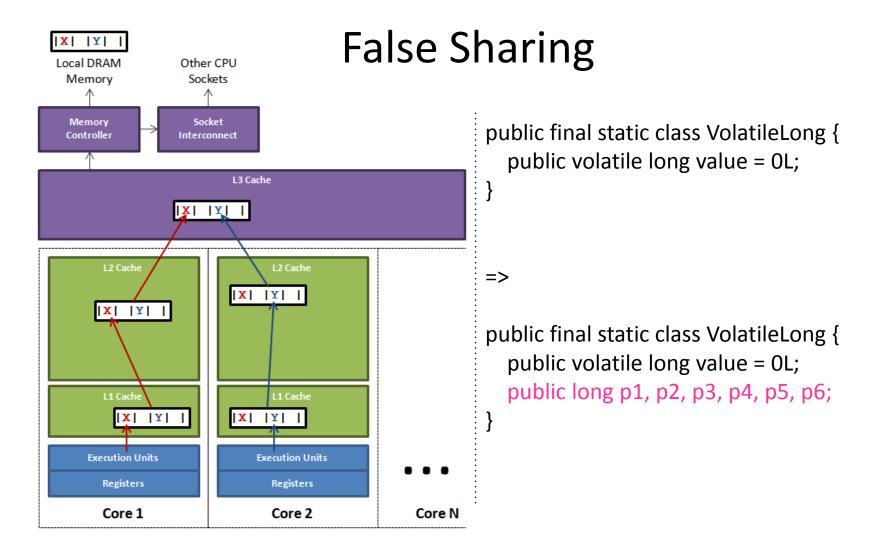


下面程序有什么问题?

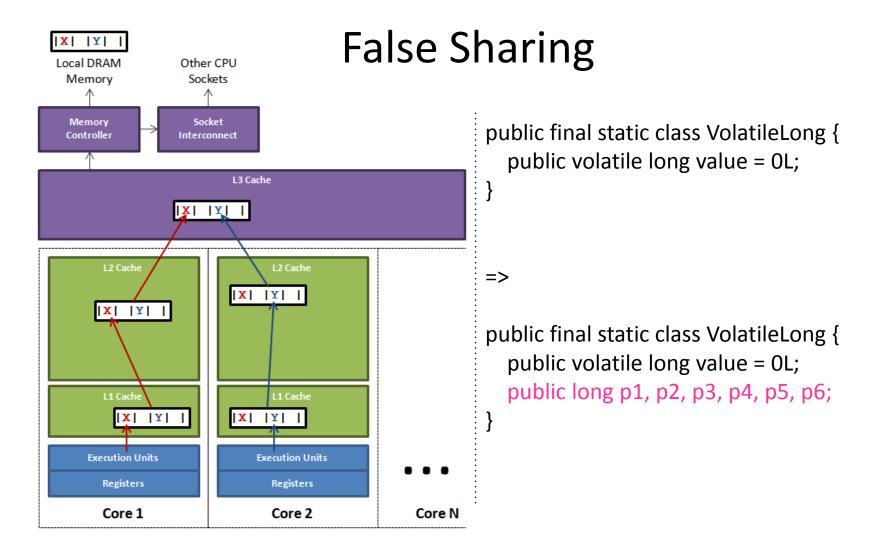
```
public final static class VolatileLong {
  public volatile long value = 0L;
public class FS implements Runnable {
  public void run() {
    long i = ITERATIONS + 1;
    while (0 != --i) {
       longs[arrayIndex].value = i;
```

```
longs = new VolatileLong[NUM THREADS];
for (int i = 0; i < longs.length; i++) {
  longs[i] = new VolatileLong();
// 每个线程更新独立的变量
for (int i = 0; i < NUM THREADS; i++) {
  threads[i] = new Thread(new FS(i)));
for (Thread t : threads) {
  t.start();
for (Thread t : threads) {
  t.join();
```

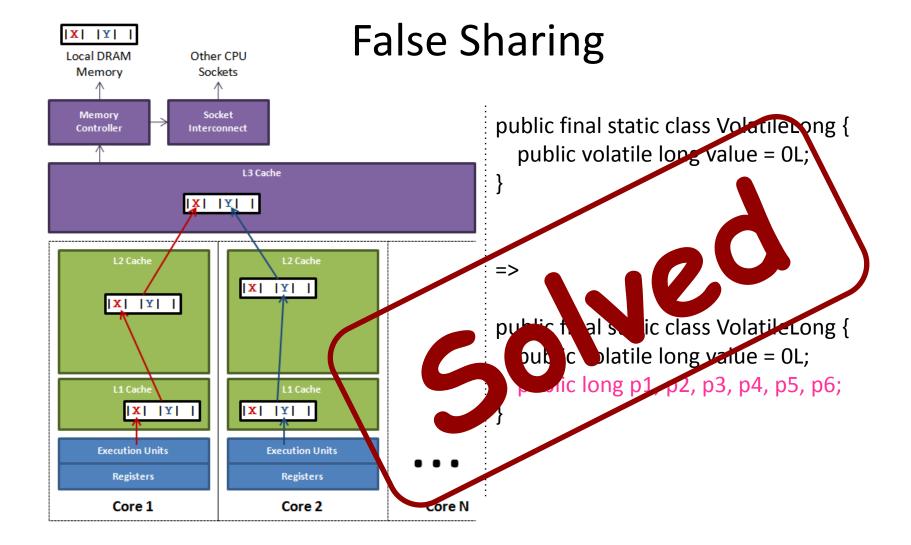








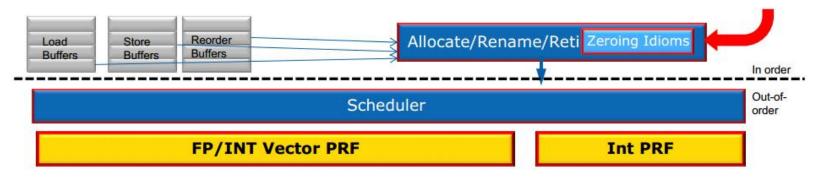






Cache Consistency & 乱序执行

• CPU指令重排序



• 编译重排序



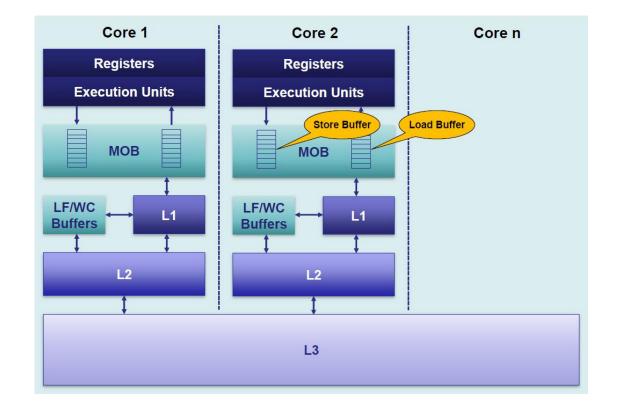
Memory Ordering

- 程序顺序(Program ordering): 读写和指令编制一致, 也称强顺序.
- 处理器顺序(Processor ordering): 加快指令执行速度, 例如读可跨越它之前的buffered写
- Intel386及之前内存顺序模型:程序顺序
- Pentium和Intel486内存顺序模型:大多数情况下遵循程序顺序
- P6及以后內存顺序模型:处理器顺序,同时提供其它加强或弱化內存顺序模型的特殊指令



内存屏障

- Load Buffer
- Store Buffer
- CPU串行化指令
 - CPUID
 - SFENCE
 - LFENCE
 - MFENCE
- Lock系指令





Java内存模型

- Happens-Before
- StoreStore
- LoadStore
- StoreLoad
- LoadLoad
- Full Fence
- 锁和synchronized块
- volatile 关键字
- final 关键字

```
// Lock
pthread mutex lock(&lock);
sequence = i;
pthread cond signal(&condition);
pthread mutex unlock(&lock);
// Soft Barrier
asm volatile("" ::: "memory");
sequence = i;
// Fence
asm volatile("" ::: "memory");
sequence = i;
asm volatile("lock addl $0x0,(%rsp)");
```



Java内存模型

重排序	次操作				
首操作	Normal Load Normal Store	Volatile Load Monitor Enter	Volatile Store Monitor Exit		
Normal Load Normal Store			No		
Volatile Load Monitor Enter	No	No	No		
Volatile store Monitor Exit		No	No		

需要内存屏 障	次操作				
首操作	Normal Load	Normal Store	Volatile Load MonitorEnt er	Volatile Store	
Normal Load				LoadStore	
Normal Store				StoreStore	
Volatile Load MonitorEnter	LoadLoad	LoadStore	LoadLoad	LoadStore	
Volatile Store MonitorExit			StoreLoad	StoreStore	



Example

```
$ java -XX:+UnlockDiagnosticVMOptions -XX:PrintAssemblyOptions=hsdis-print-bytes -
1. class X {
2.
     int a, b;
                                   XX:CompileCommand=print,X.f X
     volatile int v, u;
3.
     void f() {
4.
5.
        int i, j;
6.
                                   [Verified Entry Point]
        i = a; // load a
7.
                                    0xb3a1e28c: push %ebp ;...55
        j = b; // load b
8.
                                    0xb3a1e28d: sub $0x8,%esp ;...81ec0800 0000
        i = v; // load v
9.
                                    0xb3a1e293: mov 0x10(\%ecx),\%ebx :...8b5910 ; i = v
10.
                // LoadLoad
                                    0xb3a1e296: mov 0x14(%ecx), %edi ; ...8b7914 ; j = u
        i = u; // load u
11.
                                    0xb3a1e299: mov %ebx,0x8(%ecx) ;...895908
12.
                // LoadStore
                                                                               ; a = i
        a = i; // store a
13.
                                    0xb3a1e29c: mov %edi,0xc(%ecx) ;...89790c
                                                                               ; b = i
14.
        b = i; // store b
                                    0xb3a1e29f: mov %ebx,0x10(%ecx) ;...895910
                                                                               ; v = i
15.
                // StoreStore
                                    0xb3a1e2a2: mov %edi,0x14(%ecx) ;...897914
                                                                               ; u = j
        v = i; // store v
16.
                                    0xb3a1e2a5: lock addl $0x0,(%esp);...f0830424; memory barrier
17.
                 // StoreStore
                                    0xb3a1e2aa: mov 0x14(\%ecx),\%ebp ;...8b6914 ; i = u
18.
        u = i; // store u
                                    0xb3a1e2ad: mov %ebp,0x8(%ecx) ;...896908
                                                                               : a = i
19.
                 // StoreLoad
                                    0xb3a1e2b0: add $0x8,%esp ;...83c408
20.
        i = u; // load u
                                    0xb3a1e2b3: pop %ebp ;...5d
21.
                // LoadLoad
                                    0xb3a1e2b4: test %eax,0xb78ab000 ;...850500b0 8ab7
22.
                // LoadStore
23.
        j = b; // load b
24.
        a = i; // store a
25.
26.}
```

参考: jdk/hotspot/src/os_cpu/linux_x86/vm/orderAccess_linux_x86.inline.hpp



为什么有volatile还需要AtomicXX及 Unsafe.compareAndSwapXX?





原子指令

- CompareAndSwap: LOCK XCHG
- LOCK XADD
- ABA问题



让步锁

```
public class BackoffLock {
  private AtomicBoolean state = new
AtomicBoolean(false);
  private static final int MIN_DELAY = ...;
  private static final int MAX_DELAY = ...;

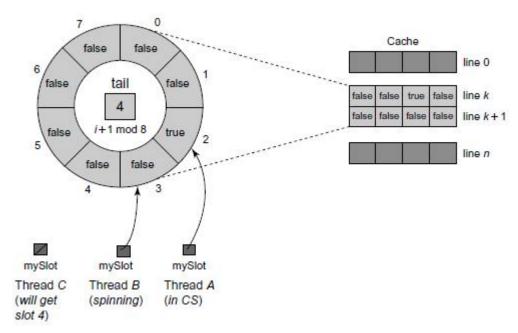
public void lock() {
   Backoff backoff = new Backoff(MIN_DELAY,
   MAX_DELAY);
   while (true) {
     while (state.get()) {};
}
```

```
if (!state.getAndSet(true)) {
    return;
    } else {
       backoff.backoff();
    }
  }
  public void unlock() {
    state.set(false);
  }
```



队列锁

- BackOff锁的问题
 - Cache-coherence Traffic
 - 临界区利用率
 - 公平性问题
 - 饥饿
- 基于数组的队列
- CLH队列
- MCS队列
- NUMA-Aware变种



https://blogs.oracle.com/dave/entry/flat_combining_numa_locks



为什么j.u.c或者jvm里面在加锁的时候,喜欢用先 CAS spin尝试N次,如果失败则yield多次(可选),如果 最后还是失败则park,同时把线程加到队列里?



- top
- vmstat
- Iscpu
- perf
- Valgrind tools suite
- OProfile
- SystemTap
- numactl
- Intel Vtune
- MAT

工具





推荐读物

- What every programmer should know about memory
- Intel® 64 and IA-32 Architectures Software Developer Manuals
- The Art of Multiprocessor Programming
- The JSR-133 Cookbook for Compiler Writers (Java Memory Model)
- 本人博客: http://coderplay.javaeye.com



Q & A



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