0x00	**CNT**	**Description**	
0..15		Counter Value	VE9x, VE4, VE214, VE234, VC1
0..31			VE1,VE3
	0x00000000	**ResetValue**	
	0xFFFF/0xFFFFFFFF	**MaskValue**	
0x04	**PSG**	**Description**	
0..15		CLK = TIM_CLK/ (PSG + 1)	
	0x00000000	**ResetValue**	
	0x0000FFFF	**MaskValue**	
0x08	**ARR**	**Description**	
0..15		Period Value	VE9x, VE4, VE214, VE234, VC1
0..31			VE1,VE3
	0x00000000	**ResetValue**	
	0xFFFF/0xFFFFFFFF	**MaskValue**	
0x0C	**CNTRL**	**Description**	
0	CNT_EN	1: Timer Enable	
1	ARRB_EN	1: ARR update on CNT completed. 0: Immediately	
2	WR_CMPL	1: writing, 0: write completed - for CNT, PSG, ARR	
3	DIR	0: Up, 1: Down - count	
4..5	FDTS	0: 1, 2, 3, 4 - F_Input_Sample = TIM_CLOCKs / FDTS	
6..7	CNT_MODE	b00: by DIR, b01: Up-Down - by TIM_CLOCK	
		b10: by DIR, b11: Up-Down by - by ExtEvents	
		b1x: by DIR - ExtEvents	VE1,VE3
8..11	EVENT_SEL	0: Rise of TIM_Clock	
		1, 2, 3, 10: CNT=ARR Tim1, Tim2, Tim3, Tim4	VE1,VE3
		4, 5, 6, 7: Event in Ch1, Ch2, Ch3, Ch4	
		8, 9: ETR Rise, Fall	VE1,VE3
	0x00000000	**ResetValue**	
	0x00000FFF	**MaskValue**	
0x10	**CCR1**	**Description**	
0x14	**CCR2**		**Нет в VK214**
0x18	**CCR3**		**Нет в VK214**
0x1C	**CCR4**		**Нет в VK214**
0..15		Captured/PWM CNT Value	VE9x, VE4, VE214, VE234, VC1
0..31			VE1,VE3
	0x00000000	**ResetValue**	
	0xFFFF/0xFFFFFFFF	**MaskValue**	
0x20	**CH1_CNTRL**	**Description**	
0x24	**CH2_CNTRL**	*Capture / PWM - CCR control*	**Нет в VK214**
0x28	**CH3_CNTRL**		**Нет в VK214**
0x2C	**CH4_CNTRL**		**Нет в VK214**
0..3	CHFLTR	*Input Rise/Fall duration to rise Event*	
		0,1,2,3: - 1,2,4,8 periods of TIM_Clock,	
		4,5: - 6, 8 periods of FDTS/2	
		6,7: - 6, 8 periods of FDTS/4	
		8,9: - 6, 8 periods of FDTS/8	
		10,11,12: - 5, 6, 8 periods of FDTS/16	
		13,14,15: - 5, 6, 8 periods of FDTS/32	
4..5	CHSEL	*Event to Fix in CCR*	
		0 - Input Rise	
		1 - Input Fall	
		2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4	
		3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4	
6..7	CHPSC	*CCR Capture Event prescaller*	
		0: div1, div2, div4, div8	
8	OCCE	1: ETR Enable	
9..11	OCCM	*PWM - REF Generate Mode*	
		0, 4: - const REF = 0	
		5: - const REF = 1	
		1: REF=1 - on (CNT = CCR) || (CNT = CCR1)	
		2: REF=0 - on (CNT = CCR) || (CNT = CCR1)	
		3: REF Switch - on (CNT = CCR) || (CNT = CCR1)	
		CCR1_EN = 0	
		6: REF=1 - while (CNT < CCR)	
		7: REF=0 - while (CNT < CCR)	
		CCR1_EN = 1	
		6: REF=!DIR - while CNT in [CCR..CCR1], UP is DIR=0	
		7: REF=DIR - while CNT in [CCR..CCR1]	
12	BRKEN	1: Enable Clear Ref by BRK - Ref = 0	

13	ETREN	1: Enable Clear Ref by ETR - Ref = 0	
14	WR_CMPL	1: CCR Writing 0: Can write CCR	
15	CAP_nPWM	0: PWM, 1: CAP - channel mode	
	0x00000000	**ResetValue**	
	0xFFFF	**MaskValue**	
0x30	**CH1_CNTRL1**	**Description**	
0x34	**CH2_CNTRL1**	*PWM driver control*	**Нет в VK214**
0x38	**CH3_CNTRL1**		**Нет в VK214**
0x3C	**CH4_CNTRL1**		**Нет в VK214**
0..1	SELOE	0: Pin_OE = 0 - Pin is IN	
		1: Pin_OE = 1 - Pin is OUT	
		3: Pin_OE = by REF - Pin is IN / OUT	
		4: Pin_OE = by DTG	
2..3	SELO	0: CHx_out = 0, 1, Ref, DTG	
4	INV	1: Invert output	
5..7	-		
8..9	NSELOE	SELOE for nCH	
10..11	NSELO	SELO for nCH	
12	NINV	INV for nCH	
	0x00000000	**ResetValue**	
	0x1F1F	**MaskValue**	
0x40	**CH1_DTG**	**Description**	
0x44	**CH2_DTG**		**Нет в VK214**
0x48	**CH2_DTG**		**Нет в VK214**
0x4C	**CH2_DTG**		**Нет в VK214**
0..3	DTG	DTG frequency Prescaller	
4	EDTS	0: TIM_CLOCK, 1: FDTS - DTG Clock Select	
5..7	-		
8..15	DTGx	DTG_Delay = DTGx*(DTG+1)	
	0x00000000	**ResetValue**	
	0xFF1F	**MaskValue**	
0x50	**BRKETR_CNTRL**	**Description**	
0	BRK_INV	1: Inv Enable	
1	ETR_INV	1: Inv Enable	
2..3	ETR_PSC	0: div1, div2, div4, div8 - External Clock Div	
4..7	ETR_FILTER	Like CHx_Contorl.CHFLTR	
	0x00000000	**ResetValue**	
	0x00FF	**MaskValue**	
0x54	**STATUS**	**Status flags**	
0x58	**IE**	**IRQ enable flags**	
0x5C	**DMA_RE**	**DMA request enable**	
0	CNT_ZERO	1: CNT=0 - wr 0 to clear	
1	CNT_ARR	1: CNT=ARR - wr 0 to clear	
2	ETR_RE	1: ETR Rise front - wr 0 to clear	
3	ETR_FE	1: ETR Fall front - wr 0 to clear	
4	BRK	1: BRK=1, wr 0 to clear (1 - Active)	
5..8	CCR_CAP_CH1,2,3,4	1: CCR Captured, wr 0 to clear	
9..12	CCR_REF_CH1,2,3,4	1: PWM REF Front, wr 0 to clear	
13..16	CCR1_CAP_CH1,2,3,4	1: CCR1 Captured, wr 0 to clear	
	0x00000000	**ResetValue**	
	0x0001FFFF	**MaskValue**	
0x60	**CH1_CNTRL2**	**Description**	
0x64	**CH2_CNTRL2**	*CCR1 Contorl*	**Нет в VK214**
0x68	**CH3_CNTRL2**		**Нет в VK214**
0x6C	**CH4_CNTRL2**		**Нет в VK214**
0..1	CHSEL1	Like CHx_CNTRL1.CHSEL - Sel input to capture	
2	CCR1_EN	1: CCR1 Enable	
3	CCRRLD	0: Immediately, 1: on CNT = 0 - CCR and CCR1 update mode	
	0x00000000	**ResetValue**	
	0x000F	**MaskValue**	
0x70	**CCR11**	**Description**	
0x74	**CCR21**		**Нет в VK214**
0x78	**CCR31**		**Нет в VK214**
0x7C	**CCR41**		**Нет в VK214**
0..15		Captured/PWM CNT Value	VE9x, VE4, VE214, VE234, VC1
0..31			VE1,VE3
	0x00000000	**ResetValue**	
	0xFFFF/0xFFFFFFFF	**MaskValue**	

0x80	**DMA_RE1**	**DMA request enable -** *for Channel1*	VE1,VE3
0x84	**DMA_RE2**	*- for Channel2*	VE1,VE3
0x88	**DMA_RE3**	*- for Channel3*	VE1,VE3
0x8C	**DMA_RE4**	*- for Channel4*	VE1,VE3
…	…	LIKE DMA_RE	
	0x00000000	**ResetValue**	
	0x0001FFFF	**MaskValue**	

		BE1	**BE3**	**BE9x**	**ВЦ1901**	**BE4**	**BK214**	**BE234**
Base Addr								
	Timer1	0x4007_0000	0x4007_0000	0x4007_0000	0x4007_0000	0x4007_0000	0x4007_0000	0x4007_0000
	Timer2	0x4007_8000	0x4007_8000	0x4007_8000	0x4007_8000	0x4007_8000	0x4007_8000	0x4007_8000
	Timer3	0x4008_0000	0x4008_0000	0x4008_0000	0x4008_0000	-	-	-
	Timer4	0x4009_8000	0x4009_8000	-	-	-	-	-