Addr Shift	Regs	Access	BE1	BE3	BE9x	ВЦ1901	BE4	BK214	BE234	
0x00	DR		+	+	+	+	+	+	+	Data Register
0x04	RSR_ECR		+	+	+	+	+	+	+	ReceiveStatus Register_ErrorClearRegister
0x08 - 0x014	-									
0x18	FR	RO	+	+	+	+	+	+	+	Flag Register
0x1C	-									
0x20	ILPR		+	+	+	+	+	+	+	Status Register
0x24	IBRD		+	+	+	+	+	+	+	Clock Prescale Register
0x28	FBRD		+	+	+	+	+	+	+	Interrupt Mask Set/Clear Register
0x2C	LCR_H		+	+	+	+	+	+	+	Raw Interrupt Status Register
0x30	CR		+	+	+	+	+	+	+	Masked Interrupt Status Register
0x34	IFLS		+	+	+	+	+	+	+	Interrupt Clear Register
0x38	IMSC		+	+	+	+	+	+	+	MDA Control Register
0x3C	RIS	RO	+	+	+	+	+	+	+	MDA Control Register
0x40	MIS	RO	+	+	+	+	+	+	+	MDA Control Register
0x44	ICR	WO	+	+	+	+	+	+	+	MDA Control Register
0x48	DMACR		+	+	+	+	+	+	+	MDA Control Register
0x4C-0x7C	-									
0x80	TCR		+	+	-	-	+	+	+	MDA Control Register
Base Addr										
	UART1		0x4003_0000	0x4003_0000	0x4003_0000	0x4003_0000	0x4000_8000	0x4000_8000	0x4000_8000	
	UART2		0x4003_8000	0x4003_8000	0x4003_8000	0x4003_8000	0x4001_0000	0x4001_0000	0x4001_0000	
	UART3		-	0x4012_0000	-	0x400D_0000	-	-	-	
	UART4		-	0x4012_8000	-	-	-	-	-	

0x00	**DR**	**Data Regiter**	
0..7	Data	WR/RD FIFO	
8	FE	Framing Error	1: Error (Incorrect Stop bit)
9	PE	Parity Error	1: Error (Incorrect Parity bit)
10	BE	Break Error	1: Error (RX signal = LOW for full word time)
11	OE	Overrun Error	1: Error, new data received but FIFO is full
		0x00000000	**ResetValue**
		0x00000FFF	**MaskValue**
0x04	**RSR_ECR**	**ReceiveStatus Register_ErrorClearRegister**	
0	FE	Framing Error	1: Error (Incorrect Stop bit)
1	PE	Parity Error	1: Error (Incorrect Parity bit)
2	BE	Break Error	1: Error (RX signal = LOW for full word time)
3	OE	Overrun Error	1: Error, new data received but FIFO is full
		0x00000000	**ResetValue**
		0x00000004	**MaskValue**
			Updates by reading from DR, Read DR first!
			Write to clear bits!
0x018	**FR**	**Flag Regiter**	**RO**
0	CTS	Clear To Send	1: Modem nCTS is LOW
1	DSR	Data Set Ready	1: Modem nDSR is LOW
2	DCD	Data Carrier Detect	1: Modem nDCD is LOW
3	BUSY	Busy	1: Trasmitting data
4	RXFE	RX FIFO Empty	1: Empty
5	TXFF	TX FIFO Full	1: Full
6	RXFF	RX FIFO Full	1: Full
7	TXFE	TX FIFO Empty	1: Empty
8	RI	Ring Indicator	1: Modem nRI is LOW
		0x00000000	**ResetValue**
		0x000001FF	**MaskValue**
0x020	**ILPR**	**IrDA Low-Power Counter register**	
0..7	DVSR	DivSampleRate	DVSR = Fuart_clk/Firlp_baud16 = Fuart_clk/1,8432MHz
			(1,42MHz < Firlp_baud16 < 2,2MHz)
			0 - disable (reset state)
		0x00000000	**ResetValue**
		0x000000FF	**MaskValue**
0x024	**IBRD**	**Integer Part of Baud Rate Divisor - UARTLCR[15..0]**	
0..15	Baud_DivInt		Integer part of Rate divisor
		0x00000000	**ResetValue**
		0x0000FFFF	**MaskValue**
0x028	**FBRD**	**Fractional Part of Baud Rate Divisor - UARTLCR[21..16]**	
0..5	Baud_DivFrac		Fractional part of Rate divisor
		0x00000000	**ResetValue**
		0x0000003F	**MaskValue**
			BaudDiv = int + (frac/64) = Fuart_clk/(16*BaudRate)
0x02C	**LCR_H**	**Line Control Register - UARTLCR[29..22]**	
0	BRK	Send Break	0: normal 1: Send LOW for 2 words
1	PEN	Parity Enable	1: enable parity
2	EPS	Even Parity Select	0: Odd parity, 1: Even parity
3	STP2	Two stop bits	1: TX two stop bits. **RX- does not check two stops!**
4	FEN	FIFO Enable	1:Enable **FIFO 16 words**, 0: FIFO - 1 word length - **Flush FIFO_TX!**
5..6	WLEN	Word Length	b00: 5, 6, 7, 8 - bits
7	SPS	Stick parity select	0: disabled, 1: Fixed - inversed of EPS value
			Write after FBRD and/or IFBR - apply by CLR_H write strobe
		0x00000000	**ResetValue**
		0x000000FF	**MaskValue**
0x030	**CR**	**Control Register**	
0	EN	Enable	1: enable
1	SIREN	SIR Enable	1: enable
2	SIRLP	SIR Low-Power	1: enable
3..6			
7	LBE	LoopBack Enable	1: enable
8	TXE	Transmit Enable	
9	RXE	Receive Enable	
10	DTR	Data Transmit Ready	1: DTS sets to LOW
11	RTS	Request to Send	1: RTS sets to LOW
12	Out1	Modem custom	1: set to LOW (for example DCD line)
13	Out2	Modem custom	1: set to LOW (for example RI line)

14	RTSEn	RTS hardware flow	1: enable (will be active when FIFO_RX has space)
15	CTSEn	CTS hardware flow	1: enable (will transfer when RTS is active)
		0x00000000	**ResetValue**
		0x0000FF87	**MaskValue**
0x034	**IFLS**	**Interrupt FIFO Level Select**	
0..2	TXIFLSEL	IRQ Level <= FIFO_TX	0: <= 2, 4, 8, 12, 14
3..5	RXIFLSEL	IRQ Level >= FIFO_RX	0: >= 2, 4, 8, 12, 14
		0x00000000	**ResetValue**
		0x0000003F	**MaskValue**
0x038	**IMSC**	**IRQ Mask Set/Clear register**	
0	RIMIM	RI line event	1: IRQ enable, write 0 to clear
1	CTSMIM	CTS line event	1: IRQ enable, write 0 to clear
2	DCDMIM	DCD line event	1: IRQ enable, write 0 to clear
3	DSRMIM	DSR line event	1: IRQ enable, write 0 to clear
4	RXIM	Data received	1: IRQ enable, write 0 to clear
5	TXIM	Data transmited	1: IRQ enable, write 0 to clear
6	RTIM	**RX timeout for 32 bit**	1: IRQ enable, write 0 to clear (for **FIFO_RX not empty!**)
7	FEIM	Frame Error event	1: IRQ enable, write 0 to clear
8	PEIM	Parity Error event	1: IRQ enable, write 0 to clear
9	BEIM	Break Error event	1: IRQ enable, write 0 to clear
10	OEIM	Overrun FIFO_RX event	1: IRQ enable, write 0 to clear
		0x00000000	**ResetValue**
		0x000007FF	**MaskValue**
0x03C	**RIS**	**Raw Interrupt Status register RO**	
0	RIMRIS	RI line event	1: Event Active
1	CTSMRIS	CTS line event	1: Event Active
2	DCDMRIS	DCD line event	1: Event Active
3	DSRMRIS	DSR line event	1: Event Active
4	RXRIS	Data received	1: Event Active
5	TXRIS	Data transmited	1: Event Active
6	RTRIS	RX timeout for 32 bit	1: Event Active
7	FERIS	Frame Error event	1: Event Active
8	PERIS	Parity Error event	1: Event Active
9	BERIS	Break Error event	1: Event Active
10	OERIS	Overrun RX Error event	1: Event Active
		0x00000000	**ResetValue**
		0x000007FF	**MaskValue**
0x040	**MIS**	**Masked Interrupt Status register RO**	
0	RIMMIS	RI line event	1: Event Active
1	CTSMMIS	CTS line event	1: Event Active
2	DCDMMIS	DCD line event	1: Event Active
3	DSRMMIS	DSR line event	1: Event Active
4	RXMIS	Data received	1: Event Active
5	TXMIS	Data transmited	1: Event Active
6	RTMIS	RX timeout for 32 bit	1: Event Active
7	FEMIS	Frame Error event	1: Event Active
8	PEMIS	Parity Error event	1: Event Active
9	BEMIS	Break Error event	1: Event Active
10	OEMIS	Overrun RX Error event	1: Event Active
		0x00000000	**ResetValue**
		0x000007FF	**MaskValue**
0x044	**ICR**	**Interrupt Clear register - WO**	
0	RIMIC	RI line event	1: clear
1	CTSMIC	CTS line event	1: clear
2	DCDMIC	DCD line event	1: clear
3	DSRMIC	DSR line event	1: clear
4	RXIC	Data received	1: clear
5	TXIC	Data transmited	1: clear
6	RTIC	RX timeout for 32 bit	1: clear
7	FEIC	Frame Error event	1: clear
8	PEIC	Parity Error event	1: clear
9	BEIC	Break Error event	1: clear
10	OEIC	Overrun RX Error event	1: clear
		0x00000000	**ResetValue**
		0x000007FF	**MaskValue**
0x048	**DMACR**	**DMA Control Register**	
0	RXDMAE	RX DMA Enable	1: Enable
1	TXDMAE	TX DMA Enable	1: Enable

2	DMAONERR		1: Disable Sreq/Req if UART has Error
		0x00000000	**ResetValue**
		0x00000007	**MaskValue**
0x080	**TCR**	**Test Control Register**	
0	ITEN	Test Mode Enable	1: Enable
1	TESTFIFO	WR to FIFO_Rx, RD from TX	1: Enable
2	SIRTEST	IrDA read transmitter	1: Enable (**use LBE!**)