Bits	Fields	BE1	BE3	BE9x	BE4	BK214	BE234	ВЦ1901	
x00	**CLOCK_STATUS**								
0	PLL_USB_RDY	+	+	+	-	-	-	+	
1	PLL_CPU_RDY	+	+	+	+	+	+	+	
2	HSE_RDY	+	+	+	+	+	+	+	
3	HSE2_RDY	+	+	-	-	-	-	PLL_DSP_RDY	
		0	***0***	***0***	***0***	***0***	***0***	***0***	***ResetValye***
		0xF	***0xF***	***0x7***	***0x6***	***0x6***	***0x6***	***0xF***	***MaskValue***
x04	**PLL_CONTROL**								
0	PLL_USB_ON	+	+	+	-	-	-	+	
1	PLL_USB_RLD	+	+	+	-	-	-	+	
2	PLL_CPU_ON	+	+	+	+	+	+	+	
3	PLL_CPU_RLD	+	+	+	+	+	+	+	
4..7	PLL_USB_MUL	+	+	+	-	-	-	+	
8..11	PLL_CPU_MUL	+	+	+	+	+	+	+	
16	PLL_DSP_ON	-	-	-	-	-	-	+	
17	PLL_DSP_PLD	-	-	-	-	-	-	+	
20..23	PLL_DSP_MUL	-	-	-	-	-	-	+	
		0	***0***	***0***	***0***	***0***	***0***	***0***	***ResetValye***
		0x0FFF	***0x0FFF***	***0x0FFF***	***0x020C***	***0x020C***	***0x020C***	***0x00F30FFF***	***MaskValue***
x08	**HS_CONTROL**								
0	HSE_ON	+	+	+	+	+	+	+	
1	HSE_BYP	+	+	+	+	+	+	+	
2	HSE2_ON	+	+	-	-	-	-	-	
3	HSE2_BYP	+	+	-	-	-	-	-	
		0	***0***	***0***	***0***	***0***	***0***	***0***	***ResetValye***
		0xF	***0xF***	***0x3***	***0x3***	***0x3***	***0x3***	***0x3***	***MaskValue***
0x0C	**CPU_CLOCK**								
0..1	CPU_C1_SEL	+	+	+	+	+	+	+	HSI, HSI/2, HSE, HSE/2
2	CPU_C2_SEL	+	+	+	+	+	+	+	CPU_C1, PLLCPU0
3	-								
4..7	CPU_C3_SEL	+	+	+	+	+	+	+	/1, /2, /4, .. /256
8..9	HCLK_SEL	+	+	+	+	+	+	+	HSI, CPU_C3, LSE, LSI
		0	***0***	***0***	***0***	***0***	***0***	***0***	***ResetValye***
		0x3F7	***0x3F7***	***0x3F7***	***0x3F7***	***0x3F7***	***0x3F7***	***0x3F7***	***MaskValue***
0x10	**USB_CLOCK**	**+**	**+**	**+**	**-**	**-**	**-**		
0..1	USB_C1_SEL	+	+	+	-	-	-	+	HSI, HSI/2, HSE, HSE/2
2	USB_C2_SEL	+	+	+	-	-	-	+	CPU_C1, PLLUSB0
3	-								
4	USB_C3_SEL	+	+	+	-	-	-	+	USB_C2, USB_C2/2
5..7	-								
8	USB_CLK_EN	+	+	+	-	-	-	+	
		0	***0***	***0***				***0***	***ResetValye***
		0x117	***0x117***	***0x117***				***0x117***	***MaskValue***

0x10	PER1_CLOCK	-	-	-	+	+	+	-	
0..1	PER1_C1_SEL	-	-	-	+	+	+	-	LSI, LSI/2, LSE, LSE/2
2..3	PER1_C2_SEL	-	-	-	+	TIM1_C2_SEL	+	-	CPU_C1, PER1_C1, PLLCPUo, HSI_C1
4	DEBUG_EN	-	-	-	+	+	+	-	
5	DMA_EN	-	-	-	+	-	+	-	
6..7	TIM2_C2_SEL	-	-	-	-	+	-	-	CPU_C1, PER1_C1, PLLCPUo, HSI_C1
8..9	UART1_C2_SEL	-	-	-	-	+	-	-	CPU_C1, PER1_C1, PLLCPUo, HSI_C1
10..11	UART2_C2_SEL	-	-	-	-	+	-	-	CPU_C1, PER1_C1, PLLCPUo, HSI_C1
12..13	SSP_C2_SEL	-	-	-	-	+	-	-	CPU_C1, PER1_C1, PLLCPUo, HSI_C1
					0	***0***	***0***		***ResetValye***
					0x3F	***0x3FDF***	***0x3F***		***MaskValue***
0x14	**ADC_CLOCK**				-	-	-		
0..1	ADC_C1_SEL	+	+	+	-	-	-	+	CPU_C1, USB_C1, CPU_C2, USB_C2
2..3									
4..5	ADC_C2_SEL	+	+	+	-	-	-	+	LSE, LSI, ADC_C1, HSI_C1
6..7									
8..11	ADC_C3_SEL	+	+	+	-	-	-	+	ADC_C2/1, /2, /4, .. /256
12									
13	ADC_CLK_EN	+	+	+	-	-	-	+	
14..15									
16..17	AUC_C1_SEL	-	+	-	-	-	-	+	HSI, HSI/2, HSE, HSE/2
18..19									
20..21	AUC_C2_SEL	-	+	-	-	-	-	+	AUC_C1, PLLCPUo, PLLUSBo, 0
22..23									
24..27	AUC_C3_SEL	-	+	-	-	-	-	+	AUC_C2/1, /2, /4, .. /256
28..30									
31	AUC_CLK_EN	-	+	-	-	-	-	+	
		0	***0***	***0***				***0***	***ResetValye***
		0x2F33	***0x8F332F33***	***0x2F33***				***0x8F332F33***	***MaskValue***
0x14	**ADC_CLOCK**	-	-	-				-	
0..1	ADC_C1_SEL	-	-	-	+	+	+	-	CPU_C1, PER1_C1, PLLCPUo, HSI_C1
2..3	ADCIU_C1_SEL	-	-	-	+	+	+	-	CPU_C1, PER1_C1, PLLCPUo, HSI_C1
4..7	ADCIU_C3_SEL	-	-	-	+	+	+	-	ADCIU_C1/1, /2, /4, .. /256
8..11	ADC_C3_SEL	-	-	-	+	+	+	-	ADC_C1/1, /2, /4, .. /256
12	ADCIU_CLK_EN	-	-	-	+	+	+	-	
13	ADC_CLK_EN	-	-	-	+	+	+	-	
					0	***0***	***0***		***ResetValye***
					0x3FFF	***0x3FFF***	***0x3FFF***		***MaskValue***
0x18	**RTC_CLOCK**								
0..3	HSE_SEL	+	+	+	+	+	+	+	HSE/1, /2, /4, .. /256
4..7	HSI_SEL	+	+	+	+	+	+	+	HSI/1, /2, /4, .. /256
8	HSE_RTC_EN	+	+	+	+	+	+	+	
9	HSI_RTC_EN	+	+	+	+	+	+	+	
		0	***0***	***0***	***0***	***0***	***0***	***0***	***ResetValye***
		0x03FF	***0x03FF***	***0x03FF***	***0x03FF***	***0x03FF***	***0x03FF***	***0x03FF***	***MaskValue***
0x1C	**PER_CLOCK**				**PER2_CLOCK**				

0		CAN1			SPI			SSP3	
1		CAN2			UART1			SSP4	
2		USB			UART2			USB	
3		EEPROM							
4		RST_CLK							
5		DMA			-		DMA		
6		UART1		COMP	I2C	-		UART1	
7		UART2		DAC	LCD	-		UART2	
8		SPI1			ADC			SPI1	
9		MIL_B1	-		WWDT			SDIO	
10		MIL_B2	I2C		IWDT			I2C	
11		POWER							
12		WWDT			BKP			WWDT	
13		IWDT			ADCIU			IWDT	
14		TIMER1							
15		TIMER2							
16		TIMER3			PORT_A			TIMER3	
17		ADC			PORT_B			ADC	
18		DAC			PORT_C			DAC	
19		TIMER4	COMP	CRC	-	CRC		COMP	
20		SPI2		-	-	-		SPI2	
21		PORT_A		-	-	-		PORT_A	
22		PORT_B		-	-	-		PORT_B	
23		PORT_C		-	-	-		PORT_C	
24		PORT_D		-	-	-		PORT_D	
25		PORT_E		-	-	-		PORT_E	
26		ARC_RX	-	-	-	-		UART3	
27		BKP		-	-	-		BKP	
28		ARC_TX	-	-	-	-		AUC	
29		PORT_F		-	-	-		PORT_F	
30		EXT_BUS		-	-	-		EXT_BUS	
31		SPI3	-	-	-	-		CRYPTO	
		0x10							
		0x0010	***0x0010***	***0x0010***	***0x0010***	***0x0010***	***0x0010***	***0x0010***	***ResetValye***
		0xFFFFFFFF	***0xFFFFFFFF***	***0x6BFFFDFF***	***0x000FFFFF***	***0x0007FDFF***	***0x000FF3FF***	***0xFFFFFFFF***	***MaskValue***
0x20	**CAN_CLOCK**				**Reserved**				
0..2	CAN1_BRG	+	+	+	-	-	-	-	HCLK/1, /2, /4, .. /128
8..10	CAN2_BRG	+	+	+	-	-	-	-	HCLK/1, /2, /4, .. /128
16..18									
24	CAN1_CLK_EN	+	+	+	-	-	-	-	
25	CAN2_CLK_EN	+	+	+	-	-	-	-	
		0	***0***	***0***					***ResetValye***
		0x03000707	***0x03000707***	***0x03000707***					***MaskValue***
0x24	**TIM_CLOCK**	**f = HCLK**			**PER1_C2**	**TIMx_C2**	**PER1_C2**	**HCLK**	
0..2	TIM1_BRG	+	+	+	+	+	+	+	f/1, /2, /4, .. /128
8..10	TIM2_BRG	+	+	+	+	+	+	+	f/1, /2, /4, .. /128
16..18	TIM3_BRG	+	+	+	-	-	-	+	f/1, /2, /4, .. /128
24	TIM1_CLK_EN	+	+	+	+	+	+	+	f/1, /2, /4, .. /128

25	TIM2_CLK_EN	+	+	+	+	+	+	+	f/1, /2, /4, .. /128
26	TIM3_CLK_EN	+	+	+	-	-	-	+	f/1, /2, /4, .. /128
		0	***0***	***0***	***0***	***0***	***0***	***0***	***ResetValye***
		0x07070707	***0x07070707***	***0x07070707***	***0x03000707***	***0x03000707***	***0x03000707***	***0x07070707***	***MaskValue***
0x28	**UART_CLOCK**	**f = HCLK**			**PER1_C2**	**UARTx_C2**	**PER1_C2**	**HCLK**	
0..2	UART1_BRG	+	+	+	+	+	+	+	f/1, /2, /4, .. /128
8..10	UART2_BRG	+	+	+	+	+	+	+	f/1, /2, /4, .. /128
16..18	TIM4_BRG	+	+	-	-	-	-	UART3_BRG	f/1, /2, /4, .. /128
24	UART1_CLK_EN	+	+	+	+	+	+	+	
25	UART2_CLK_EN	+	+	+	+	+	+	+	
26	TIM4_CLK_EN	+	+	-	-	-	-	UART3_CLK_EN	
		0	***0***	***0***	***0***	***0***	***0***	***0***	***ResetValye***
		0x07070707	***0x07070707***	***0x03000707***	***0x03000707***	***0x03000707***	***0x03000707***	***0x07070707***	***MaskValue***
0x2C	**SSP_CLOCK**	**f = HCLK**			**PER1_C2**	**SSPx_C2**	**PER1_C2**	**HCLK**	
0..2	SSP1_BRG	+	+	+	+	+	+	+	f/1, /2, /4, .. /128
8..10	SSP2_BRG	+	+	+	-	-	-	+	f/1, /2, /4, .. /128
16..18	SSP3_BRG	+	+	+	-	-	-	+	f/1, /2, /4, .. /128
24	SSP1_CLK_EN	+	+	+	+	+	+	+	f/1, /2, /4, .. /128
25	SSP2_CLK_EN	+	+	+	-	-	-	+	f/1, /2, /4, .. /128
26	SSP3_CLK_EN	+	+	+	-	-	-	+	f/1, /2, /4, .. /128
		0	***0***	***0***	***0***	***0***	***0***	***0***	***ResetValye***
		0x07070707	***0x07070707***	***0x07070707***	***0x01000007***	***0x01000007***	***0x01000007***	***0x07070707***	***MaskValue***
				End addr = 0x30					
0x30	**DSP_CLOCK**	**-**	**-**						
0..1	DSP_C1_SEL	-	-					+	HSI, HSI/2, HSE, HSE/2
2	DSP_C2_SEL	-	-					+	DSP_C1, PLLDSP0
3	-								
4	DSP_C3_SEL	-	-					+	DSP_C2, DSP_C2/2
5..7	-								
8	DSP_CLK_EN	-	-					+	
								0	***ResetValye***
								0x117	***MaskValue***
0x34	**ETH_CLOCK**								
0..2	ETH_BRG	+	+						Always set 0
8..10	MAN_BRG	+	+						HCLK/1, /2, /4, .. /128
16..18	PHY_BRG	+	+						PHY1_CLK/1, /2, /4, .. /128
24	ETH_CLK_EN	+	+						
25	MAN_CLK_EN	+	+						
26	SLEEP	+	+						
27	PHY_CLK_EN	+	+						
28..29	PHY_CLK_SEL	+	+						HSI, HSE, PLLCPUo, HSE2
30	ETH2_CLK_EN	-	+						
		0	***0***						***ResetValye***
		0x3F070707	***0x7F070707***						***MaskValue***
	End Addr	*0x38*							

0x34	**SSP_CLOCK2**		-						
0..2	SSP4_BRG		-					+	HCLK/1, /2, /4, .. /128
24	SSP4_CLK_EN		-					+	
								0	***ResetValye***
								0x01000007	***MaskValue***
0x38	**PER2_CLOCK**								
0			AUC						
1			LED						
2			KEY						
3			PORT_G						
4			UART3						
5			UART4						
6			SPI4						
7			PORT_H						
8			PORT_I						
			0						***ResetValye***
			0x01FF						***MaskValue***
0x38	**DSP_CONTROL_STATUS**		-						
0	RST_DSP		-					+	1 - reset, 0 - work
1	RST_DSP_CPU		-					+	1 - reset, 0 - work
2	RST_DSP_MEM		-					+	1 - reset, 0 - work
3	RST_DSP_PER		-					+	1 - reset, 0 - work
4	HOLD		-					+	0 - Stop, 1 - work
5	BIO		-					+	
6	XF_EN		-					+	XF - to PA[15]
7	-								
8	XF		-					+	
9	HOLDA		-					+	0 - Stop, 1 - work
10..11	IDLE_NUM		-					+	
12..13	-		-						XF - to PA[15]
14	BRTRD		-					+	
15	RD_BUF_EN		-					+	
								0	***ResetValye***
								0xCF7F	***MaskValue***
	End Addr							*0x3C*	
0x3C	**UART_SSP_CLOCK**								
0..2	UART3_BRG		+						HCLK/1, /2, /4, .. /128
8..10	UART4_BRG		+						HCLK/1, /2, /4, .. /128
16..18	SSP4_BRG		+						HCLK/1, /2, /4, .. /128
24	UART3_CLK_EN		+						
25	UART4_CLK_EN		+						
26	SSP4_CLK_EN		+						
			0						***ResetValye***
			0x07070707						***MaskValue***
	End Addr		*0x40*						