BaseAddr	**VE1**	**VE3**	**VE9x**	**VC1**	**VE4**	**VK214**	**VK234**
WWDT	0x4006_0000				0x4004_8000		
IWDT	0x4006_8000				0x4005_0000		

IWDT		
0x00	**KR**	**WR-only**
0..15	KEY	0xAAAA - clear reset event
		0x5555 - Enable access to PR and RLR
		0xCCCC - Start timer (Can't be stopped!)

0x04	**PR**	**R/W**	**Clock only fr**	
0..2	PR	**LSI** div: 0 - div4, 1 - div 8, 2 - div 16, … 7 - div256		

0x08	**RLR**	**R/W**
0..11	RLR	Period to decrement, restore by 0x5555. (Write on RVU = 0)

0x0C	**SR**	**RD-only**
0	PVU	1 - PR is updating, 0 - can write PR
1	RVU	1 - PRL is updating, 0 - can write PRL

WWDT		
0x00	**CR**	**R/W**
0..6	T	Peiod (Tick = 4096*2^WGTB of PCLK APB)
7	WDGA	1 - Reset Enable (Clear by Reset)

0x04	**CFR**	**R/W**
0..6	W	Window for set T = 0x40-0x7F. Reset: T > W, T = 0x3F
7..8	WGTB	0: CLK = PCLK/4096/**1**, .../**2**, .../**4**, .../**8**
9	EWI	Enable IRQ on T=0x40 (Disable by reset)

0x08	**SR**	**R/W**
0	EWIF	1 - on T=0x40. Write 0 to clear