0x00 015	1		
015	CNT	Description	
		Counter Value	VE9x, VE4, VE214, VE234, VC1
031			VE1,VE3
	0x00000000	ResetValue	
	0xFFFF <mark>/0xFFFFFFF</mark>	MaskValue	
	J. T. T. J. OALTTITT		<u> </u>
0x04	PSG	Description	
	PSG		
015		CLK = TIM_CLK/ (PSG + 1)	
	0x0000000	ResetValue	
	0x0000FFFF	MaskValue	
0x08	ARR	Description	
015		Period Value	VE9x, VE4, VE214, VE234, VC1
031			VE1,VE3
031	00000000	Doorth/olive	VLI,VLS
	0x00000000	ResetValue	
	0xFFFF/0xFFFFFFFF	MaskValue	
0x0C	CNTRL	Description	
0	CNT_EN	1: Timer Enable	
1	ARRB_EN	1: ARR update on CNT completed. 0: Immediately	
2	WR_CMPL	1: writing, 0: write completed - for CNT, PSG, ARR	
3	DIR	0: Up, 1: Down - count	<u> </u>
45	FDTS	0: 1, 2, 3, 4 - F_Input_Sample = TIM_CLOCKs / FDTS	
67	CNT_MODE	b00: by DIR, b01: Up-Down - by TIM_CLOCK	
		b10: by DIR, b11: Up-Down by - by ExtEvents	
		b1x: by DIR - ExtEvents	VE1,VE3
811	EVENT_SEL	0: Rise of TIM_Clock	
		1, 2, 3, 10: CNT=ARR Tim1, Tim2, Tim3, Tim4	VE1,VE3
		4, 5, 6, 7: Event in Ch1, Ch2, Ch3, Ch4	
		8, 9: ETR Rise, Fall	VE1,VE3
	0x00000000	ResetValue	VL1,VL3
	0x00000FFF	MaskValue	
0x10	CCR1	Description	
0x14	CCR2		Нет в VK214
0x18	CCR3		Нет в VK214
0x1C	CCR4		Нет в VK214
015		Captured/PWM CNT Value	VE9x, VE4, VE214, VE234, VC1
		Supturcult valvi civi value	
031	000000000	December 2	VE1,VE3
	0x00000000	ResetValue	
	0xFFFF/0xFFFFFFF	MaskValue	
0x20	CH1_CNTRL	Description	
0x24	CH2_CNTRL	Capture / PWM - CCR control	Нет в VK214
0x28	CH3_CNTRL		Нет в VK214
0x2C	CH4_CNTRL		Нет в VK214
		Input Dica/Fall demotion to vice Front	LICI D VICE14
03	CHFLTR	Input Rise/Fall duration to rise Event	
		0,1,2,3: - 1,2,4,8 periods of TIM_Clock,	
		4,5: - 6, 8 periods of FDTS/2	
		6,7: - 6, 8 periods of FDTS/4	
		8,9: - 6, 8 periods of FDTS/8	
		10,11,12: - 5, 6, 8 periods of FDTS/16	i
		[10,11,12, - 5, 6, 8 periods of FD15/16	
4.5	CHCEI	13,14,15: - 5, 6, 8 periods of FDTS/32	
45	CHSEL	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR	
45	CHSEL	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise	
45	CHSEL	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall	
45	CHSEL	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4	
45	CHSEL	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall	
45 67	CHSEL	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4	
		13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable PWM - REF Generate Mode	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable PWM - REF Generate Mode 0, 4: - const REF = 0	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable PWM - REF Generate Mode 0, 4: - const REF = 0 5: - const REF = 1	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable PWM - REF Generate Mode 0, 4: - const REF = 0	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable PWM - REF Generate Mode 0, 4: - const REF = 0 5: - const REF = 1	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable PWM - REF Generate Mode 0, 4: - const REF = 0 5: - const REF = 1 1: REF=1 - on (CNT = CCR) (CNT = CCR1) 2: REF=0 - on (CNT = CCR) (CNT = CCR1)	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable PWM - REF Generate Mode 0, 4: - const REF = 0 5: - const REF = 1 1: REF=1 - on (CNT = CCR) (CNT = CCR1) 2: REF=0 - on (CNT = CCR) (CNT = CCR1) 3: REF Switch - on (CNT = CCR) (CNT = CCR1)	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable PWM - REF Generate Mode 0, 4: - const REF = 0 5: - const REF = 1 1: REF=1 - on (CNT = CCR) (CNT = CCR1) 2: REF=0 - on (CNT = CCR) (CNT = CCR1) 3: REF Switch - on (CNT = CCR) (CNT = CCR1)	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable PWM - REF Generate Mode 0, 4: - const REF = 0 5: - const REF = 1 1: REF=1 - on (CNT = CCR) (CNT = CCR1) 2: REF=0 - on (CNT = CCR) (CNT = CCR1) 3: REF Switch - on (CNT = CCR) (CNT = CCR1) CCR1_EN = 0 6: REF=1 - while (CNT < CCR)	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable PWM - REF Generate Mode 0, 4: - const REF = 0 5: - const REF = 1 1: REF=1 - on (CNT = CCR) (CNT = CCR1) 2: REF=0 - on (CNT = CCR) (CNT = CCR1) 3: REF Switch - on (CNT = CCR) (CNT = CCR1) CCR1_EN = 0 6: REF=1 - while (CNT < CCR) 7: REF=0 - while (CNT < CCR)	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable PWM - REF Generate Mode 0, 4: - const REF = 0 5: - const REF = 1 1: REF=1 - on (CNT = CCR) (CNT = CCR1) 2: REF=0 - on (CNT = CCR) (CNT = CCR1) 3: REF Switch - on (CNT = CCR) (CNT = CCR1) CCR1_EN = 0 6: REF=1 - while (CNT < CCR)	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable PWM - REF Generate Mode 0, 4: - const REF = 0 5: - const REF = 1 1: REF=1 - on (CNT = CCR) (CNT = CCR1) 2: REF=0 - on (CNT = CCR) (CNT = CCR1) 3: REF Switch - on (CNT = CCR) (CNT = CCR1) CCR1_EN = 0 6: REF=1 - while (CNT < CCR) 7: REF=0 - while (CNT < CCR)	
67	CHPSC	13,14,15: - 5, 6, 8 periods of FDTS/32 Event to Fix in CCR 0 - Input Rise 1 - Input Fall 2 - Rise in CH2_Inp for Ch1 / Inp3 for Ch2 / Inp4 for Ch3 / Inp1 for Ch4 3 - Rise in CH3_Inp for Ch1 / Inp4 for Ch2 / Inp1 for Ch3 / Inp2 for Ch4 CCR Capture Event prescaller 0: div1, div2, div4, div8 1: ETR Enable PWM - REF Generate Mode 0, 4: - const REF = 0 5: - const REF = 1 1: REF=1 - on (CNT = CCR) (CNT = CCR1) 2: REF=0 - on (CNT = CCR) (CNT = CCR1) 3: REF Switch - on (CNT = CCR) (CNT = CCR1) CCR1_EN = 0 6: REF=1 - while (CNT < CCR) CCR1_EN = 1	

12	CTDCN	1. Enable Clear Def by ETD Def C			
13	ETREN W.P. CMPI	1: Enable Clear Ref by ETR - Ref = 0 1: CCR Writing 0: Can write CCR			
14 15	WR_CMPL CAP_nPWM	0: PWM, 1: CAP - channel mode			
12	0x00000000	ResetValue			
	0xFFFF	MaskValue			
0x30	CH1_CNTRL1	Description			
0x34	CH2_CNTRL1	PWM driver control	Нет в VK214		
0x38	CH3_CNTRL1		Нет в VK214		
0x3C	CH4_CNTRL1	Нет в VK214			
01	SELOE	0: Pin_OE = 0 - Pin is IN			
		1: Pin_OE = 1 - Pin is OUT			
		3: Pin_OE = by REF - Pin is IN / OUT			
2 2	651.0	4: Pin_OE = by DTG			
23	SELO INV	0: CHx_out = 0, 1, Ref, DTG 1: Invert output			
57	IINV	1: invert output			
89	NSELOE	SELOE for nCH			
1011	NSELO	SELO for nCH			
12	NINV	INV for nCH			
	0x00000000	ResetValue			
	0x1F1F	MaskValue			
0x40	CH1_DTG	Description			
0x44	CH2_DTG		Нет в VK214		
0x48	CH2_DTG		Нет в VK214		
0x4C	CH2_DTG		Нет в VK214		
03	DTG	DTG frequency Prescaller			
4	EDTS	0: TIM_CLOCK, 1: FDTS - DTG Clock Select			
57	-	DTC D.L. DTC */DTC.4)			
815	DTGx 0x00000000	DTG_Delay = DTGx*(DTG+1) ResetValue			
	0x00000000	MaskValue			
	OXFFIF	Iviaskvalue			
0x50	BRKETR_CNTRL	Description			
OKSO	-	·			
0	BRK INV	I1: Inv Enable			
0	BRK_INV ETR_INV	1: Inv Enable 1: Inv Enable			
1	ETR_INV	1: Inv Enable			
1 23	ETR_INV ETR_PSC	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div			
1 23	ETR_INV ETR_PSC ETR_FILTER	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR			
1 23 47	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue			
1 23 47	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags			
1 23 47 0x54 0x58	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags			
1 23 47 0x54 0x58 0x5C	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable			
1 23 47 0x54 0x58	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear			
1 23 47 0x54 0x58 0x5C 0	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear			
1 23 47 0x54 0x58 0x5C 0 1	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear			
1 23 47 0x54 0x58 0x5C 0	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear			
1 23 47 0x54 0x58 0x5C 0 1	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear			
1 23 47 0x54 0x58 0x5C 0 1 2 3 4	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear (1 - Active)			
1 23 47 0x54 0x58 0x5C 0 1 2 3 4 58	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_REF_CH1,2,3,4 CCR1_CAP_CH1,2,3,4	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear 1: CCR Captured, wr 0 to clear 1: PWM REF Front, wr 0 to clear 1: CCR1 Captured, wr 0 to clear			
1 23 47 0x54 0x58 0x5C 0 1 2 3 4 58 912	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_REF_CH1,2,3,4 Ox00000000	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear 1: PWM REF Front, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue			
1 23 47 0x54 0x58 0x5C 0 1 2 3 4 58 912	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_REF_CH1,2,3,4 CCR1_CAP_CH1,2,3,4	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear 1: CCR Captured, wr 0 to clear 1: PWM REF Front, wr 0 to clear 1: CCR1 Captured, wr 0 to clear			
1 23 47 0x54 0x58 0x5C 0 1 2 3 4 58 912 1316	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_REF_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 0x00000000 0x0001FFFF	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear 1: CCR Captured, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue MaskValue			
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 0x0000000 0x0001FFFF CH1_CNTRL2	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear 1: PWM REF Front, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue MaskValue Description			
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_REF_CH1,2,3,4 CCR1_CAP_CH1,2,3,4	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear 1: CCR Captured, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue MaskValue	Het B VK214		
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_REF_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 Ox0000000 0x0001FFFF CH1_CNTRL2 CH2_CNTRL2 CH3_CNTRL2	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear 1: PWM REF Front, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue MaskValue Description	Нет в VK214		
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68 Ox6C	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear (1 - Active) 1: CCR Captured, wr 0 to clear 1: PWM REF Front, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue MaskValue Description CCR1 Contorl			
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68 Ox6C 01	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_REF_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear (1 - Active) 1: CCR Captured, wr 0 to clear 1: PWM REF Front, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue MaskValue Description CCR1 Contorl	Нет в VK214		
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68 Ox6C 01 2	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear 1: CCR Captured, wr 0 to clear 1: CCR Captured, wr 0 to clear 1: CCR1 Captured, wr 0 to clear	Нет в VK214		
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68 Ox6C 01	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_REF_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear (1 - Active) 1: CCR Captured, wr 0 to clear 1: PWM REF Front, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue MaskValue Description CCR1 Contorl	Нет в VK214		
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68 Ox6C 01 2	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_REF_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear (1 - Active) 1: CCR Captured, wr 0 to clear 1: PWM REF Front, wr 0 to clear 1: CCR1 Captured, wr 0 to clear	Нет в VK214		
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68 Ox6C 01 2	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear 1: CCR Captured, wr 0 to clear 1: CCR Captured, wr 0 to clear 1: CCR1 Captured, wr 0 to clear	Нет в VK214		
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68 Ox6C 01 2	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear 1: CCR Captured, wr 0 to clear 1: CCR Captured, wr 0 to clear 1: CCR1 Captured, wr 0 to clear	Нет в VK214		
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68 Ox6C 01 2 3	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_REF_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear (1 - Active) 1: CCR Captured, wr 0 to clear 1: PWM REF Front, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue MaskValue Like CHx_CNTRL1.CHSEL - Sel input to capture 1: CCR1 Enable 0: Immediately, 1: on CNT = 0 - CCR and CCR1 update mode ResetValue MaskValue	Нет в VK214		
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68 Ox6C 01 2 3	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 Ox0000000 0x0001FFFF CH1_CNTRL2 CH2_CNTRL2 CH3_CNTRL2 CH4_CNTRL2 CH4_CNTRL2 CH5EL1 CCR1_EN CCRLD 0x0000000 0x000F	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear (1 - Active) 1: CCR Captured, wr 0 to clear 1: PWM REF Front, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue MaskValue Like CHx_CNTRL1.CHSEL - Sel input to capture 1: CCR1 Enable 0: Immediately, 1: on CNT = 0 - CCR and CCR1 update mode ResetValue MaskValue	Нет в VK214 Нет в VK214		
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68 Ox6C 01 2 3 Ox70 Ox74 Ox78 Ox7C	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_REF_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 Ox0000000 0x0001FFFF CH1_CNTRL2 CH2_CNTRL2 CH3_CNTRL2 CH4_CNTRL2 CH4_CNTRL2 CCR1_EN CCRLD 0x0000000 0x000F CCR11 CCR21	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear 1: CCR Captured, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue MaskValue Description CCR1 Contorl Like CHx_CNTRL1.CHSEL - Sel input to capture 1: CCR1 Enable 0: Immediately, 1: on CNT = 0 - CCR and CCR1 update mode ResetValue MaskValue Description Description	Нет в VK214		
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68 Ox6C 01 2 3 Ox70 Ox74 Ox78 Ox78 Ox7C 015	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 Ox00000000 0x0001FFFF CH1_CNTRL2 CH2_CNTRL2 CH3_CNTRL2 CH4_CNTRL2 CH4_CNTRL2 CH4_CNTRL2 CH4_CNTRL2 CCR1_EN CCRRLD 0x00000000 0x000F CCR11 CCR21 CCR21	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear (1 - Active) 1: CCR Captured, wr 0 to clear 1: PWM REF Front, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue MaskValue Like CHx_CNTRL1.CHSEL - Sel input to capture 1: CCR1 Enable 0: Immediately, 1: on CNT = 0 - CCR and CCR1 update mode ResetValue MaskValue	Нет в VK214 VE9x, VE4, VE214, VE234, VC1		
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68 Ox6C 01 2 3 Ox70 Ox74 Ox78 Ox7C	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 Ox0000000 0x0001FFFF CH1_CNTRL2 CH2_CNTRL2 CH3_CNTRL2 CH4_CNTRL2 CH4_CNTRL2 CH5EL1 CCR1_EN CCR1_EN CCR1_CR1 CCR21 CCR31 CCR41	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear 1: PWM REF Front, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue MaskValue Description CCR1 Contorl Like CHx_CNTRL1.CHSEL - Sel input to capture 1: CCR1 Enable 0: Immediately, 1: on CNT = 0 - CCR and CCR1 update mode ResetValue MaskValue Description Captured/PWM CNT Value	Нет в VK214		
1 23 47 Ox54 Ox58 Ox5C 0 1 2 3 4 58 912 1316 Ox60 Ox64 Ox68 Ox6C 01 2 3 Ox70 Ox74 Ox78 Ox78 Ox7C 015	ETR_INV ETR_PSC ETR_FILTER 0x00000000 0x00FF STATUS IE DMA_RE CNT_ZERO CNT_ARR ETR_RE ETR_FE BRK CCR_CAP_CH1,2,3,4 CCR_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 CCR1_CAP_CH1,2,3,4 Ox00000000 0x0001FFFF CH1_CNTRL2 CH2_CNTRL2 CH3_CNTRL2 CH4_CNTRL2 CH4_CNTRL2 CH4_CNTRL2 CH4_CNTRL2 CCR1_EN CCRRLD 0x00000000 0x000F CCR11 CCR21 CCR21	1: Inv Enable 0: div1, div2, div4, div8 - External Clock Div Like CHx_Contorl.CHFLTR ResetValue MaskValue Status flags IRQ enable flags DMA request enable 1: CNT=0 - wr 0 to clear 1: CNT=ARR - wr 0 to clear 1: ETR Rise front - wr 0 to clear 1: ETR Fall front - wr 0 to clear 1: BRK=1, wr 0 to clear 1: CCR Captured, wr 0 to clear 1: CCR1 Captured, wr 0 to clear ResetValue MaskValue Description CCR1 Contorl Like CHx_CNTRL1.CHSEL - Sel input to capture 1: CCR1 Enable 0: Immediately, 1: on CNT = 0 - CCR and CCR1 update mode ResetValue MaskValue Description Description	Нет в VK214 VE9x, VE4, VE214, VE234, VC1		

0x80	DMA_RE1	DMA request enable - for Channel1	VE1,VE3
0x84	DMA_RE2	- for Channel2	VE1,VE3
0x88	DMA_RE3	- for Channel3	VE1,VE3
0x8C	DMA_RE4	- for Channel4	VE1,VE3
		LIKE DMA_RE	
	0x00000000	ResetValue	
	0x0001FFFF	MaskValue	

		BE1	BE3	ВЕ9х	ВЦ1901	BE4	BK214	BE234
Base Addr								
	Timer1	0x4007_0000						
	Timer2	0x4007_8000						
	Timer3	0x4008_0000	0x4008_0000	0x4008_0000	0x4008_0000	-	-	-
	Timer4	0x4009_8000	0x4009_8000	-	-	-	-	-