Addr Shift	Regs	Access	BE1	BE3	BE9x	ВЦ1901	BE4	BK214	BE234	
0x00	CR0	RW	+	+	+	+	+	+	+	Control Register 0
0x04	CR1	RW	+	+	+	+	+	+	+	Control Register 1
0x08	DR	RW	+	+	+	+	+	+	+	Data Register, FIFO RX and TX by 8 words
0x0C	SR	RO	+	+	+	+	+	+	+	Status Register
0x10	CPSR	RW	+	+	+	+	+	+	+	Clock Prescale Register
0x14	IMSC	RW	+	+	+	+	+	+	+	Interrupt Mask Set/Clear Register
0x18	RIS	RO	+	+	+	+	+	+	+	Raw Interrupt Status Register
0x1C	MIS	RO	+	+	+	+	+	+	+	Masked Interrupt Status Register
0x20	ICR	WO	+	+	+	+	+	+	+	Interrupt Clear Register
0x24	DMACR	RW	+	+	+	+	+	+	+	MDA Control Register
Base Addr										
	SSP1		0x4004_0000	0x4004_0000	0x4004_0000	0x4004_0000	0x4000_0000	0x4000_0000	0x4000_0000	
	SSP2		0x400A_0000	0x400A_0000	0x400A_0000	0x400A_0000	-	-	-	
	SSP3		0x400F_8000	0x400F_8000	-	0x4000_0000	-	-	-	
	SSP4		-	0x4013_0000	-	0x4000_8000	-	-	-	

0x00	**CR0**	**Control Register 0**	
0..3	DSS	Data Size Select	0..2 - reserved. 3 - 4bits, …, 0xF - 16bits
4..5	FRF	Frame Format	b00 - SPI, b01 - SSI, b10 - Microwire, b11 - reserved
6	SPO	Clock Polarity	SPI Only! 0 - Idle is Low
7	SPH	Clock Capture Phase	SPI Only! 0 - capture on Rise, set on Fall
8..15	SCR	Signal Clock Rate	0..255, BitRate = Fsspclk/(CPSDVR * (1 + SCR))
		0x00000000	**ResetValue**
		0x0000FFFF	**MaskValue**
0x04	**CR1**	**Control Register 1**	
0	LBM	Loop Back Mode	0 - Normal, 1 - LoopBack
1	SSE	SyncSerial Enable	1 - Enabled
2	MS	Master or Slave Mode	0 - Master, 1 - Slave
3	SOD	Slave Output Disable	0 - Normal, 1 - Output disabled
		0x00000000	**ResetValue**
		0x0000000F	**MaskValue**
0x08	**DR**	**Data Register**	
0..15	DATA	Data	WR - Out FIFO, RD - Read FIFO
		0x00000000	**ResetValue**
		0x0000FFFF	**MaskValue**
0x0C	**SR**	**Status Register**	
0	TFE		1 - FIFO_TX Empty
1	TNF		1 - FIFO_TX Not Full
2	RNE		1 - FIFO_RX Not Empty
3	RFF		1 - FIFO_RX Full
4	BSY		1 - Transfering, 0 - Idle
		0x00000003	**ResetValue**
		0x0000001F	**MaskValue**
0x10	**CPSR**	**Clock Prescaler Reg**	
0..7	CPSDVSR		2..254, BitRate = Fsspclk/(CPSDVR * (1 + SCR)) EVEN ONLY!

		0x00000000	**ResetValue**
		0x000000FF	**MaskValue**
0x14	**IMSC**	**IRQ Mask Set/Clear**	
0	RORIM	overrun	1 - Enable on FIFO_RX overflow (can't write new data)
1	RTIM		1 - Enable on RX timeout (No data for 32 bits time & FIFO_RX not empty)
2	RXIM		1 - Enable on FIFO_RX >= 4 words
3	TXIM		1 - Enable on FIFO_TX <= 4 words
		0x00000000	**ResetValue**
		0x0000000F	**MaskValue**
0x18	**RIS**	**All IRQ Status**	
0	RORRIS		1 - FIFO_RX overflow (can't write new data)
1	RTRIS		1 - RX timeout
2	RXRIS		1 - FIFO_RX >= 4 words
3	TXRIS		1 - FIFO_TX <= 4 words
		0x00000008	**ResetValue**
		0x0000000F	**MaskValue**
0x1C	**MIS**	**Masked IRQ Status**	
0	RORMIS		1 - FIFO_RX overflow (can't write new data)
1	RTMIS		1 - RX timeout
2	RXMIS		1 - FIFO_RX >= 4 words
3	TXMIS		1 - FIFO_TX <= 4 words
		0x00000000	**ResetValue**
		0x0000000F	**MaskValue**
0x20	**ICR**	**IQR Clear Register**	
0	RORIC		1 - Clear FIFO_RX overflow flag
1	RTIC		1 - Clear RX timeout
		0x00000000	**ResetValue**
		0x00000003	**MaskValue**

0x24	DMACR	Masked IRQ Status	
0	RXDMAE		1 - Enable DMA call on FIFO_RX has data
1	TXDMAE		1 - Enable DMA call on FIFO_TX not Full
		0x00000000	**ResetValue**
		0x00000003	**MaskValue**