0x00	**STATUS**	**RO**	**Status Register**
0	master_enable		1: Controller is enabled
1..3	-		
4..7	state		b0000 - idle
			b0001 - reading channel controller data
			b0010 - reading source data end pointer
			b0011 - reading destination data end pointer
			b0100 - reading source data
			b0101 - writing destination data
			b0110 - waiting for DMA request to clear
			b0111 - writing channel controller data
			b1000 - stalled
			b1001 - done
			b1010 = peripheral scatter-gather transition
			b1011-b1111 = undefined
8..15	-		
16..20	chnls_minus1		Number of available DMA channels minus one
			b00000 = controller configured to use 1 DMA channel
			b00001 = controller configured to use 2 DMA channels
			…
21..27			
28..31	test_status		0x0 = controller does not include the integration test logic
			0x1 = controller includes the integration test logic
			0x2-0xF = undefined.
	0x00000000		**ResetValue**
	0xF01F0F01		**MaskValue**
0x04	**CFG**	**WO**	**Config Register**
0	master_enable		1: Enable controller
1..4			
5..7	Chnl_Prot_Ctrl		b[7] = 1: Enable Cachable AHB transfer
			b[6] = 1: Enable Bufferable AHB transfer

			b[5] = 1: Enable Privileged AHB transfer
	0x00000000		**ResetValue**
	0x000000E1		**MaskValue**
0x08	**CTRL_BASE_PTR**	**RW**	**Address of channels table**
0..9	-		
10..31	ctrl_base_ptr		
0x0C	**ALT_CTRL_BASE_PTR**	**RO**	**Address of channels alter table**
0..9	-		
10..31	alt_ctrl_base_ptr		
	0x00000000		**ResetValue**
	0xFFFFFC00		**MaskValue**
0x10	**WAITONREQ_STATUS**	**RO**	**Channel wait on request status**
0..31	ch_bit_select		1: waitonreq is Active (High) - Wait Request from block
			When HIGH, it prevents dma_active[] from deasserting until
			dma_req[] and dma_sreq[] are LOW.
0x14	**CHNL_SW_REQUEST**	**WO**	**Channel Software Request**
0..31	ch_bit_select		1: Activate request for transfer
0x18	**CHNL_USEBURST_SET**	**RW**	**Disable single transfer requests**
0x1C	**CHNL_USEBURST_CLR**	**WO**	
0..31	ch_bit_select		1: Disable Sreq requests
0x20	**CHNL_REQ_MASK_SET**	**RW**	**Disable channel processing**
0x24	**CHNL_REQ_MASK_CLR**	**WO**	
0..31	ch_bit_select		1: Ignore requests Req and SReq
0x28	**CHNL_ENABLE_SET**	**RW**	**Start channel**
0x2C	**CHNL_ENABLE_CLR**	**WO**	
0..31	ch_bit_select		1: Start DMA cycle

0x30	**CHNL_PRI_ALT_SET**	**RW**	**Select structure**
0x34	**CHNL_PRI_ALT_CLR**	**WO**	
0..31	ch_bit_select		0: use Rimary structure 1: use Alter structure
0x38	**CHNL_PRIORITY_SET**	**RW**	**Rise Priority**
0x3C	**CHNL_PRIORITY_CLR**	**WO**	
0..31	ch_bit_select		0: default 1: High priority
0x4C	**ERR_CLR**	**RW**	**AHB-Lite bus error clear**
0..31	ch_bit_select		0: no Errors 1: Error
	0x00000000		**ResetValue**
	0xFFFFFFFF		**MaskValue**

	BE1	BE3	BE9x	ВЦ1901	BE4	ВК214	BE234
Base Addr	0x4002_8000	0x4002_8000	0x4002_8000	0x4002_8000	0x4002_8000	-	0x4002_8000
Size	**80 Bytes**						