Addr Shift	Regs	BE1	BE3	BE9x	BE4	BK214	BE234	ВЦ1901	
0x00 - 0x34	REG_00 - REG_0D	+	+	+	+	+	+	+	
0x38	REG_0E	+	+	+	+	+	+	+	
0x3C	REG_0F	+	+	+	+	+	+	+	
0x40	RTC_CNT, 32 bit	+	+	+	+	+	+	+	
0x44	RTC_DIV, 20 bit	+	+	+	+	+	+	+	
0x48	RTC_PRL, 20 bit	+	+	+	+	+	+	+	
0x4C	RTC_ALRM, 32 bit	+	+	+	+	+	+	+	
0x50	RTC_CS	+	+	+	+	+	+	+	
		0x400D8000	0x400D8000	0x400D8000	0x40060000	0x40060000	0x40060000	0x400D8000	Base Address
0x38	**REG_0E**								
0..2	LOW	+	+	+	+	+	+	+	**0:** < 10MHz, < 200KHz, < 500KHz, <1MHz, **4:** GensOff, < 40MHz, < 80MHz, > 80MHz
3..5	SelectRI	+	+	+	+	+	+	+	=LOW
6	StandAlone	+	+	-	-	-	-	-	0: MK, 1: StandAlone
6	JTAG_A	-	-	+	+	+	+	+	1 - EN **(One of A or B Only)**
7	JTAG_B	-	-	+	+	+	+	+	1 - EN **(One of A or B Only)**
8..10	Trim_dDUcc	+	+	+	+	+	+	+	Ducc B: ***0:*** +0.1, +0.06, +0.04, +0.01, ***4:*** -0.01, -0.04, -0.06, -0.1
11	FPOR	+	+	+	+	+	+	+	=1 in BootLoader
12..13	Trim_DUcc	+	-	-	+	+	+	-	Ducc: **0:** 1.8V, 1.6V, 1.4V, 3: 1.2V
12..13	Trim_DUcc	-	+	-	-	-	-	-	Ducc: **0:** 1.8V, 1.6V, 1.4V, **3:** - forbiden
14	COVDET	-	-	-	+	+	+	-	1 - Было несанкционированное вскрытие
12..14	MODE	-	-	+	-	-	-	-	0: JtagB, 1: JtagA, 2: ExtMem_JtagB, 3: ExtMem_JtagOff, 4: res, 5: Uart, 6: Uart, 7: res
12..14	MODE	-	-	-	-	-	-	+	0: JtagB, 1: JtagA, 2: ExtMem_JtagB, 3: ExtMem_JtagOff, 4: res, 5: res, 6: Uart, 7: res
15	I_limEn	+	+	-	+	+	+	-	150mA protection: 1 - ON
		0	***0***	***0***	***0***	***0***	***0***	***0***	***ResetValue***
		0xBF7F	***0xBF7F***	***0x7FFF***	***0xFFFF***	***0xFFFF***	***0xFFFF***	***0x7FFF***	***MaskValue***
0x3C	**REG_0F**								
0	LSE_ON	+	+	+	+	+	+	+	1 - ON
1	LSE_BYP	+	+	+	+	+	+	+	0 - Osc, 1 - Gen (ByPass)
2..3	RTC_SEL	+	+	+	+	+	+	+	0: LSI, 1: LSE, 2: HSIRTC, 3: HSERTC
4	RTC_EN	+	+	+	+	+	+	+	1 - EN
5..12	RTC_CAL	+	+	+	+	+	+	+	F_rtc = CLK_rtc / (2^20) * (2^20 - RTC_CAL)
13	LSE_RDY	+	+	+	+	+	+	+	1 - Ready
14	res	-	-	-	-	-	-	-	
15	LSI_ON	+	+	+	+	+	+	+	1 - ON
16..20	LSI_TRIM	+	+	+	+	+	+	+	11~ 40KHz, 17 ~ 30KHz
21	LSI_RDY	+	+	+	+	+	+	+	1 - Ready
22	HSI_ON	+	+	+	+	+	+	+	1 - ON
23	HSI_RDY	+	+	+	+	+	+	+	1 - Ready
24..29	HSI_TRIM	+	+	+	+	+	+	+	24 ~ 8MHz
30	STANDBY	+	+	+	+	+	+	+	1 - Go to Standby
31	RTC_RESET	+	+	+	+	+	+	+	1 - Reset
		0	***0***	***0***	***0***	***0***	***0***	***0***	***ResetValue***
		0xFFFFBFFF	***0xFFFFBFFF***	***0xFFFFBFFF***	***0xFFFFBFFF***	***0xFFFFBFFF***	***0xFFFFBFFF***	***0xFFFFBFFF***	***MaskValue***

0x50	**RTC_CS**								
0	OWF	+	+	+	+	+	+	+	1 - CNT overflowed, set 1 for clear.
1	SECF	+	+	+	+	+	+	+	1 - DIV == PRL, set 1 for clear
2	ALRF	+	+	+	+	+	+	+	1 - CNT == ALRM, set 1 for clear
3	OWF_IE	+	+	+	+	+	+	+	1 - Enable IRQ by OWF
4	SECF_IE	+	+	+	+	+	+	+	1 - Enable IRQ by SECF
5	ALRF_IE	+	+	+	+	+	+	+	1 - Enable IRQ by ALRF
6	WEC	+	+	+	+	+	+	+	0 - RTC Regs Write Enable, 1 - Busy
		0	***0***	***0***	***0***	***0***	***0***	***0***	***ResetValue***
		0x7F	***0x7F***	***0x7F***	***0x7F***	***0x7F***	***0x7F***	***0x7F***	***MaskValue***