1. Description

1.1. Project

Project Name	PWMchannels
Board Name	NUCLEO-H743ZI
Generated with:	STM32CubeMX 5.5.0
Date	05/24/2020

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration

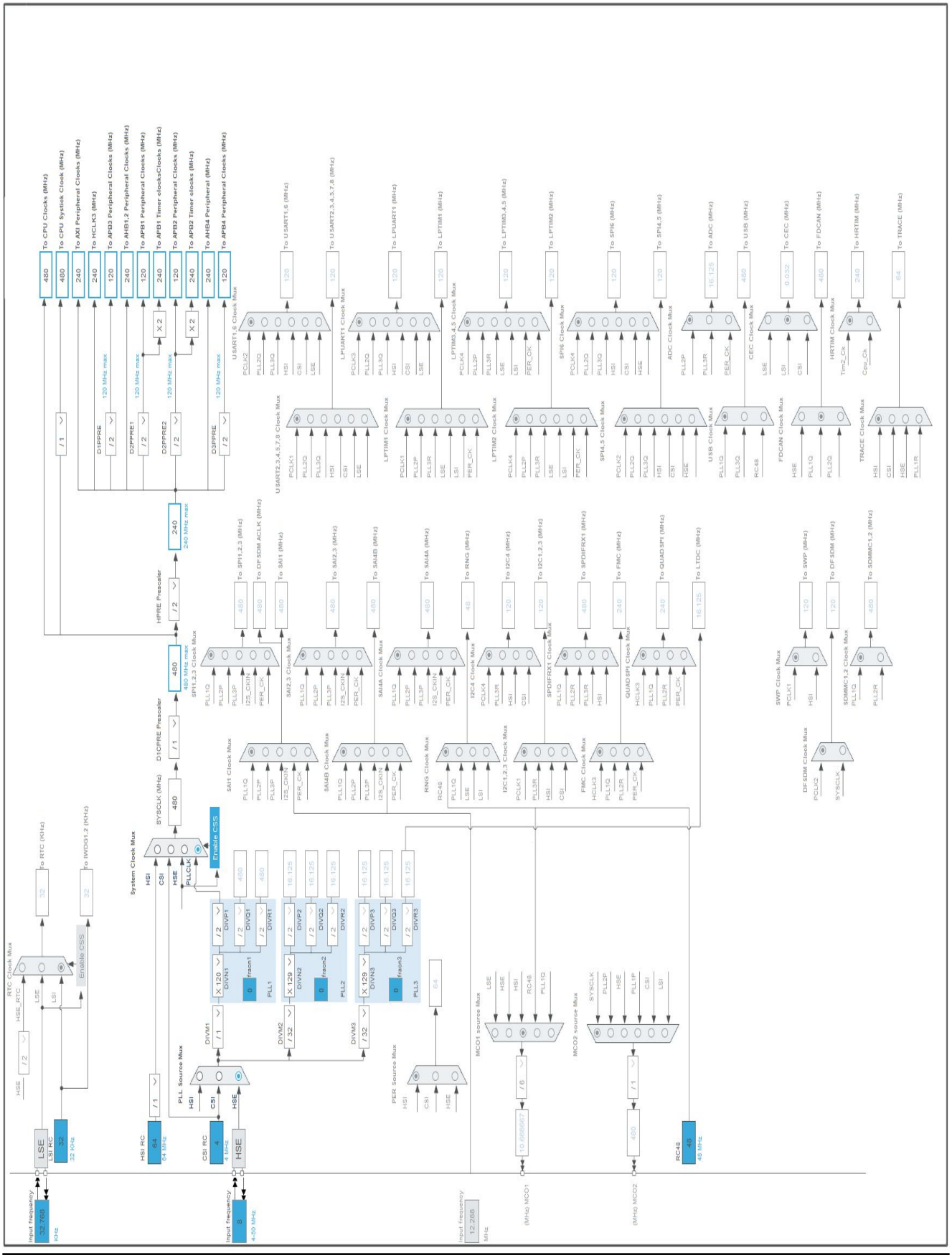
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
34	PA0 *	I/O	GPIO_Output	
38	VSS	Power		
39	VDD	Power		
41	PA5	I/O	TIM8_CH1N	
46	PB0	I/O	TIM8_CH2N	
47	PB1	I/O	TIM8_CH3N	
51	VSS	Power		
52	VDD	Power		
59	PE8	I/O	TIM1_CH1N	
60	PE9	I/O	TIM1_CH1	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	TIM1_CH2N	
64	PE11	I/O	TIM1_CH2	
65	PE12	I/O	TIM1_CH3N	
66	PE13	I/O	TIM1_CH3	
67	PE14	I/O	TIM1_CH4	
71	VCAP	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
87	PG2	I/O	GPIO_EXTI2	
94	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
95	VDD33_USB	Power		
96	PC6	I/O	TIM8_CH1	
97	PC7	I/O	TIM8_CH2	
98	PC8	I/O	TIM8_CH3	
99	PC9	I/O	TIM8_CH4	
106	VCAP	Power		
107	VSS	Power		
108	VDD	Power		
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDD	Power		
134	PB4 (NJTRST) *	I/O	GPIO_Input	
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	PWMchannels
Project Folder	C:\usr\dp\astro\stm32
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.5.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743ZITx
Datasheet	DS12110_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. CORTEX_M7

7.1.1. Parameter Settings:

Cortex Interface Settings:

CPU ICache	**Enabled ***
CPU DCache	**Enabled ***

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.2. GPIO

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

SupplySource	PWR_LDO_SUPPLY

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range

7.4. SYS

Timebase Source: SysTick

7.5. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1 CH1N

Channel2: PWM Generation CH2 CH2N

Channel3: PWM Generation CH3 CH3N

Channel4: PWM Generation CH4

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	**Center Aligned mode1 ***
Counter Period (AutoReload Register - 16 bits value)	**12000-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable

- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	0

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 3 and 3N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

CH Idle State	Reset

7.6. TIM8

Clock Source : Internal Clock

Channel1: PWM Generation CH1 CH1N

Channel2: PWM Generation CH2 CH2N

Channel3: PWM Generation CH3 CH3N

Channel4: PWM Generation CH4

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	**Center Aligned mode1 ***
Counter Period (AutoReload Register - 16 bits value)	**12000-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable

- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	0

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 3 and 3N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

CH Idle State	Reset

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14-OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
TIM1	PE8	TIM1_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE10	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE12	TIM1_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
TIM8	PA5	TIM8_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB0	TIM8_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB1	TIM8_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PC8	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC9	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PA0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High *	
	PG2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PB4 (NJTRST)	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM1 capture compare interrupt	true	0	0
TIM8 capture compare interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line2 interrupt	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		

*** User modified value**

9. Software Pack Report