Contents

Flip Flops

The purpose of a flip flop is to preserve the data over a duration of time. Ones that are clocked will ignore all of the inputs given until the clock is signaled.

Clocks

- Rising Edge: the transition from low to high
- Falling Edge: the transition from high to low

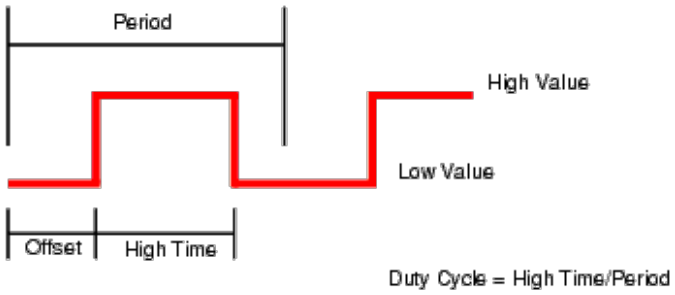


Figure 1: Clock Diagram

Caveat

There is a problem called **metastability** which is when the clock and data line are changed at around the same time, the hardware has a hard time telling which one came first, so there may be undefined behavior that would incur.

D Flip Flop

- When E is high (1), Q follows D with Q' the complement of Q
- When E is low (0), the output remains the same (no state change) and D is ignored
- E: Enable
- D: Data
- Q Q' : Output

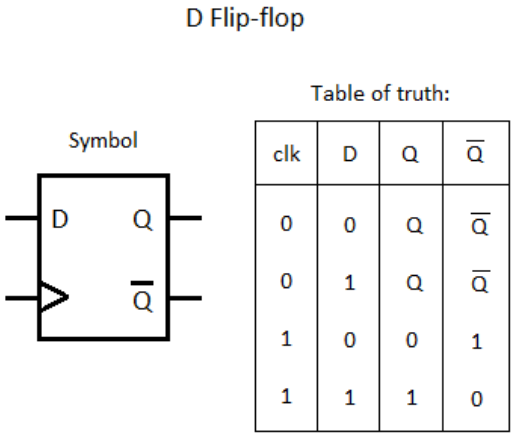


Figure 2: D Flip Flop with Truth Table

D Flip Flop (Clocked)

- Captures the value of the D input at a specific portion of the clock cycle (rising or falling edge)
- **Clock Cycle**: the clock line going high and then low again

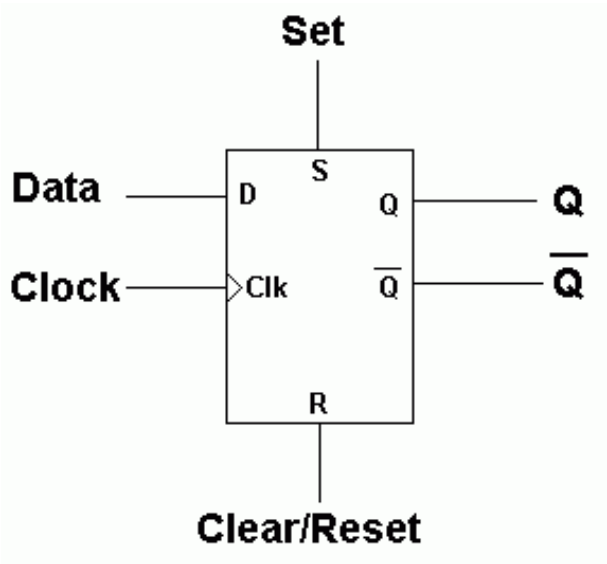


Figure 3: D Latch Diagram

SR Flip Flop

- When both S and R are low, the outputs are in a constant state
- Q and Q' are complementary; when Q is high, Q' is low

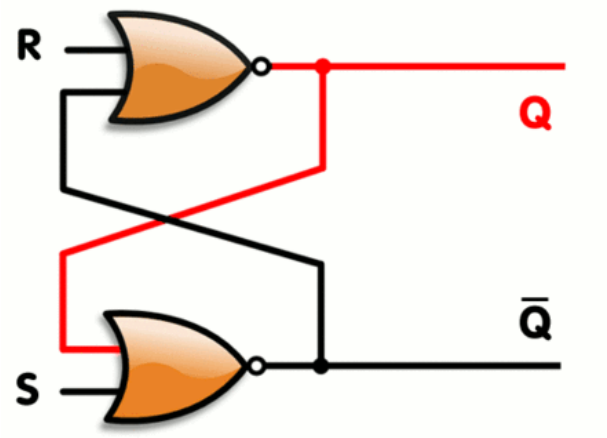


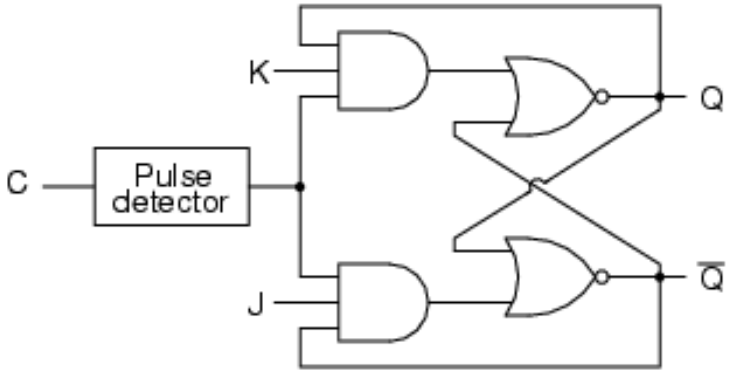
Figure 4: SR Latch

INPUTS			OUTPUT	STATE
CLK	S	R	Q	
X	0	0	No Change	Previous
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	-	Forbidden

Figure 5: SR Truth Table

JK Flip Flop

- All state changes are synced to a clock point
  - When J is 1 and K is 0, on the next clock rising edge, Q will go high
  - When K is 1 and J is 0, on the next clock rising edge Q will go low
  - When J and K are both 0, nothing will happen when the clock is pulsed
  - If J and K are 1, no matter the state of Q, it will change to the opposite state (flipping)



C	J	K	Q	$\overline{Q}$
⎍	0	0	latch	latch
⎍	0	1	0	1
⎍	1	0	1	0
⎍	1	1	toggle	toggle
x	0	0	latch	latch
x	0	1	latch	latch
x	1	0	latch	latch
x	1	1	latch	latch

Figure 6: JK Flip Flop Diagram

T Flip Flop

- When T is high, every clock cycle will toggle the outputs

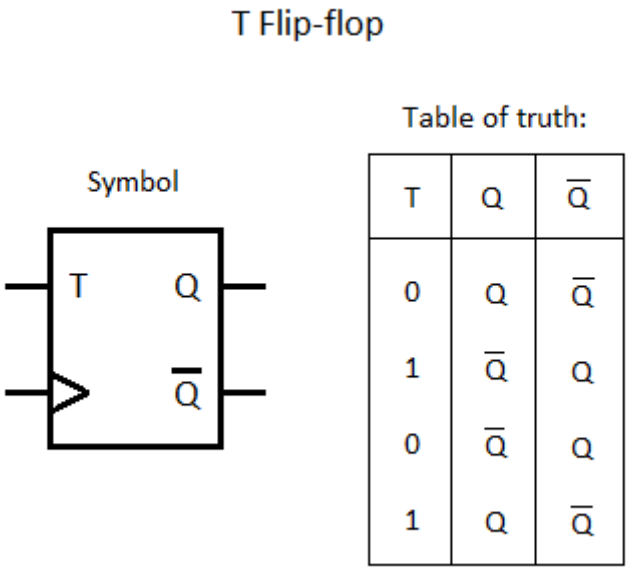


Figure 7: T Flip Flop Diagram