

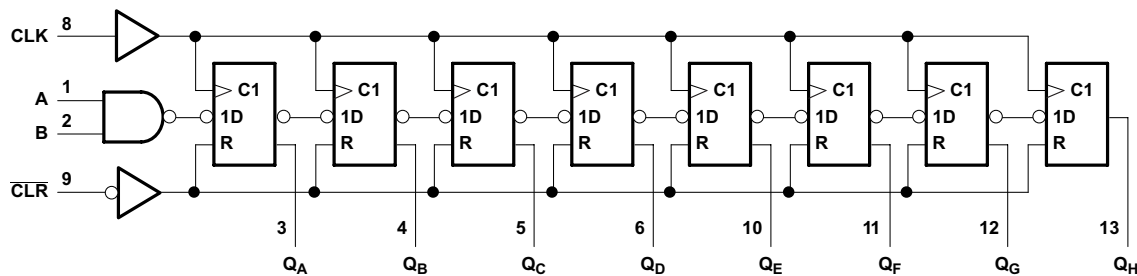
## 9 Detailed Description

### 9.1 Overview

The SN74HC164 is an 8-bit shift register with 2 serial inputs (A and B) connected through an AND gate, as well as an asynchronous clear (CLR). The device requires a high signal on both A and B in order to set the input data line high; a low signal on either input will set the input data line low. Data at A and B can be changed while CLK is high or low, provided that the minimum set-up time requirements are met.

The CLK pin of the SN74HC164 is triggered on a positive or rising-edge signal, from LOW to HIGH. Upon a positive-edge trigger, the device will store the result of the ( $A \bullet B$ ) input data line in the first register and propagate each register's data to the next register. The data of the last register, Q<sub>H</sub>, will be discarded at each clock trigger. If a low signal is applied to the CLR pin of the SN74HC164, the device will set all registers to a value of 0 immediately.

### 9.2 Functional Block Diagram



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

### 9.3 Feature Description

The HC164 has a wide operating voltage range of 2 V to 6 V, outputs that can drive up to 10 LSTTL loads and Low Power Consumption, 80-μA maximum I. It is typically  $t_{pd} = 20$  ns and has  $\pm 4$ -mA output drive at 5 V with low input current of 1-μA maximum. It also has AND-gated (enable/disable) serial inputs a fully buffered clock and serial inputs as well as a direct clear.

### 9.4 Device Functional Modes

Table 1 lists the functional modes of the SNx4HC164.

**Table 1. Function Table<sup>(1)(2)</sup>**

INPUTS				OUTPUTS			
$\overline{\text{CLR}}$	CLK	A	B	Q <sub>A</sub>	Q <sub>B</sub>	...	Q <sub>H</sub>
L	X	X	X	L	L		L
H	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>		Q <sub>H0</sub>
H	↑	H	H	H	Q <sub>An</sub>		Q <sub>Gn</sub>
H	↑	L	X	L	Q <sub>An</sub>		Q <sub>Gn</sub>
H	↑	X	L	L	Q <sub>An</sub>		Q <sub>Gn</sub>

- (1) Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>H0</sub> = the level of Q<sub>A</sub>, Q<sub>B</sub>, or Q<sub>H</sub>, respectively, before the indicated steady-state input conditions were established.
- (2) Q<sub>An</sub>, Q<sub>Gn</sub> = the level of Q<sub>A</sub> or Q<sub>G</sub> before the most recent ↑ transition of CLK: Indicates a 1-bit shift.

## 10 Application and Implementation

### 10.1 Application Information

The SNx4HC164 is an 8-bit shift register that can be used as a deserializer in order to reduce the number of GPIO's needed when driving multiple LED's. In order to correctly display the proper output in the LED's a sink MOSFET was added to prevent the LED's from lighting up until the correct data or the proper clock signal has been achieved.

### 10.2 Typical Application

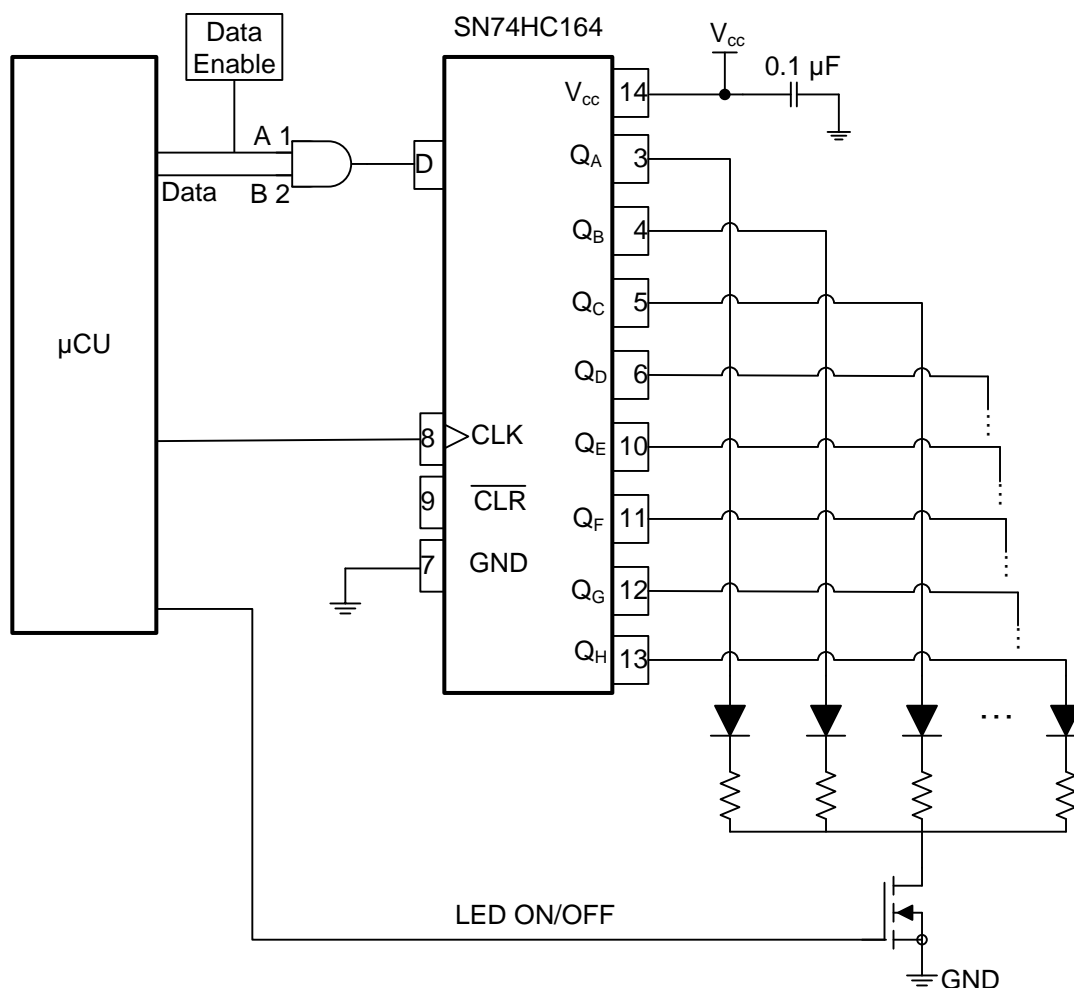


Figure 4. Typical Application Diagram

#### 10.2.1 Design Requirements

Ensure that the incoming clock rising edge meets the criteria in [Recommended Operating Conditions](#).

#### 10.2.2 Detailed Design Procedure

Ensure that input and output voltages do not exceed ratings in [Absolute Maximum Ratings](#).

Input voltage threshold information can be found in [Recommended Operating Conditions](#).

Detailed timing requirements can be found in [Timing Requirements](#),  $T_A = 25^\circ\text{C}$ .