UROP Proposal application.

Title of Proposal: Abstraction models for manufacturability aware silicon photonics.

State the Problem/Topic of Research or Creative Work: Silicon photonic circuits are becoming more relevant in AI. Based on university Ph.D. student Pratishtha's work, we know that there is a way to simulate a single silicon photonic circuit with varying manufacturing. When trying to simulate larger more complex circuits by combining multiple devices, the current simulation programs like Ansys Lumerical fail due to how complex the transfer matrix equations become. Especially when trying to model larger complex circuits that may have up to a hundred or maybe even thousands of these optical devices. Therefore, it is important to build abstraction models to help with simulating those complex silicon photonic circuits.

My proposal is to develop a computer program that will read in an interconnected complex photonic silicon circuit and be able to simulate and synthesize them. I will need to first develop a data structure for the circuits that will be Sinusoidal functions (matrix-based) to represent and store the transfer functions that represent the devices. With the data structures abstraction in place, I can now represent the silicon photonic circuit in parts and build complex circuits through abstraction. This program will be built with either c++ or python. The main challenge will be studying and figuring out the most appropriate data structures that can be integrated with the cad tools and building a netlist format to read these data structures to build the circuit. One of the benefits of my program will be being able to represent any known manufactural defect of a silicon photonic circuit and run an algorithm to determine the best location within the circuit to do post-fabrication tunning (affecting reflective index). This will Improve yield and reduce cost for silicon photonic circuits.

Relevant Background/Literature Review: efforts are needed to develop defect models, tests, and validation procedures [pratishtha cite]. These silicon photonic devices are sensitive when it comes to their manufacturing and different manufacturing processes can result in defects within those devices at a very small scale. It can geometrically change the circuit design which will affect the refractive index of waveguides and potentially cause the circuit to malfunction. [pratishtha cite]

Photonic silicon circuits can be modeled and represented through transfer matrix equations. [insert equation here and pratishtha cite] you can start adding more parameters to the optical circuits which can also be introduced into the transfer matrices such as phase modulators. By creating simulations of these photonic optical devices, you can represent manufacturing defects and simulate the effect of the circuits as well as determine the best place to make fixes within the circuit.

I will add more here with the other paper you sent me.

Specific Activities to be Undertaken and a Timetable Allotted for Each Activity:

During this upcoming fall semester, I plan to establish a working data structure that will support holding and reading different silicon photonic devices through their transfer matrix equations. I also plan to begin building the application program that will be able to read a file containing thousands of these data structures and be able to build the complete circuit within the program to run simulations and debug it. Finally, my last goal for the fall semester is to research and implement a topological searching algorithm that will find the best place within a circuit that can be fixed or improved to get better output from the circuit. I plan to spend about 8 hours every week working on my project and having a weekly meeting

with my mentor professor to make sure I get any questions answered and that I am making good progress in my project.

August 22 – Sept 2: I plan to research and experiment with different data structures that I find best fitting to represent and hold photonic circuit's transfer matrix equations. This will also include choosing the best programming language that will allow me to create my program with the most efficiency possible. I also will be developing the file type needed to store these circuits that can also be read from by a program.

Sept 5 – 16: During these next two weeks I will start creating UML (Unified Modeling Language) diagram to help myself plan out the key features and implementations I want in my program. I will also be researching what types of programming libraries are out there that can help me create a more efficient program.

Sept 19 – 30: I plan to begin the process of writing the code for my program and making sure I follow my UML design. I will break each part of my program into smaller parts so that I do not overwhelm myself by trying to write different parts of the program at the same time. Finishing the first small instance of my program which will be the data structure system and fie read/write process.

Oct 3 – 9 & 17-28: I will move on to the next part of the program which will be to visually represent the circuit I read from a file to the user in the program through a graphical user interface (GUI). I want the GUI to show the design of the circuit and outline the different parts within the circuit so the user can see each optical device within it. I also want to display any important information about the circuit to the user based on the file it reads in.

Oct 31 – Nov 23: Implement the topological sorting algorithm to measure and find the best point to debug a faulty or inefficient optical device within the circuit. I know this part will take me a little longer because there will be a lot of trial and error to fine-tune the algorithm and there might be a chance that I need to use a completely different algorithm than I anticipated. For that reason, I am giving myself more time to make sure I can find a good efficient algorithm.

Nov 29 – Dec 9: At this point, I should have everything I wanted to implement in my program but will be fixing up all my code and making improvements where they need to be to make sure my GUI looks clean and easy to understand. I will also be checking in with my mentor professor and ask if there are any details/features that I should add. I will be making this period somewhat light so that I can focus on finishing my classes with good grades as well as beginning to study for my finals.

Total hours: 120

Relationship of the Proposed Work to the Expertise of the Mentor: post-cmos design, comperer aided design and testing for cmos post cmos applications.

Relationship of the Proposed Work to Your Future Goals: