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New... Edit... Add...

Hier: Device F

system [system.qsys*]
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System Contents | Address Map | Interconnect Requirements

System: system **Path:** clk_0

Use	Connections	Name	Description	Export	Clock	Base	End	IRQ	Tags
✔		**clk_0**	Clock Source						
		clk_in	Clock Input	**clk**	***exported***				
		clk_in_reset	Reset Input	**reset**					
		clk	Clock Output	*Double-click to export*	clk_0				
		clk_reset	Reset Output	*Double-click to export*					
✔		**altpll_0**	ALTPLL Intel FPGA IP						
		inclk_interface	Clock Input	*Double-click to export*	**clk_0**				
		inclk_interface_reset	Reset Input	*Double-click to export*	[inclk_inte...				
		pll_slave	Avalon Memory Mapped Slave	*Double-click to export*	[inclk_inte...	**0x0400_0020**	0x0400_002f		
		c0	Clock Output	*Double-click to export*	altpll_0_c0				
		c1	Clock Output	**clk_25**	altpll_0_c1				
		c2	Clock Output	**sdram_clk_100**	altpll_0_c2				
✔		**jtag_master**	JTAG to Avalon Master Bridge						
		clk	Clock Input	*Double-click to export*	**clk_0**				
		clk_reset	Reset Input	*Double-click to export*					
		master	Avalon Memory Mapped Master	*Double-click to export*	[clk]				
		master_reset	Reset Output	*Double-click to export*					
✔		**sdram_controller**	SDRAM Controller Intel FPGA IP						
		clk	Clock Input	*Double-click to export*	**altpll_0_c0**				
		reset	Reset Input	*Double-click to export*	[clk]				
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	**0x0000_0000**	0x03ff_ffff		
		wire	Conduit	**sdram**					
✔		**bridge_0**	External Bus to Avalon Bridge						
		clk	Clock Input	*Double-click to export*	**altpll_0_c0**				
		reset	Reset Input	*Double-click to export*	[clk]				
		avalon_master	Avalon Memory Mapped Master	*Double-click to export*	[clk]				
		external_interface	Conduit	**interface**					
✔		**clock_bridge**	Clock Bridge						
		in_clk	Clock Input	*Double-click to export*	**altpll_0_c0**				
		out_clk	Clock Output	**clk_100**	clock_brid...				
✔		**framecount**	PIO (Parallel I/O) Intel FPGA IP						
		clk	Clock Input	*Double-click to export*	**altpll_0_c0**				
		reset	Reset Input	*Double-click to export*	[clk]				
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	**0x0400_0000**	0x0400_000f		
		external_connection	Conduit	**framecount**					
✔		**imagecount**	PIO (Parallel I/O) Intel FPGA IP						
		clk	Clock Input	*Double-click to export*	**altpll_0_c0**				
		reset	Reset Input	*Double-click to export*	[clk]				
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	**0x0400_0010**	0x0400_001f		
		external_connection	Conduit	**imagecount**					

Current filter:

Messages

Type	Path	Message
	1 Info Message	
	system.sdram_controller	SDRAM Controller will only be supported in Quartus Prime Standard Edition in the future release.

0 Errors, 0 Warnings

Generate HDL... Finish