CHAPTER 2

FPGA Development Board Hardware and I/O Features

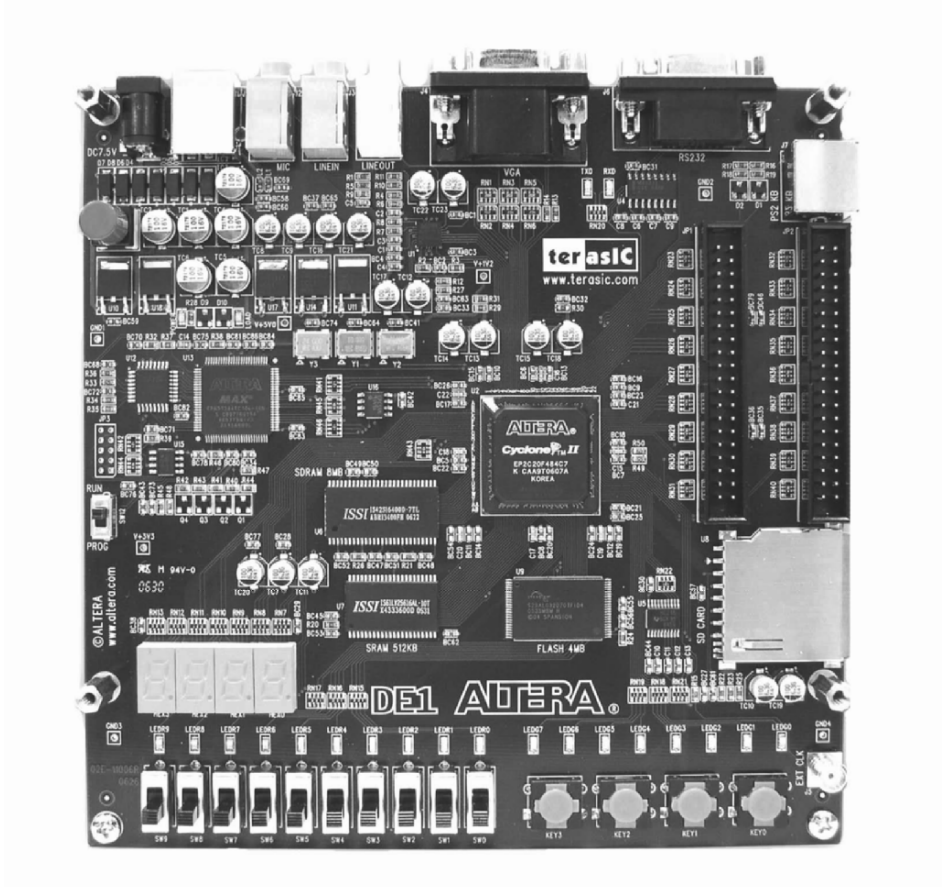

Photo: The Altera DE1 board contains a Cyclone II FPGA, external SRAM, SDRAM & Flash memory, and a wide assortment of I/O devices and connectors.

2 FPGA Development Board Hardware and I/O Features

Each of the five different FPGA boards (DE1, DE1, UP3, UP2, and UP1) have a slightly different feature set of logic, I/O interfaces, memory and other assorted hardware. As long as the FPGA board has enough logic and it has the required I/O features, a project can be implemented on any of the boards.

FPGAs are available in a wide range of sizes with different feature sets. In general, FPGAs with more logic, more I/O pins, higher speed, or more memory are more expensive. When designing new products, choosing the FPGA with the proper feature set at the lowest cost is an important design consideration.

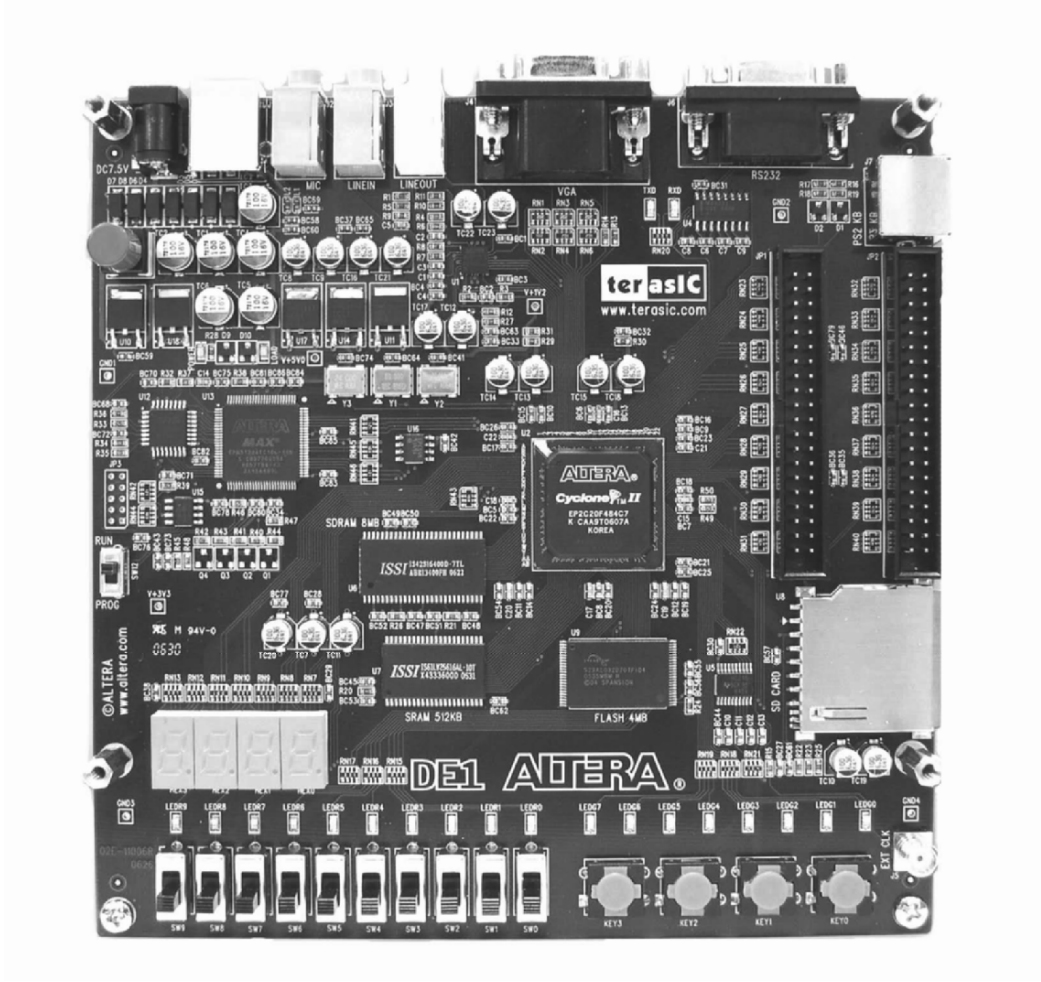

Figure 2.1 The Altera DE1 board has a number of onboard I/O devices.

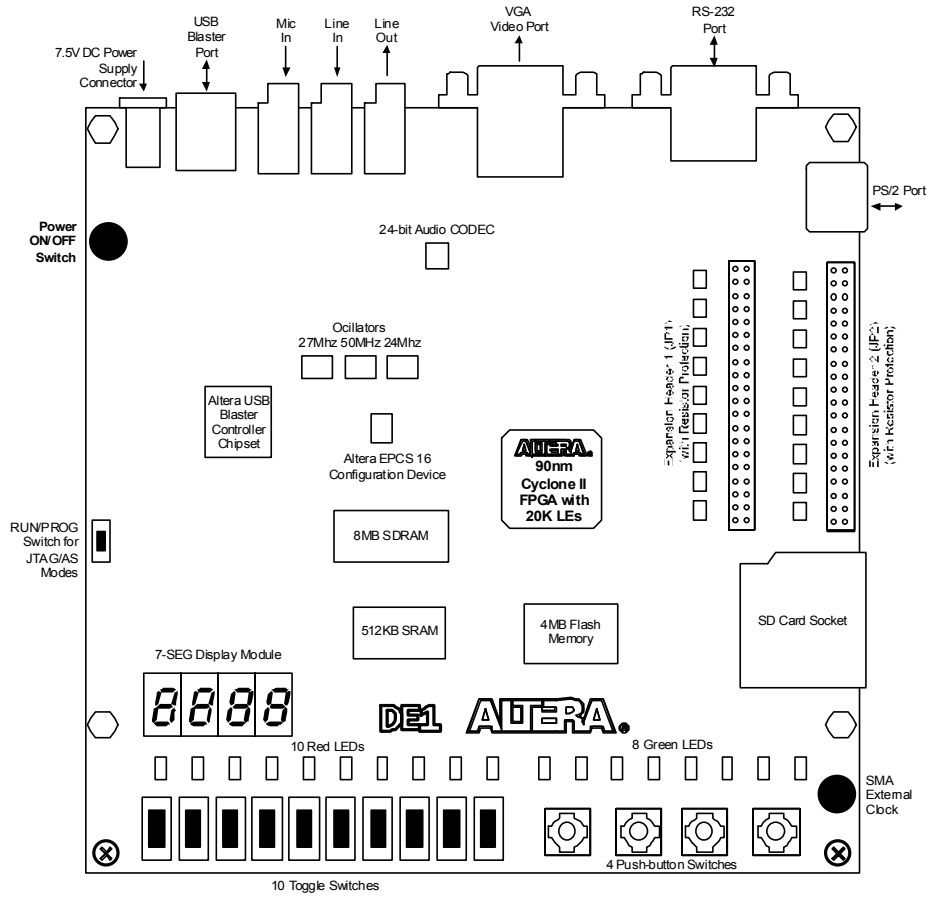

Figure 2.2 The Altera DE1 board's I/O features.

2.1 FPGA and External Hardware Features

On each of the boards, the FPGA is the large square chip located near the center of the development board. Locate the FPGA chip on the DE1 board as seen in Figures 2.1 and 2.2. Each of the various board's FPGAs has a different array of features. These are summarized for the different boards in Table 2.1. Each FPGA has a different number of logic elements (LE) that are used to implement user logic. They also contain varying amounts of both internal embedded memory blocks and the newer boards also have external memory.

FPGAs such as the Cyclone II found on the DE1 and DE2 boards are designed to support Digital Signal Processing (DSP) applications, so they also contain hardware integer multipliers.

On larger FPGAs, phase locked loops (PLLs) are used to divide, multiply, and shift the phase of clock signals. Remember that you must always compile your design for the correct board's FPGA device and pin assignments or it will not download to the device and operate correctly.

Table 2.1 FPGA and Hardware Features of the different development boards.

FPGA & Hardware Features	DE1	DE2	UP3	UP2 & 1
Introduction Year	2006	2006	2004	2001 & 1999
FPGA Family	Cyclone II	Cyclone II	Cyclone	Flex10K
Logic Elements (LEs)	18,752	35,000	6,000 (1C6) or 12,000 (1C12)	3,744 or 1,152 (UP1)
Approximate Max. Logic Gate Count[1]	500,000	1,000,000	189,000 (1C6) or 378,000	118,000 or 63,000(UP1)
FPGA Device Part Number	EP2C20F484C7	EP2C35F672 C6	EP1C6Q240C8 or (1C12) EP1C12Q240C 8	EPF10K70 RC240-4 or EPF10K20 RC240-4 (UP1)
Memory in bits	204K bits	483K bits	80K or 208K bits	18K bits 12K (UP1)
PLLs	4	4	2	No
Integer 18 by 18 bit Multipliers	26	35	No	No
External Clocks	24, 27, 50 Mhz	27, 50Mhz	48, 66, or 100Mhz	25Mhz
External SRAM Memory	256K by 16 bits	256K by 16 bits	64k by 16 bits	No
External SDRAM Memory	1M by 16 bits with 4 banks	1M by 16 bits with 4 banks	1M by 16 bits	No
Ext. Flash Memory	4M by 8 bits	4M by 8 bits	1M by 8 bits	No
Nios II Processor SoC Designs Supported	Yes	Yes	Yes	No

2.2 The FPGA Board's Memory Features

In addition to the FPGA's internal memory, the newer boards provide several external ROM and RAM memory devices as seen in Table 2.1. Capacities of external memory are much larger than the internal memory, but they will have a slower access time.

FPGA processor cores such as the Nios II used in System-on-a-Chip (SoC) designs use external memory for program and data memory, and typically use the FPGA's smaller and faster internal memory for register files and a cache. Flash and EEPROM are used to provide non-volatile memory storage. The EPCS1 serial Flash chip is used to automatically load the FPGA's serial configuration data at power up in final systems where you do not want to download the board with the ByteBlaster each time power is applied.

[1] This is only a very crude estimate of the number of equivalent two input NANDs in the FPGA's hardware design. This should be viewed only as a very rough estimate since any real design cannot use every feature of every logic element. The estimates given here also include additional gates in the total count to account for the FPGA's embedded memory blocks and hardware multipliers. Such crude gate count estimates can also vary by a factor of two or more between different FPGA venders for a similar device and they are rarely used now in industry.

A larger Flash memory chip is typically used to boot the initial program code on SoC designs that include a processor. Note that the older UP2 and UP1s cannot support a Nios processor since they lack external memory and have a smaller older FPGA. Links to detailed datasheets for many of the different board's memory chips can be found on the book's DVD or at the book's website.

Each board contains a crystal controlled clock circuit that is normally used as the master clock for the user's digital logic circuit. Note that the frequency of the clock is different on the boards as seen in table 2.1. PLLs can be used to scale the crystal controlled clock to provide other clock frequencies.

2.3 The FPGA Board's I/O Features

Each board provides a wide variety of I/O features as summarized in Table 2.2. For most devices, the FPGA board's hardware provides only an electrical interface to the FPGA's I/O pins. Logic that provides a device interface circuit or controller will need to be constructed by the user using the FPGA's internal logic. Many design examples of interfacing to these various I/O devices can be found in the following chapters of this book.

Standard 0.1 inch headers on each of the boards can be used to interface to external devices off of the board. A small custom PCB can be designed or a 0.1 inch predrilled perforated protoboard can be used to plug into the header connectors on the board. Standard 0.1 inch ribbon cable connector technology can also be used to connect to another board with custom user hardware.

Table 2.2 The I/O Features of the different development boards.

I/O Features	DE1	DE2	UP3	UP1& 2
Pushbuttons	4 - debounced	4 - debounced	4 –no debounce	2 –no debounce
User Switches	18	10	4	8
User LEDs	8 green 10 red	9 green 18 red	4	No
LCD Panel	No	16 char x 2 line	16 char x 2 line	No
Seven Segment LED Displays	4	8	No	2
PS/2	Yes	Yes	Yes	Yes
RS-232 Serial	Yes	Yes	Yes	No
VGA output	2^{12} colors	2^{30} colors	8 colors	8 colors
I/O Expansion Header Pins	2 – 40 Pin connectors	2 – 40 Pin connectors	4 – 72 I/O Pins total	3 – add 60 Pin headers
TV Decoder	No	Yes	No	No
SD Card slot	Yes	Yes	No	No
Printer Port	No	No	Yes	No
Audio CODEC	24-bit	24-bit	No	No
User USB	No	Yes	No	No
IrDA	No	Yes	No	No
Network	No	10/100Mhz	No	No
Optional Camera and Color LCD Panel	Yes	Yes	No	No

Modern FPGAs are surface-mount chips that are soldered directly to the board. It is difficult if not impossible to replace the FPGA chip without expensive surface mount soldering equipment, so extreme care should be exercised when interfacing the FPGA I/O pins to any external devices.

Standard I/O connector pin assignments used for external PS/2, serial, parallel, VGA, network and USB I/O cables can be found in Appendix F.

Table 2.3 Requirements to use the different I/O Features

I/O Device	Description	Hardware Interface Needed
USB 1.1	Full Speed and Low Speed	Processor & USB SIE engine core
Serial Port	RS 232 Full Modem	UART to send and receive data
Parallel Port	IEEE 1284	State machine or Proc. for handshake
PS/2 Port	PC Keyboard or Mouse	Serial Data - PS/2 state machine
VGA Port for Video Display on Monitor	RGB three 1-bit signals on UP1,2,3, 10-bits on DE2 and 3-bits on DE1	State machine for sync signals & user logic to generate RGB color signals
IDE Port	Connector on UP3	Processor & IDE Device Driver
Reset Switch	Global Reset on UP3	Must use a reset in design
Pushbutton Switches	debounced on DE1 & DE2 but not on the UP1,2, & 3	Most applications will need a switch debounce Circuit on UP1,2,3
Expansion Cards	Connect to .1 inch headers	Depends on expansion card used
LEDs	1=ON (DE1 & DE2)	None, but uses 1 FPGA I/O pin
LCD Display	16 Character by 2 line ASCII Characters on DE2& UP3	State machine or Processor to send ASCII characters and LCD commands
Real Time Clock	I^2C clock chip on UP3	Serial Data - I^2C state machine
DIP/Slide Switch	Switches (1=ON)	None or Synchronizer Circuit

WHEN CONNECTING EXTERNAL HARDWARE, ADDITIONAL PINS ARE AVAILABLE FOR USE ON THE HEADER CONNECTORS ON THE BOARD. FOR DETAILS, REFER TO THE BOARD'S REFERENCE MANUAL, WHICH IS ON THE BOOK'S DVD, AND IS ALSO AVAILABLE FREE AT HTTP://WWW.ALTERA.COM OR AT HTTP://WWW.TERASIC.COM.

Also, remember to assign pins as shown in the tutorials to avoid randomly turning on several of the memory devices at the same time. A tri-state bus conflict occurs when several tri-state outputs are turned on and they attempt to drive a single signal line to different logic levels. It is possible that such a tri-state bus conflict on the memory data bus could damage the devices by overheating after several minutes of operation.

Table 2.4 contains the pin assignments and names used for the DE1, DE2, UP3, and UP2 board's most commonly used I/O devices that are used in basic digital designs. A complete list of all pin assignments for all of the boards is too lengthy to include here; however, they can be found in each of the FPGA board's user manuals that are available on the book's DVD in *Board*\Chap2.

Table 2.4 DE1, DE2, UP3, and UP2 Board's FPGA I/O pin names and assignments

Pin Name	DE1	DE2	UP3	UP2, UP1	Pin Type	Function of Pin
KEY0	R22	G26	48	28 PB1	Input	Pushbutton KEY0 (debounced, 0 = button hit)
KEY1	R21	N23	49	29 PB2	Input	Pushbutton KEY1 (debounced, 0 = button hit)
KEY2	T22	P23	57	-	Input	Pushbutton KEY2 (debounced, 0 = button hit)
KEY3	T21	W26	62	-	Input	Pushbutton KEY3 (debounced, 0 = button hit)
LEDR0	R20	AE23	56	25 0=on	Output	RED LED R0 (1 = LED ON, 0= LED OFF)
LEDR1	R19	AF23	55	14 0=on	Output	RED LED R1 (1 = LED ON, 0= LED OFF)
LEDR2	U19	AB21	54	-	Output	RED LED R2 (1 = LED ON, 0= LED OFF)
LEDR3	Y19	AC22	53	-	Output	RED LED R3 (1 = LED ON, 0= LED OFF)
SW0	L22	N25	58	41	Input	Slide or DIP Switch (0=Down, non-debounced)
SW1	L21	N26	59	40	Input	Slide or DIP Switch (0=Down, non-debounced)
SW2	M22	P25	60	39	Input	Slide or DIP Switch (0=Down, non-debounced)
SW3	V12	AE14	61	38	Input	Slide or DIP Switch (0=Down, non-debounced)
HEX0[0]	J2	AF10	-	6	Output	Seven Segment Display 0 LED Segment A (0=on)
HEX0[1]	J1	AB12	-	7	Output	Seven Segment Display 0 LED Segment B (0=on)
HEX0[2]	H2	AC12	-	8	Output	Seven Segment Display 0 LED Segment C (0=on)
HEX0[3]	H1	AD11	-	9	Output	Seven Segment Display 0 LED Segment D (0=on)
HEX0[4]	F2	AE11	-	11	Output	Seven Segment Display 0 LED Segment E (0=on)
HEX0[5]	F1	V14	-	12	Output	Seven Segment Display 0 LED Segment F (0=on)
HEX0[6]	E2	V13	-	13	Output	Seven Segment Display 0 LED Segment G (0=on)
HEX1[0]	E1	V20	-	17	Output	Seven Segment Display 1 LED Segment A (0=on)
HEX1[1]	H6	V21	-	18	Output	Seven Segment Display 1 LED Segment B (0=on)
HEX1[2]	H5	W21	-	19	Output	Seven Segment Display 1 LED Segment C (0=on)
HEX1[3]	H4	Y22	-	20	Output	Seven Segment Display 1 LED Segment D (0=on)

Pin Name	DE1	DE2	UP3	UP2, UP1	Pin Type	Function of Pin
HEX1[4]	G3	AA24	-	21	Output	Seven Segment Display 1 LED Segment E (0=on)
HEX1[5]	D2	AA23	-	23	Output	Seven Segment Display 1 LED Segment F (0=on)
HEX1[6]	D1	AB24	-	24	Output	Seven Segment Display 1 LED Segment G (0=on)
LCD_E	-	K3	50	-	Output	LCD Enable line
LCD_RW	-	K4	73	-	Output	LCD R/W control line
LCD_RS	-	K1	108	-	Output	LCD Register Select Line
LCD_DATA[0]	-	J1	94	-	Bidir.	LCD Data Bus
LCD_DATA[1]	-	J2	96 (133)	-	Bidir.	LCD Data Bus
LCD_DATA[2]	-	H1	98	-	Bidir.	LCD Data Bus
LCD_DATA[3]	-	H2	100	-	Bidir.	LCD Data Bus
LCD_DATA[4]	-	J4	102 (108)	-	Bidir.	LCD Data Bus
LCD_DATA[5]	-	J3	104	-	Bidir.	LCD Data Bus
LCD_DATA[6]	-	H4	106	-	Bidir.	LCD Data Bus
LCD_DATA[7]	-	H3	113	-	Bidir.	LCD Data Bus
PS2_CLK	H15	D26	12	30	Bidir.	PS2 Connector
PS2_DATA	J14	C24	13	31	Bidir.	PS2 Connector
CLOCK	L1	N2	153 48Mhz	91 25Mhz	Input	50MHz Crystal Controlled Clock
VGA_RED	B7	E10	228	236	Output	VGA Red Video Signal (highest bit)
VGA_GREEN	A8	D12	122	237	Output	VGA Green Video Signal (highest bit)
VGA_BLUE	B10	B12	170	238	Output	VGA Blue Video Signal (highest bit)
VGA_VSYNC	B11	D8	226	239	Output	VGA Connector Vertical Sync Signal
VGA_HSYNC	A11	A7	227	240	Output	VGA Connector Horizontal Sync Signal

The pushbuttons are not debounced on the UP3 and its clock frequency depends on the board's JP3 jumper settings. Set JP3 to short pins 3-4 for the 48Mhz clock. UP3 pins enclosed in parenthesis in table 2.4 are for the larger FPGA used in the 1C12 version of the UP3 board. It requires more power and ground pins so there are some minor pin differences.

On the UP2 board, the two pushbuttons are not debounced, the LEDs are the seven segment decimal points, and its clock is 25Mhz. The original UP1 boards look very similar to a UP2 and they use the same pin assignments as the UP2, but they contain a smaller EPF10K20RC240 FPGA. Verify the part number on the large FPGA chip on the right side of the board, if you are uncertain.

NOTE: If you ever switch a design to a different board, you will need to change the device type, redo all of the pin assignments, and then recompile for the new FPGA device. The voltage levels on FPGA pins can vary (3.3V or 5V), so be sure to check for the proper voltage levels when selecting an I/O pin to interface external hardware to the board.

Do not connect high current devices such as motors or relay coils directly to FPGA I/O pins. These pins cannot provide the high current levels needed, and it may damage the FPGA's.

2.4 Obtaining an FPGA Development Board and Cables

FPGA boards are available for purchase from Altera's University Program at special educational pricing for schools and students (www.altera.com in the University Program area). The newest board, the DE1, is ordered, produced, and shipped directly from the manufacturer to minimize cost (www.terasic.com). Other DE2 and DE1 accessories such as a camera module and a small 320 by 240 color LCD panel are also available. Some UP3 add-on boards such as an A/D card can also be found at www.slscorp.com .

A Longer Cable for the ByteBlaster on UP3, UP2, and UP1 boards

For use with the UP3, UP2 or UP1 boards, a longer 25pin to 25pin PC M/F parallel printer cable is useful since the 1 foot Byteblaster II cable provided with the boards is often too short to reach the PC's printer port. All 25 wires must be connected in the printer extension cable. Any computer store should have these cables. A three-foot well-shielded cable works best. Avoid using extra long cables or very low-cost cables without good shielding as they can cause problems. The newer DE1 and DE2 boards come with a newer USB-based ByteBlaster that has a longer USB cable, so no additional cable is needed.

ADDITIONAL REFERENCE MATERIALS AND DOCUMENTATION FOR EACH FPGA BOARD CAN BE FOUND ON THE BOOK'S DVD IN THE *\BOARD*CHAP2 SUBDIRECTORIES.