20-EECE-681—Quarter Project
April 1, 2009

Your overall goal for this quarter is to design and implement on the provided Altera boards an "optimal" processor. Parameters for optimization include speed, size, power usage, and potential for upgrading with wider datapath, more instructions, etc. The processor will be designed in three phases. Your processor must have the following characteristics:

Phase 1:
--8 or 16 bit datapath
--maximal clock speed
--input may be through a preloaded data file, along with a menu on the CRT which is accessed through the mouse
--output may be to a file which can be displayed appropriately on the CRT
--ability to execute 4 benchmark programs:
a. mergesort of a list of integers
b. quicksort of the same list
c. matrix multiplication
d. fast Fourier transform

Phase II: add pipelining

Phase III: add a second processor and memory management for dual-core processing

The initial specifications for the architecture will be given to you.
You may want to develop a simple assembly language to make programming the processor easier.

Your project will be completed through a series of weekly assignments. Each assignment will consist of a written report and appropriate VHDL source code, test results, and demonstrations. Written work should be submitted in ONE DOCUMENT, in the old .doc format, to the course digital dropbox. The NAME of this document MUST BE:

TEAMLETTER_REPORT_NUMBER.doc

where TEAMLETTER is the letter assigned to your team and NUMBER is the assignment number (Example, W_REPORT_1.doc). Documents submitted using any other naming format will be deleted unread.

Week 1 REPORT_1, due Monday, April 6:

Include the following sections:

a. **RESOURCES AND PLANNING**

SECTION 1: RESOURCES.

a. List all personnel and skills of each (VHDL or Altera experience, hardware or software project experience, good writing skills, etc.)

b. List the number of hours each team member has available to devote to the project over the quarter (8 hours per week is probably a minimum)

c. List all hardware and software resources that will be used for development. Include any computers owned by the team members as well as the hardware and software in 890 Rhodes.

SECTION 2: PLANNING.

a. List who will be assigned to oversee each of the following: documentation; testing; version control and backups; tracking and productivity

b. Describe how the team members will communicate, including meetings, email, phone, etc., and how they will coordinate their work.

c. Give the time and place of weekly team meetings (at least one meeting per week is required).

d. Describe completely how you will handle version control and backups.

e. Describe your plan for testing. Altera does not support testbenches, only .vec files. How will you document your testing?

f. Provide both a Gantt chart and Tracking Document for your project. You will need to update the tracking document each week and include the updated documents in your project report.

g. Describe the coding and documentation standards you will use.

h. Describe how you will produce up-to-date documentation (content and form—online?) in parallel with the project. You will need to produce supporting documents, including a user manual, along with code documentation.

SECTION 3: HARDWARE BASICS

a. Describe the board you will be using, including:
    chip capability, including gate count, clock speed, memory, etc.
    I/O devices

b. Describe the capabilities of other chips which you can simulate using the design tools provided (in the event that the chip you have will not support dual-core processing)

c. Describe the information you can obtain from the design tools about gate usage, speed, power, layout, etc. which will be needed to analyze the performance of your processor.

d. Explain the procedure you will use for testing a hardware module with the given tools and documenting your test results.

e. Perform the following simple experiments and report the results:

1. What is the length of a critical path between two flipflops? Does this depend on the placement of the flipflops? Do "glitches" occur in the simulation? In the circuit? Are these significant?

2. Design a D flip-flop starting from the gate level. Compare its behavior with the D flipflop in the Altera VHDL library. Can you vary the clocking strategy—rising-edge, falling-edge, level triggered? Is one strategy preferable for this hardware?

3. Repeat problem 2 for a 4-bit adder.

4. Can you detect changes in a simple gate's switching behavior which depend on its fanout?

Example charts (see next page):

Sample Gantt chart:

Work Tasks	**Week 1**				**Week 2**				**Week 3**				**Week 4**				**Week 5**			
1. plan project																				
define project needs	x																			
define resources	x																			
determine skill levels	x																			
conduct prelim. exper.		x	x																	
Milestone: project planned			@																	
2. define requirements			x																	
write req document			x	x	x															
Milestone: req defined					@															
3. Write specifications					x															
create architecture						x	x													
……..																				

Sample tracking document:

Work Tasks	Start-Plan	Start-Actual	Done-Plan	Done-Actual	Per-son (s)	Effort (hours)	Notes
1. plan project							
define project needs	w1,d1	w1,d1	w1,d1	w1,d1	ab	4	
define resources	w1,d1	w1,d1	w1,d1	w1,d1	cd	3	
determine skill levels	w1,d1	w1,d1	w1,d1	w1,d1	cd	3	
conduct prelim. exper.	w1,d2	w1,d2	w1,d3	**w1,d4**	ab,cd	8	exper too large
Milestone: project planned	w1,d3	w1,d3	w1,d3	**w1,d4**			1 day behind
2. define requirements							
write req document							
Milestone: req defined							
3. Write specifications							
create architecture							
……..							