UART HDL Technical Reference Manual

Version 1.0

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1 Device Operation

You can find the HDL for this module in this github repository: GregWills97/fpga-uart-project

2 Configuration Registers

2.1 Register Overview

This section describes the hardware configuration registers for the UART HDL module.

2.2 Data Register: UARTDR

The UARTDR is the data register for the UART device.

To transmit words, the user issues a write to this register. When written to, the data is placed into the transmit FIFO and the write address is incremented. Data is automatically prefixed with a start bit and appended with parity and stop bits if needed.

Received byte reads are performed by issuing a read to the UARTDR register. The read will return data from the receive FIFO and increment the FIFO address along with any errors associated with that character. A write to bits 7:0 of this register clears the error bits.

The receiver detects the following errors:

- **Overrun Error**: when HIGH indicates that the rx fifo is full and data was received.
- **Break Error**: when HIGH indicates that the rx input has been held LOW for longer than a full-word transmission.
- **Parity Error**: when HIGH indicates that the parity of the data character does not match the parity indicated by the parity setting in the LCTRL register.
- **Framing Error**: when HIGH indicates invalid stop bit.

Field Description

Bits	Name	Access	Reset	Description
31:12	RESERVED	-	0x0	Reserved.
11	OE	R	0x0	Overrun error bit, set HIGH when rx fifo is full.
10	BE	R	0x0	Break error bit, set HIGH when break error detected.
9	PE	R	0x0	Parity error bit, set HIGH when parity error detected.
8	FE	R	0x0	Framing error bit, set HIGH when framing error detected.
7:0	DATA	R/W	0x00	READ: data from rx fifo is returned. WRITE: data written is put on the tx line.

Table 2.1: UARTDR Field Description

Notes:

- Writes will be ignored if transmit FIFO is full.