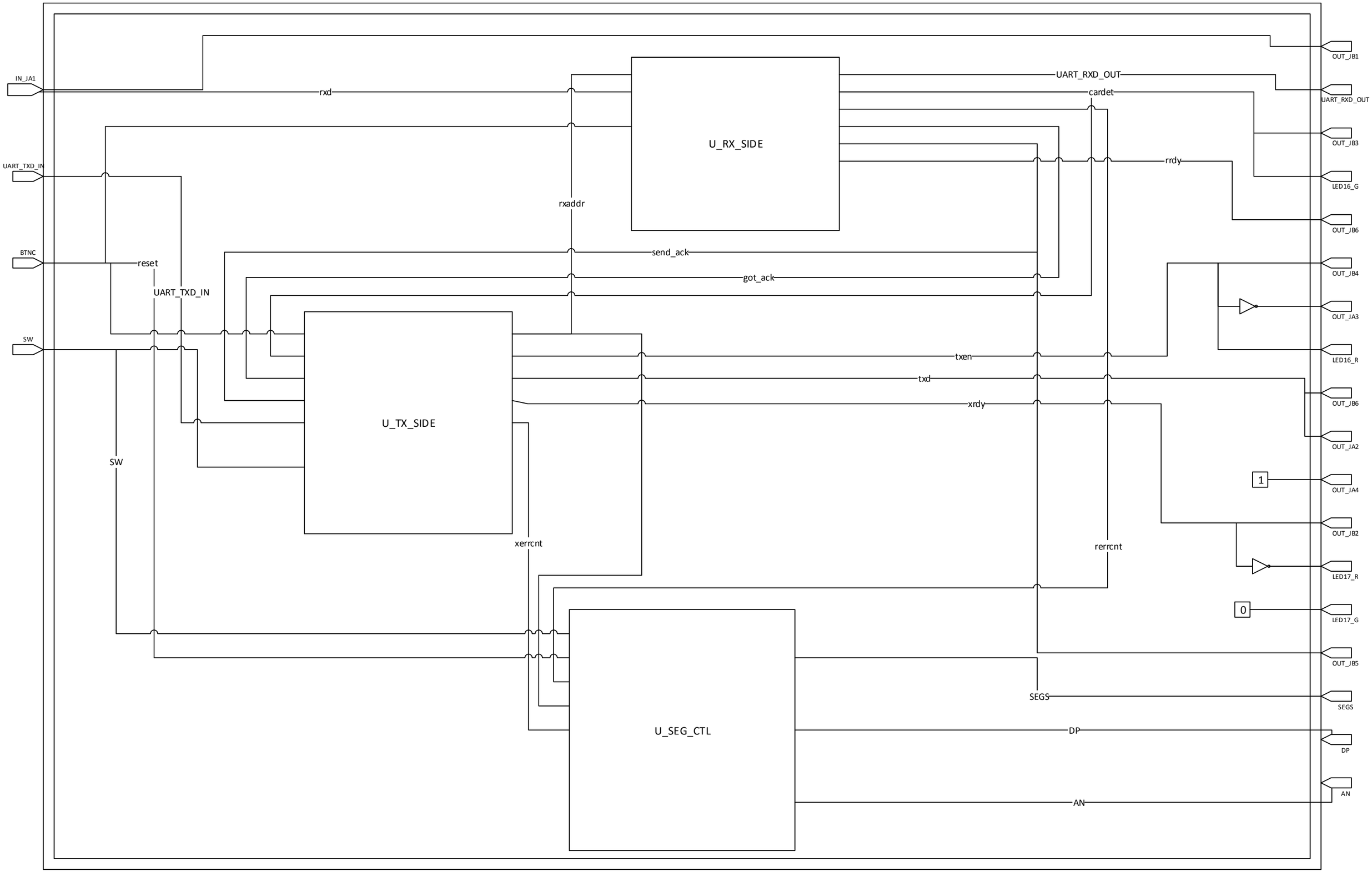
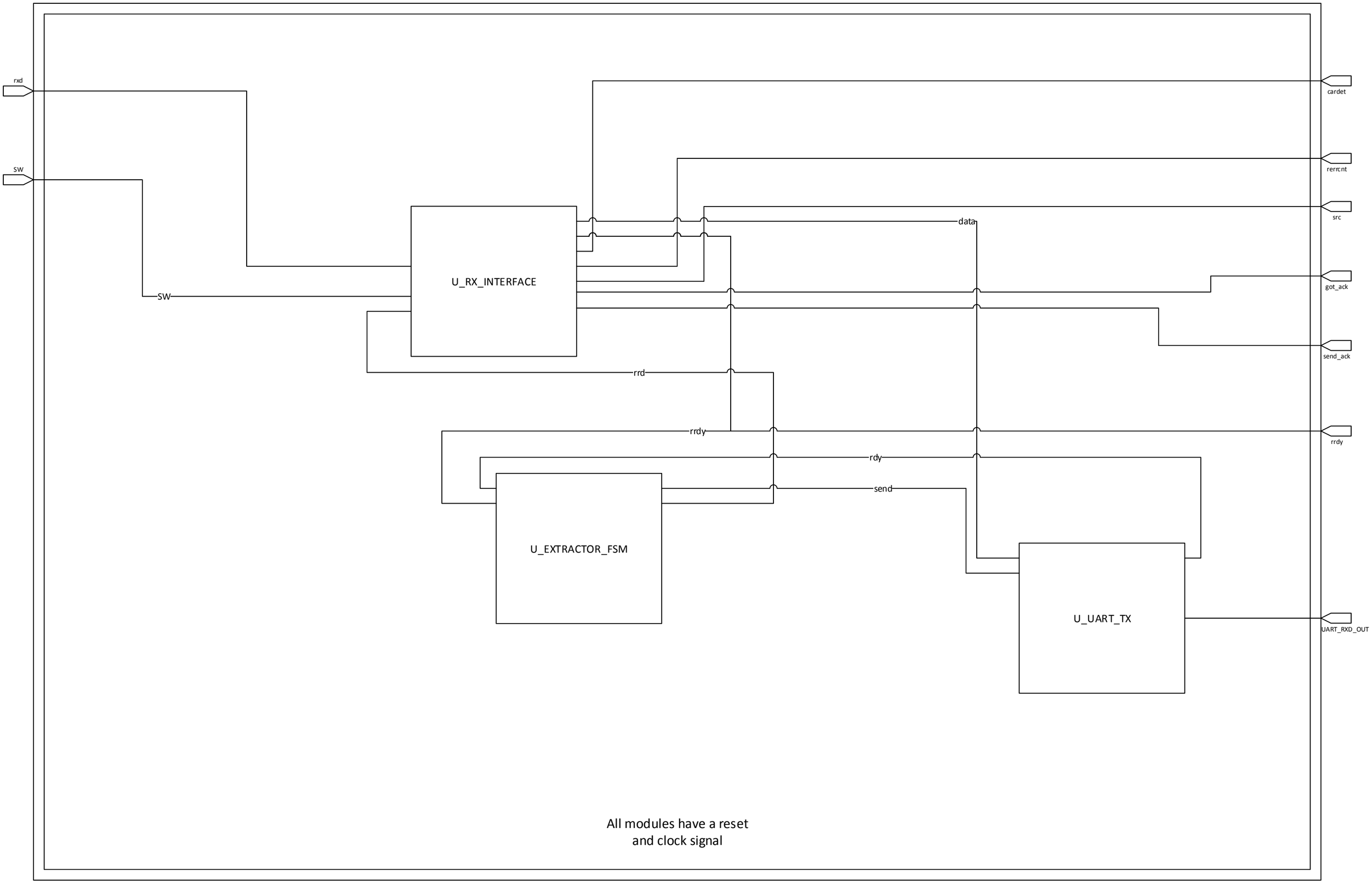
Top level Block Diagram



Receiver side



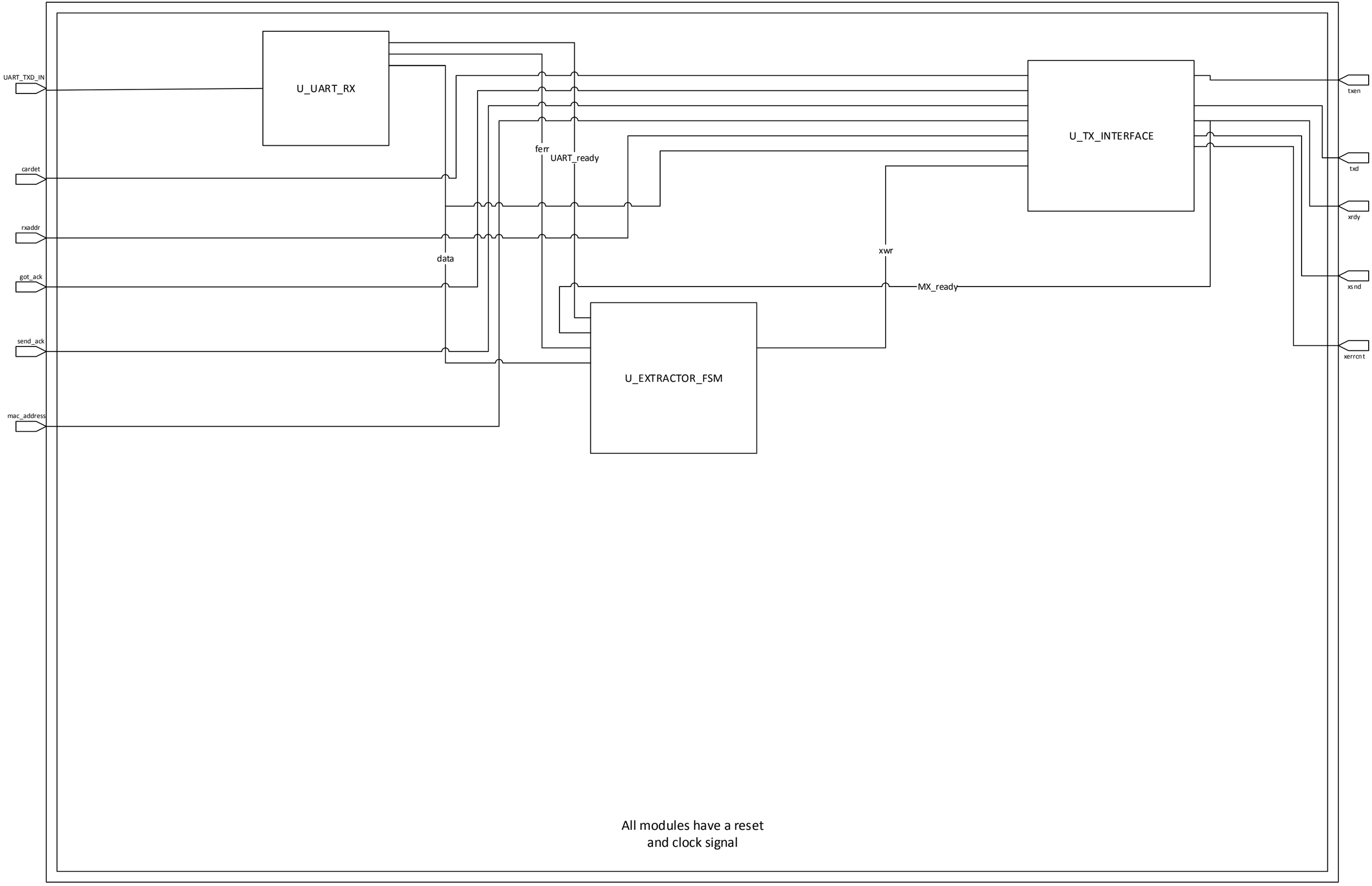
All modules have a reset
and clock signal

Receiver Interface

rxd
mac
rrd
cardet
rerrcnt
src
got_ack
send_ack
rrdy
rdata
empty
we
U_RX_MX
U_CRC_ERROR_COUNT
Frame_type == 3
Data_available
Frame_type == 2
Data_available
Dest != ALL_CALL
U_FSM_ADDR
U_FCS_FSM
U_CRC_GEN
U_FIFO
U_FSM_FRAME_ID
U_FRAME_TYPE_COUNTER
&
|
Data_rx
error
write_rx
dest
Pop_fifo
Data_available
Inc_rerr
Force_write
crc
dout
Enb_crc
Reset_crc
Write_enb
Clear_fifo
Frame_type
Byte_count

All modules have a reset
and clock signal

Transmitter side



All modules have a reset
and clock signal

Transmitter interface