

```

bit4To7segX2_dec.v
Compilation Report - bit4To7segX2_dec
1  /** 4 bit binary to 7 segment encoder.
2  - dec output
3  - active low
4
5  @Param z least significant
6  @Param w most significant
7  @Return 1-9 , blank otherwise
8
9  */
10 module bit4To7segX2_dec(
11     input w,x,y,z,
12     output reg
13     a1,b1,c1,d1,e1,f1,g1, //1
14     a2,b2,c2,d2,e2,f2,g2 //10
15 );
16 always @ (w,x,y,z) begin
17     //1's
18     case ({w,x,y,z})
19         4'b0000: {a1,b1,c1,d1,e1,f1,g1} = 7'b00000001; //0
20         4'b0001: {a1,b1,c1,d1,e1,f1,g1} = 7'b10011111; //1
21         4'b0010: {a1,b1,c1,d1,e1,f1,g1} = 7'b00100010; //2
22         4'b0011: {a1,b1,c1,d1,e1,f1,g1} = 7'b00001100; //3
23         4'b0100: {a1,b1,c1,d1,e1,f1,g1} = 7'b10011100; //4
24         4'b0101: {a1,b1,c1,d1,e1,f1,g1} = 7'b01001000; //5
25         4'b0110: {a1,b1,c1,d1,e1,f1,g1} = 7'b01000000; //6
26         4'b0111: {a1,b1,c1,d1,e1,f1,g1} = 7'b00011111; //7
27         4'b1000: {a1,b1,c1,d1,e1,f1,g1} = 7'b00000000; //8
28         4'b1001: {a1,b1,c1,d1,e1,f1,g1} = 7'b00011000; //9
29         4'b1010: {a1,b1,c1,d1,e1,f1,g1} = 7'b00000001; //10 -> 0
30         4'b1011: {a1,b1,c1,d1,e1,f1,g1} = 7'b10011111; //11 -> 1
31         4'b1100: {a1,b1,c1,d1,e1,f1,g1} = 7'b00100010; //12 -> 2
32         4'b1101: {a1,b1,c1,d1,e1,f1,g1} = 7'b00001100; //13 -> 3
33         4'b1110: {a1,b1,c1,d1,e1,f1,g1} = 7'b10011100; //14 -> 4
34         4'b1111: {a1,b1,c1,d1,e1,f1,g1} = 7'b01001000; //15 -> 5
35     endcase
36     //10's
37     if (w == 1 & (x == 1 | y == 1))
38         {a2,b2,c2,d2,e2,f2,g2} = 7'b10011111; //x >= 10 -> 1
39     else
40         {a2,b2,c2,d2,e2,f2,g2} = 7'b11111111; // x < 10 -> [blank]
41 end
42 endmodule
43

```

Assignment Editor - D:\uta\_stuff\cse2441\cse2441\_labs\lab6\part2\bit4To7segX2\_dec - bit4To7segX2...

File Edit View Tools Window Help

Search altera.com

<<new>> Filter on node names: \* Category: All

	tatu	From	To	Assignment Name	Value	Enabled	Entity
1	✓		out a2	Location	PIN_C18	Yes	
2	✓		out b1	Location	PIN_E15	Yes	
3	✓		out b2	Location	PIN_D18	Yes	
4	✓		out c1	Location	PIN_C15	Yes	
5	✓		out c2	Location	PIN_E18	Yes	
6	✓		out d1	Location	PIN_C16	Yes	
7	✓		out d2	Location	PIN_B16	Yes	
8	✓		out e1	Location	PIN_E16	Yes	
9	✓		out e2	Location	PIN_A17	Yes	
10	✓		out f1	Location	PIN_D17	Yes	
11	✓		out f2	Location	PIN_A18	Yes	
12	✓		out g1	Location	PIN_C17	Yes	
13	✓		out g2	Location	PIN_B17	Yes	
14	✓		in w	Location	PIN_C12	Yes	
15	✓		in x	Location	PIN_D12	Yes	
16	✓		in y	Location	PIN_C11	Yes	
17	✓		in z	Location	PIN_C10	Yes	
18	✓		out a1	Location	PIN_C14	Yes	
19		<<new>>	<<new>>	<<new>>			