Name: _____ ID# _____

Date Submitted: _____ Time Submitted _____

CSE 3341 Digital Logic Design II

CSE 5357 Advanced Digital Logic Design

Fall Semester 2024

Lab 4 – Registered Four x Four Signed Multiplier

Due Date – October 11, 2024 (11:59 PM)

Submit on Canvas Assignments
(Note new submission requirements below)

Note – Late submissions will not be accepted!

Submission Requirements

- Submit the entire Quartus project in a zipped folder to ensure all files are included for execution.
- Name the zip file as `netid_assignment_x` where `netid` is your university network ID, and `x` corresponds to the assignment number (e.g., `jdx1234_assignment_1`).
- Make sure the project files can be run seamlessly on another machine without any missing dependencies.

Contact the TA for any clarification or help.

CSE 3341/5357 **LAB ASSIGNMENT 4** **FALL 2024**

Registered Four x Four Signed Multiplier

(200 POINTS)

ASSIGNMENT

Your assignment is to design a registered four-by-four signed multiplier by modifying the four-by-four unsigned shift-and-add multiplier shown below and discussed in class.

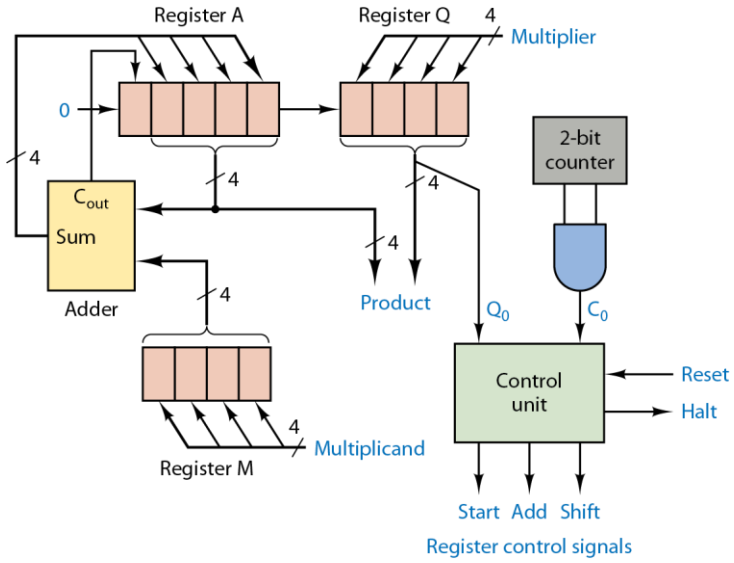

Figure 1. Four-by-four Unsigned Shift-and-Add Multipler Data Path

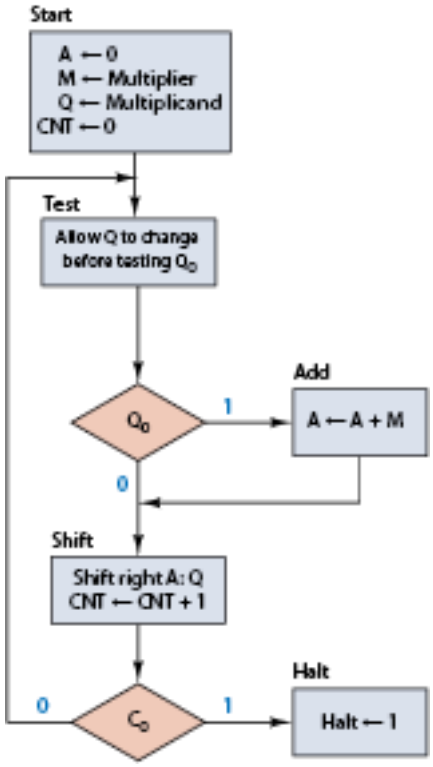

Figure 2. Four-by-four Unsigned Shift-and-Add Multiplier Control Path.

DESIGN REQUIREMENTS

1. Registered 4 x 4 multiplier
2. Signed numbers (use 2's complement for negative numbers)
3. DE10-Lite realization
4. CSE 5357 students must implement a counter to display the number of clock cycles required for each test case below to earn full credit (20 points).

DESIGN PROCESS

1. Design, implement, and test an ***unsigned version***. (50 points)
2. Design, implement, and realize a ***signed version***. (150 points)

RTL ANALYSIS

1. Generate RTL diagrams using the Quartus Prime Netlist Viewer for each version.
2. Record the compilation summary for your report. How many ALM, registers, and pins does your design require?

TIMING ANALYSIS

1. Run a timing analysis on your **signed multiplier** and determine its maximum operating speed in GHz.
2. Capture a screen shot of your timing analysis waveform showing the fastest clock speed your design will accommodate.

DE10-Lite IMPLEMENTATION

1. Implement your signed multiplier on the DE10-Lite using the following inputs/outputs. Use pin assignments of your choice.

   Inputs *M, Q, InM, InQ,*
   Outputs *Mout*, *Qout*, *Pout.* Display in hexadecimal on the HEXboard display.

2. Include a table of your pin assignments in your report.
3. Program the DE10-Lite with your design.

DE10-Lite TESTING

1. Test your implementations by applying these test patterns
   a. 0111 x 0001
   b. 0001 x 0001
   c. 0101 x 1010
   d. 0111 x 1111
   e. 1010 x 0011
   f. 1010 x 1110
   g. 1101 x 1101
   h. 1111 x 1111
2. Record the test results in a table for your report.
3. Take a picture of your results for your report.

REPORT REQUIREMENTS

1. Cover sheet
2. Datapath and control path diagrams*
3. Verilog code*
4. RTL diagrams*
5. Timing analysis results
6. I/O assignments
7. Test results
8. Photos of test results

* Both unsigned and signed versions.