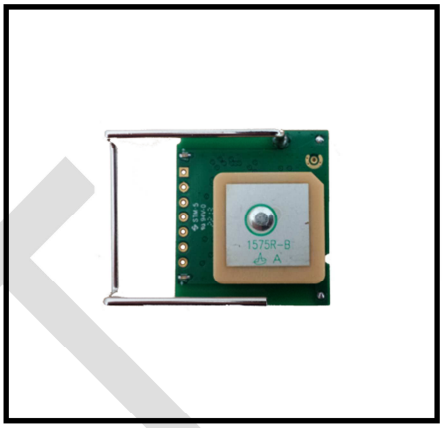
TD1205

HIGH-PERFORMANCE, LOW-CURRENT SIGFOX™ GATEWAY AND GPS RECEIVER WITH INTEGRATED ANTENNAS

Features



SIGFOX™ certified Gateway and RF transceiver with antenna

- Frequency range = ISM 868 MHz
- Receive sensitivity =-126 dBm
- Modulation
  - (G)FSK, 4(G)FSK, GMSK
  - OOK
- Max power radiated from integrated antenna
  - +14 dBm
- Low active radio power consumption
  - 20µA RX (windowed mode)
  - 95 mA TX @ +14 dBm

Multi-GNSS GPS Receiver with active antenna

- Multi-GNSS support
  - GPS/GLONASS
  - SBAS augmentation services
- Ultra-low power consumption
  - 29 mA Acquisition
  - 12 µA Backup
- High Sensitivity
  - 56-channel engine
  - -162 dBm Tracking
  - -148 dBm Cold start

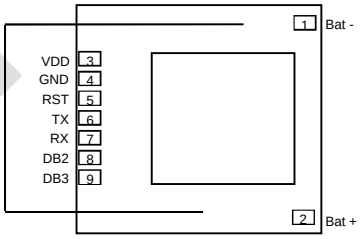
Ultra-low power 3D Accelerometer

- Up to ±16g full scale

Board characteristics

- Power supply = 2.3 to 3.6 V
- 2.5 µA idle state consumption
- Small form factor: 30x38x10.5mm
- Green and Red LED

Pin Assignments



Patents pending

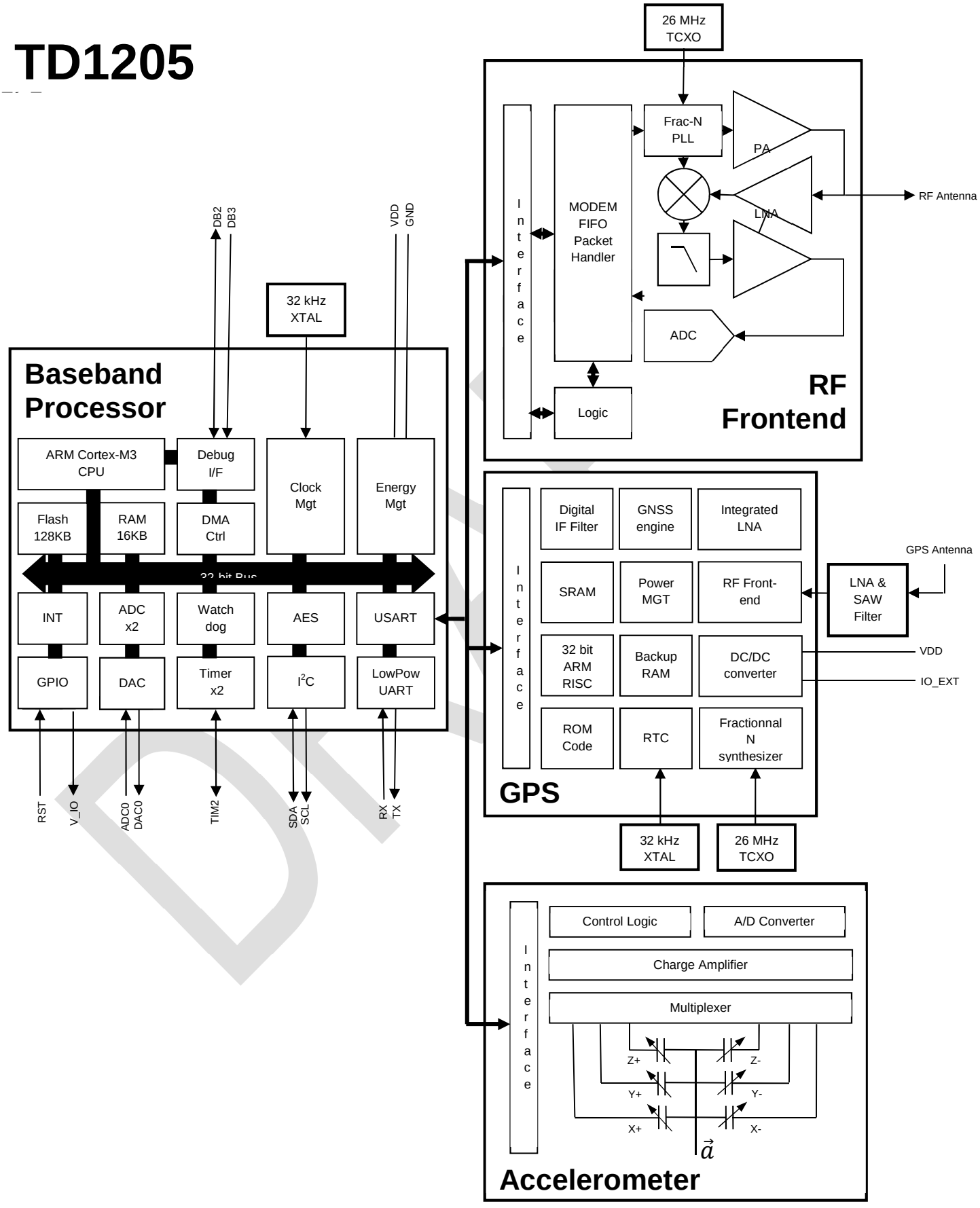
Applications

- SIGFOX™ transceiver (fully certified)
- Geolocation and Tracking
- Universal Timing and Synchronization
- People and pets geolocation
- Sensor network

Description

Telecom Design's TD1205 devices are high performance, low current SIGFOX™ gateways, RF transceiver and GPS receiver with integrated antennas. The combination of a powerful radio transceiver, a state-of-the-art ARM Cortex M3 baseband processor and a high-efficiency GPS receiver achieves extremely high performance while maintaining ultra-low active and standby current consumption. The TD1205 device offers an outstanding RF sensitivity of –126 dBm while providing an exceptional power radiated from integrated antenna of up to +14 dBm. The TD1205 device versatility provides the gateway function from a local Narrow Band ISM network to the long-distance Ultra Narrow Band SIGFOX™ network at no additional cost. Moreover the fully integrated on-board GPS receiver combines outstanding sensitivity with ultra low power which allows you to achieve excellent accuracy and Time-To-First-Fix performance. Combining the SIGFOX™ network possibilities with accurate geolocation will give you access to a brand new world of embedded applications. The TD1205 also embeds an ultra-low power 3D accelerometer with motion and free fall detection to further extend application range. Featuring an AES encryption engine and a DMA controller, the powerful 32-bit ARM Cortex-M3 baseband processor can implement highly complex and secure protocols in an efficient environmental and very low consumption way. Eventually the integrated antennas for both SIGFOX™ and GPS make the TD1205 a turnkey solution which does not require any additional design.

Functional Block Diagram



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1 Electrical Specifications

Table 1. Absolute Maximum Ratings

Parameter	Value	Units
V_{DD} to GND	0 to +3.6	V
V_{Bat+} to V_{Bat-}	0 to +3.6	V
Voltage on Digital Inputs	0 to V_{DD}	V
Voltage on Analog Inputs	0 to V_{DD}	V
RX Input Power	+10	dBm
GPS Input Power	+15	dBm
Operating Ambient Temperature Range T_A	-30 to +75	°C
Storage Temperature Range T_{STG}	–40 to +125	°C
Maximum soldering Temperature	260	°C
Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Caution: ESD sensitive device.		

Table 2. DC Power Supply Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Range[2]	V_{DD}		2.3	3.3	3.6	V
Power Saving Mode[2]	I_{Sleep}	Sleep current using the 32 kHz crystal @ 25°C	1.5	1.8	3.5	µA
Active CPU Mode	I_{Active}	CPU performing active loop @ 14 MHz	2.55	3.0	3.45	mA
Active CPU Mode + RX Mode Current[2]	I_{RX}		—	13	16	mA
Active CPU Mode + TX Mode Current[2]	I_{TX_+14}	+14 dBm, 868 MHz, 3.3 V	—	95	—	mA
GPS Acquisition	I_{ACQ}			29		mA
GPS Tracking	I_{TRA}		—	23	—	mA
GPS Backup	I_{BCKP}		—	12	—	µA
Green Led	I_{green}		—	320	—	µA
Red Led	I_{red}		—	700	—	µA

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section in “1.1. Definition of Test Conditions” on page 5.
2. Guaranteed by qualification. Qualification test conditions are listed in the “Qualification Test Conditions” section in “1.1. Definition of Test Conditions” on page 14.

Table 3. Transmitter RF Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TX Frequency Range[2]	F_{TX}		868.0	—	869.7	MHz
Modulation Deviation Range[3]	Δf	868.0-869.7 MHz	—	1.5	—	MHz
Modulation Deviation Resolution[3]	F_{RES}	868.0-869.7 MHz	—	28.6	—	Hz
Frequency Error[2]	F_{ERR_25}	868.0-869.7 MHz, 25°C, 3.3 V	—	±2	—	kHz
	F_{ERR_M20}	868.0-869.7 MHz, -20°C, 3.3 V	—	±3	—	kHz
	F_{ERR_55}	868.0-869.7 MHz, 55°C, 3.3 V	—	±3	—	kHz
Average Radiated Power	P_{AVCDP1}	-20°C to 55°C, 868.0 MHz to 868.6 MHz, 3.3 V	—	—	14	dBm
	P_{AVCDP2}	-20°C to 55°C, 868.6 MHz to 868.7 MHz, 3.3 V	—	—	10	dBm
	P_{AVCDP3}	-20°C to 55°C, 868.7 MHz to 869.2 MHz, 3.3 V	—	—	14	dBm
	P_{AVCDP4}	-20°C to 55°C, 869.2 MHz to 869.25 MHz, 3.3 V	—	—	10	dBm
	P_{AVCDP5}	-20°C to 55°C, 869.25 MHz to 869.3 MHz, 3.3 V	—	—	10	dBm
	P_{AVCDP6}	-20°C to 55°C, 869.3 MHz to 869.4 MHz, 3.3 V	—	—	10	dBm
	P_{AVCDP7}	-20°C to 55°C, 869.65 MHz to 869.7 MHz, 3.3 V	—	—	14	dBm
Transient Power[2]	P_{TP}	868.0-869.7 MHz, 25°C, 3.3 V, 4800 bps, deviation 2500 Hz	—	—	3	dB
Adjacent Channel Power[2]	P_{ACP_25}	868.0-869.7 MHz, 25°C, 3.3 V, 4800 bps, deviation 2500 Hz	—	-50	—	dBm
	P_{ACP_M20}	868.0-869.7 MHz, -20°C, 3.3 V, 4800 bps, deviation 2500 Hz,	—	-51	—	dBm
	P_{ACP_55}	868.0-869.7 MHz, 55°C, 3.3 V, 4800 bps, deviation 2500 Hz	—	-50	—	dBm
Spurious Emissions[2]	P_{OB_TX1}	Frequencies < 30 MHz, 868.0-869.7 MHz, 25°C, 3.3 V, 4800 bps, deviation 2500 Hz,	—	-82	—	dBm
	P_{OB_TX2}	Frequencies < 1 GHz, 868.0-869.7 MHz, 25°C, 3.3 V, 4800 bps, deviation 2500 Hz,	—	-58	—	dBm
	P_{OB_TX3}	Frequencies > 1 GHz, 868.0-869.7 MHz, 25°C, 3.3 V, 4800 bps, deviation 2500 Hz,	—	-37	—	dBm

Notes:

3. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section of “1.1. Definition of Test Conditions” on page 5.
4. Guaranteed by qualification. Qualification test conditions are listed in the “Qualification Test Conditions” section in “1.1. Definition of Test Conditions” on page 14.
5. Guaranteed by component specification.

Table 4. Receiver RF Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RX Frequency Range[2]	F_{RX}		868.0	—	869.7	MHz
Synthesizer Frequency Resolution[3]	F_{RES}	868.0-869.7 MHz	—	28.6	—	Hz
Blocking[2,4]	$2M_{BLOCK}$	Frequency offset ± 2 MHz, 868.0-869.7 MHz, 25°C, 3.3 V	—	-38	—	dB
	$10M_{BLOCK}$	Frequency offset ± 10 MHz, 868.0-869.7 MHz, 25°C, 3.3 V	—	-62	—	dB
Spurious Emissions[2]	P_{OB_RX1}	From 9 kHz to 1 GHz, 868.0-869.7 MHz, 25°C, 3.3 V	—	-84	—	dBm
	P_{OB_RX2}	From 1 GHz to 6 GHz, 868.0-869.7 MHz, 25°C, 3.3 V	—	-70	—	dBm
RX Sensitivity[3]	$P_{RX\_0.5}$	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250 Hz)	—	-126	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)	—	-110	—	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)	—	-106	—	dBm
	P_{RX_125}	(BER < 0.1%) (125 kbps, GFSK, BT = 0.5, Δf = ±62.5 kHz)	—	-105	—	dBm
	P_{RX_500}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, Δf = ±250 kHz)	—	-97	—	dBm
	$P_{RX\_9.6}$	(BER < 0.1%) (9.6 kbps, GFSK, BT = 0.5, Δf = ±2.4 kHz)	—	-110	—	dBm
	P_{RX_1M}	(BER < 0.1%) (1 Mbps, GFSK, BT = 0.5, Δf = ±1.25 kHz)	—	-88	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)	—	-109	—	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)	—	-104	—	dB
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)	—	-99	—	dBm
RSSI Resolution[3]	RES_{RSSI}		—	±0.5	—	dB

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section of “1.1. Definition of Test Conditions” on page 5.
2. Guaranteed by qualification. Qualification test conditions are listed in the “Qualification Test Conditions” section in “1.1. Definition of Test Conditions” on page 14.
3. Guaranteed by component specification.
4. The typical blocking values were obtained while seeking for EN 300-220 Category 2 compliance only. The typical value specified in the component datasheet are -75 dB and -84 dB at 1 and 8 MHz respectively, with desired reference signal 3 dB above sensitivity, BER = 0.1%, interferer is CW, and desired is modulated with 2.4 kbps, ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz. The RF component manufacturer provides a reference design featuring a SAW filter which is EN 300-220 Category 1 compliant. Please contact Telecom Design for more information on EN 300-220 Category 1 compliance.

Table 5. All Digital I/O DC & AC Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Low Voltage[2]	V_{IOIL}		—	—	$0.3V_{DD}$	V
Input High Voltage[2]	V_{IOIH}		$0.7V_{DD}$	—	—	V
Output High Voltage[2]	V_{IOOH}	Sourcing 6 mA, VDD = 3.0V, Standard Drive Strength	$0.95V_{DD}$	—	—	V
		Sourcing 20 mA, VDD = 3.0V, High Drive Strength	$0.9V_{DD}$	—	—	V
Output Low Voltage[2]	V_{IOOL}	Sinking 6 mA, VDD=3.0V, Standard Drive Strength	—	—	$0.05V_{DD}$	V
		Sinking 20 mA, VDD=3.0V, High Drive Strength	—	—	$0.1V_{DD}$	V
Input Leakage Current[2]	I_{IOLEAK}	High Impedance I/O connected to GND or V_{DD}	—	—	±25	nA
I/O Pin Pull-Up Resistor[2]	R_{PU}		—	40	—	kΩ
I/O Pin Pull-Down Resistor[2]	R_{PD}		—	40	—	kΩ
Internal ESD Series Resistor[2]	R_{IOESD}		—	200	—	Ω
Pulse Width of Pulses to be Removed by the Glitch Suppression Filter[2]	$t_{IOGLITCH}$		10	—	50	ns
Output Fall Time[2]	t_{IOOF}	0.5 mA Drive Strength and Load Capacitance C_L = 12.5 to 25 pF	$20+0.1C_L$	—	250	ns
		2 mA Drive Strength and Load Capacitance C_L = 350 to 600 pF	$20+0.1C_L$	—	250	ns
I/O Pin Hysteresis (V_{IOTHR+} - V_{IOTHR-})[2]	V_{IOHYST}	V_{DD} = 2.3 to 3.6 V	$0.1V_{DD}$	—	—	V

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section of “1.1. Definition of Test Conditions” on page 14.
2. Guaranteed by component specification.

Table 6. ADC DC & AC Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range[2]	V_{ADCIN}	Single Ended	0	—	V_{REF}	V
		Differential	$-V_{REF}/2$	—	$V_{REF}/2$	V
Common Mode Input Range[2]	$V_{ADCCMIN}$		0	—	V_{DD}	V
Input Current[2]	I_{ADCIN}	2 pF Sampling Capacitors	—	<100	—	nA
Analog Input Common Mode Rejection Ratio[2]	$CMRR_{ADC}$		—	65	—	dB
Average Active Current[2]	I_{ADC}	10 ksps/s 12 bit, Internal 1.25 V Reference, Warmup Mode = 0	—	67	—	µA
		10 ksps/s 12 bit, Internal 1.25 V Reference, Warmup Mode = 1	—	63	—	µA
		10 ksps/s 12 bit, Internal 1.25 V Reference, Warmup Mode = 2	—	64	—	µA
Current Consumption of Internal Voltage Reference[2]	I_{ADCREF}		—	65	—	µA
Input Capacitance[2]	C_{ADCIN}		—	2	—	pF
Input ON Resistance[2]	R_{ADCIN}		1	—	—	MΩ
Input RC Filter Resistance[2]	$R_{ADCFILT}$		—	10	—	kΩ
Input RC Filter/Decoupling Capacitance[2]	$C_{ADCFILT}$		—	250	—	fF
ADC Clock Frequency[2]	f_{ADCCLK}		—	—	13	MHz
Conversion Time[2]	$t_{ADCCONV}$	6 bit	7	—	—	ADC CLK Cycles
		10 bit	11	—	—	ADC CLK Cycles
		12 bit	13	—	—	ADC CLK Cycles
Acquisition Time[2]	t_{ADCACQ}	Programmable	1	—	256	ADC CLK Cycles
Required Acquisition Time for $V_{DD}/3$ Reference[2]	$t_{ADCACQVDD3}$		2	—	—	µs

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section of “1.1. Definition of Test Conditions” on page 14.
2. Guaranteed by component specification.

Table 7. ADC DC & AC Characteristics[1] (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Startup Time of Reference Generator and ADC Core in NORMAL Mode[2]	$t_{ADCSTART}$		—	5	—	µs
Startup Time of Reference Generator and ADC Core in KEEPADCWARM Mode[2]			—	1	—	µs
Offset Voltage[2]	$V_{ADCOFFSET}$	After calibration, single ended	—	0.3	—	mV
		After calibration, differential	—	0.3	—	mV
Thermometer Output Gradient[2]	$TGRAD_{ADCTH}$		—	-1.92	—	mV/°C
			—	-6.3	—	ADC Codes / °C
Differential Non-Linearity (DNL)[2]	DNL_{ADC}		—	±0.7	—	LSB
Integral Non-Linearity (INL), End Point Method[2]	INL_{ADC}		—	±1.2	—	LSB
No Missing Codes[2]	MC_{ADC}		11.999[3]	12	—	bits
Gain Error Drift[2]	$GAIN_{ED}$	1.25V Reference	—	0.01[4]	0.033[5]	%/°C
		2.25V Reference	—	0.01[4]	0.03[5]	%/°C
		1.25V Reference	—	0.2[4]	0.07[5]	LSB/°C
		2.25V Reference	—	0.2[4]	0.62[5]	LSB/°C

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section of “1.1. Definition of Test Conditions” on page 14.
2. Guaranteed by component specification.
3. On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbor codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.
4. Typical numbers given by abs(Mean) / (85 - 25).
5. Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

Table 8. DAC DC & AC Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage Range[2]	V_{DACOUT}	V_{DD} voltage reference, Single Ended	0	—	V_{DD}	V
Output Common Mode Voltage Range[2]	V_{DACCM}		0	—	V_{DD}	V
Active Current Including References for 2 Channels[2]	I_{DAC}	500 ksps/s 12 bit	—	400	—	µA
		500 ksps/s 12 bit	—	200	—	µA
		100 ksps/s 12 bit NORMAL	—	38	—	µA
Sample Rate[2]	SR_{DAC}		—	—	500	ksps
DAC Clock Frequency[2]	f_{DAC}	Continuous Mode	—	—	1000	kHz
		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
Clock Cycles per Conversion[2]	$CYC_{DACCONV}$		—	2	—	DAC CLK Cycles
Conversion Time[2]	$t_{DACCONV}$		2	—	—	µs
Settling Time[2]	$t_{DACSETTLE}$		—	5	—	µs
Signal to Noise Ratio (SNR)[2]	SNR_{DAC}	500 ksps, 12 bit, single ended, internal 1.25V reference	—	58	—	dB
		500 ksps, 12 bit, single ended, internal 2.5V reference	—	59	—	dB
Signal to Noise-Pulse Distortion Ratio (SNDR)[2]	$SNDR_{DAC}$	500 ksps, 12 bit, single ended, internal 1.25V reference	—	57	—	dB
		500 ksps, 12 bit, single ended, internal 2.5V reference	—	54	—	dB
Spurious-Free Dynamic Range(SFDR)[2]	$SFDR_{DAC}$	500 ksps, 12 bit, single ended, internal 1.25V reference	—	62	—	dB
		500 ksps, 12 bit, single ended, internal 2.5V reference	—	56	—	dB
Offset Voltage[2]	$V_{DACOFFSET}$	After calibration, single ended	—	2	—	mV
Differential Non-Linearity[2]	DNL_{DAC}		—	±1	—	LSB
Integral Non-Linearity[2]	INL_{DAC}		—	±5	—	LSB
No Missing Codes[2]	MC_{DAC}		—	12	—	bits

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section of “1.1. Definition of Test Conditions” on page 14.
2. Guaranteed by component specification.

Table 9. Accelerometer mechanical characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Measurement range	FS		±2	—	±16	g
Sensitivity	So		1	—	12	mg/digit
Sensitivity change vs temperature	TCSo	FS=±2g	—	0.01	—	%/°C
Typical zero-g level offset accuracy	TyOff	FS=±2g		±40		mg
Zero-g level change vs temperature	TCOff	Max delta from 25°C		±0.5		mg/°C
Acceleration noise density	An	FS=±2g		220		µg/sqrt(Hz)
Notes:						

1.1 Indicative energy requirements

The following tables show indicative energy requirements for key-point functionalities of a TD1205 module based on Telecom Design's software library. All indicated values are for V_{DD} = 3.0V.

Table 10. Indicative energy requirements for SIGFOX™ and LAN RF Application

Function	Conditions	Min	Typ	Max	Units
Idle state	Per hour	—	0.0025	—	mAh
LAN RF Reception	Windowed mode, per hour	—	0.02	—	mAh
LAN RF TX+ACK[1]		—	0.01	—	mAh
Sigfox™ Transmission	Transmission of 12 payload bytes	—	0.083	—	mAh

Notes:
1. Includes transmission of 17 payload bytes and reception of an ACK.

Table 11. Indicative energy requirements for GPS application

Function	Conditions	Min	Typ	Max	Units
3D movement detection	Accelerometer 1Hz, per hour	—	0.004	—	mAh
GPS position acquisition	Cold start fix obtained in 30 seconds	—	0.225	—	mAh
GPS position acquisition and SIGFOX™ transmission	Accelerometer 1Hz, Cold start fix obtained in 30 seconds	—	0.308	—	mAh

Notes:
1. Transmission of longitude, latitude and altitude information.

Table 12. Indicative battery life for typical user case

The following table shows indicative battery life for some typical user-cases based on the TD1205 module.

User case	Battery capacity (mAh)[1]	Lifetime
1 SIGFOX™ transmission per day[2]	100	1.8 years
	250	4.4 years
	500	8 years
1 GPS position acquisition and SIGFOX™ transmission per day[3]	100	270 days
	250	1.8 years
	500	3.4 years
Movement detection plus 1 GPS position acquisition and SIGFOX™ transmission per day[3]	100	246 days
	250	1.6 years
	500	3.1 years
GPS position acquisition every 10 minutes and position transmission when long-distance movements detected[4]	500	90 days
	1000	180 days
	2500	1.2 years

Notes:
1. Assuming a 3V battery with 0.16% discharge per month.
2. With a 12-byte payload and +14dBm power.
2. Assuming a 30 seconds cold start fix. Transmission of longitude, latitude and altitude information.
3. Assuming a 5 second hot start fix and 12 long-distance movements per day. Transmission of longitude, latitude and altitude information.

1.2 Definition of Test Conditions

1.2.1 Production Test Conditions:

- T_A = + 25°C
- V_{DD} = +3.3 VDC
- Production test schematics (unless noted otherwise)
- All RF input and output levels referred to the pins of the TD1205 module

1.2.2 Qualification Test Conditions:

- T_A = -30 to +75°C (Typical T_A = 25°C)
- V_{DD} = +2.3 to 3.6 VDC (Typical V_{DD} = 3.3 VDC)
- Using TX/RX Split Antenna reference design or production test schematic
- All RF input and output levels referred to the pins of the TD1205 module

2 Functional Description

The TD1205 devices are high-performance, low-current, wireless SIGFOX™ gateways, RF transceiver, GPS receiver and accelerometer with integrated antennas. The wide operating voltage range of 2.3–3.6 V and low current consumption make the TD1205 an ideal solution for geolocation battery-powered applications.

The TD1205 operates as a time division duplexing (TDD) transceiver where the device alternately transmits and receives data packets. The device uses a single-conversion mixer to downconvert the 2-level FSK/GFSK or OOK/ASK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance ΔΣ ADC allowing filtering, demodulation, slicing, and packet handling to be performed in the built-in DSP increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is output to the baseband CPU by reading the 64-byte RX FIFO.

A single high precision local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver do not operate at the same time. The LO is generated by an integrated VCO and ΔΣ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates from 0.123 kbps to 1 Mbps. The TD1205 operates in the frequency bands of 868.0–869.7 MHz with a maximum frequency accuracy step size of 28.6 Hz. The transmit FSK data is modulated directly into the ΔΣ data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. A highly configurable packet handler allows for autonomous encoding/decoding of nearly any packet structure.

As both the local Narrow Band ISM network and the long-distance Ultra Narrow Band SIGFOX™ network can be addressed seamlessly, the TD1205 device provides a natural gateway function at no additional cost. Thus, the same TD1205 module can be used both for local RF communication with peer modules, and also connect to the wide-area SIGFOX™ RF network.

Featuring an AES encryption engine and a DMA controller, the powerful 32-bit ARM Cortex-M3 baseband processor can implement highly complex and secure protocols in an efficient environmental and very low consumption way. This unique combination of a powerful 32-bit ARM Cortex-M3 CPU including innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of intelligent peripherals allows any application to connect to the SIGFOX™ network.

The application shown in Figure 1 shows the minimum interconnection required to operate the TD1205 module. Basically only a battery supply has to be connected between pin 1 and pin 2. Pins 3 to 9 can be used to flash new software into the TD1205 module and pins 6 to 9 give access to several peripherals such as UART, ADC, Low-Energy Timer or GPIO.

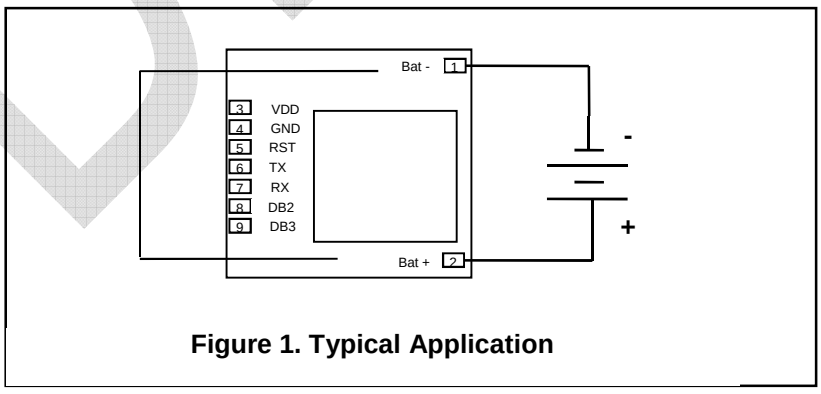


Figure 1. Typical Application

3 Module Interface

3.1 Low-Power UART (Universal Asynchronous Receiver/Transmitter)

The TD1205 communicates with the host MCU over a standard asynchronous serial interface consisting of only 2 pins: TX and RX. The TX pin is used to send data from the TD1205 module to the host MCU, and the RX pin is used to receive data into the TD1205 module coming from the host MCU.

This interface allows two-way UART communication to be performed in low energy modes, using only a few µA during active communication and only 150 nA when waiting for incoming data.

This serial interface is designed to operate using the following serial protocol parameters:

- LVTTL electrical level
- 9600 bps
- 8 data bits
- 1 stop bit
- No parity
- No hardware/software flow control

This interface operates using LVTTL signal levels to satisfy the common interface to a low power host MCU. If an EIA RS232-compliant interface voltage level is required, an RS232 level translator circuit must be used. It is also possible to use a common USB/UART interface chip to connect to an USB bus.

Over this serial interface, the TD1205 device provides a standard Hayes “AT” command set used to control the module using ASCII readable commands and get answers, as well as to send or receive data.

The list of available commands with their corresponding arguments and return values, a description of their operation and some examples are detailed into the “*TD1205 Reference Manual*”.

3.2 ADC (Analog to Digital Converter)

The TD1205 provides an interface to an integrated low-power SAR (Successive Approximation Register) ADC, capable of a resolution of up to 12 bits at up to 1 Msps or 6 bits at up to 1.86 Msps. The TX or RX pin can be used as an external interface to the ADC.

The ADC also provides an internal temperature, VDD, and GND input channel that may be used to get a digital representation of analog temperature or voltage values. It is also possible to loopback the analog output of the integrated DAC (see section **Erreur ! Source du renvoi introuvable.**, “**Erreur ! Source du renvoi introuvable.**”).

The internal ADC provides an optional input filter consisting of an internal low-pass RC filter or simple internal decoupling capacitor. The resistance and capacitance values are given in the electrical characteristics for the device, named $R_{ADCFILT}$ and $C_{ADCFILT}$ respectively.

The reference voltage used by the ADC can be selected from several sources, including a 1.25 V internal bandgap, a 2.5 V internal bandgap, V_{DD}, a 5 V internal differential bandgap or unbuffered $2V_{DD}$.

Additionally, to achieve higher accuracy, hardware oversampling can be enabled. With oversampling, each selected input is sampled a number of times, and the results are filtered by a first order accumulate and dump filter to form the end result. Using 16x oversampling minimum, it is thus possible to achieve result resolution of upt to 16 bits.

The operation of this interface is controlled by the mean of Hayes “AT” commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the “TD1205 Reference Manual”.

3.3 GPIO (General Purpose Input/Output)

All the TX, RX, DB2 and DB3 pins can be configured individually as tristate (default reset state), push-pull, open-drain, with/without pull-up or pull-down resistor, and with a programmable drive strength (0.5 mA/2 mA/6 mA/20 mA).

When configured as inputs, these pins feature an optional glitch suppression filter and full (rising, falling or both edges) interrupt with wake-up from low-power mode capabilities. Of course, the pin configuration is retained even when using these low-power modes.

The operation of the GPIOs is controlled by the mean of Hayes “AT” commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the “TD1205 Reference Manual”.

3.4 RST (Reset)

The TD1205 module features an active-low RST pin. This pin is held high by an internal pull-up resistor, so when not used, this pin can be left floating.

3.5 Debug

The TD1205 module devices include hardware debug support through a 2-pin serial-wire debug interface. The 2 pins DB2 and DB3 are used for this purpose. The DB2 pin is the ARM Cortex-M3’s SWDIO Serial Wire data Input/Output. This pin is enabled after a reset and has a built in pull-up. The DB3 pin is the ARM Cortex-M3’s SWCLK Serial Wire Clock input. This pin is enabled after reset and has a built-in pull down. When not used for debug operation, these 2 pins can be configured to perform other functions using “AT” configuration commands, please refer to the “TD1205 Reference Manual” for details.

Although the ARM Cortex-M3 supports advanced debugging features, the TD1205 devices only use two port pins for debugging or programming. The systems internal and external state can be examined with debug extensions supporting instruction or data access break- and watch points.

For more information on how to enable the debug pin outputs/inputs the reader is referred to Section 28.3.4.1 (p. 457), the ARM Cortex-M3 Technical Reference Manual and the ARM CoreSight™ Technical Reference Manual.

3.6 VDD & GND

The TD1205 provides a VDD and GND pin in addition to battery supply. These pins are only provided for programming convenience and can be left open when a battery supply is provided.

3.7 LEDs

A green and a red led are available on the TD1205.

3.8 Battery Supply

As a stand-alone solution, the TD1205 only required a 2.3V to 3.6V battery supply to work.

3.9 Integrated antennas and packaging

The TD1205 includes integrated antennas for both RF transmission and GPS reception. These antennas are both already matched to obtain best possible performance. Therefore care must be taken when adding a package around the module for the antennas could become improperly matched. Please make sure the distance between packaging and both RF and GPS antenna is greater than 1cm to obtain best possible performance.

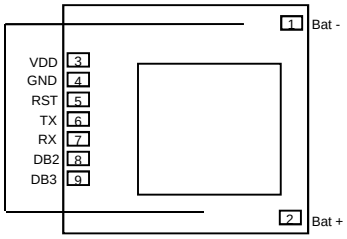
4 Bootloader

The TD1205 module contains an integrated bootloader which allows reflashing the module firmware either over the RX/TX UART connection, or over the air using the built-in RF transceiver.

The bootloader is automatically activated upon module reset. Once activated, the bootloader will monitor the UART/RF activity for a 200 ms period, and detect an incoming update condition.

If the update condition is met, the TD1205 will automatically proceed to flash the new firmware with safe retry mechanisms, or falls back to normal operation.

5 Pin Descriptions



Pin	Pin Name	I/O	Description
1	BAT -	GND	**Battery (+2.3V to 3.6V) Negative Input**
2	BAT +	VDD	**Battery (+2.3V to 3.6V) Positive Input**
3	VDD	VDD	**+2.3V to +3.6 V Supply Voltage Input** Not required if a battery is used.
4	GND	GND	**Connect to PCB Ground** Not required if a battery is used.
5	RST	I	**Active Low RESET input signal** This signal resets the TD1205 module to its initial state. If not used, this signal can be left floating, as it is internally pulled up by an integrated resistor.
6	TX	O	**Low-Power UART Data Transmit Signal** This signal provides the UART data going from the TD1205 module out to the host application processor. This signal is internally pulled up by an integrated resistor. This pin may be configured as an ADC input or as a GPIO.
7	RX	I	**Low-Power UART Data Receive Signal** This signal provides the UART data coming from the host application processor going to the TD1205 module. This signal is internally pulled up by an integrated resistor. This pin may be configured as an ADC input or as a GPIO.
8	DB2	I/O	**SWDIO (SWD Data I/O) Signal** This signal provides the SWD programming/debugging signal interface to the integrated TD1205 ARM® CPU. This pin may be configured as a Low-Energy Timer or as a GPIO.
9	DB3	I	**SWDCLK (SWD Clock) Signal** This signal provides the SWD clock signal to the integrated TD1205 ARM® CPU. This pin may be configured as a Low-Energy Timer or as a GPIO.

6 Package Outline

Figure 2 illustrates the package details for the TD1205.

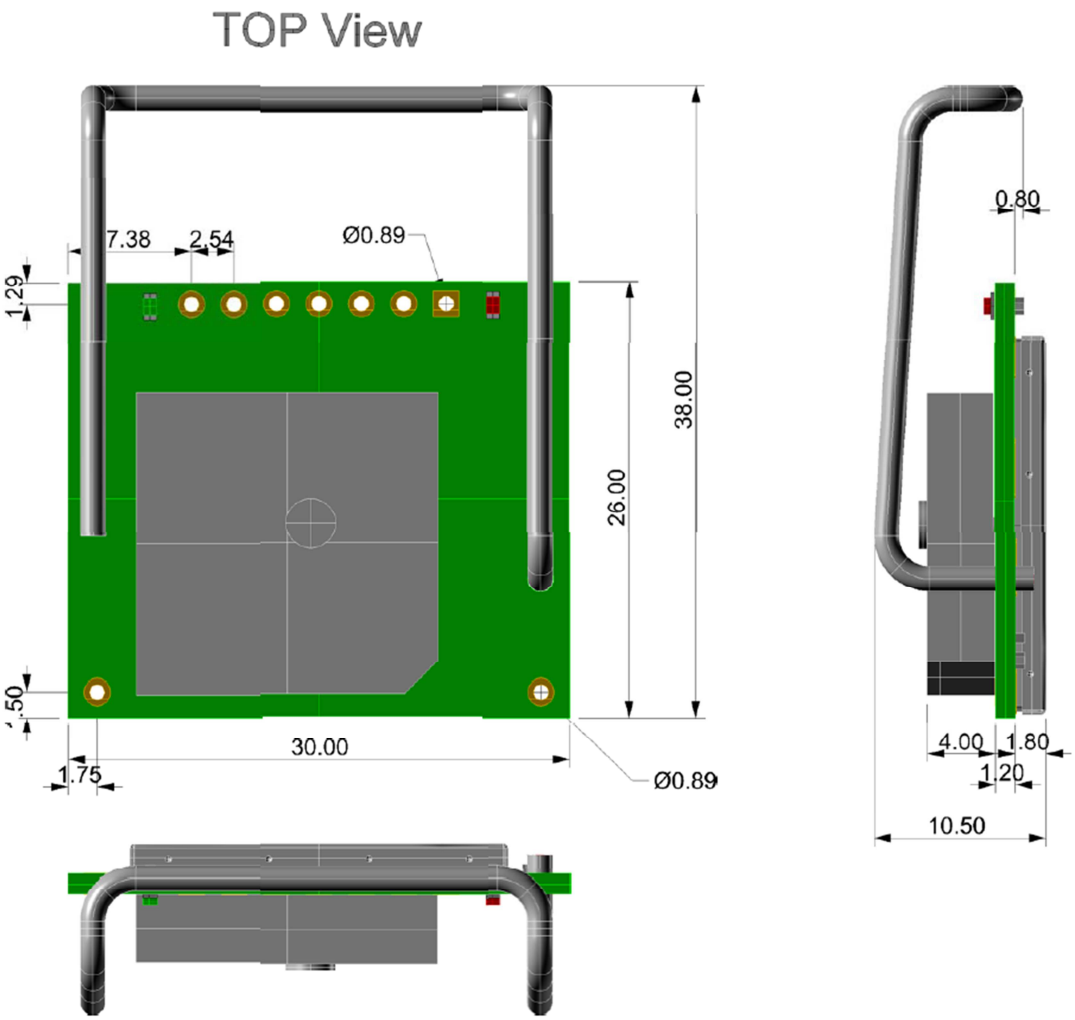


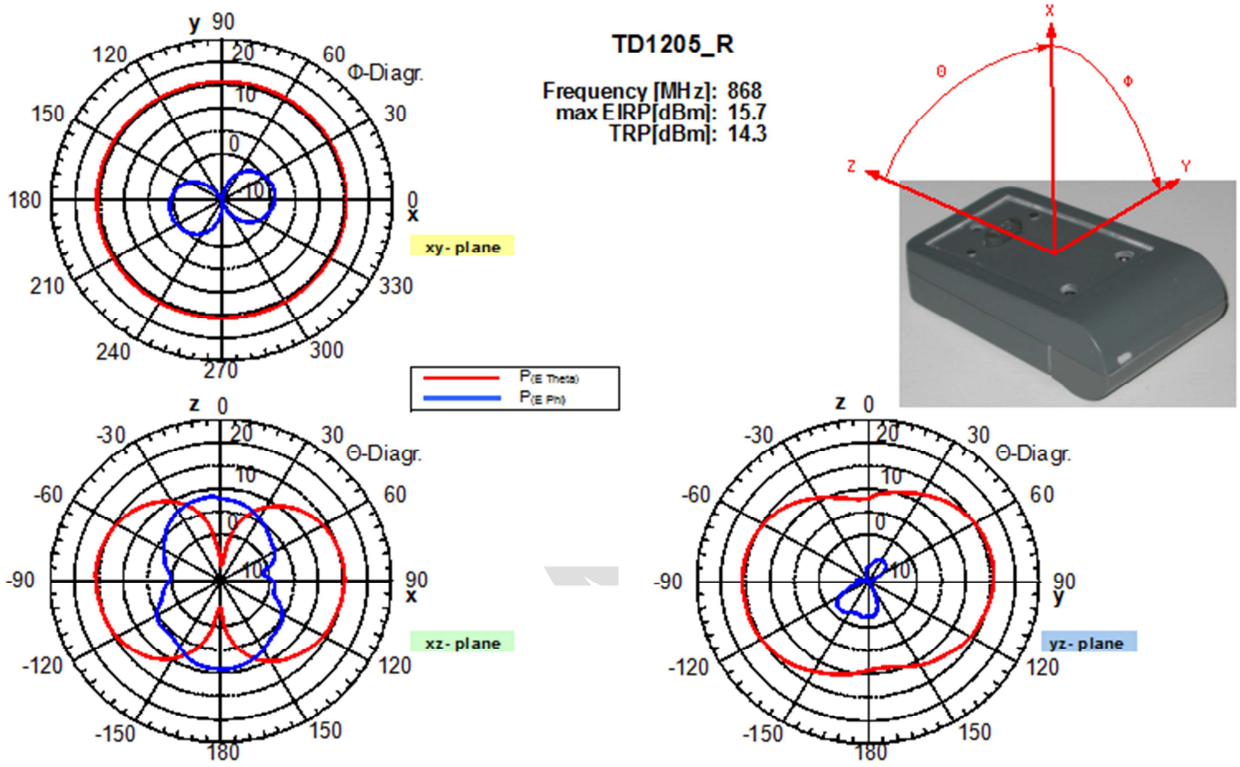
Figure 2. TD1205 Package

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.

7 Radiation pattern

PA set to maximum power



DOCUMENT CHANGE LIST

Revision 0.1

- Draft

Revision 0.2

- Changed contact information

Revision 0.3

- Added Radiation Pattern

Revision 0.4

- Fixed TX current value

NOTES:

NOTES:

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