

RISC-V ISA

Additional information

RISC-V ISA is divided into extensions

I	Integer instructions (frozen)
E	Reduced number of registers
M	Multiplication and Division (frozen)
A	Atomic instructions (frozen)
F	Single-Precision Floating-Point (frozen)
D	Double-Precision Floating-Point (frozen)
C	Compressed Instructions (frozen)
X	Non Standard Extensions

15TRV2:
A 16 BIT



- Kept very simple and extendable
 - Wide range of applications from IoT to HPC
- RV + word-width + extensions
 - RV32IMC: 32bit, integer, multiplication, compressed
- User specification:
 - Separated into extensions, only I is mandatory
- Privileged Specification (WIP):
 - Governs OS functionality: Exceptions, Interrupts
 - Virtual Addressing
 - Privilege Levels

Work continues on new RISC-V extensions

- Foundation members work in **task-groups**
- Dedicated task-groups
 - Formal specification
 - Memory Model
 - Marketing
 - External Debug Specification

Q Quad-precision Floating-Point

L Decimal Floating Point

B Bit Manipulation

T Transactional Memory

P Packed SIMD

J Dynamically Translated Languages

V Vector Operations

N User-Level Interrupts

Reduced Instruction Set: all in one page

Free & Open RISC-V Reference Card

Base Integer Instructions (RV32I, RV64I, and RV128I)					RV Privileged Instructions				
Category	Name	Fmt	RV32I Base	+RV(64,128)	Category	Name	RV mnemonic		
Loads	Load Byte	I	LB rd,rs1,imm		CSR Access	Atomic R/W	CSRRW rd,csr,rs1		
	Load Halfword	I	LH rd,rs1,imm			Atomic Read & Set Bit	CSRRS rd,csr,rs1		
	Load Word	I	LD rd,rs1,imm			Atomic Read & Clear Bit	CSRRC rd,csr,rs1		
	Load Byte Unsigned	I	LBU rd,rs1,imm			Atomic R/W Imm	CSRRI rd,csr,imm		
	Load Half Unsigned	I	LHU rd,rs1,imm			Atomic Read & Clear Imm	CSRRI rd,csr,imm		
Stores	Store Byte	S	SB rs1,rs2,imm		Change Level	Env. Call	ECALL		
	Store Halfword	S	SH rs1,rs2,imm			Environment Base	EBREAK		
	Store Word	S	SW rs1,rs2,imm			Environment	ENVRET		
Shifts	Shift Left	R	SLL rd,rs1,rs2	SLL(W/D) rd,rs1,rs2	Trap Redirect to Supervisor	MRTS			
	Shift Left Immediate	I	SLLI rd,rs1,shamt	SLLI(W/D) rd,rs1,shamt		Redirect Trap to Hypervisor	MRTM		
	Shift Right	R	SRL rd,rs1,rs2	SRL(W/D) rd,rs1,rs2		Hypervisor Trap to Supervisor	MRTS		
	Shift Right Immediate	I	SRLI rd,rs1,shamt	SRLI(W/D) rd,rs1,shamt	Interrupt	Wait for Interrupt	RFI		
	Shift Right Arithmetic	R	SRA rd,rs1,rs2	SRA(W/D) rd,rs1,rs2		Supervisor Fence	RFENCE.VM rs1		
Arithmetic	Shift Right Arith Imm	I	SRAI rd,rs1,shamt	SRAI(W/D) rd,rs1,shamt					
	ADD	I	ADD rd,rs1,rs2	ADD(W/D) rd,rs1,rs2					
	ADD Immediate	I	ADDI rd,rs1,imm	ADDI(W/D) rd,rs1,imm					
	SUBtract	I	SUB rd,rs1,rs2						
	Load Upper Imm	I	LUI rd,imm						
Logical	ADD Upper Imm to PC	I	AUIPC pc,imm						
	XOR	I	XOR rd,rs1,rs2						
	XOR Immediate	I	XORI rd,rs1,imm						
	OR	I	OR rd,rs1,rs2						
	OR Immediate	I	ORI rd,rs1,imm						
Compare	AND	I	AND rd,rs1,rs2						
	AND Immediate	I	ANDI rd,rs1,imm						
	Set <	I	SLT rd,rs1,rs2						
	Set < Immediate	I	SLTI rd,rs1,imm						
	Set < Unsigned	R	SLTU rd,rs1,rs2						
Branches	Set < Imm Unsigned	R	SLTIU rd,rs1,imm						
	Branch =	I	BEQ rs1,rs2,imm						
	Branch ≠	I	BNE rs1,rs2,imm						
	Branch >	I	BGT rs1,rs2,imm						
	Branch ≥	I	BGE rs1,rs2,imm						
Jump & Link	Branch < Unsigned	I	BLTU rs1,rs2,imm						
	Branch < Imm Unsigned	I	BLTIU rs1,rs2,imm						
	Jump & Link Register	I	JAL rd,rs1,imm						
	Synch thread	I	FENCE						
	Synch Instr & Data	I	FENCE.I						
System	System CALL	I	SCALL						
	System BREAK	I	SBREAK						
	Counters READ CYCLE	I	RDYCYCLE rd						
	Read Cycle upper Half	I	RDYCYCLEH rd						
	Read TIME	I	RDTIME rd						
Jump & Link	Read TIME upper Half	I	RDTIMEH rd						
	Read INSTR RETired	I	RDINSTRET rd						
	Read INSTR upper Half	I	RDINSTRETH rd						

Encoding of the instructions, main groups

- **Reserved** opcodes for standard extensions
- Rest of opcodes free for **custom** implementations
- Standard extensions will be frozen/not change in the future

inst[4:2]	000	001	010	011	100	101	110	111
inst[6:5]								(> 32b)
00	LOAD	LOAD-FP	<i>custom-0</i>	MISC-MEM	OP-IMM	AUIPC	OP-IMM-32	48b
01	STORE	STORE-FP	<i>custom-1</i>	AMO	OP	LUI	OP-32	64b
10	MADD	MSUB	NMSUB	NMADD	OP-FP	<i>reserved</i>	<i>custom-2/rv128</i>	48b
11	BRANCH	JALR	<i>reserved</i>	JAL	SYSTEM	<i>reserved</i>	<i>custom-3/rv128</i>	≥ 80b