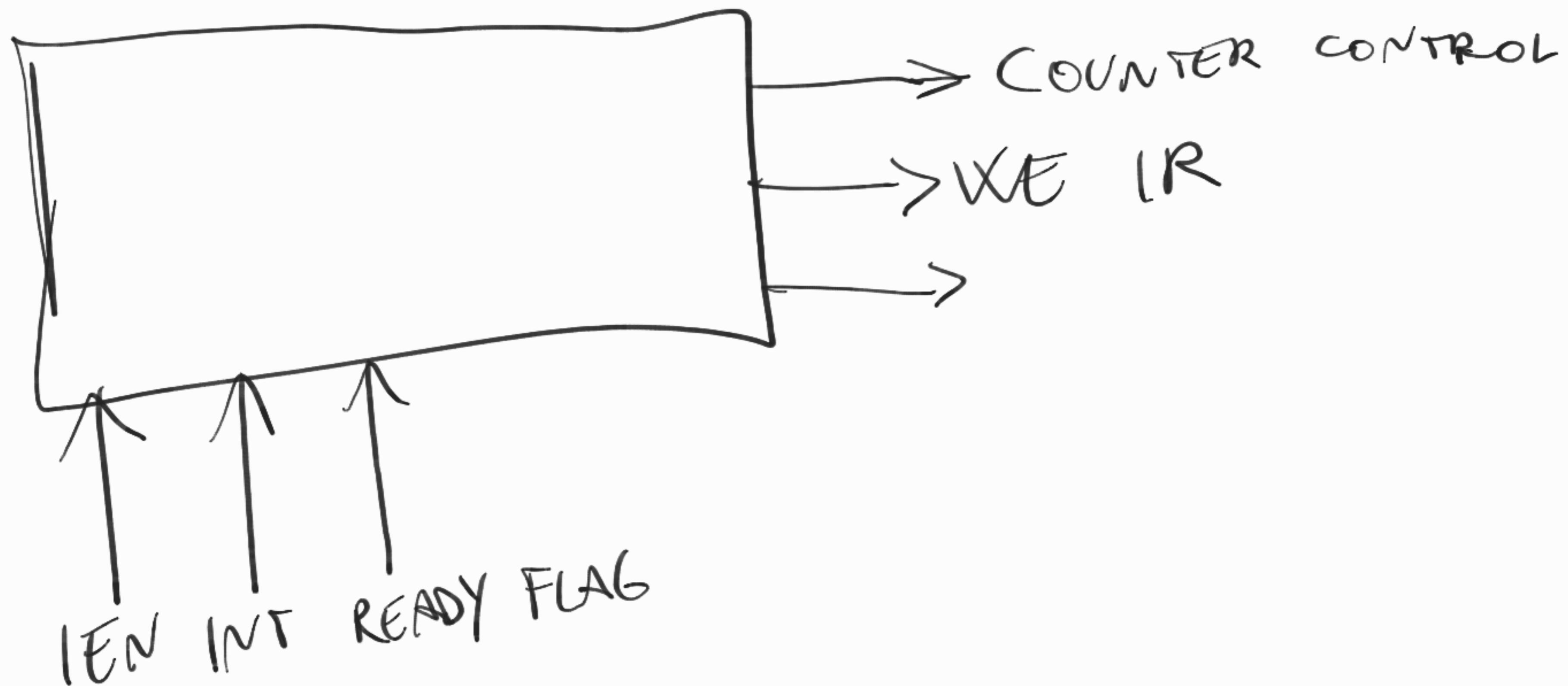
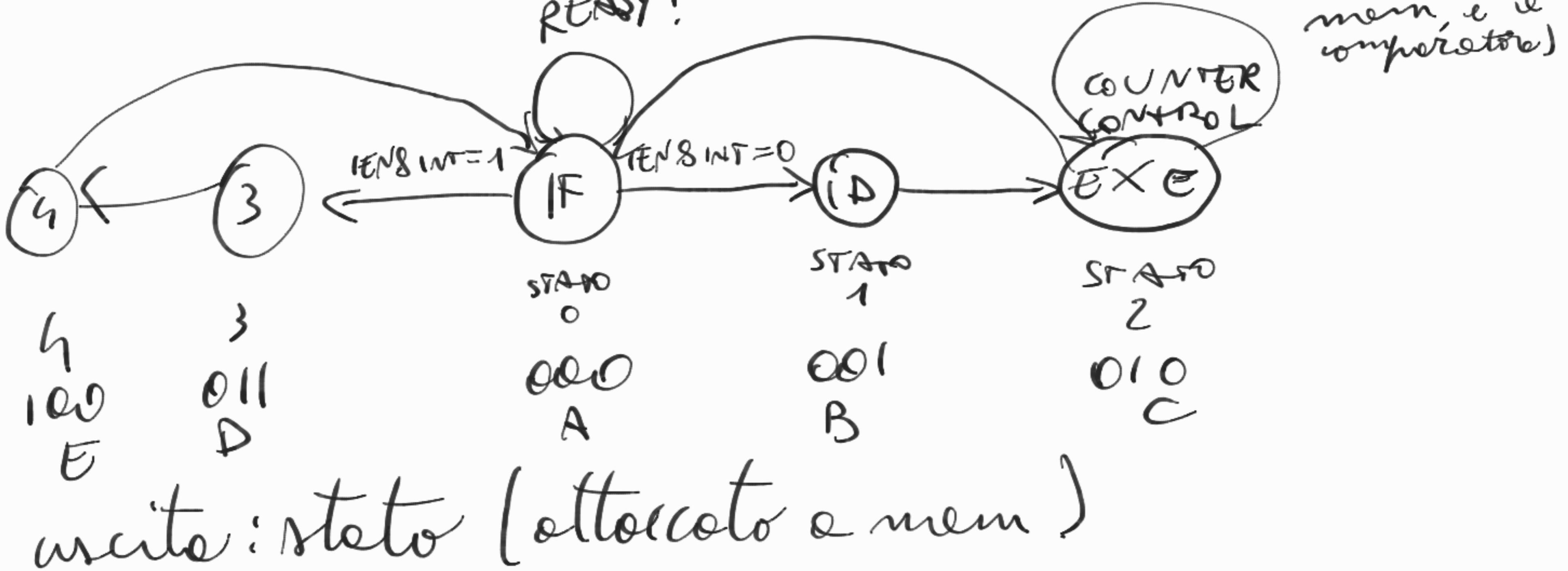


SEGNALE



env. 1 = n
0 = no

READY? (non viene
bloccato dalle



$READY = I_0$

$TENS\ INT = I_1$

I_1, T_0

SP	00	01	10	11
A	A	B	D	D
B	C	C	C	C
C	C	A	C	A
D	E	E	E	E
E	A	A	A	A

I_1, T_0

	q_2	q_1	q_0	00	01	10	11
A	0	0	0	000	001	101	111
B	0	0	1	000	010	010	010
C	0	1	0	010	000	010	000
D	0	1	1	100	100	100	100
E	1	0	0	000	000	000	000

$Q_2 \& Q_0$

Q_0

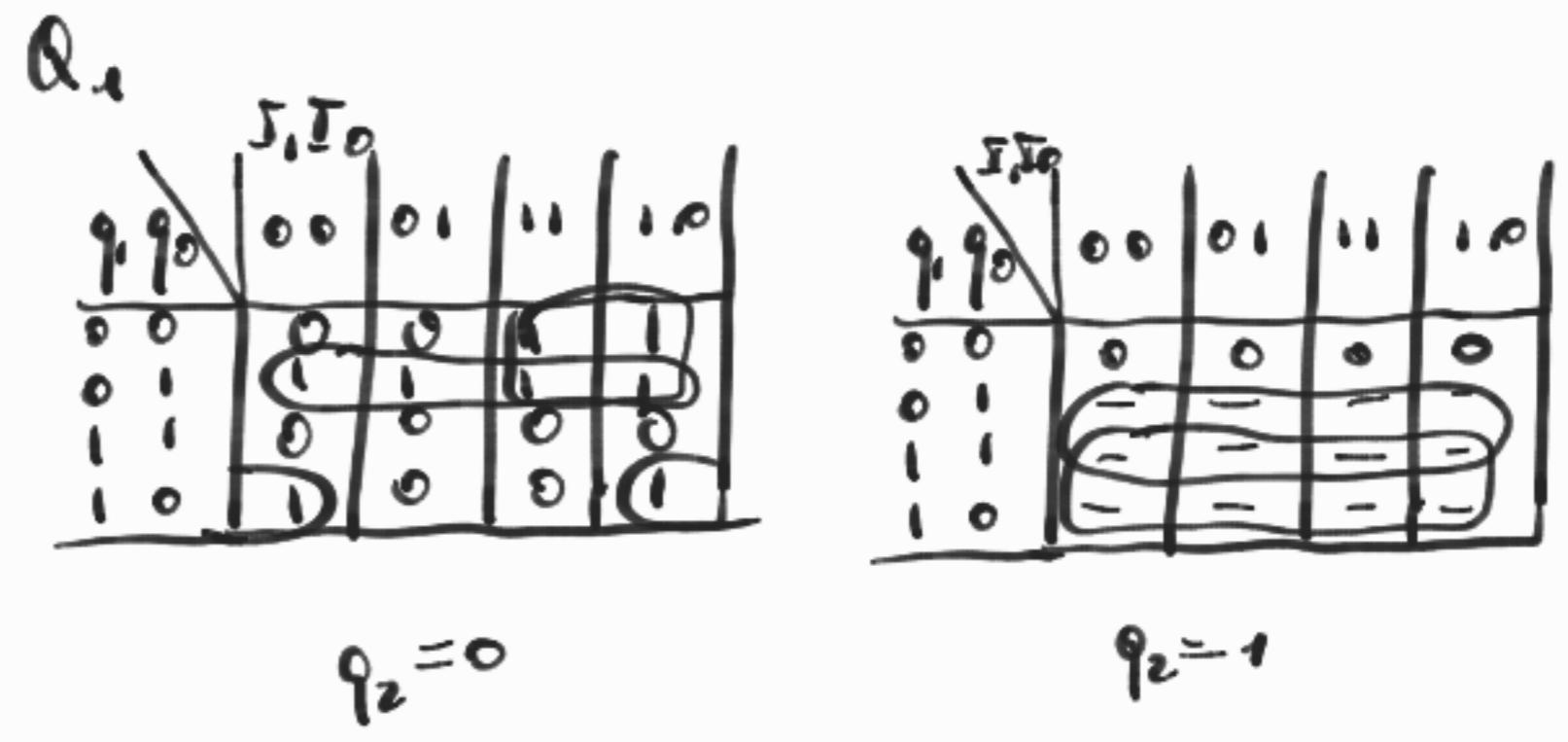
	q_2	q_1	q_0	00	01	11	10
0	0	0	0	00	01	11	10
1	0	0	1	00	01	11	10
2	0	1	0	00	01	11	10
3	0	1	1	00	01	11	10
4	1	0	0	00	01	11	10

$q_2 = 0$

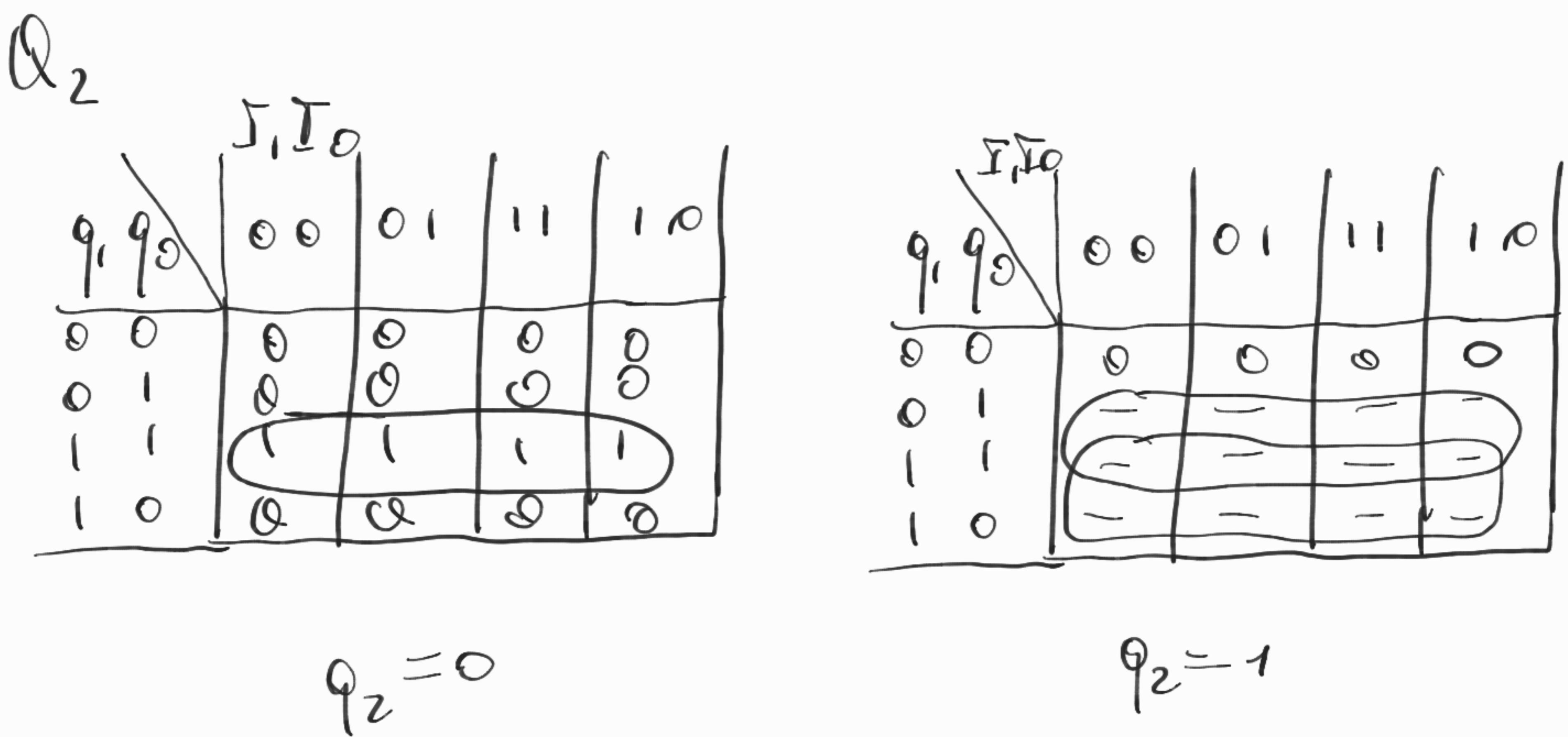
	q_2	q_1	q_0	00	01	11	10
0	0	0	0	00	01	11	10
1	0	0	1	00	01	11	10
2	0	1	0	00	01	11	10
3	0	1	1	00	01	11	10
4	1	0	0	00	01	11	10

$q_2 = 1$

$$Q_0 = (\bar{q}_2 \bar{q}_1 \bar{q}_0 T_0) + (\bar{q}_2 \bar{q}_1 q_0 T_1)$$



$$Q_1 = (\bar{q}_2 \bar{q}_1 \mathbb{I}_1) + (\bar{q}_2 \bar{q}_1 q_0 \quad) + (\bar{q}_2 q_1 \bar{q}_0 \mathbb{I}_0)$$



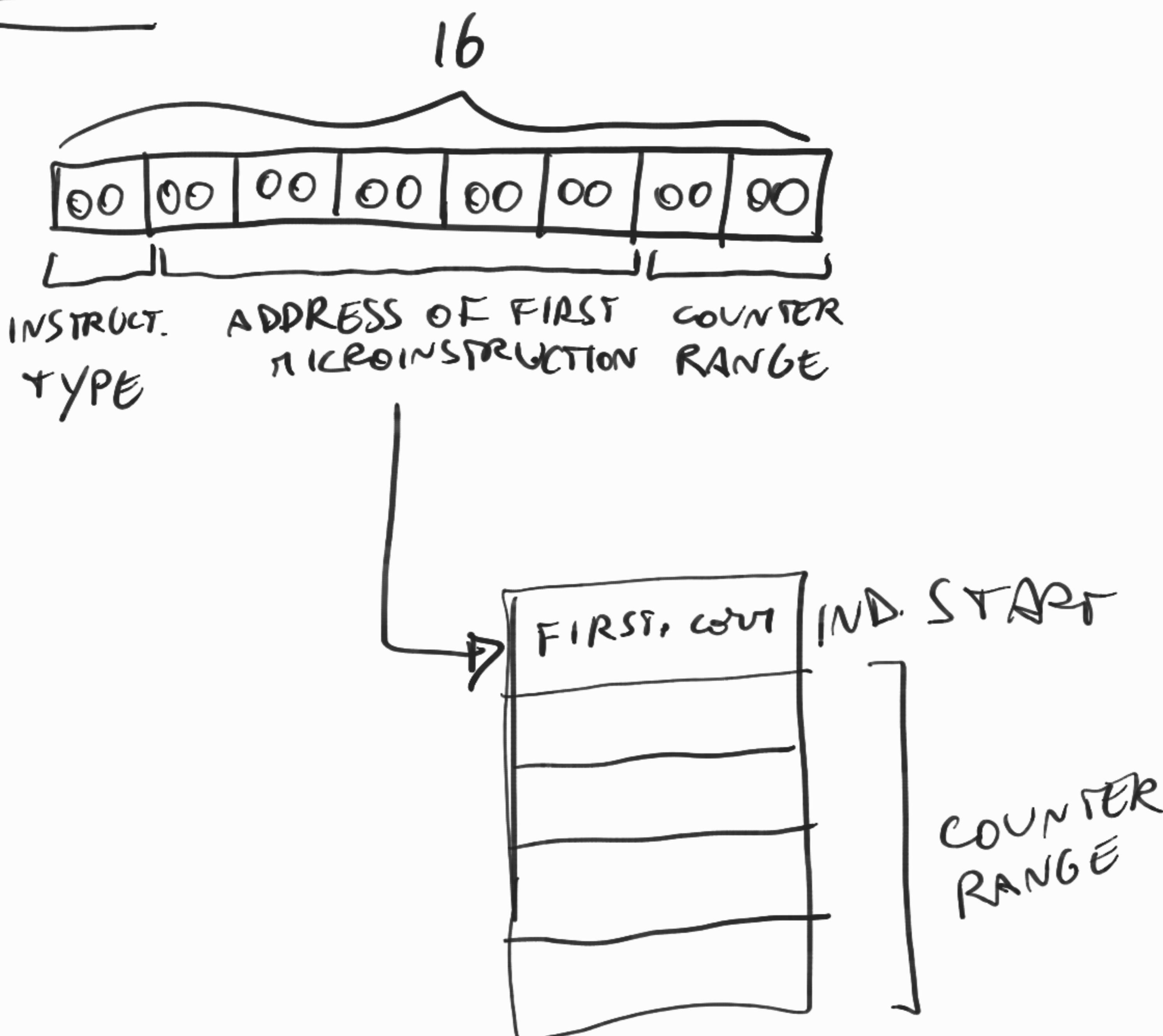
$$Q_2 = \bar{q}_2 q_1 q_0$$

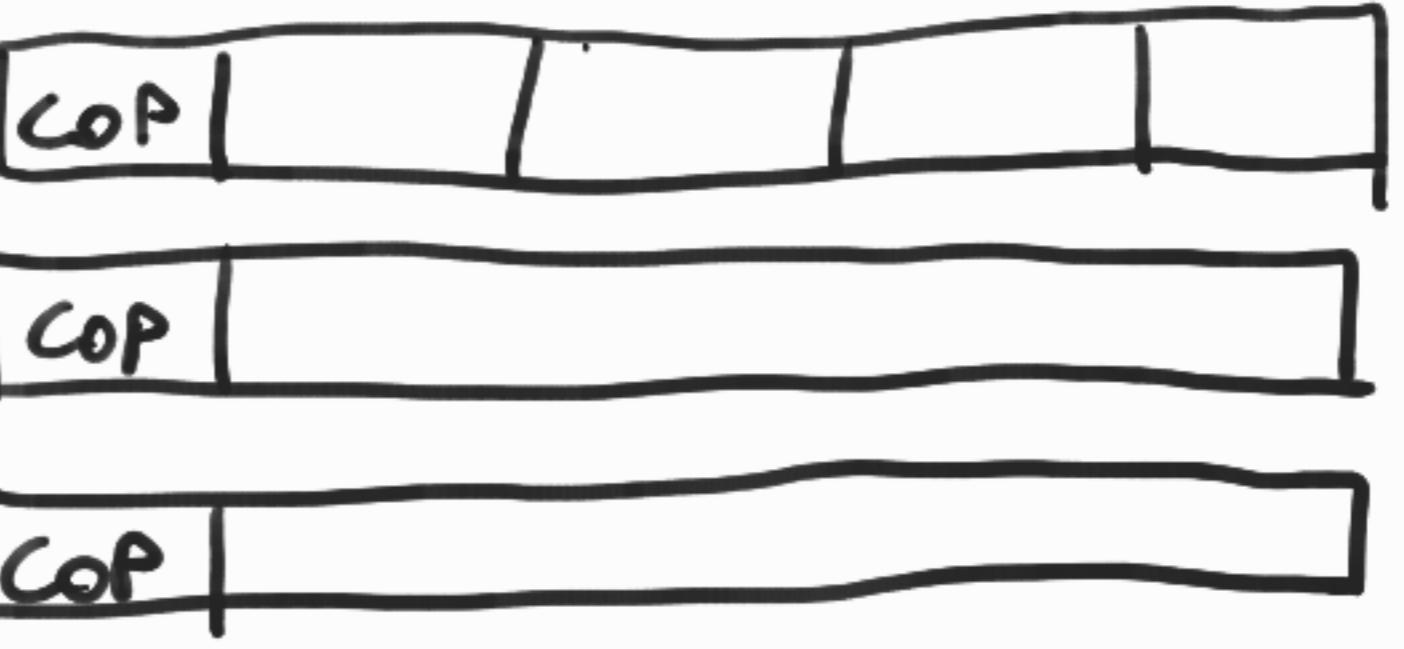
CONFIG MASTER CONTROL

S celle \rightarrow S com. in memoria

	OP	IN	OP	VER	CIN	VAL
000	0	1	0	1	0	0af
001	0	1	1	0	1	09f
010	1	1	1	0	0	1Cf
011	0	1	0	0	0	08f
100	0	1	0	0	0	08f

MEM 2 (COP MEMORY)

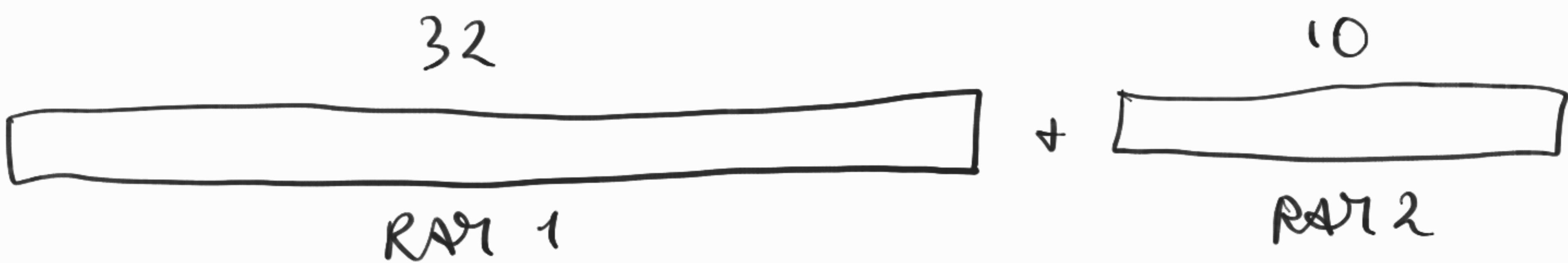
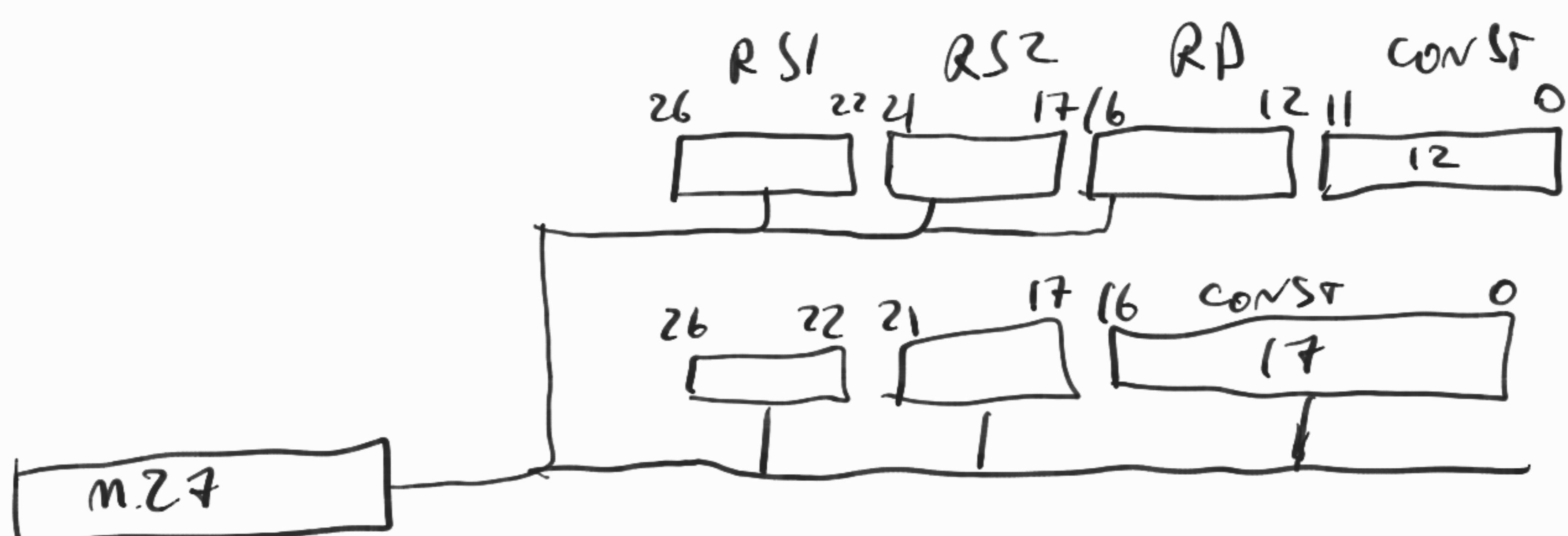


- INSTRUCT. TYPE : 00 \rightarrow R 
 - 01 \rightarrow I
 - 11 \rightarrow J

- ADDRESS - RISERVATI : 0000000000 (per FETCH)
0000000001 (per ID)

m. max address = 2^{10}

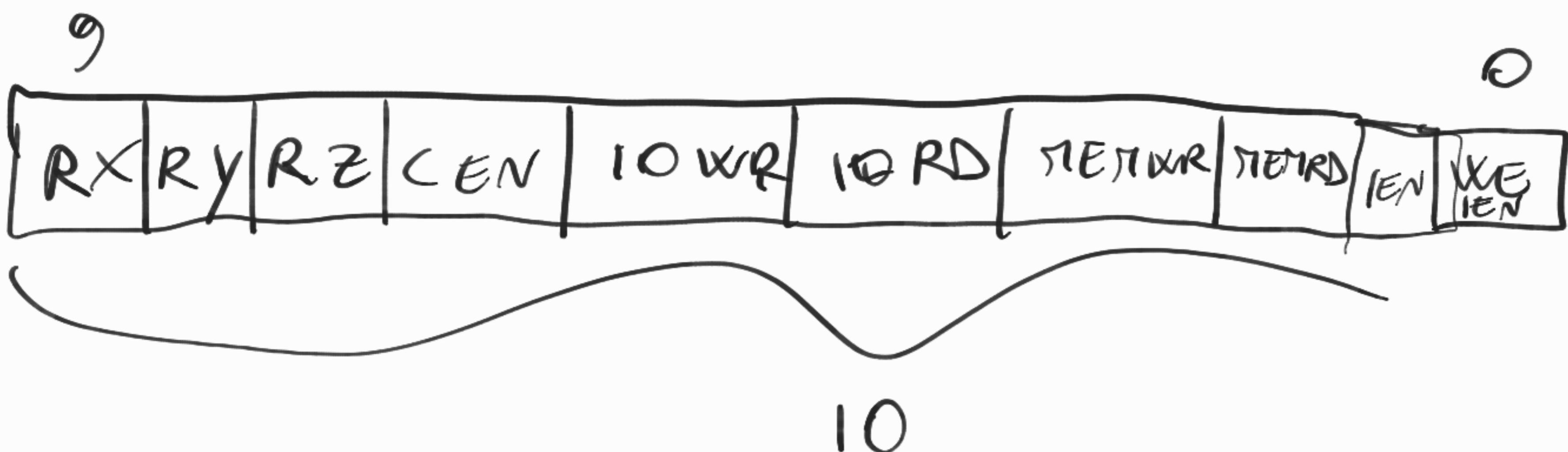
m max di indirizzi



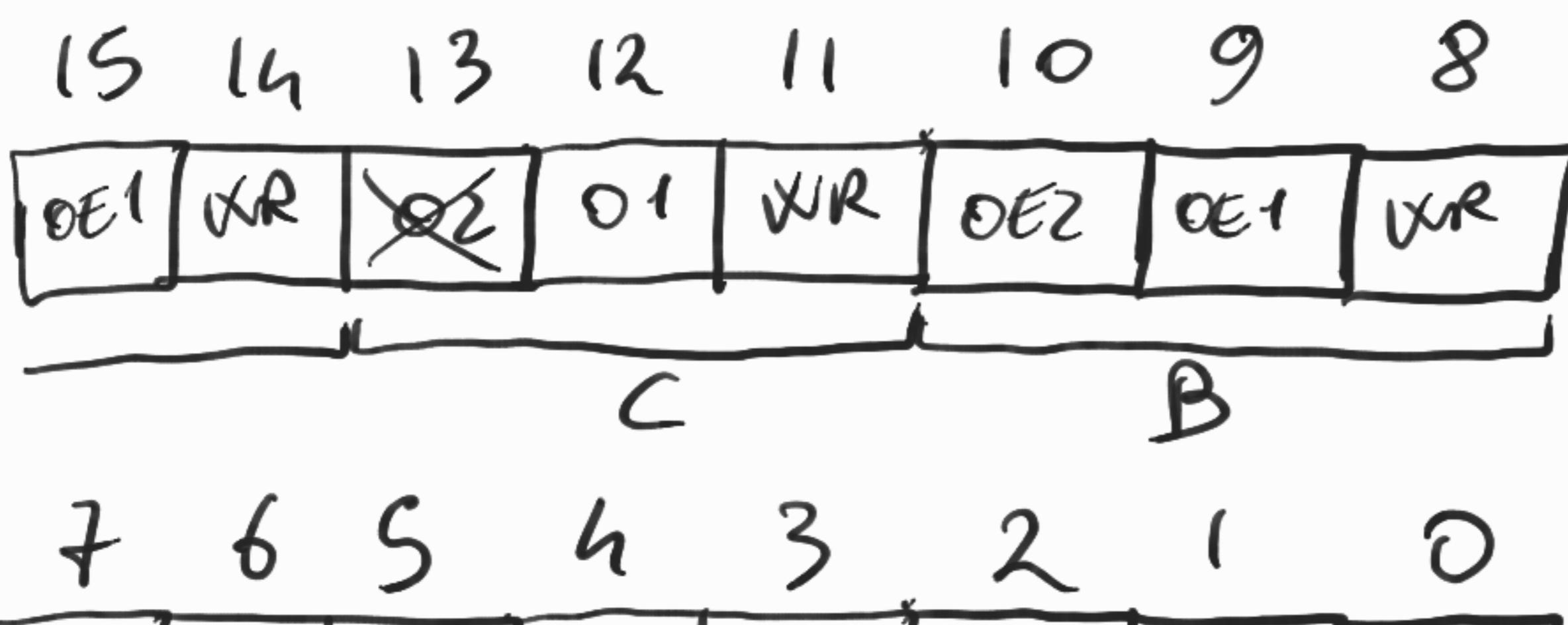
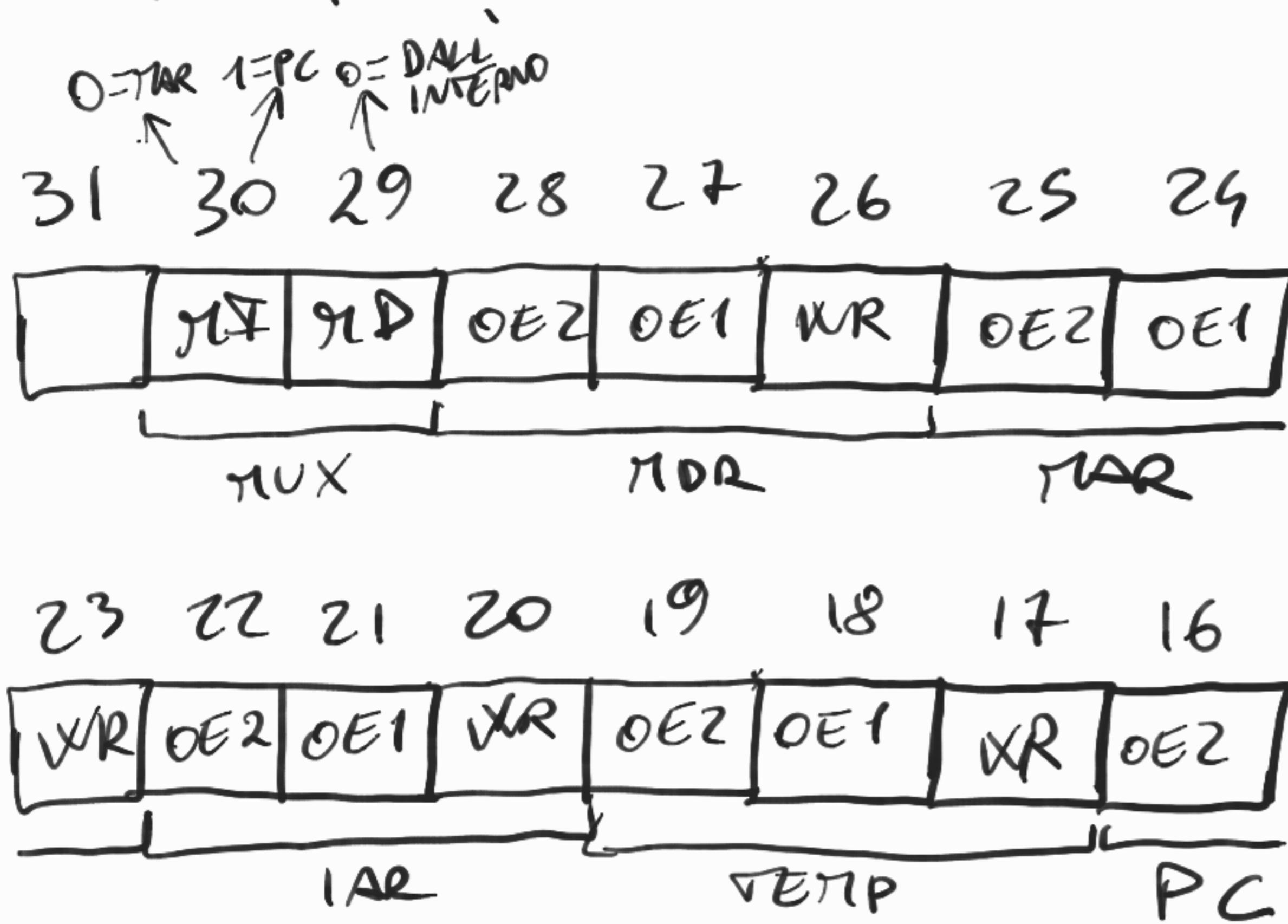
SEGNALI DI
CORIANDO

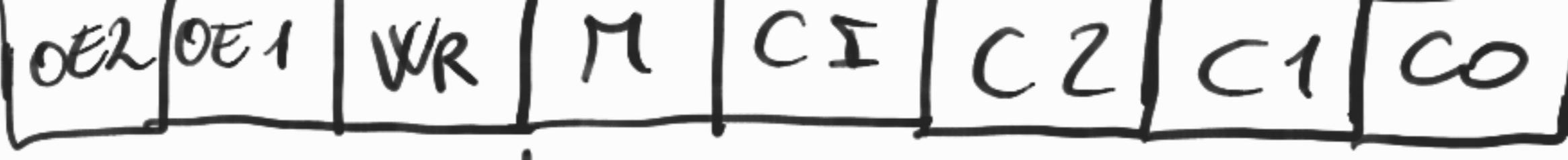
SEGNALI
DI CONTROLLO
+
ALCUNI DI
CORIANDO

• RAM2



• RAM 1



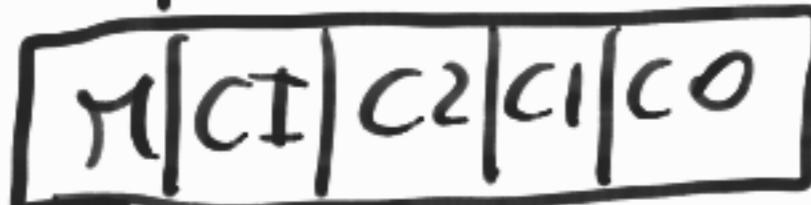


A

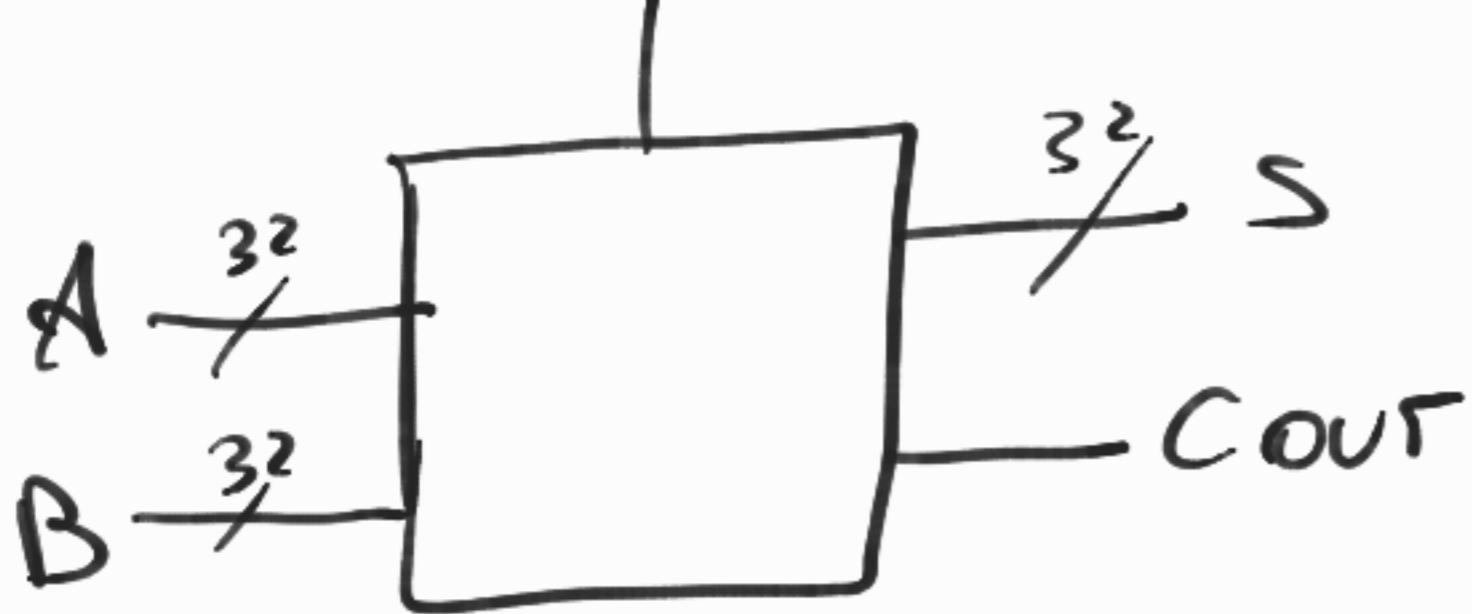
ALU CRLL



b_4, b_3, b_2, b_1, b_0



ALU CTRL



ALU CTRL	$M = 1$	$M = 0$ mod. logic	
C_2, C_1, C_0	$C1 = 0$	$C1 = 1$	$C1 = \text{IND.}$
0 0 0	$x + y$	$x + y + 1$	$x \oplus y$, $x \oplus y'$
0 0 1	$x - y - 1$	$x - y$	x , x'
0 1 0	x	$x + 1$	
0 1 1	$x - 1$	x	
1 0 0	y	$y + 1$	y
1 0 1	$-y - 1$	$-y$	y'
1 1 0	0	1	0000
1 1 1	-1	0

