GNU Radio Zedboard Implementation with FPGA Acceleration

Khodamoradi, Hong, Pandit, Parikh

Outline

- Overview
- Accomplishments
- Milestones
- Two week sprint
- Quarter Plan
- Conclusion

Overview

Deliverable Status

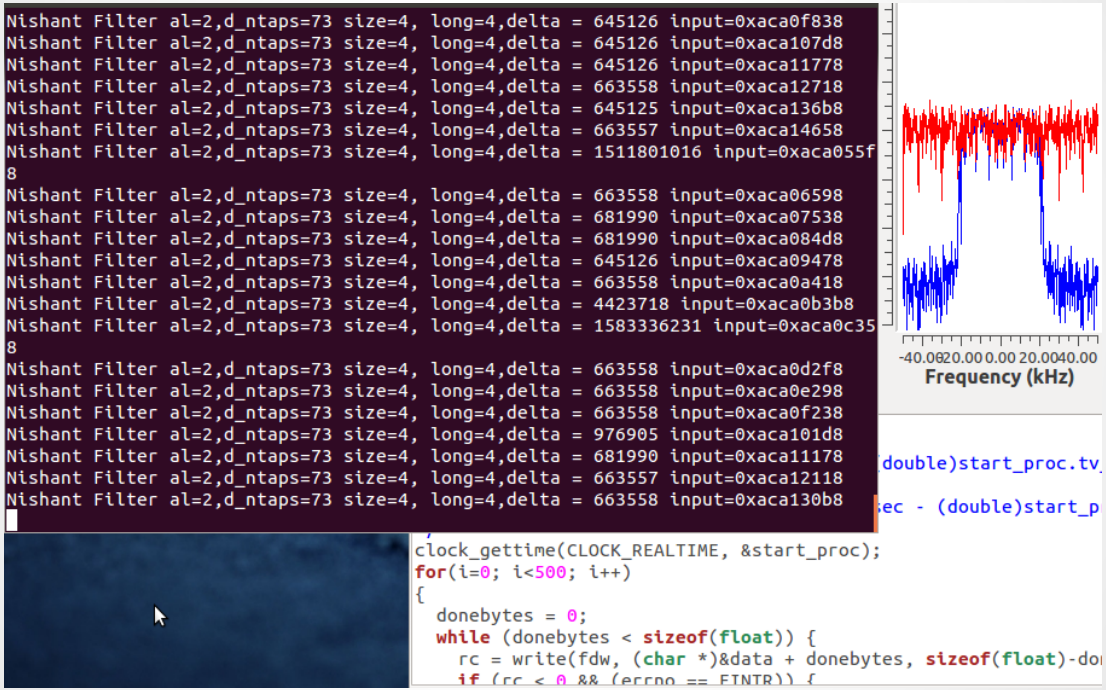
Xillybus Integration with GNU Radio (GR)
Successes and Hurdles

Function Replacement

Accomplishments

- Modified Low Pass Filter Block Created
- Verified FIR in Test Bench
- FPGA with Xillybus Loopback
- Host code for FPGA integrated into GR
- Throughput measurements

Measurements



Pure Software Throughput: Approximately 6 MB/sec

Measurements

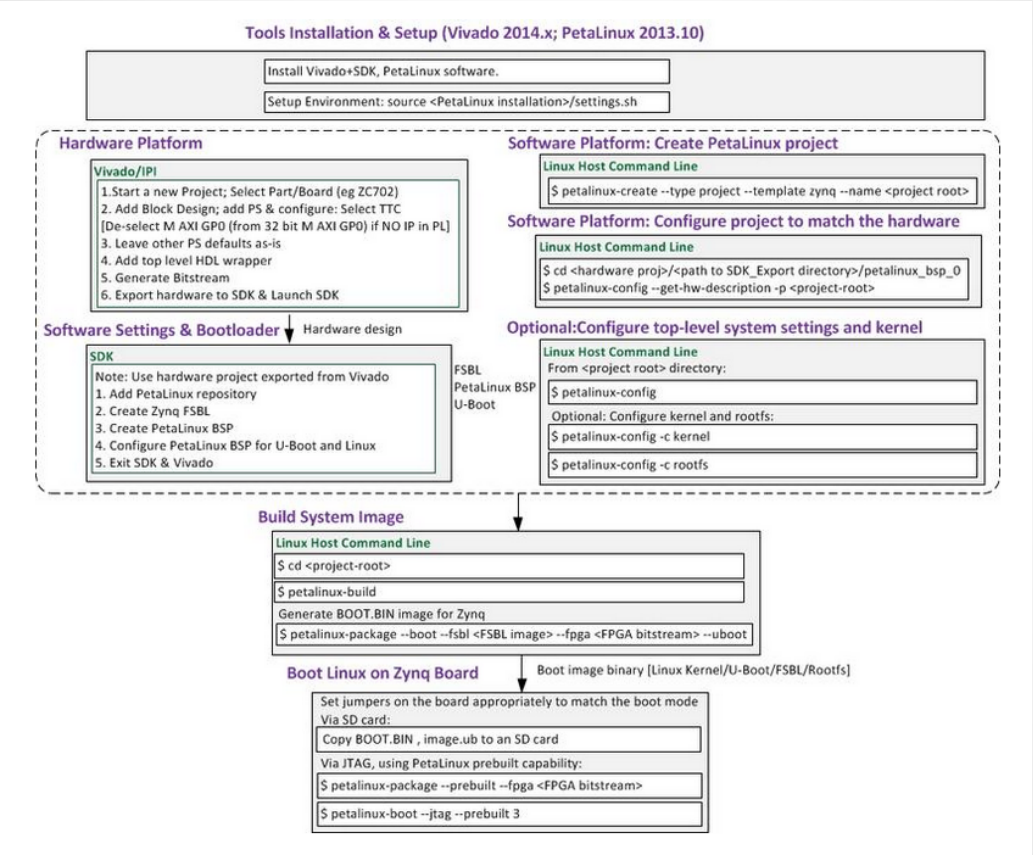
```
write nsec: 1548.302000
read  nsec: 1290.252000
data = 1.000000, rdata = 3.000000
input data=2
write nsec: 1548.302000
read  nsec: 1290.252000
data = 2.000000, rdata = 4.000000
input data=2.5
write nsec: 1548.302000
read  nsec: 1253.388000
data = 2.500000, rdata = 4.500000
input data=2.55
write nsec: 1548.302000
read  nsec: 1290.250000
data = 2.550000, rdata = 4.550000
input data=2.566
write nsec: 1548.300000
read  nsec: 1253.388000
data = 2.566000, rdata = 4.566000
input data=2.579345
write nsec: 1548.302000
read  nsec: 1253.388000
data = 2.579345, rdata = 4.579345
input data=
```

test.c

```
}
clock_gettime(CLOCK_REALTIME, &end_proc);
printf("write nsec: %f\n", (double)( 1000000000*(end_proc.
+(end_proc.tv_nsec - start_proc.tv_nsec) )/500 );


usleep(10000); //around 10ms

clock_gettime(CLOCK_REALTIME, &start_proc);
for(i=0; i<500; i++)
{

 //read
  donebytes = 0;
  while (donebytes < sizeof(float)) {
    rc = read(fdr, (char *)&rdata + donebytes, sizeof(floa
    if (rc < 0 && (errno == EINTR)) {
      printf("read error\n");
      continue;
    }
    if (rc <= 0)
      break;
    donebytes += rc;
  }
}
clock_gettime(CLOCK_REALTIME, &end_proc);
printf("read  nsec: %f\n", (double)( 1000000000*(end_proc.
+(end_proc.tv_nsec - start_proc.tv_nsec) )/500 );
  printf("data = %f, rdata = %f\n",data, rdata);

}//end input number
```

Xillybus Throughput: Approximately 1.5 MB/sec
(max supported 200MBps)

About the PetaLinux



Examples:

Using QEMU for Gnu Radio embedded applications

FPGA-based Implementation of Multiple PHY Layers of IEEE 802.15.4 Targeting SDR Platform

Upcoming Two Week Sprint

- Optimize speed of Xillybus (Jun, Ali)
- Identify Blocks to Recreate (Team)
- Create test benches using captured data (Keyur, Nishant)
- Prove blocks will fit on FPGA via simulation(Team)

Quarter Plan

Two demonstration goals at the end of this project

- show that data is processed to nearly the same fidelity on the Zedboard as on a laptop
- Integrate Verilog code with GNU Radio and demo
  - with previously recorded samples
  - in real-time (stretch goal)

Conclusion

- Proven we can work with Xillybus from within GNU Radio.
- The function we choose to implement performed faster on arm processor than FPGA.