GNU Radio Zedboard Implementation with FPGA Acceleration

Khodamoradi, Hong, Pandit, Parikh

Overview

Deliverable Status

Wideband FM (WBFM) Block Analysis down to C++ levels

Function Replacement

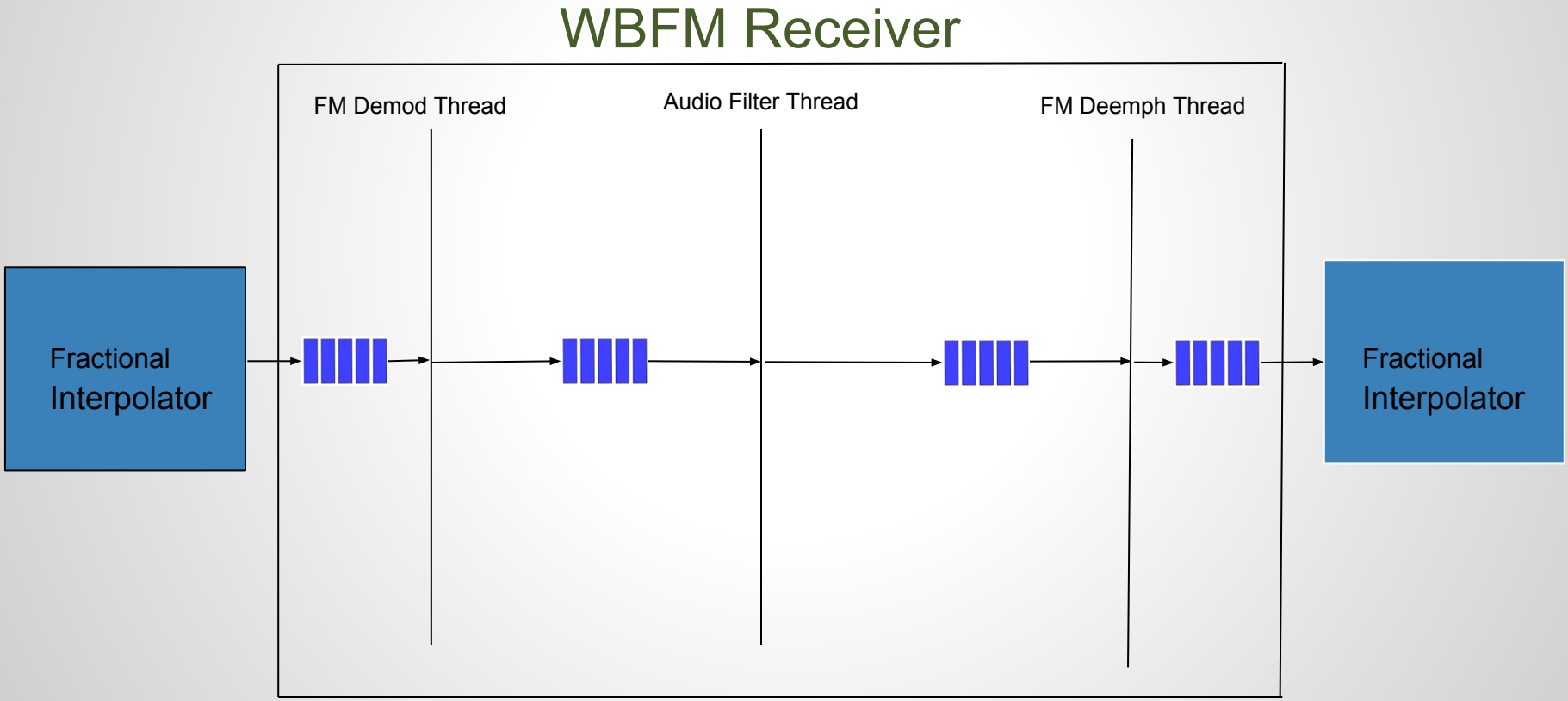
Accomplishments

- Correcting Xillybus usage via more efficient data transfer - speeds of up to 285 MB/sec
- Full analysis of WBFM block - python script calls to other .py files and .cc files
- Part of the WBFM block analysis included what values can be hardcoded.
- Have determined steps on how to create a new OTT block in GRC to wrap our host code
- Test bench data for each individual .cc function as well as the WBFM block as a whole

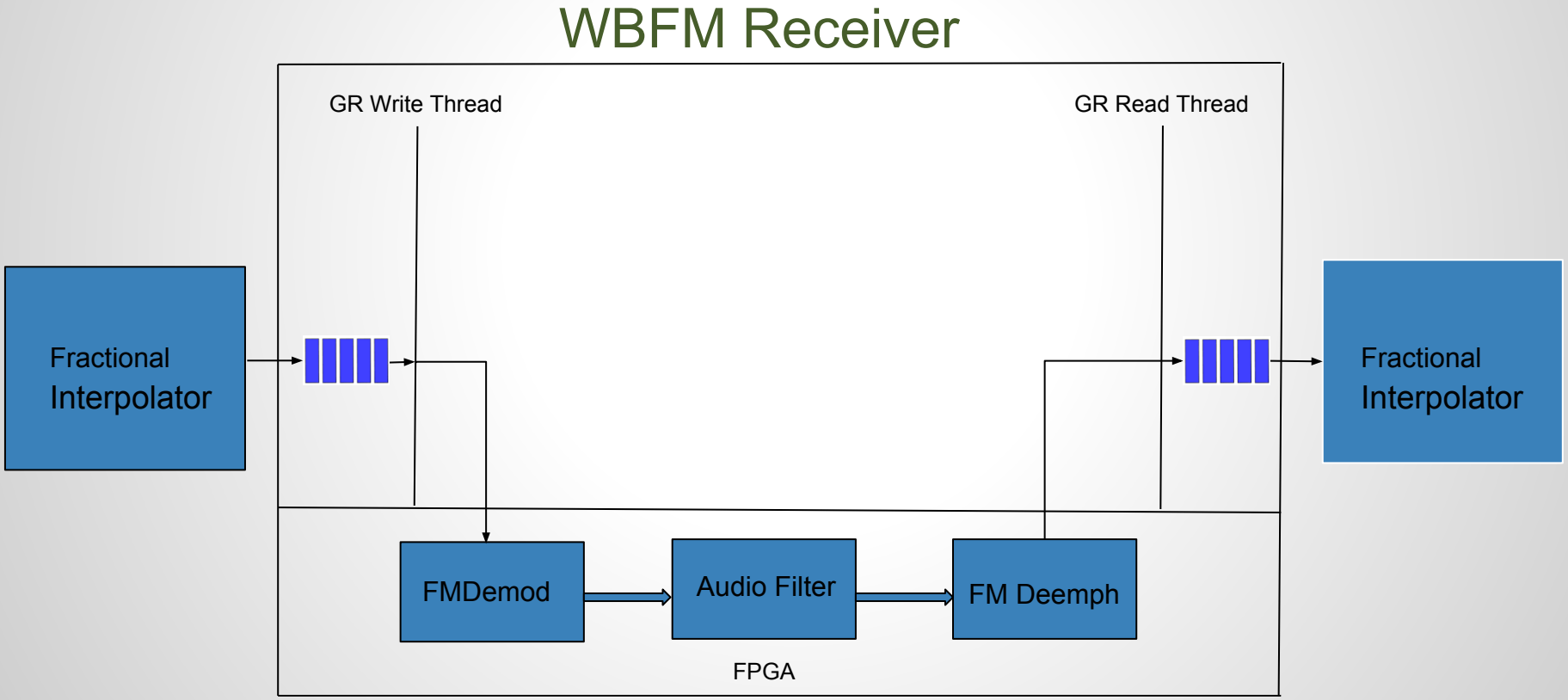
Non-changing Variables

- Several demodulator parameters
  - quad_rate
  - audio_decimation
  - fm_demod_gain
  - audio_rate
  - width_of_transition_band
  - WINDOW
- FIR has 309 non-changing taps
- IIR has 4 non-changing taps

Current Design



Proposed Design



Xillibus Interface in Xilinux

- We have both AXI and AXI-Lite available

Xillibus in Xilinux device tree

```
xillybus@50000000 {
        compatible = "xillybus,xillybus-1.00.a";
        reg = <0x50000000 0x1000>;
        interrupts = <0x0 0x3b 0x1>;
        interrupt-parent = <0x2>;
        dma-coherent;
};

xillybus_lite@50002000 {
        compatible = "xillybus,xillybus_lite_of-1.00.a";
        reg = <0x50002000 0x1000>;
        interrupts = <0x0 0x3a 0x1>;
        interrupt-parent = <0x2>;
};
```

Loaded devices in Xilinux /sys/devices

```
root@localhost:/sys/devices/amba.0/50000000.xillybus# cat uevent
DRIVER=xillybus_of
OF_NAME=xillybus
OF_FULLNAME=/amba@0/xillybus@50000000
OF_COMPATIBLE_0=xillybus,xillybus-1.00.a
OF_COMPATIBLE_N=1
MODALIAS=of:NxillybusT<NULL>Cxillybus,xillybus-1.00.a
root@localhost:/sys/devices/amba.0/50000000.xillybus# cat ../50002000.xillybus_lite/uevent
DRIVER=xillybus_lite_of
OF_NAME=xillybus_lite
OF_FULLNAME=/amba@0/xillybus_lite@50002000
OF_COMPATIBLE_0=xillybus,xillybus_lite_of-1.00.a
OF_COMPATIBLE_N=1
MODALIAS=of:Nxillybus_liteT<NULL>Cxillybus,xillybus_lite_of-1.00.a
```

Xillibus' loaded modules (lsmod)

```
xillybus_of            3599  2
xillybus_core         17819  3 xillybus_of
xillybus_lite_of       2257  0
```

Speed Measurement

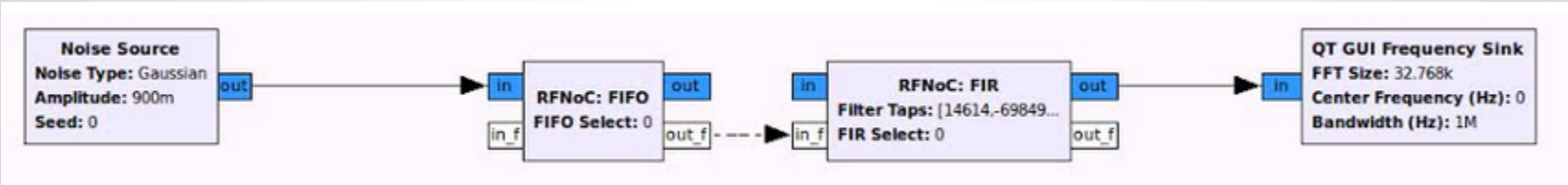
- **Received data in WBFM block**
  - **~2.3 MB over 300 mSec ≈ 7MB/sec**
- **Xillibus speed test**

Delay (nSec)	Speed MB/sec
0	285
1e3	111
1e4	91
1e5	47
1e6	7

```
for(i=8; i<SIZE; i++)
buf[i] = 33+i;
clock_gettime(CLOCK_MONOTONIC, &start_tm);
nsec_tm = (double)(1000000000*start_tm.tv_sec + start_tm.tv_nsec);
memcpy(&buf, &nsec_tm, 8);//copy time to send buf
for(k=0; k<NUM_TRY; k++)
{
   for(j=0; j<COMPLX; j++)
   {
    allwrite(fd, buf, rc);
   }
   usleep(DELAY_MS);
}
```

Some news! RFNoC (Radio Frequency Network on Chip)

- Same approach as us.
- Eases SR + FPGA design process (prebuild FPGS blocks).
- Alpha release issues:
  - XML description of blocks not complete
  - MIMO/aligned streaming not supported in GR
  - Overruns in radio can stall RX stream
- Ettus E300 USRP (ZYNQ) $2,700.00



Upcoming Two Weeks Sprint

- Test FM demodulation, Audio Filter (FIR filter), and FM De-emphasis (IIR filter) .c code - the three pieces of what will go on the FPGA
- Test fully replaced WBFM block in FPGA
- Wrap host code in new GRC block

Quarter Plan

Goals left to complete this project

- Validate functions ported to C
- Integrate Verilog code with GNU Radio
  - ensure data is being processed quickly enough
  - beware scheduling issues
- Listen to GNU Radio without skipping due to buffer overflows