CMP3006 LAB CHEATSHEET

Last updated: 12.04.2020

Topics covered:

1- PIN/PORT/DDR

2- ADC

3- Interrupts

4- Timers

5- Motors

6- Interfacing: SPI / I2C

Useful links:

https://github.com/berkileri/CMP3006-Lab-Work/

https://www.arduino.cc/reference/en/

https://web.ics.purdue.edu/~jricha14/Port_Stuff/PortA_ADC.htm

http://sculland.com/ATmega168/Interrupts-And-Timers/8-bit-Timer-Example-Software/

http://sculland.com/ATmega168/Interrupts-And-Timers/16-Bit-Timer-Setup/

Reminder! *You can google anything that you don't know, including but not limited to:*

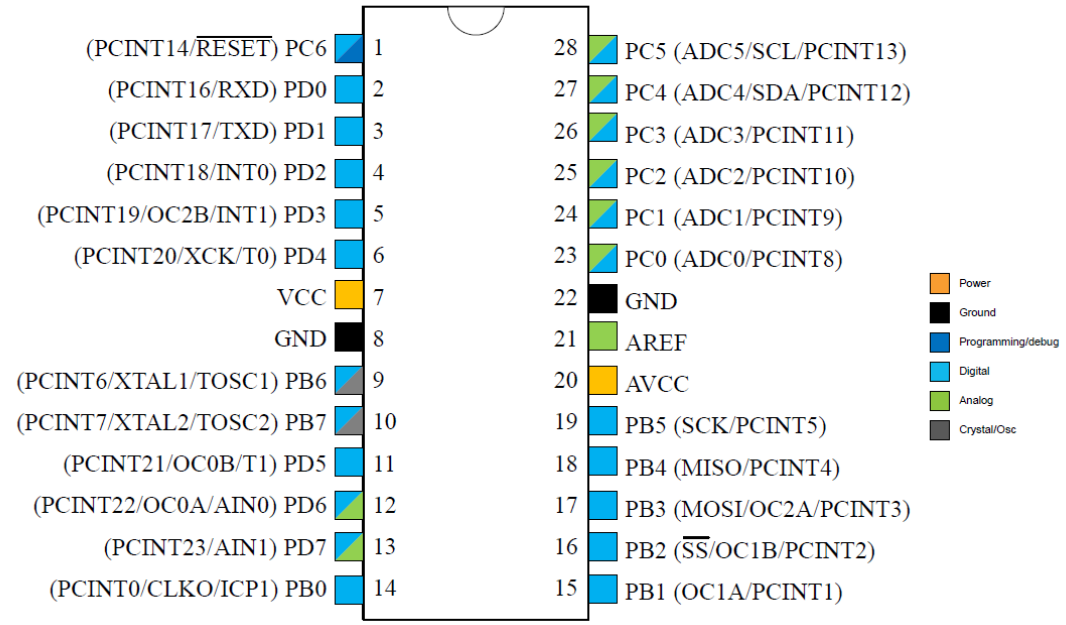
-the register names

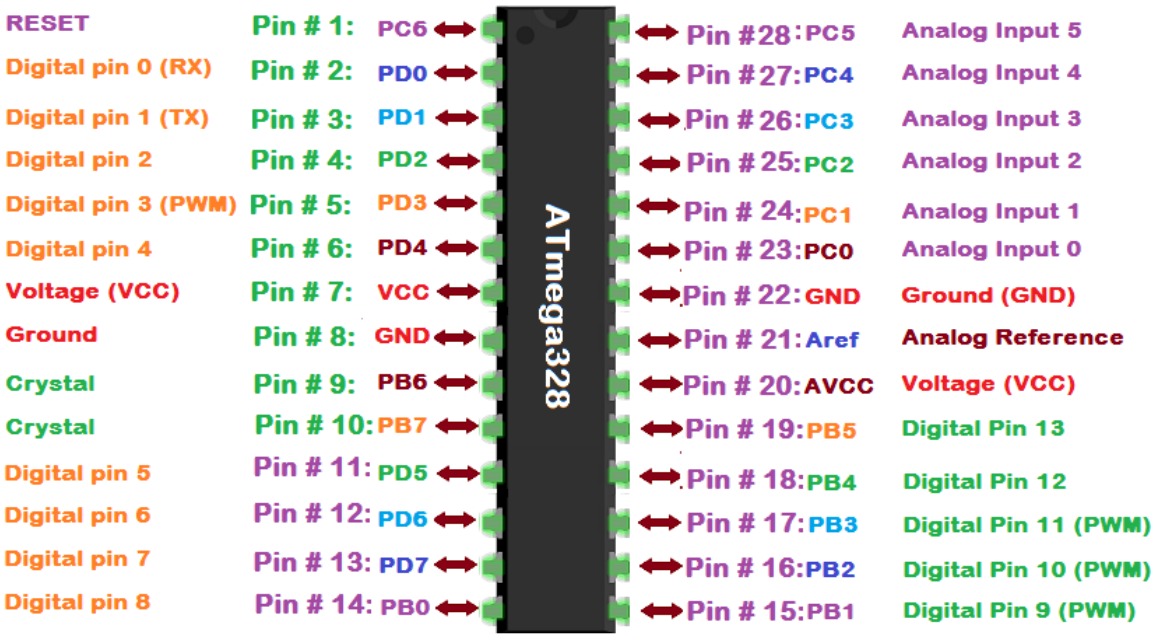
-each bit of each register

-using components like motors and LCD screens.

Pin-out

Figure 5-1. 28-pin PDIP





Status Register

Bit	7	6	5	4	3	2	1	0
	I	T	H	S	V	N	Z	C
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – I: Global Interrupt Enable

Bit 6 – T: Copy Storage
Bit 5 – H: Half Carry Flag
Bit 4 – S: Sign Flag, S = N ⊕ V
Bit 3 – V: Two's Complement Overflow Flag
Bit 2 – N: Negative Flag
Bit 1 – Z: Zero Flag
Bit 0 – C: Carry Flag

2. **ADC Control and Status Register A**

7	6	5	4	3	2	1	0
ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 – ADEN: ADC Enable
Bit 6 – ADSC: ADC Start Conversion
Bit 5 – ADATE: ADC Auto Trigger Enable
Bit 4 – ADIF: ADC Interrupt Flag
Bit 3 – ADIE: ADC Interrupt Enable
Bits 2:0 – ADPSn: ADC Prescaler Select [n = 2:0]

ADPS[2:0]	Division Factor
000	2
001	2
010	4
011	8
100	16
101	32
110	64
111	128

ADC Multiplexer Selection Register

Bit	7	6	5	4	3	2	1	0
	REFS1	REFS0	ADLAR		MUX3	MUX2	MUX1	MUX0
ss	R/W	R/W	R/W		R/W	R/W	R/W	R/W
iet	0	0	0		0	0	0	0

Bits 7:6 – REFSn: Reference Selection [n = 1:0]

REFS[1:0]	Voltage Reference Selection
00	AREF, Internal V_{ref} turned off
01	AV_{CC} with external capacitor at AREF pin
10	Reserved
11	Internal 1.1V Voltage Reference with external capacitor at AREF pin

Bit 5 – ADLAR: ADC Left Adjust Result

Bits 3:0 – MUXn: Analog Channel Selection [n = 3:0]

MUX[3:0]	Single Ended Input
0000	ADC0
0001	ADC1
0010	ADC2
0011	ADC3
0100	ADC4
0101	ADC5
0110	ADC6
0111	ADC7
1000	Temperature sensor
1001	Reserved
1010	Reserved
1011	Reserved
1100	Reserved
1101	Reserved
1110	1.1V (V_{BG})
1111	0V (GND)

16.1. Interrupt Vectors in ATmega328/P

Table 16-1. Reset and Interrupt Vectors in ATmega328/P

Vector No	Program Address(2)	Source	Interrupts definition
1	0x0000(1)	RESET	External Pin, Power-on Reset, Brown-out Reset and Watchdog System Reset
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	INT1	External Interrupt Request 0
4	0x0006	PCINT0	Pin Change Interrupt Request 0
5	0x0008	PCINT1	Pin Change Interrupt Request 1
6	0x000A	PCINT2	Pin Change Interrupt Request 2
7	0x000C	WDT	Watchdog Time-out Interrupt
8	0x000E	TIMER2_COMPA	Timer/Counter2 Compare Match A
9	0x0010	TIMER2_COMPB	Timer/Coutner2 Compare Match B
10	0x0012	TIMER2_OVF	Timer/Counter2 Overflow
11	0x0014	TIMER1_CAPT	Timer/Counter1 Capture Event
12	0x0016	TIMER1_COMPA	Timer/Counter1 Compare Match A
13	0x0018	TIMER1_COMPB	Timer/Coutner1 Compare Match B
14	0x001A	TIMER1_OVF	Timer/Counter1 Overflow
15	0x001C	TIMER0_COMPA	Timer/Counter0 Compare Match A
16	0x001E	TIMER0_COMPB	Timer/Coutner0 Compare Match B
17	0x0020	TIMER0_OVF	Timer/Counter0 Overflow
18	0x0022	SPI STC	SPI Serial Transfer Complete
19	0x0024	USART_RX	USART Rx Complete
20	0x0026	USART_UDRE	USART Data Register Empty
21	0x0028	USART_TX	USART Tx Complete
22	0x002A	ADC	ADC Conversion Complete
23	0x002C	EE READY	EEPROM Ready
24	0x002E	ANALOG COMP	Analog Comparator
25	0x0030	TWI	2-wire Serial Interface (I^2C)
26	0x0032	SPM READY	Store Program Memory Ready

17.2.1. External Interrupt Control Register A

Bit	7	6	5	4	3	2	1	0
					ISC11	ISC10	ISC01	ISC00
Access					R/W	R/W	R/W	R/W
Rese					0	0	0	0

Bits 3:2 – ISC1n: Interrupt Sense Control 1 [n = 1:0]

Value	Description
00	The low level of INT1 generates an interrupt request.
01	Any logical change on INT1 generates an interrupt request.
10	The falling edge of INT1 generates an interrupt request.
11	The rising edge of INT1 generates an interrupt request.

17.2.2. External Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0
							INT1	INT0
Access							R/W	R/W
Reset							0	0

-Enables external pin interrupt for INTx

17.2.3. External Interrupt Flag Register

Bit	7	6	5	4	3	2	1	0
							INTF1	INTF0
Access							R/W	R/W
Reset							0	0

-If INTx pin triggers an interrupt request, INTFx is set.

17.2.4. Pin Change Interrupt Control Register

Bit	7	6	5	4	3	2	1	0
						PCIE2	PCIE1	PCIE0
Access						R/W	R/W	R/W
Reset						0	0	0

-Enables pin change interrupt for PCIEx

17.2.5. Pin Change Interrupt Flag Register

Bit	7	6	5	4	3	2	1	0
						PCIF2	PCIF1	PCIF0
Access						R/W	R/W	R/W
Reset						0	0	0

-If PCIEx pin triggers an interrupt request, PCIFx is set.

17.2.6. Pin Change Mask Register 2

Bit	7	6	5	4	3	2	1	0
	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16
cess	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

2.7. Pin Change Mask Register 1

Bit	7	6	5	4	3	2	1	0
		PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8
:cess		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Pin Change Mask Register 0

Bit	7	6	5	4	3	2	1	0
	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0
ss	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

-PCINTx selects whether pin change interrupt is enabled on the corresponding I/O pin

8-bit Timer Registers

Counter 0	Description	Counter 2
TCCR0A	Timer/Counter Control Register A	TCCR2A
TCCR0B	Timer/Counter Control Register B	TCCR2B
TIMSK0	Timer/Counter Interrupt Mask Register	TIMSK2
TIFR0	Timer/Counter Interrupt Flag Register	TIFR2
TCNT0	Timer/Counter Register (The Timer)	TCNT2
OCR0A	Output Compare Register A	OCR2A
OCR0B	Output Compare Register B	OCR2B

8-bit Timer Register Tables For Counter 0 & Counter 2

TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00
TCCR2A	COM2A1	COM2A0	COM2B1	COM2B0	-	-	WGM21	WGM20
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Stores Compare Output settings and 2 of the 3 Waveform Generation Mode settings.								

TCCR0B	FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00
TCCR2B	FOC2A	FOC2B	-	-	WGM22	CS22	CS21	CS20
Read/Write	W	W	R	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Stores A and B Force Output Compare bits, 1 of the 3 Waveform Generation Mode settings, and the Clock Speed Selection settings.								

TIMSK0	-	-	-	-	-	OCIE0B	OCIE0A	TOIE0
TIMSK2	-	-	-	-	-	OCIE2B	OCIE2A	TOIE2
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Stores the Output Compare Match Interrupt Enable A and B bits and Timer Overflow Interrupt Enable bit								

TIFR0	-	-	-	-	-	OCF0B	OCF0A	TOV0
TIFR2	-	-	-	-	-	OCF2B	OCF2A	TOV2
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Stores the Output Compare Match Flags A and B and Timer Overflow Interrupt flag								

Waveform Generation Mode (WGM):

Mode	WGM02	WGM01	WGM00	Description (Counter 0)	TOP
Mode	WGM22	WGM21	WGM20	Description (Counter 2)	TOP
0	0	0	0	Normal	0XFF
1	0	0	1	Phase Correct Pulse Width Modulation (PWM)	0XFF
2	0	1	0	Clear Timer on Compare (CTC)	OCRA
3	0	1	1	Fast Pulse Width Modulation (PWM)	0XFF
4	1	0	0	Reserved	-
5	1	0	1	Phase Correct Pulse Width Modulation (PWM)	OCRA
6	1	1	0	Reserved	-
7	1	1	1	Fast Pulse Width Modulation (PWM)	OCRA

Clock Speed Selection

CS02	CS01	CS00	Description (Counter 0)
CS22	**CS21**	**CS20**	**Description (Counter 2)**
0	0	0	No clock source (Timer/Counter stopped)
0	0	1	Clock (No prescaling)
0	1	0	Clock/8 (From prescaler)
0	1	1	Clock/64 (From prescaler)
1	0	0	Clock/256 (From prescaler)
1	0	1	Clock/1024 (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

16-bit Timer Registers

Counter 1	Description
TCCR1A	Timer/Counter Control Register A
TCCR1B	Timer/Counter Control Register B
TCCR1C	Timer/Counter Control Register C
ICR1H	Input Capture Register 1 High
ICR1L	Input Capture Register 1 Low
TIMSK1	Timer/Counter Interrupt Mask Register
TIFR1	Timer/Counter Interrupt Flag Register
TCNT1H	Timer/Counter Register High (The Timer - High)
TCNT1L	Timer/Counter Register Low (The Timer - Low)
OCR1AH	Output Compare Register A High
OCR1AL	Output Compare Register A Low
OCR1BH	Output Compare Register B High
OCR1BL	Output Compare Register B Low

16-bit Timer Register Tables For Counter 1

TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	-	-	WGM11	WGM10
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Stores Compare Output settings and 2 of the 4 Waveform Generation Mode settings.								

TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10
Read/Write	W	W	R	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Stores the Input Capture Noise Canceller and Input Capture Edge Select bits, 2 of the 4 Waveform Generation Mode settings, and the Clock Speed Selection settings.								

TCCR1C	FOC1A	FOC1B	-	-	-	-	-	-
Read/Write	W	W	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Stores A and B Force Output Compare bits.								

TIMSK1	-	-	ICIE1	-	-	OCIE1B	OCIE1A	TOIE1
Read/Write	R	R	R/W	R	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Stores the Input Capture Interrupt Enable bit, the Output Compare Match Interrupt Enable A and B bits and the Timer Overflow Interrupt Enable bit								

TIFR1	-	-	ICF1	-	-	OCF1B	OCF1A	TOV1
Read/Write	R	R	R/W	R	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Stores the Input Capture Flag, the Output Compare Match Flags A and B and the Timer Overflow Interrupt flag								

Waveform Generation Mode (WGM) 16-bit timer settings

Mode	WGM13	WGM12	WGM11	WGM10	Description	TOP
0	0	0	0	0	Normal	0xFFFF
1	0	0	0	1	Pulse Width Modulation (PWM), Phase Correct, 8-bit	0x00FF
2	0	0	1	0	Pulse Width Modulation (PWM), Phase Correct, 9-bit	0x01FF
3	0	0	1	1	Pulse Width Modulation (PWM), Phase Correct, 10-bit	0x03FF
4	0	1	0	0	Clear Timer on Compare (CTC)	OCR1A
5	0	1	0	1	Fast Pulse Width Modulation (PWM), 8-bit	0x00FF
6	0	1	1	0	Fast Pulse Width Modulation (PWM), 9-bit	0x01FF
7	0	1	1	1	Fast Pulse Width Modulation (PWM), 10-bit	0x03FF
8	1	0	0	0	Pulse Width Modulation (PWM), Phase and Frequency Correct	ICR1
9	1	0	0	1	Pulse Width Modulation (PWM), Phase and Frequency Correct	OCR1A
10	1	0	1	0	Pulse Width Modulation (PWM), Phase Correct	ICR1
11	1	0	1	1	Pulse Width Modulation (PWM), Phase Correct	OCR1A
12	1	1	0	0	Clear Timer on Compare (CTC)	ICR1
13	1	1	0	1	(Reserved)	-
14	1	1	1	0	Fast Pulse Width Modulation (PWM)	ICR1
15	1	1	1	1	Fast Pulse Width Modulation (PWM)	OCR1A

Clock Speed Selection

CS12	CS11	CS10	Description (Counter 1)
0	0	0	No clock source (Timer/Counter stopped)
0	0	1	Clock (No prescaling)
0	1	0	Clock/8 (From prescaler)
0	1	1	Clock/64 (From prescaler)
1	0	0	Clock/256 (From prescaler)
1	0	1	Clock/1024 (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

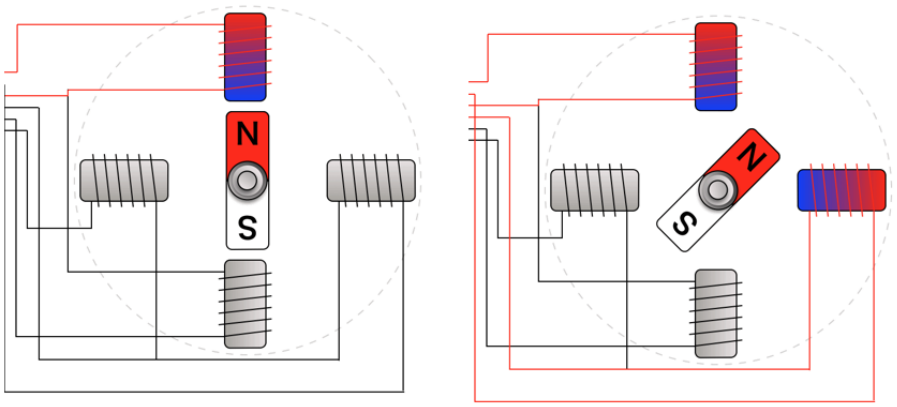
Stepper Motors

$$Step\ angle\ = \frac{90}{Num\ of\ teeth}$$

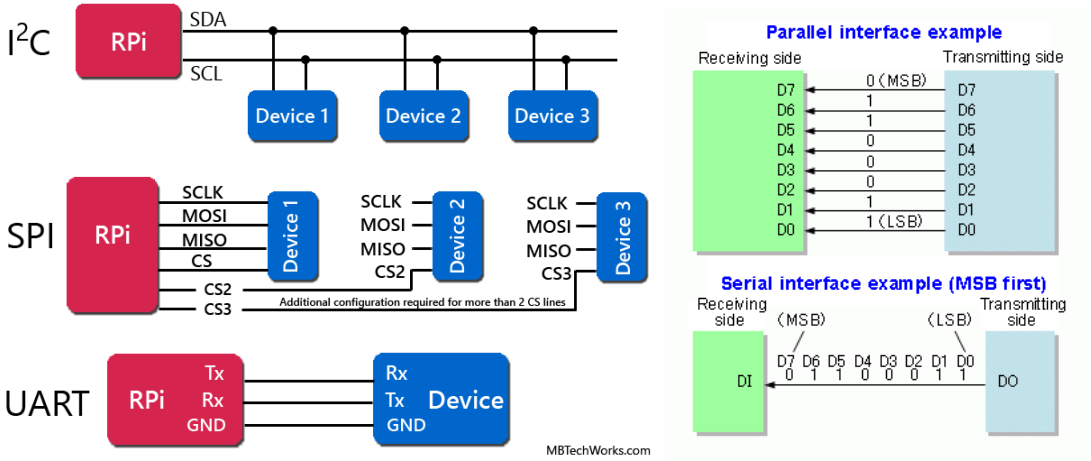
$$Steps\ per\ revolution\ = \frac{360}{Step\ angle} = 4 * Num\ of\ teeth$$

$$Steps\ per\ second\ = \frac{RPM * Steps\ per\ revolution}{60}$$

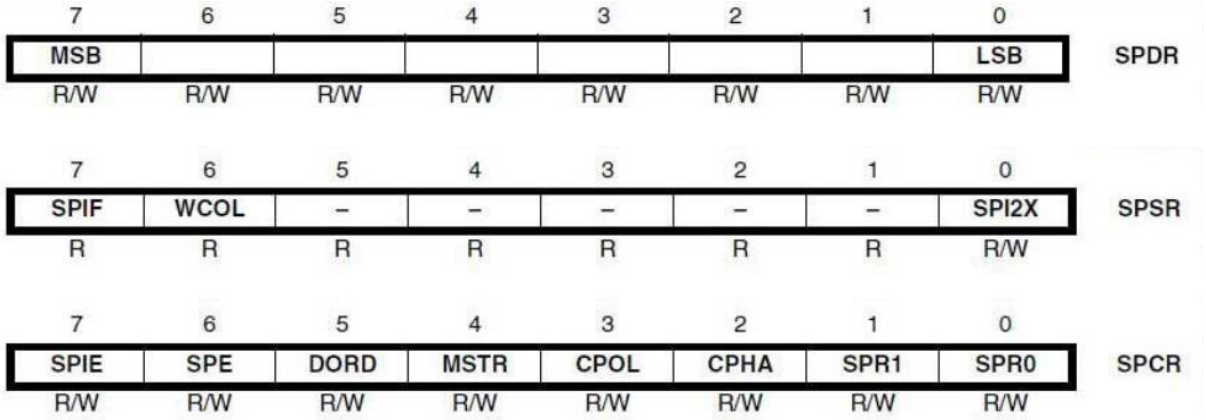
1 phase drive —— 2 phase drive ——



Interfacing



SPI



7	6	5	4	3	2	1	0	
MSB							LSB	SPDR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
7	6	5	4	3	2	1	0	
SPIF	WCOL	–	–	–	–	–	SPI2X	SPSR
R	R	R	R	R	R	R	R/W	
7	6	5	4	3	2	1	0	
SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

SPDR: -**MSB/LSB**: Most/Least Significant Bit

SPSR: -SPIF: Interrupt Flag -**WCOL**: Write Collision Flag -**SPI2X:** 2 times speed up

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SPCR: -SPIE: Interrupt Enable **-SPE:** SPI Enable **-DORD**: Data Order **-MSTR**: Master **-CPOL:** Clock Polarity – **CPHA:** Clock Phase -**SPRx:** Prescaler

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Table 18-2. SPI Modes

SPI Mode	Conditions	Leading Edge	Trailing eDge
0	CPOL=0, CPHA=0	Sample (Rising)	Setup (Falling)
1	CPOL=0, CPHA=1	Setup (Rising)	Sample (Falling)
2	CPOL=1, CPHA=0	Sample (Falling)	Setup (Rising)
3	CPOL=1, CPHA=1	Setup (Falling)	Sample (Rising)

SPI2X	SPR1	SPR0	SCK Frequency
0	0	0	$f_{osc}/4$
0	0	1	$f_{osc}/16$
0	1	0	$f_{osc}/64$
0	1	1	$f_{osc}/128$
1	0	0	$f_{osc}/2$
1	0	1	$f_{osc}/8$
1	1	0	$f_{osc}/32$
1	1	1	$f_{osc}/64$

I2C

TWI Status Register (TWSR)

TWS7	TWS6	TWS5	TWS4	TWS3	-	TWPS1	TWPS0

Bits 7..3 – TWS: TWI Status
These five bits show the status of the TWI control and bus.

Bits 1..0 – TWPS: TWI Prescaler Bits
These bits control the bit rate prescaler.

Figure 18-12. TWSR: TWI Status Register

TWI Bit Register (TWBR)

TWBR7	TWBR6	TWBR5	TWBR4	TWBR3	TWBR2	TWBR1	TWBR0

TWI Address Register (TWAR)

Bit	7	6	5	4	3	2	1	0	
	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	TWAR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	1	1	1	1	1	1	0	

TWA6-0 (TWI slave Address)

TWGCE (TWI General Call Recognition Enable bit)

- 1: Answer to general call

TWI Control Register (TWCR)

Bit	7	6	5	4	3	2	1	0	
	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	TWCR
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

TWINT (TWI Interrupt Flag)

TWEA (TWI Enable Acknowledge Bit)

- 1: ACK, 0: NACK

TWSTA (TWI Start condition bit)

TWSTO (TWI Stop condition bit)

TWWC (TWI Write Collision flag)

TWEN (TWI Enable bit)

TWIEN (TWI Interrupt Enable)