

3 Processor – Memory Interface and DDR3 DIMMs

3.1 Introduction

This chapter contains information and details on the DDR3 system memory topologies, layout guidelines, schematic connection details, and any specific considerations that will provide a robust design for Havendale/Lynnfield platforms using DDR3 unbuffered DIMMs.

The guidelines documented in this chapter are based on the use of standard 90-degree 240-pin DDR3 DIMM connectors, standard JEDEC and Intel compliant DIMMs, standard JEDEC and Intel compliant DRAMs, and other physical motherboard parameters outlined in this document. Deviations from the recommended system memory guidelines in terms of topology, layout, connector type, and configuration can cause system instability. If any deviations from this design guide occur, Intel highly recommends designers perform extensive modeling, simulation, and validation.

Table 3-1 summarizes all of the DDR3 system memory signal groupings discussed and covered in this chapter.

Table 3-1. DDR3 System Memory Signal Groups (Sheet 1 of 2)

Section	Group	Signal Name	Description	Note
Section 3.2.3	Clock	SA_CK[3:0] SB_CK[3:0] SA_CK#[3:0] SB_CK#[3:0]	Differential Clocks Differential Clock Complements	
Section 3.2.4	Data	SA_DQ[63:0] SB_DQ[63:0] SA_DM[7:0] SB_DM[7:0] SA_DQS[8:0] SB_DQS[8:0] SA_DQS#[8:0] SB_DQS#[8:0] SA_ECC_CB[7:0] SB_ECC_CB[7:0]	Data Bus Data Mask (output only) Data Strobes Data Strobe Complements ECC Check Bits	1

Table 3-1. DDR3 System Memory Signal Groups (Sheet 2 of 2)

Section	Group	Signal Name	Description	Note
Section 3.2.5	Control	SA_CKE[3:0] SB_CKE[3:0] SA_CS#[3:0] SB_CS#[3:0] SA_ODT[3:0] SB_ODT[3:0]	Clock Enable (One per DIMM Rank) Chip Select (One per DIMM Rank) On-Die Termination (One per DIMM Rank)	
Section 3.2.6	Command / Address	SA_MA[15:0] SB_MA[15:0] SA_BS[2:0] SB_BS[2:0] SA_RAS# SB_RAS# SA_CAS# SB_CAS# SA_WE# SB_WE#	Address Bus Bank Select Row Address Select Column Address Select Write Enable	
Section 3.2.7	Miscellaneous	SA_DIMM_VREFDQ SB_DIMM_VREFDQ SM_RCOMP[2:0] SM_DRAMRST#	Output DDR3 DIMM DQ Reference Voltages System Memory Compensation Signals DDR3 DRAM Reset	

1. The DQS[8], DQSB[8], and ECC_CB[7:0] signals are ECC specific data group signals. The LGA1156 socket breakout has been optimized to enable the routing of these ECC signals in a 4-layer Foxhollow platform design. The Piketon/KingsCreek platform does not support ECC therefore the DQS[8], DQSB[8], and ECC_CB[7:0] pins must be left as no connects. Foxhollow platforms do support ECC.

3.2 DDR3 System Memory Signal Topologies and Layout Design Guidelines

3.2.1 DDR3 DIMM Pad Stack Recommendations

To maximize spacing within the DIMM pin field, a 50/40/28 (antipad/pad/finished hole) pad stack is recommended. The recommended pad stack will allow greater than 20 mils spacing in the DIMM pin field for 2-track routing of data group signals. This also allows 3-track 6.5 mil trace width with 4.5 mil spacing for control signals and 5.0 mil trace width with 6.0 mil spacing for address/command signals

3.2.2 Byte Lane Motherboard Ordering Requirements

For proper group isolation in a 4-layer stackup the following byte lane requirements must be followed on a Piketon/KingsCreek platform design:

- Top Layer (Motherboard Layer 1):
A[0] - A[1] - A[2] - A[3] - Address/Command/Control - A[5] - A[6] - A[7]
- Bottom Layer (Motherboard Layer 4):
B[0] - B[1] - B[2] - B[3] - Clocks - B[4] - A[4] - B[5] - B[6] - B[7]

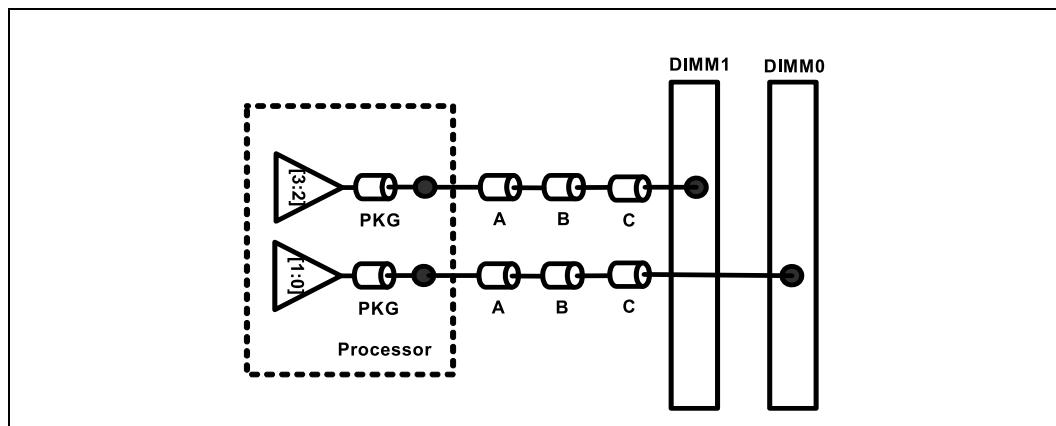
3.2.3 Clock Group Signals

The clock signal group includes four differential clock pairs total per channel. The memory controller generates and drives two separate differential clock pairs to each DDR3 DIMM connector. [Table 3-2](#) summarizes the clock signal mapping.

Table 3-2. Differential Clock Signal Mapping

Processor Signal	Relative To
SA_CK/SA_CK#[3:2]	Channel A DIMM1
SA_CK/SA_CK#[1:0]	Channel A DIMM0
SB_CK/SB_CK#[3:2]	Channel B DIMM1
SB_CK/SB_CK#[1:0]	Channel B DIMM0

The diagrams and table below depict the recommended topology and layout routing guidelines for the clock group signals.

Figure 3-1. Clock Group Signal Routing Topology**Table 3-3. Clock Group Routing Guidelines (Sheet 1 of 2)**

Routing Parameters	Channel A Details			Channel B Details			Units	Notes
	A	B	C	A	B	C		
Signal Reference	VSS	VSS	VSS	VSS	VSS	VSS		
Motherboard Layer	4	4	4	4	4	4		
Single-Ended Trace Impedance			36			36	Ohms	
Impedance Tolerance			±15			±15	%	
Trace Width	4.0	4.0	8.0	4.0	4.0	8.0	mils	
Minimum Trace Spacing	10.0	15.0	20.0	10.0	15.0	20.0	mils	2
Maximum Trace Length per Region	200	400	3500	200	300	4000	mils	
Ball to Via Maximum Length	50			50			mils	
Differential Spacing	4.0	4.0	5.0	4.0	4.0	5.0	mils	3
Minimum Serpentine Spacing	n/a	n/a	20.0	n/a	n/a	20.0	mils	4
Minimum Isolation Spacing	10.0	15.0	20.0	10.0	15.0	20.0	mils	5
Length and Matching Rules	Channel A Die To DIMM Details			Channel B Die To DIMM Details			Units	Notes

Table 3-3. Clock Group Routing Guidelines (Sheet 2 of 2)

Routing Parameters	Channel A Details			Channel B Details			Units	Notes
	A	B	C	A	B	C		
CK/CK#[3:0] Total Length	2700 to 3600			3600 to 4500			mils	6
CK/CK#[1:0] (max – min)	0 to 10			0 to 10			mils	6
CK/CK#[3:2] (max – min)	0 to 10			0 to 10			mils	6

Notes:

1. For single DIMM connector per channel or single memory channel platform designs the un-used DIMM1 SCK/CK#[3:2] clock group signals must be left as no connects.
2. Trace Spacing refers to the minimum trace-to-trace spacing between the clock pair signals.
3. Differential Spacing is identified as the trace spacing between a clock signal Sx_CK[n] and its compliment Sx_CK#[n].
4. Serpentine Spacing, also known as self spacing, is the minimum distance required from a clock group signal to itself when it serpentine on the motherboard. Clock signal group serpentine routing in Region A or Region B is not recommended.
5. Isolation Spacing is the minimum distance required between the clock and data group signals routed on layer four.
6. Length and matching rules include the processor package length + motherboard trace length (Die-To-DIMM1, Die-To-DIMM0).

3.2.4 Data Group Signals

The data signal group includes eighty-eight total signals for non-ECC based systems and ninety eight total signals for ECC based systems per channel. There is an associated differential data strobe pair and data mask signal for each data byte where each data byte must be routed together with its associated strobe and data mask on the same layer. **Table 3-4** summarizes the DQ/DM/ECC_CB to DQS/DQSB mapping.

Note that the processor does not have a DM[8] signal for either channel. As a result the DM[8] of each DDR3 DIMM connector (pin 161) must be tied directly to ground. The Piketon/KingsCreek platform does not support ECC therefore the DQS[8], DQSB[8], and ECC_CB[7:0] pins must be left as no connects at the processor side. Foxhollow platforms do support ECC.

Table 3-4. DQ/DM to DQS/DQSB Byte Group Mapping

Byte Group	DQ Signal	DM Signal	Associated Diff Strobe Pair
0	DQ[7:0]	DM[0]	DQS/DQS#[0]
1	DQ[15:8]	DM[1]	DQS/DQS#[1]
2	DQ[23:16]	DM[2]	DQS/DQS#[2]
3	DQ[31:24]	DM[3]	DQS/DQS#[3]
4	DQ[39:32]	DM[4]	DQS/DQS#[4]
5	DQ[47:40]	DM[5]	DQS/DQS#[5]
6	DQ[55:48]	DM[6]	DQS/DQS#[6]
7	DQ[63:56]	DM[7]	DQS/DQS#[7]
8	ECC_CB[7:0]	n/a	DQS/DQS#[8]

3.2.4.1 Data Group Signal Recommended Good Routing Practices

The DDR3 data bus (not address, command, control, or clocks) is the main limiter to the maximum interface transfer rates. This is due to data bus motherboard signal crosstalk effects where signal crosstalk is impacted by both overall signal length and signal spacing. The following are some recommended data bus layout optimizations for reducing crosstalk:

- Keep the data group signal Die-to-DIMM lengths as short as possible
 - Increase spacing in the break out Regions A and B as much as possible; especially important for the longer byte lanes
 - Reduce the break out Region A and B lengths and get to main route Region C as quickly as possible
 - Anywhere there is extra room to squeeze in additional spacing, the time and care should be spent to optimize the design
 - Special care should be applied to the spacing between data bus signals from adjacent byte lanes within the same channel and between adjacent data bus signals from different channels
 - Increase spacing as much as possible between adjacent data group signals from different byte lanes within same channel
 - Increase spacing as much as possible between adjacent data group signals from different channels
 - No signal serpentine routing in the compressed break-out Regions A and B

The table and diagram below depict the recommended topology and layout routing guidelines for the data group signals.

Figure 3-2. Data Group Signal Routing Topology

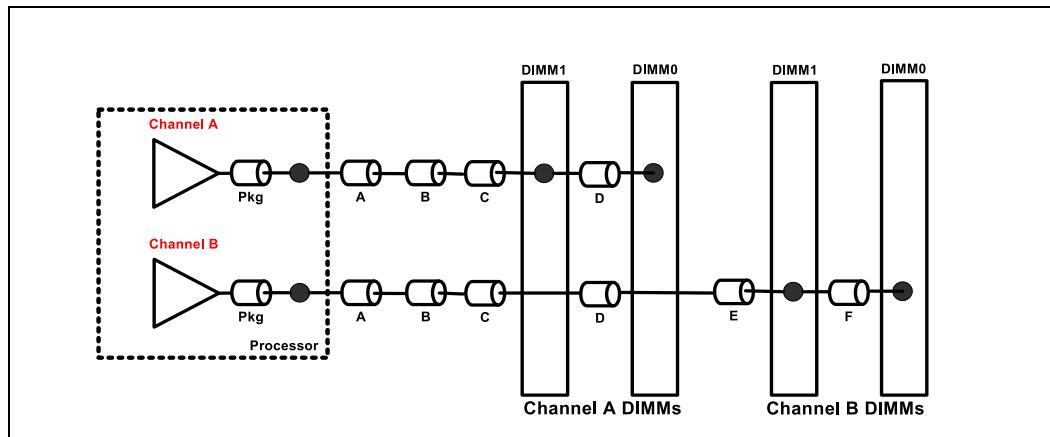


Table 3-5. Data Group Routing Guidelines

Table 3-5. Data Group Routing Guidelines

Routing Parameters	Channel A Details				Channel B Details						Units	Notes
	A	B	C	D	A	B	C	D	E	F		
Minimum Trace Spacing If Die-To-DIMM1 Length < 3.0" If Die-To-DIMM1 Length ≥ 3.0"	4.0 4.0	10.0 10.0	15.0 20.0	15.0 20.0	4.0 4.0	10.0 10.0	20.0 20.0	20.0 20.0	20.0 20.0	20.0 20.0	mils mils	3,4,5,6
Maximum Trace Length per Region	200	500	4000	500	200	500	4000	500	1500	500	mils	
Ball to Via Maximum Length	50				50						mils	2
DQS/DQS# Differential Spacing	4.0	5.0	5.0	5.0	4.0	5.0	5.0	5.0	5.0	5.0	mils	7
Minimum Serpentine Spacing If Die-To-DIMM1 Length < 3.0" If Die-To-DIMM1 Length ≥ 3.0"	n/a n/a	n/a n/a	15.0 20.0	15.0 20.0	n/a n/a	n/a n/a	20.0 20.0	20.0 20.0	20.0 20.0	20.0 20.0	mils mils	8
Minimum Isolation Spacing	4.0	10.0	20.0	20.0	4.0	10.0	20.0	20.0	20.0	20.0	mils	4,5,6,9
Minimum Channel to Channel Spacing	n/a	10.0	20.0	20.0	n/a	10.0	20.0	20.0	20.0	20.0	mils	10,11
Length and Matching Rules	Channel A Details				Channel B Details						Units	Notes
	Die To DIMM1	Die To DIMM0	Die To DIMM1		Die To DIMM0							
Byte Group [0] Total Length	2700 to 4200	3000 to 4600	3600 to 5100		3900 to 5500						mils	12
Byte Group [1] Total Length	2700 to 4200	3000 to 4600	3100 to 4600		3400 to 5000						mils	12
Byte Group [2] Total Length	2200 to 3600	2500 to 4100	3100 to 4500		3400 to 5000						mils	12
Byte Group [3] Total Length	2200 to 3500	2500 to 4000	2600 to 4100		2900 to 4500						mils	12
Byte Group [4] Total Length	2200 to 3500	2500 to 4000	2600 to 4100		2900 to 4500						mils	12
Byte Group [5] Total Length	2200 to 3500	2500 to 4000	3400 to 4500		3700 to 5000						mils	12
Byte Group [6] Total Length	2700 to 4200	3000 to 4600	3600 to 5100		3900 to 5500						mils	12
Byte Group [7] Total Length	3200 to 4200	3500 to 4600	3600 to 5100		3900 to 5500						mils	12
Byte Group [8] (ECC) Total Length	2100 to 3500	2400 to 4000	2600 to 4100		2900 to 4500						mils	12
Byte[X] (max - min), X = 0 to 8	0 to 15	0 to 15	0 to 15		0 to 15						mils	12,13
DIMM CK/CK# - DQS/DQS#[0]	-1000 to 0	-1000 to 0	-1000 to 0		-1000 to 0						mils	12, 14
DIMM CK/CK# - DQS/DQS#[1]	-1000 to 0	-1000 to 0	-500 to 500		-500 to 500						mils	12, 14
DIMM CK/CK# - DQS/DQS#[2]	-500 to 500	-500 to 500	-500 to 500		-500 to 500						mils	12, 14
DIMM CK/CK# - DQS/DQS#[3]	-500 to 500	-500 to 500	0 to 1000		0 to 1000						mils	12, 14
DIMM CK/CK# - DQS/DQS#[4]	-500 to 500	-500 to 500	0 to 1000		0 to 1000						mils	12, 14
DIMM CK/CK# - DQS/DQS#[5]	-500 to 500	-500 to 500	-800 to 200		-800 to 200						mils	12, 14
DIMM CK/CK# - DQS/DQS#[6]	-1000 to 0	-1000 to 0	-1000 to 0		-1000 to 0						mils	12, 14
DIMM CK/CK# - DQS/DQS#[7]	-1500 to -500	-1500 to -500	-1000 to 0		-1000 to 0						mils	12, 14
DIMM CK/CK# - DQS/DQS#[8]	-400 to 600	-400 to 600	0 to 1000		0 to 1000						mils	12, 14

Notes:

- For single memory channel platform designs the un-used channel data group signals must be left as no connects.
- If necessary the Channel A byte group 4 can be routed on layer 4, but all the signals within byte 4 must transition and route together on the same layer.
- Trace Spacing refers to the minimum trace-to-trace spacing between the data group signals.
- Adjacent data bus signals from different bytes within the same channel must route their Region A for no more than 80 mils maximum and their Region B must route for no more than 200 mils maximum.
- For data bus signals that route next to a clock signal Region A is not allowed and Region B must route for no more than 30 mils maximum.
- For data bus signals that route next to a Command/Address/Control signal Region A must route for no more than 70 mils maximum and Region B must route for no more than 400 mils maximum.
- Differential Spacing is identified as the trace spacing between a data strobe Sx_DQS[n] signal and its compliment Sx_DQS#[n].

8. Serpentine Spacing, also known as self spacing, is the minimum distance required from a data group signal to itself when it serpentines on the motherboard. Data group signal serpentine routing in Region A or Region B is not recommended.
9. Isolation Spacing is the minimum distance required between the data group signals and signals from the control and command/address signal groups. Data group signal to clock group signal isolation spacing requirements are defined in [Table 3-3](#).
10. Minimum Channel to Channel Spacing is the minimum distance required between data group signals from different channels routed adjacent to one another.
11. Adjacent data bus signals from different channels must not route a Region A and Region B must route for no more than 60 mils maximum.
12. Length and matching rules include the processor package length + motherboard trace length (Die-To-DIMM, Die-To-DIMM0).
13. Byte[X] refers to the DQ/DM/CB/DQS/DQS# signals within the byte groups 0 to 8 (ECC)
14. DIMM CK/CK# refers to the DIMM specific CK/CK# differential pairs. CK/CK#[3:2] are the DIMM1 clock pairs and CK/CK#[1:0] are the DIMM0 clock pairs.

3.2.5 Control Group Signals

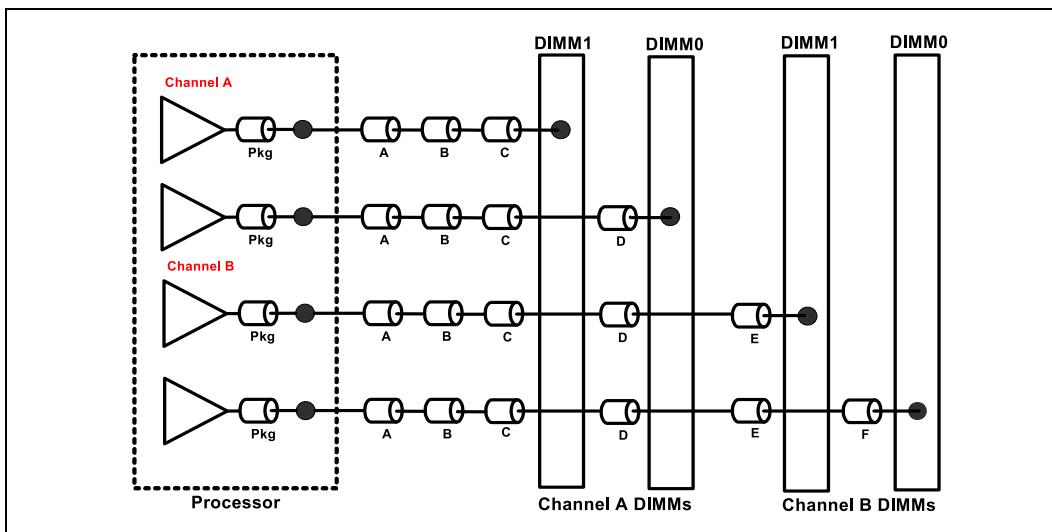
The control signal group includes twelve total signals per channel. The memory controller provides one chip select, one clock enable, and one On-Die Termination (ODT) control signal per DIMM rank. [Table 3-6](#) summarizes the control signal mapping.

Table 3-6. Control Signal Mapping

Control Signals	Channel	DIMM Rank	System Rank	DIMM Connector
SA_CS#[2], SA_CKE[2], SA_ODT[2]	A	0	2	1
SA_CS#[3], SA_CKE[3], SA_ODT[3]		1	3	1
SA_CS#[0], SA_CKE[0], SA_ODT[0]		0	0	0
SA_CS#[1], SA_CKE[1], SA_ODT[1]		1	1	0
SB_CS#[2], SB_CKE[2], SB_ODT[2]	B	0	2	1
SB_CS#[3], SB_CKE[3], SB_ODT[3]		1	3	1
SB_CS#[0], SB_CKE[0], SB_ODT[0]		0	0	0
SB_CS#[1], SB_CKE[1], SB_ODT[1]		1	1	0

The diagrams and table below depict the recommended topology and layout routing guidelines for the control group signals.

Note that the processor SA_CS#[7:4] and SB_CS#[7:4] signals are not used and as a result these processor signals should be left as no connects.

Figure 3-3. Control Group Signal Routing Topology**Table 3-7. Control Group Routing Guidelines**

Routing Parameters	Channel A Details				Channel B Details						Units	Notes
	A	B	C	D	A	B	C	D	E	F		
Signal Reference	VCCSM				VCCSM							
Motherboard Layer	1	1	1	1	1	1	1	1	1	1		
Single-Ended Trace Impedance		36	36			36	36				Ohms	
Impedance Tolerance		±15	±15			±15	±15				%	
Trace Width	4.0	8.0	8.0	6.5	4.0	8.0	8.0	6.5	6.5	6.5	mils	2
Minimum Trace Spacing	4.0	4.0	9.0	4.5	4.0	4.0	9.0	4.5	9.0	4.5	mils	2, 3
Maximum Trace Length per Region	400	400	2300	500	400	400	2000	1000	1500	500	mils	
Minimum Serpentine Spacing	n/a	n/a	9.0	4.5	n/a	n/a	9.0	4.5	9.0	4.5	mils	4
Minimum Isolation Spacing	4.0	4.0	9.0	4.5	4.0	4.0	9.0	4.5	9.0	4.5	mils	5
Length and Matching Rules	Channel A Details				Channel B Details						Units	Notes
	Die To DIMM1	Die To DIMM0	Die To DIMM1	Die To DIMM0								
Control Signal Total Length	2100 to 3400	2300 to 3600	2900 to 4200	3200 to 4500							mils	6
DIMM CK/CK# - Control Signal	200 to 600	0 to 400	300 to 700	0 to 400							mils	5, 7
CS#/ODT[3] (max - min)	0 to 10	n/a	0 to 10	n/a							mils	5
CS#/ODT[2] (max - min)	0 to 10	n/a	0 to 10	n/a							mils	5
CS#/ODT[1] (max - min)	n/a	0 to 10	n/a	0 to 10							mils	5
CS#/ODT[0] (max - min)	n/a	0 to 10	n/a	0 to 10							mils	5

Notes:

- For single DIMM connector per channel or single memory channel platform designs the un-used associated DIMM rank control group signals must be left as no connects.
- As the first DIMM (DIMM1) control signals route to their DIMM1 pins if needed they may route with 6.5 mil trace width and minimum of 4.5 mil trace spacing for no more than 500mils.
- Trace Spacing refers to the minimum trace-to-trace spacing between the control group signals.
- Serpentine Spacing, also known as self spacing, is the minimum distance required from a control group signal to itself when it serpentine on the motherboard. Control group signal serpentine routing in Region A or Region B is not recommended.
- Isolation Spacing is the minimum distance required between the control group signals and signals from the command/address signal group. Control group signal to data group signal isolation spacing requirements are defined in Table 3-5.

Processor – Memory Interface and DDR3 DIMMs

6. Length and matching rules include the processor package length + motherboard trace length (Die-To-DIMM1, Die-To-DIMM0).
7. DIMM CK/CK# refers to the DIMM specific CK/CK# differential pairs. CK/CK#[3:2] are the DIMM1 clock pairs and CK/CK#[1:0] are the DIMM0 clock pairs.

3.2.6 Command/Address Group Signals

The command/address signal group includes twenty-two total signals per channel. The memory controller drives the command and address signals to every DRAM device within a channel.

The diagrams and table below depict the recommended topology and layout routing guidelines for the command/address group signals.

Figure 3-4. Command/Address Group Signal Routing Topology

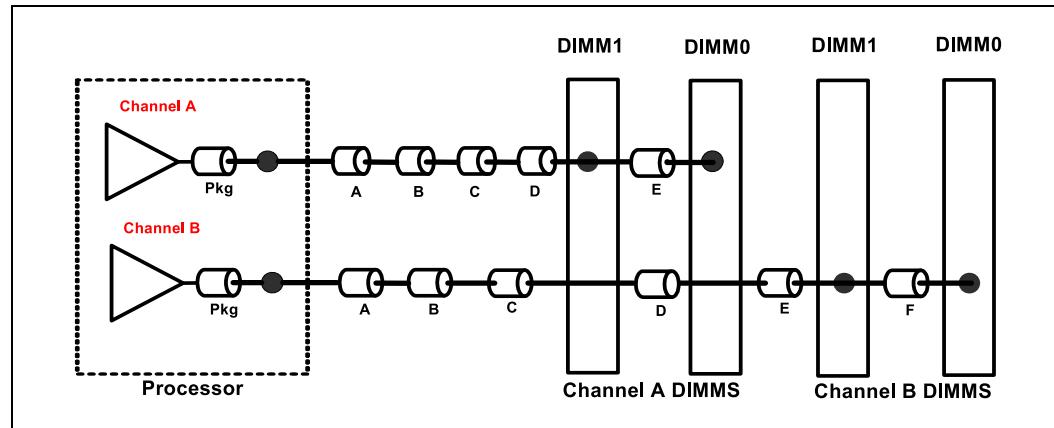


Table 3-8. Command/Address Group Routing Guidelines

Routing Parameters	Channel A Details					Channel B Details						Units	Notes
	A	B	C	D	E	A	B	C	D	E	F		
Signal Reference	VCCSM					VCCSM							
Motherboard Layer	1	1	1	1	1	1	1	1	1	1	1		
Single-Ended Trace Impedance		32	32				32	32				Ohms	
Impedance Tolerance		±15	±15				±15	±15				%	
Trace Width	4.0	9.5	9.5	6.5	5.0	4.0	9.5	9.5	6.5	6.5	5.0	mils	
Minimum Trace Spacing	4.0	4.0	5.5	4.5	6.0	4.0	4.0	5.5	4.5	6.0	6.0	mils	2
Maximum Trace Length per Region	400	400	2000	(D+E)<500		400	400	2000	1000	1500	500	mils	
Minimum Serpentine Spacing	n/a	n/a	5.5	4.5	6.0	n/a	n/a	5.5	4.5	6.0	6.0	mils	3
Minimum Isolation Spacing	4.0	4.0	9.0	4.5	6.0	4.0	4.0	9.0	4.5	9.0	6.0	mils	4
Length and Matching Rules	Channel A Details					Channel B Details						Units	Notes
	Die To DIMM1		Die To DIMMO		Die To DIMM1		Die To DIMMO						
Command/Address Signal Total Length	1700 to 3300		2000 to 3600		2600 to 4100		3000 to 4500						5
DIMM CK/CK# - Command/Address Signal	300 to 1000		0 to 700		400 to 1000		0 to 600						5, 6

Notes:

1. For single memory channel platform designs the un-used channel command/address group signals must be left as no connects.

2. Trace Spacing refers to the minimum trace-to-trace spacing between the command/address group signals.
3. Serpentine Spacing, also known as self spacing, is the minimum distance required from a command/address group signal to itself when it serpentine on the motherboard. Command/Address group signal serpentine routing in Region A or Region B is not recommended.
4. Isolation Spacing is the minimum distance required between the command/address group signals and signals from the control signal group. Command/Address group signal to data group signal isolation spacing requirements are defined in [Table 3-5](#).
5. Length and matching rules include the processor package length + motherboard trace length (Die-To-DIMM1, Die-To-DIMM0).
6. DIMM CK/CK# refers to the DIMM specific CK/CK# differential pairs. CK/CK#[3:2] are the DIMM1 clock pairs and CK/CK#[1:0] are the DIMM0 clock pairs.

3.2.7 Miscellaneous Signal Group

3.2.7.1 Resistive Compensation

The memory controller uses the compensation signals to determine, check, and adjust the system memory buffer pull-up and pull-down output impedance characteristics for both channels over temperature, process, and voltage variations by comparing the buffer impedance against a standard reference resistor.

The diagrams and table below depict the recommended topology and layout routing guidelines for the resistive compensation signals.

Figure 3-5. SM_RCOMP[2:0] Resistive Compensation Circuits

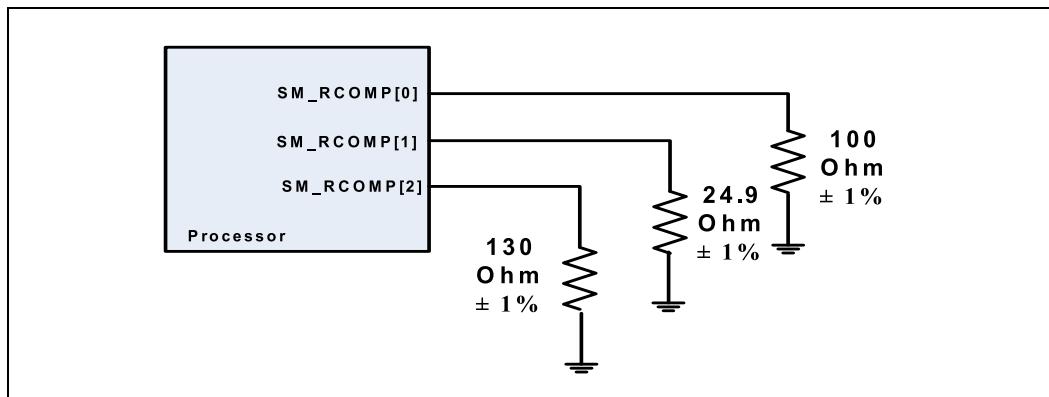
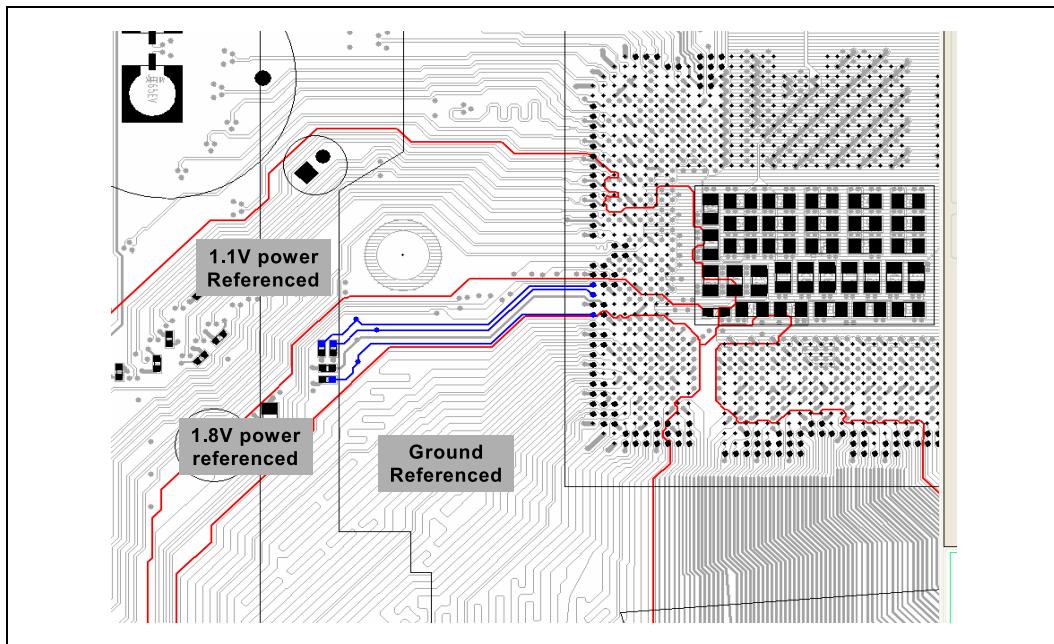


Figure 3-6. SM_RCOMP[2:0] Resistive Compensation Signal Example Routing**Table 3-9. SM_RCOMP[2:0] Resistive Compensation Signal Routing Guidelines**

Routing Parameters	Details	Units	Notes
Signal Reference	Power or Ground		1
Motherboard Layer	1		
Trace Width	8	mils	
Motherboard Break-Out Details:			
Minimum Trace Spacing	10	mils	2
Maximum Trace Length	500	mils	
Motherboard Main Route Details:			
Minimum Trace Spacing	15	mils	2
Maximum Trace Length	1300	mils	
Maximum Motherboard Trace Length (Break-Out + Main Route)	1300	mils	

Notes:

1. Signal reference can be power or ground. All compensation signals must maintain the same referencing and not cross plane splits. Routing on layer one referenced to 1.8V is the optimal design.
2. Trace Spacing refers to the minimum trace-to-trace spacing between the resistive compensation signals and other neighboring signals.

3.2.7.2 System Memory Reference Voltage

The system memory reference voltage is used by the DDR3 DRAM devices to compare the input signal levels of the data, command/address, and control group signals. There are a total of four DDR3 reference voltages that are required:

- Channel A VREFDQ (DIMM pin 1) and VREFCA (DIMM pin 67)
- Channel B VREFDQ (DIMM pin 1) and VREFCA (DIMM pin 67)

VREFCA is generated by two fixed voltage resistor dividers (one for Channel A and one for Channel B) located on the motherboard near the DIMM connectors. See [Figure 3-7](#) and [Table 3-10](#) for VREFCA topology and layout routing guidelines.

VREFDQ is generated by multiple methods to provide increased flexibility for fine tuning the VREFDQ levels and to optimize the data group voltage and timing margins.

For One DIMM Per Channel Platform Designs:

- See [Figure 3-8](#), [Table 3-11](#), and [Table 3-12](#) for VREFDQ topology and layout routing guidelines

For Two DIMM Per Channel Platform Designs:

- See [Figure 3-9](#), [Table 3-11](#), and [Table 3-12](#) for VREFDQ topology and layout routing guidelines
- Note: Leave programmable DIMM VREFDQ circuit footprints on motherboard next to DIMM connectors
 - Digital potentiometer and op-amp controlled by the Intel® 5 Series Chipset SMBUS.
 - May be required at a later time if validation shows its needed.

To minimize any discontinuity and maximize margin budgets it is recommended but not required that the following guidelines be implemented for VREFCA and VREFDQ:

- If possible route completely referenced to the same plane (VSS or VCC).
- If you can't route referenced to the same plane, if possible place a stitching capacitor near the point of reference plane transition.
- If you transition layers and maintain the same referencing, if possible place a stitching via as close as possible to the point where the signal transitions from one layer to another.

Figure 3-7. System Memory VREFCA Generation Example Circuit

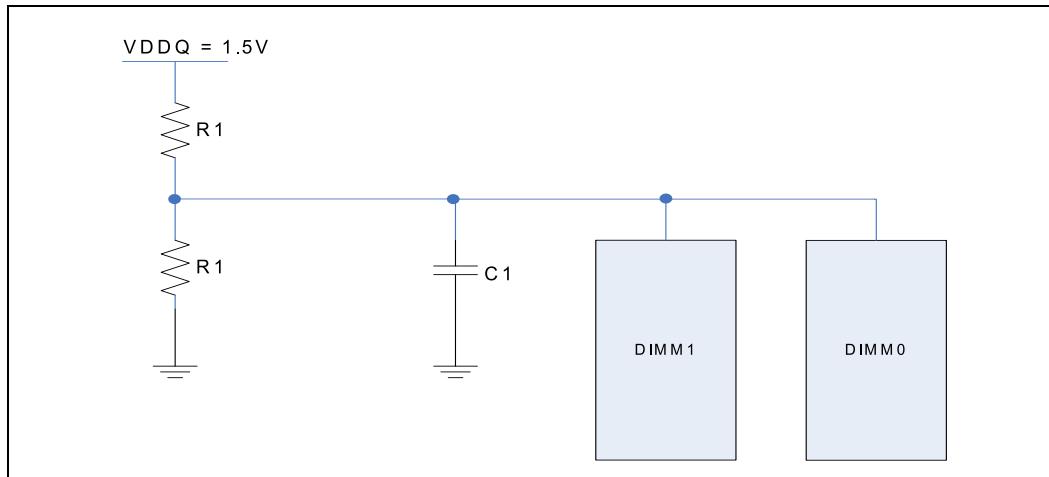


Table 3-10. System Memory VREFCA Routing Guidelines

Routing Parameters	Details	Units	Notes
Signal Reference	Power or Ground		1
Motherboard Layer	1 or 4		
Trace Width	12	mils	

Table 3-10. System Memory VREFCA Routing Guidelines

Routing Parameters	Details	Units	Notes
Minimum Trace Spacing	12	mils	2
Resistor R1	$1\text{ K} \pm 1\%$	Ohms	
Decoupling C1	$0.1\text{ }\mu\text{F}$	Farads	3

Notes:

1. Signal reference can be power or ground. Signals must maintain the same referencing and not cross plane splits.
2. Trace Spacing refers to the minimum trace-to-trace spacing between the Vref signals and other neighboring signals.
3. Suggested decoupling capacitor is a $0.1\mu\text{F}$ 10% tolerance 0402 package surface mount capacitor.

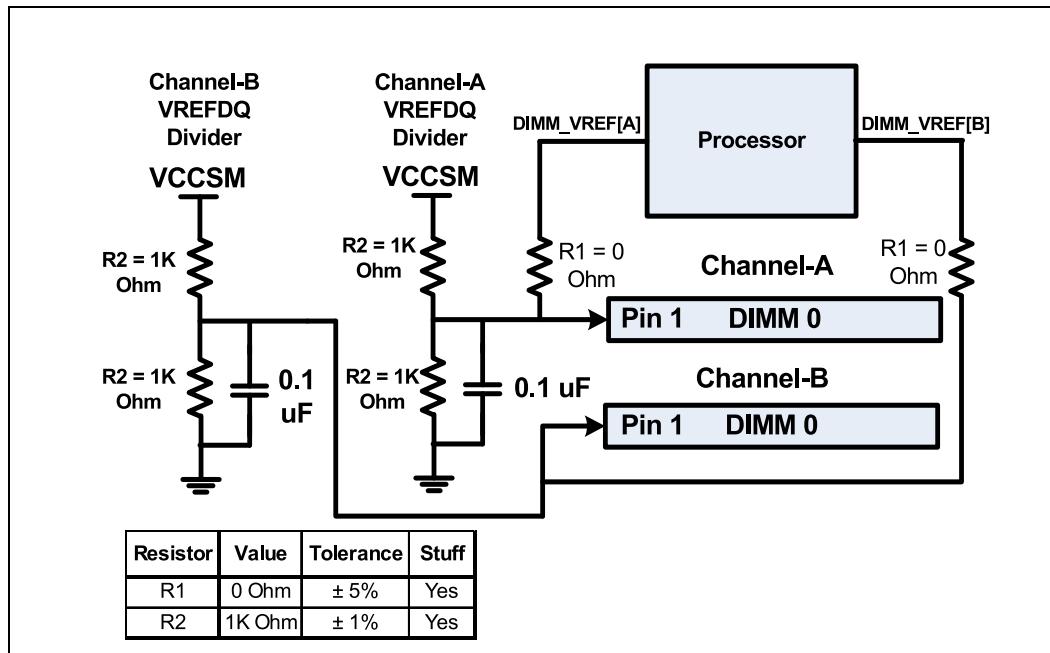
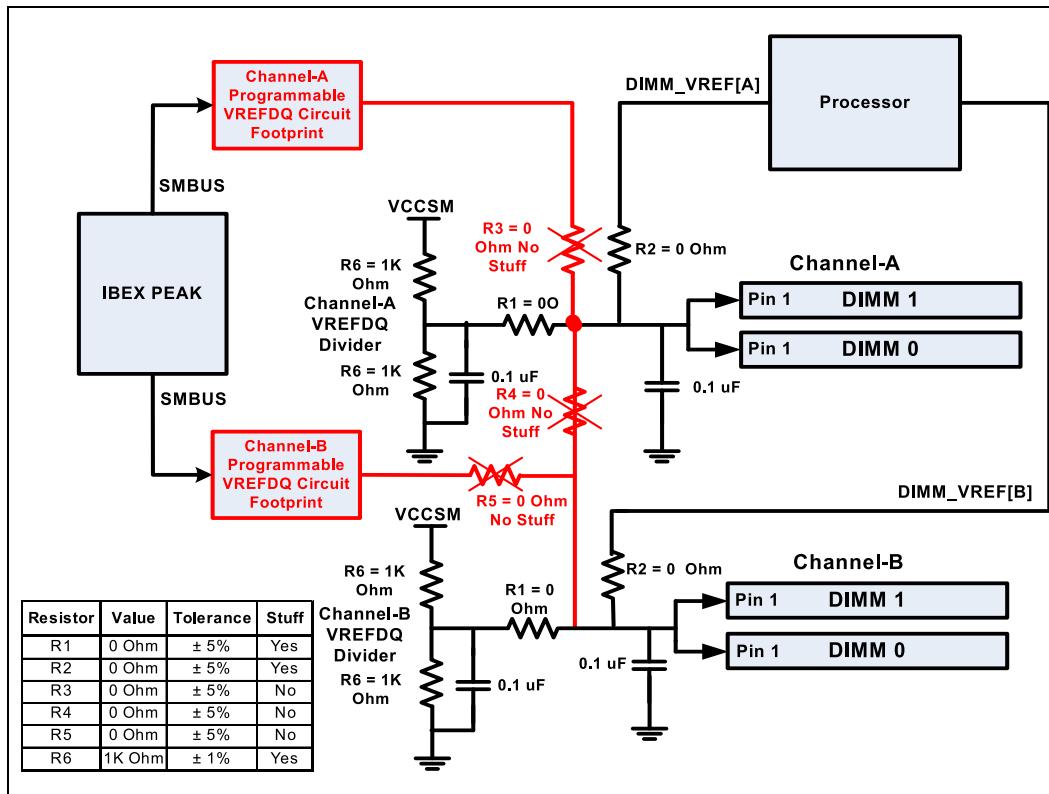
Figure 3-8. VREFDQ Generation Requirement for One DIMM per channel configurations

Figure 3-9. VREFDQ Generation Requirement for Two DIMM per channel configurations**Table 3-11. SA_DIMM_VREFDQ/SB_DIMM_VREFDQ Routing Guidelines**

Routing Parameters	Rule	Units	Notes
Signal Reference	Power or Ground		
Maximum Via Transitions per signal	4		
Minimum Trace Width	4.0	mils	
Break Out Minimum Trace Spacing	4.0	mils	
Maximum Break Out Trace Length	250	mils	
Main Route Minimum Trace Spacing	10.0	mils	1
Minimum Isolation Spacing	20.0	mils	2
Maximum Motherboard Length	5000	mils	

Notes:

1. Trace Spacing refers to the minimum trace-to-trace spacing between the SA_DIMM_VREFDQ and SB_DIMM_VREFDQ signals.
2. Isolation Spacing is the minimum distance required between the SA_DIMM_VREFDQ/ SB_DIMM_VREFDQ signals and other signals.

Table 3-12. System Memory Voltage Divider VREFDQ Routing Guidelines

Routing Parameters	Details	Units	Notes
Signal Reference	Power or Ground		1
Motherboard Layer	1 or 4		
Trace Width	12	mils	
Minimum Trace Spacing	12	mils	2

Notes:

1. Signal reference can be power or ground. Signals must maintain the same referencing and not cross plane splits.
2. Trace Spacing refers to the minimum trace-to-trace spacing between the Vref signals and other neighboring signals.

3.2.7.3 DDR3 System Memory Reset

The processor's integrated memory controller asserts SM_DRAMRST# signal to the DIMMs to reset the DDR3 DRAM devices as the system memory voltage plane is ramping or power cycling. The SM_DRAMRST# signal must be connected to all of the the DDR3 DIMM RESET# signals (DIMM pin 168).

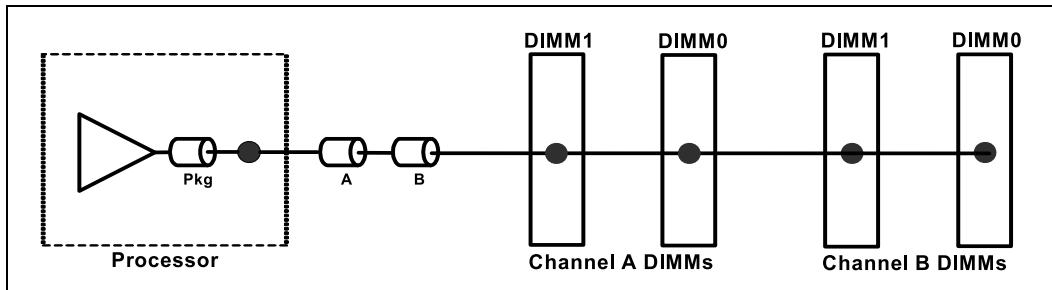
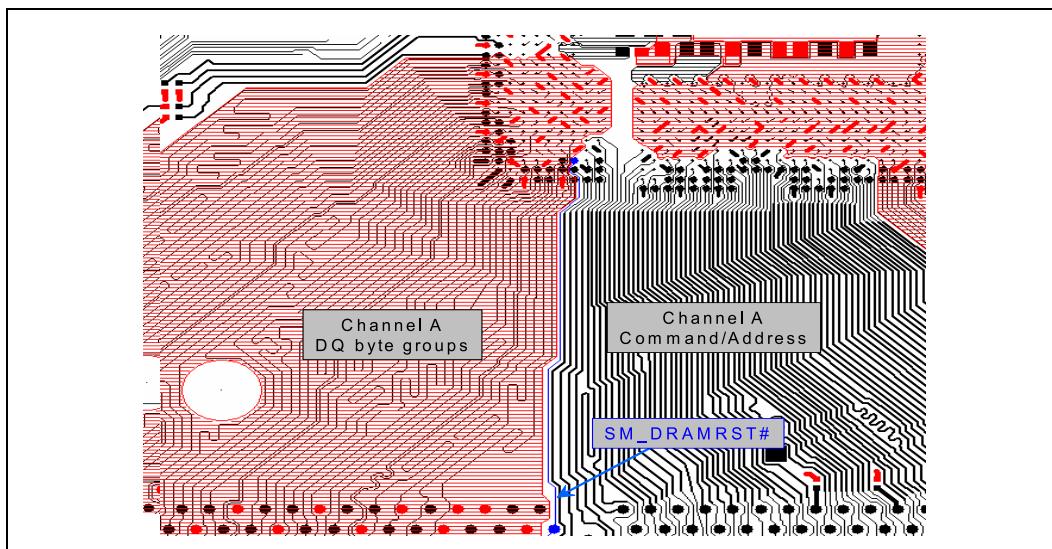
Figure 3-10. DIMM System Memory Reset (SM_DRAMRST#) Signal Routing Topology**Figure 3-11. DDR3 System Memory Reset Example Routing**

Table 3-13. DIMM System Memory Reset (SM_DRAMRST#) Routing Guideline

Routing Parameters	Details		Units	Notes
	Region A	Region B		
Signal Reference	Power	Power		
Motherboard Layer	1	1		
Trace Width	4	4	mils	
Minimum Trace Spacing	4	9 and 20	mils	¹

Notes:

1. Trace Spacing refers to the minimum trace-to-trace spacing between the signal and other signals. In the ball field Region A, 4 mil trace spacing to other layer 1 signals are used. In Region B, 9 mils trace spacing to the adjacent signal SB_CKE[0] is used. In Region B, 20 mils trace spacing to the adjacent signal SA_DQ[27] is used.