

Project : Dashcam Prototype / CPU Board

Revision and Version : 1.0A

Current Released : NA

Table of Content :

Page 1: Cover and Rev History

Page 2: Top Level

Revision History:

02.27.2024 : Starting Design

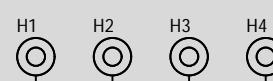
03.02.2024 : Schematics Finished

04.04.2024 : Starting PCB Layout

04.19.2024 : Dashcam CPU PCB Layout Done

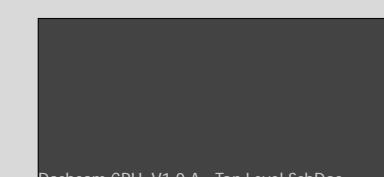
04.19.2024 : Starting with Review it

Mechanicals :



4 mount Holes in the corners
3mm Diameter

Main Schematics :



PCB Des :		
ELIO F.		
Approv By :		
ELIO F.		
Project Title :	Sheet Title :	
Dashcam CPU_V1.0 A.PrjPcb	Cover Page	
Date : 4/19/2024	PCB Version : 1.0	Size : A3
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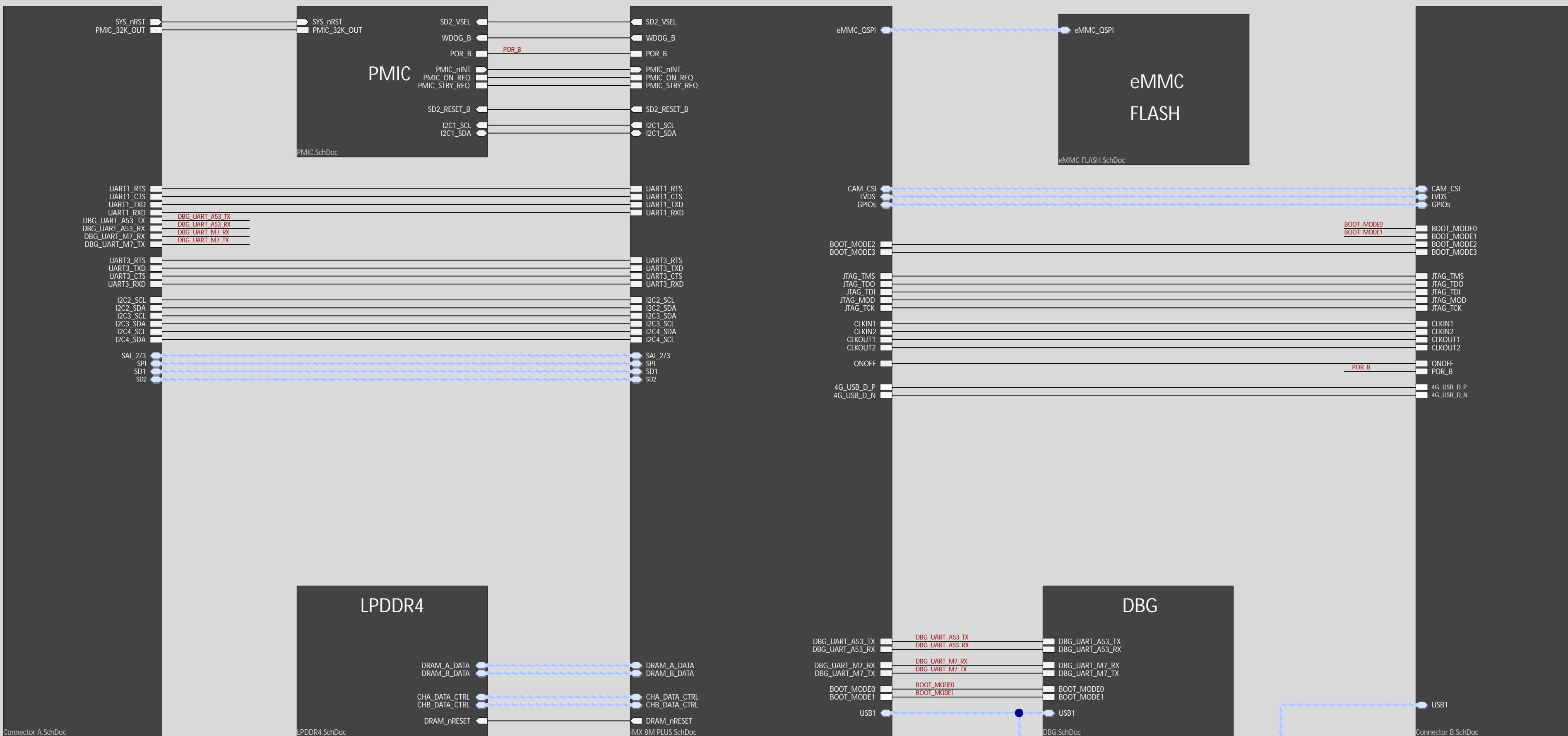
Top Level / Block Diagram

A

Connector A

i.MX 8M Plus

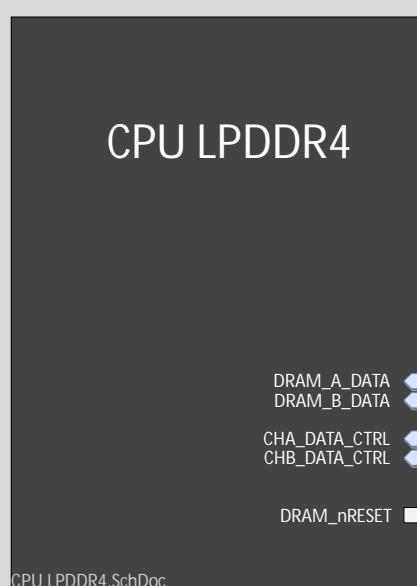
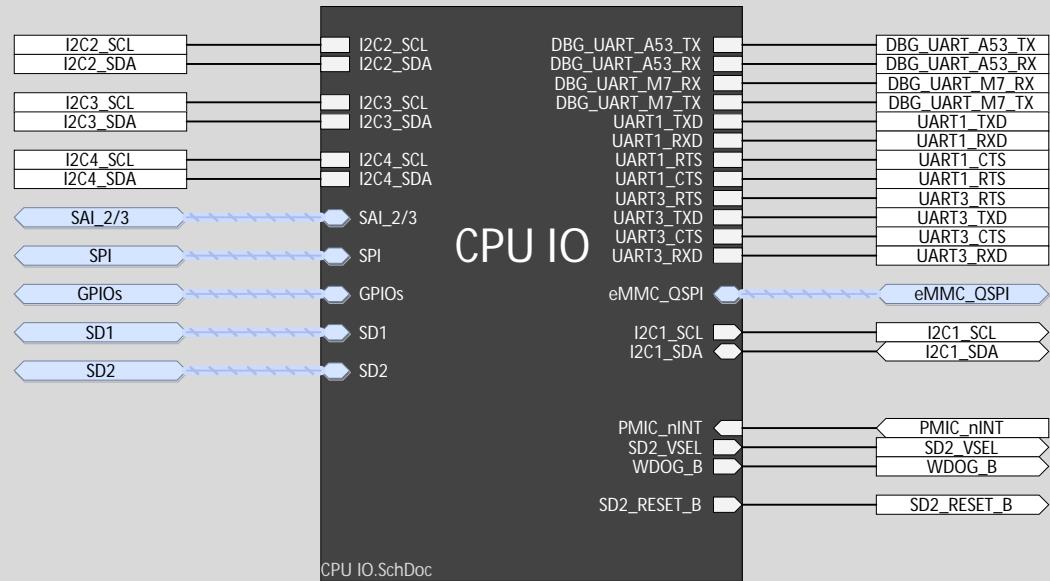
Connector B



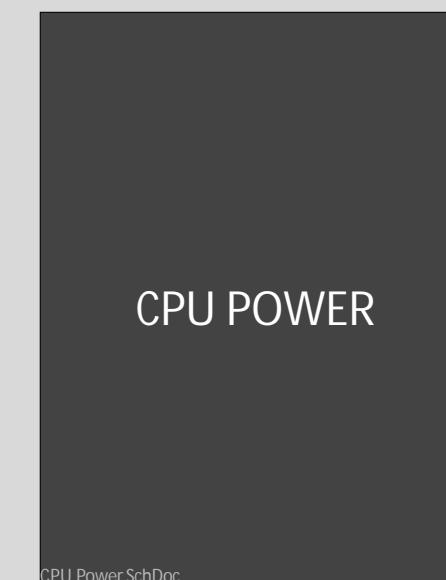
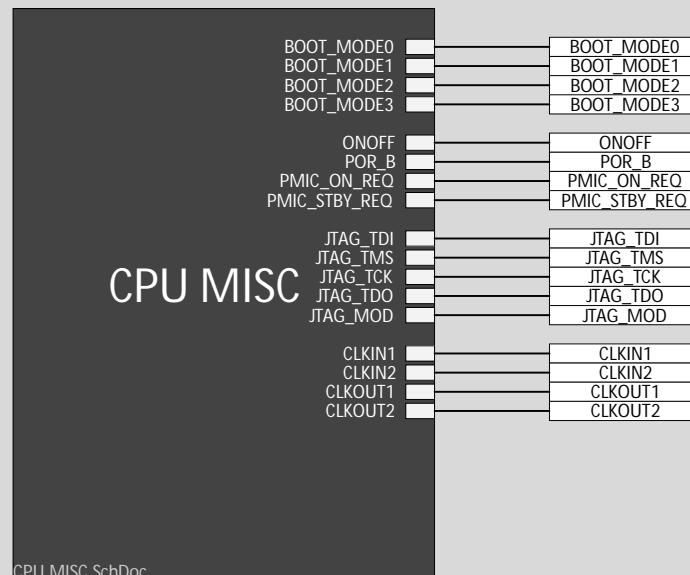
PCB Des :	ELIO F.	
Approv By :	ELIO F.	
Project Title :	Dashcam CPU_V1.0 A PrjPcb	Sheet Title : Top Level
Date :	4/25/2024	PCB Version : 1.0
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		Size : A2

iMX 8M PLUS / Block Diagram

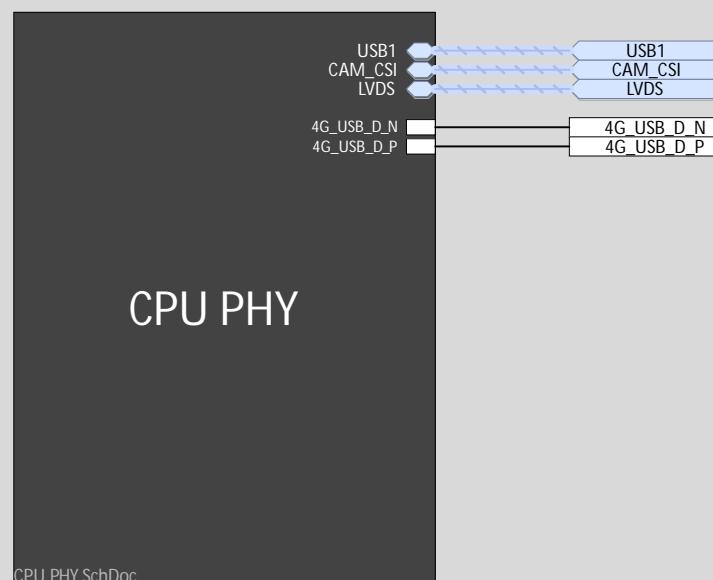
A



B

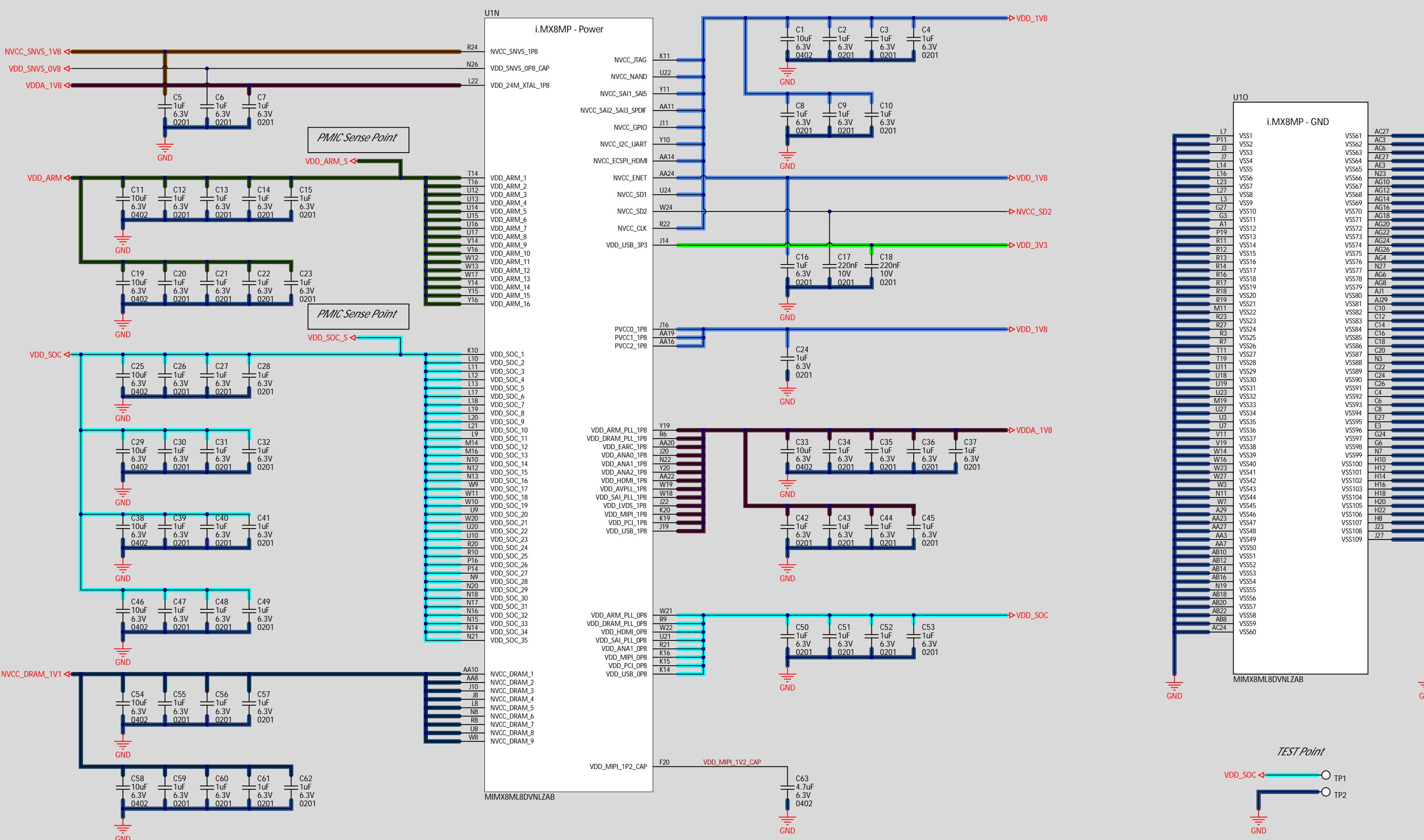


C



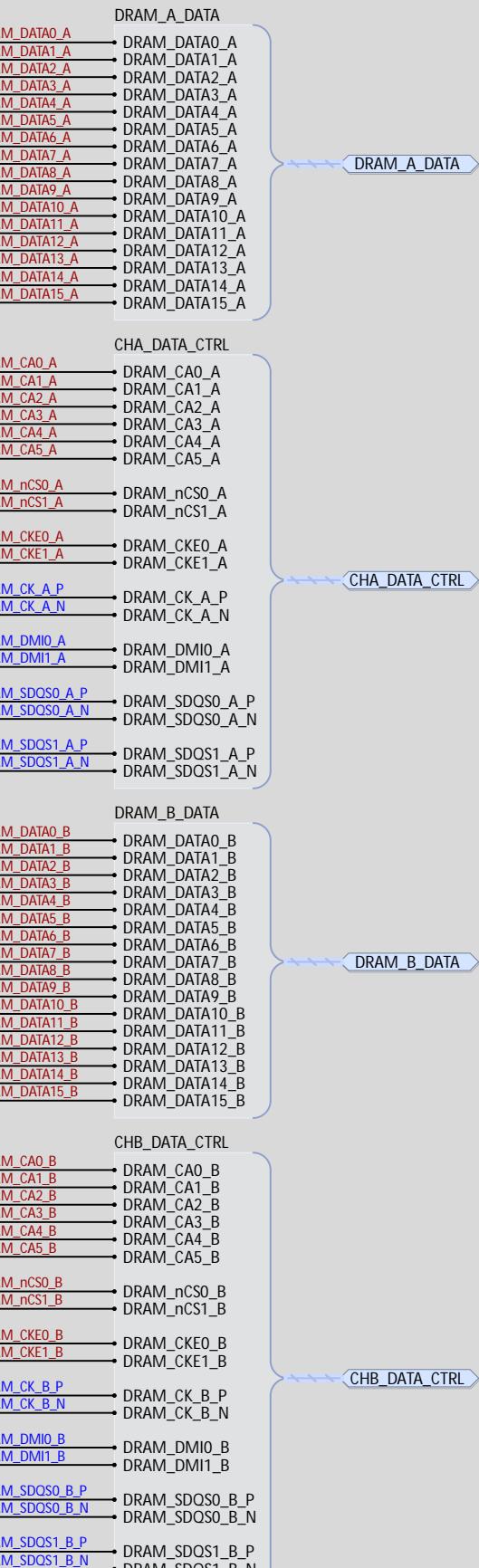
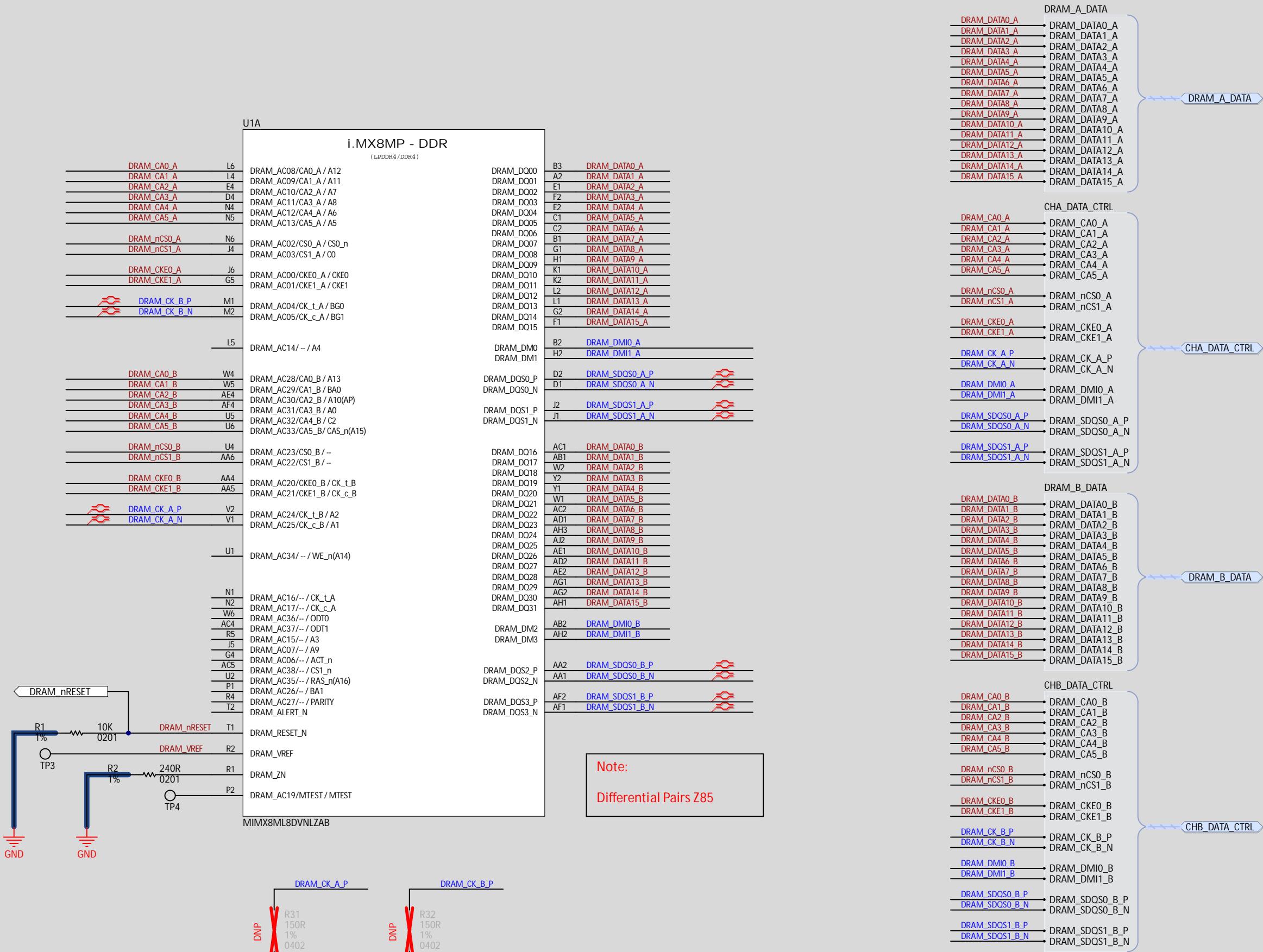
PCB Des :		
ELIO F.		
Approv By :		
ELIO F.		
Project Title :	Sheet Title :	
Dashcam CPU_V1.0.A.PjPcb	'i.MX 8M - BLOCK DIAGRAM	
Date : 4/25/2024	PCB Version : 1.0	Size : A3
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CPU Power

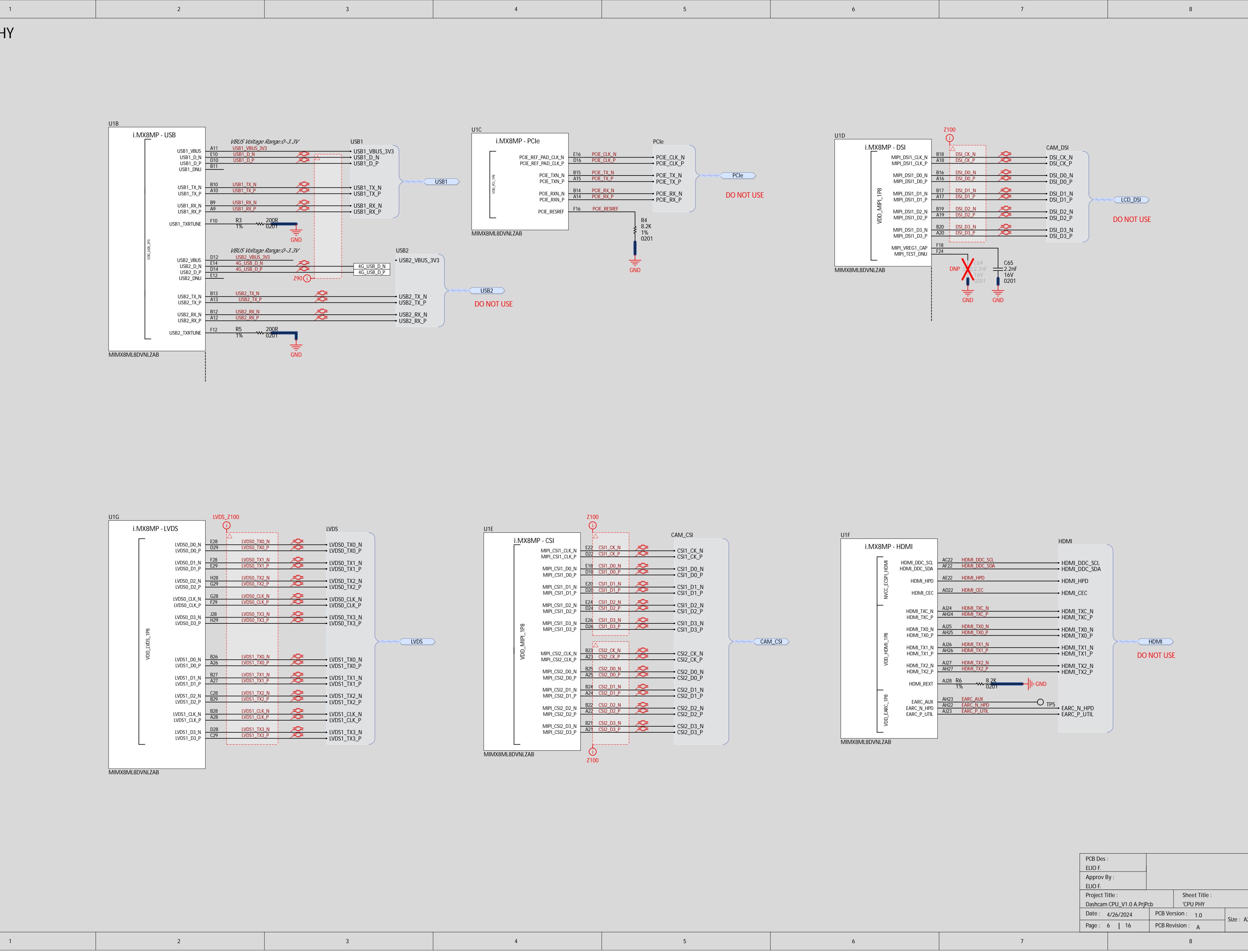


PCB Des :		
ELIO F.		
Approv By :		
ELIO F.	Project Title :	Sheet Title :
	Dashcam CPU_V1.0 A PrjPcb	'CPU POWER
Date : 4/19/2024	PCB Version : 1.0	Size : A2
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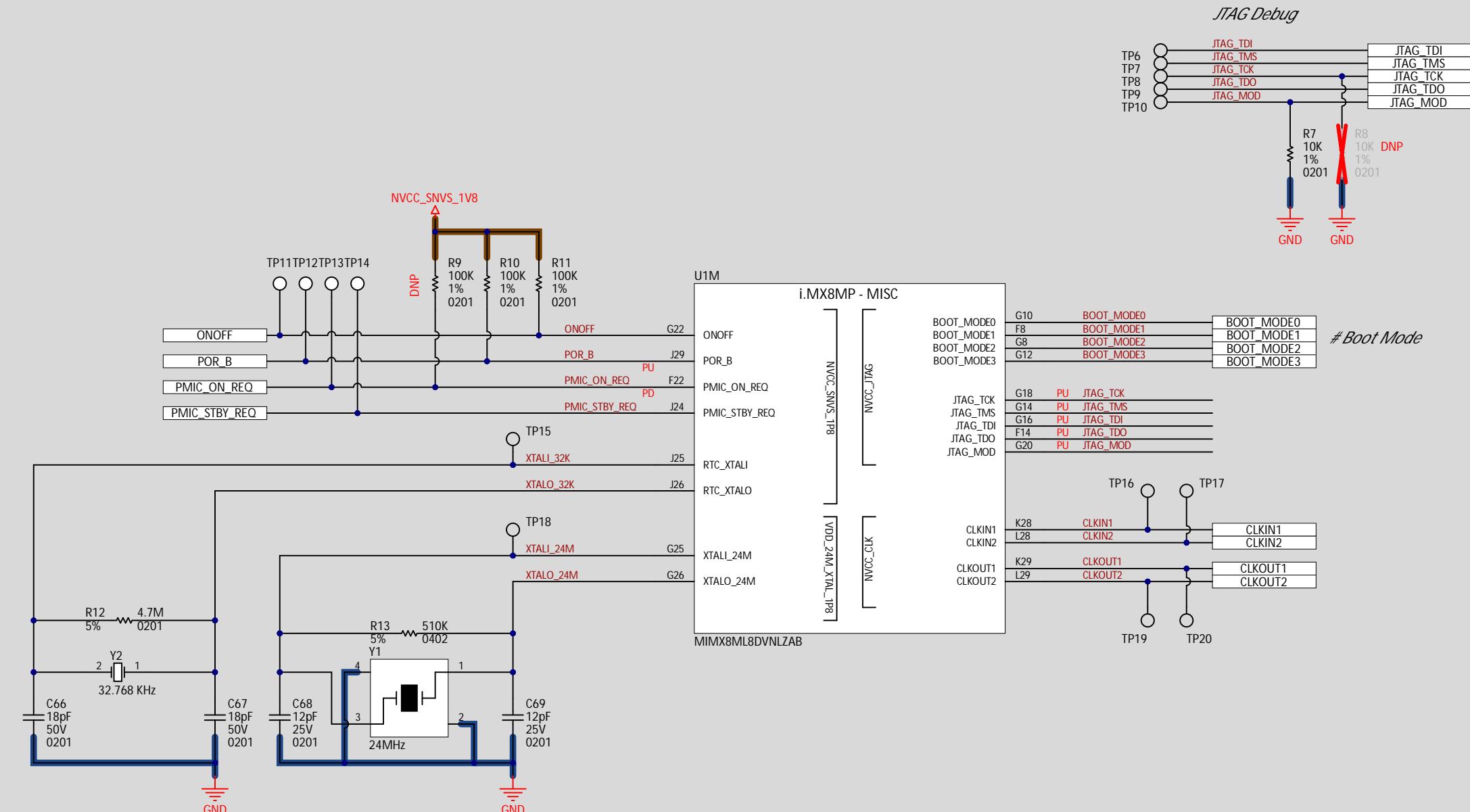
CPU DDR



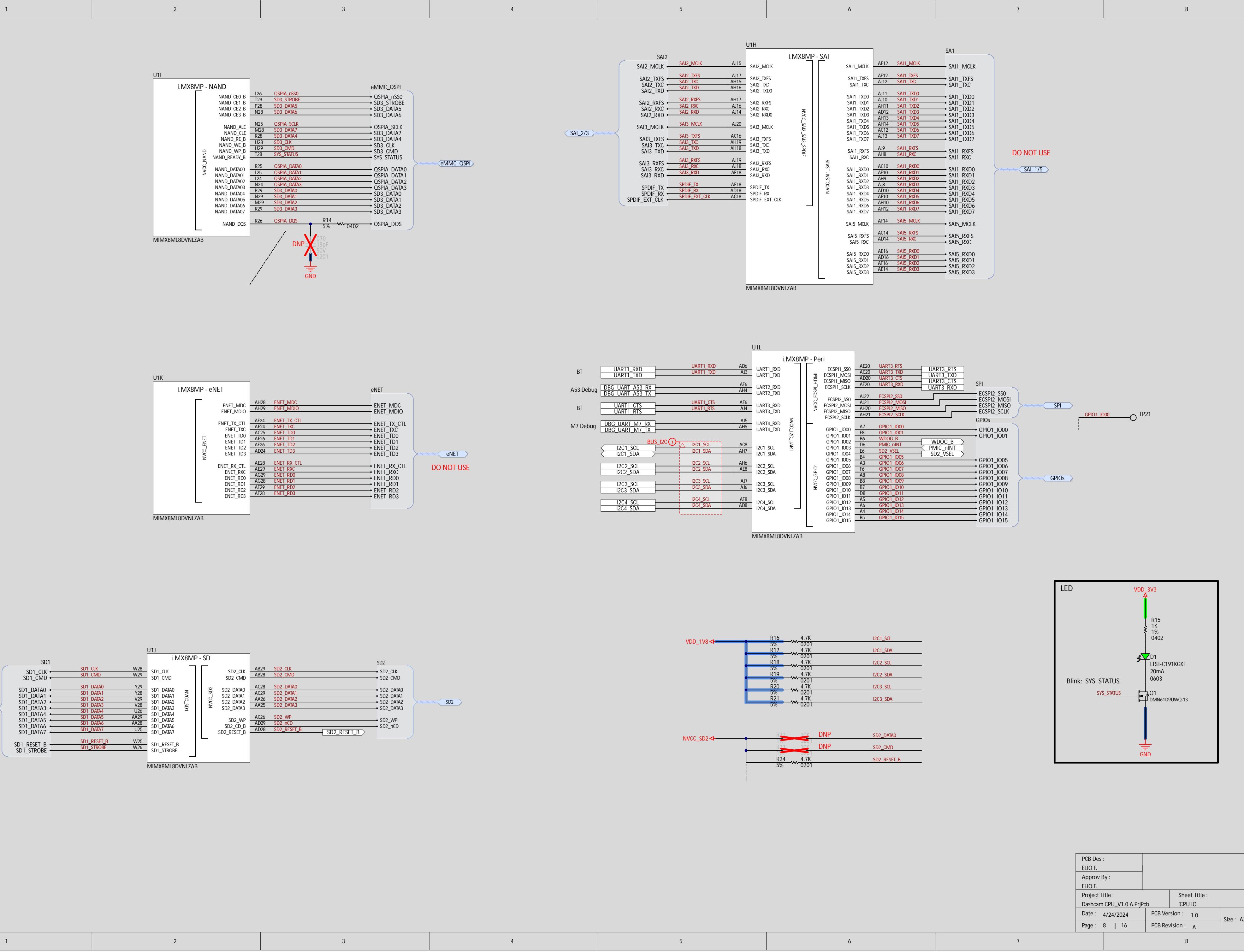
PCB Des :		
ELIO F.		
Approv By :		
ELIO F.		
Project Title :	Sheet Title :	
Dashcam CPU_V1.0 A.PjPcb	'CPU DDR	
Date : 4/19/2024	PCB Version : 1.0	
Page : 5 16	PCB Revision : A	Size : A3



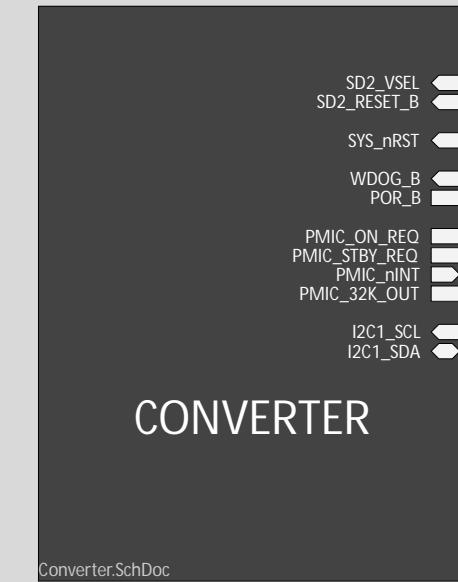
CPU Misc



PCB Des :		
ELIO F.		
Approv By :		
ELIO F.		
Project Title :	Sheet Title :	
Dashcam CPU_V1.0.A.PnjPcb	'CPU MISC	
Date :	4/19/2024	PCB Version : 1.0
Page :	7 16	PCB Revision : A
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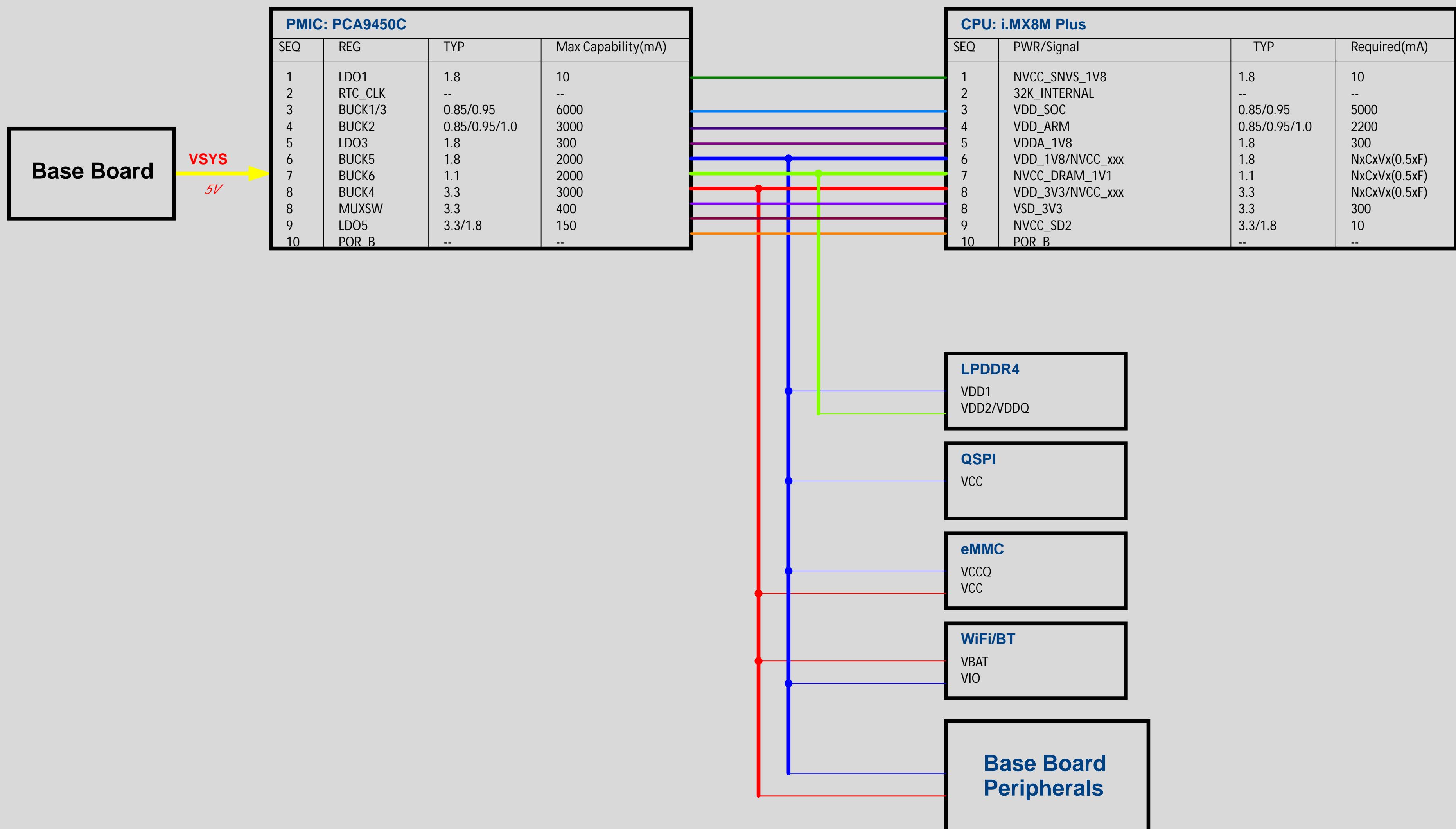


PMIC / Bloack Diagram



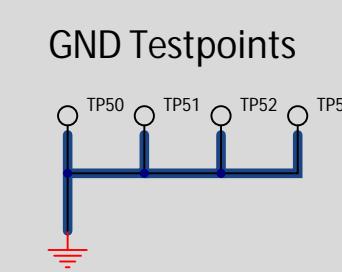
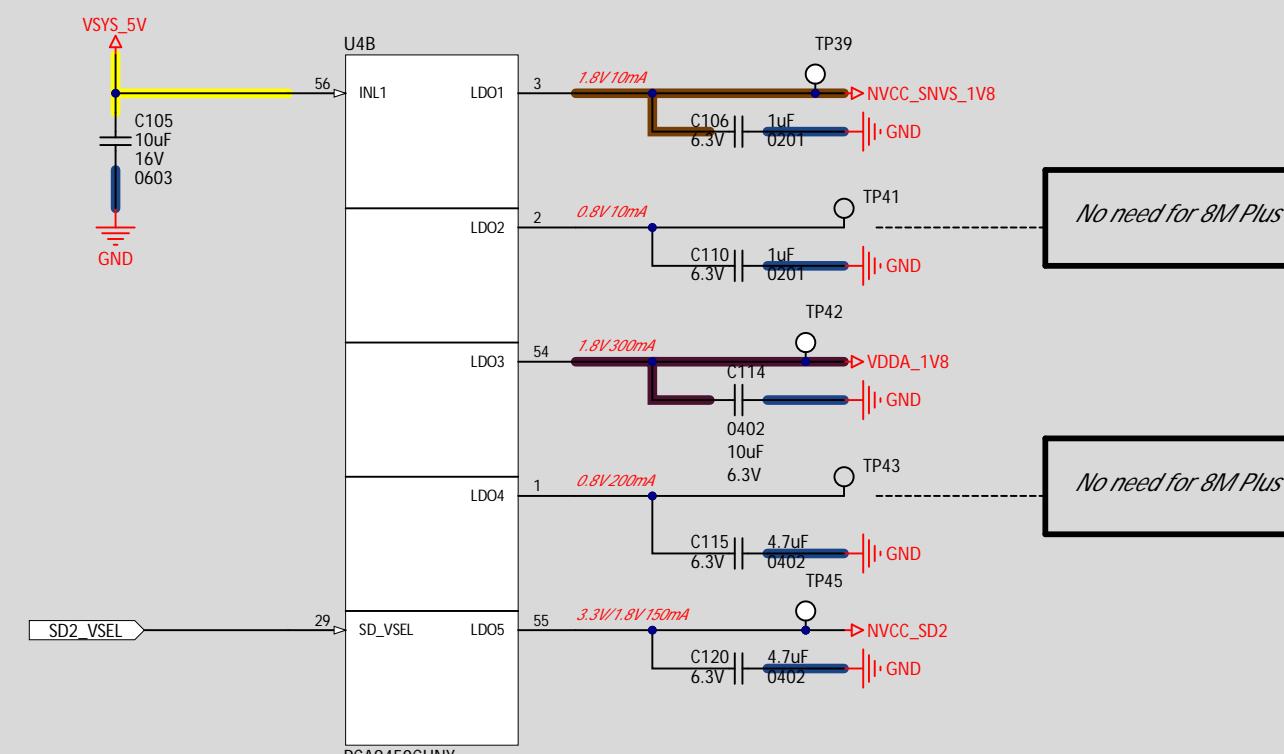
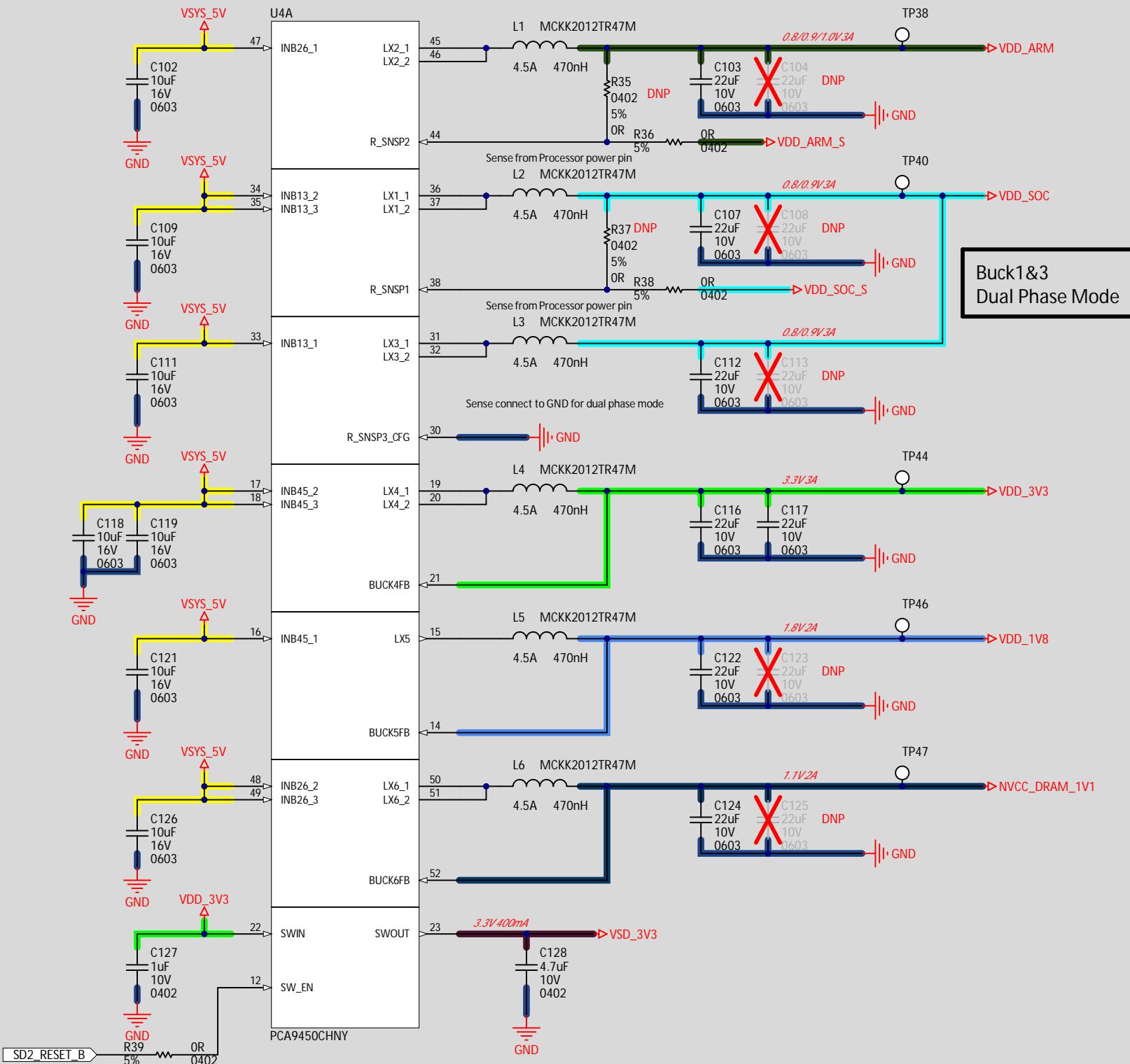
PCB Des :		
ELIO F.		
Approv By :		
ELIO F.		
Project Title :	Sheet Title :	
Dashcam CPU_V1.0 A.PrjPcb	'PMIC - BLOCK DIAGRAM	
Date : 4/19/2024	PCB Version : 1.0	Size : A3
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CPU Power TREE

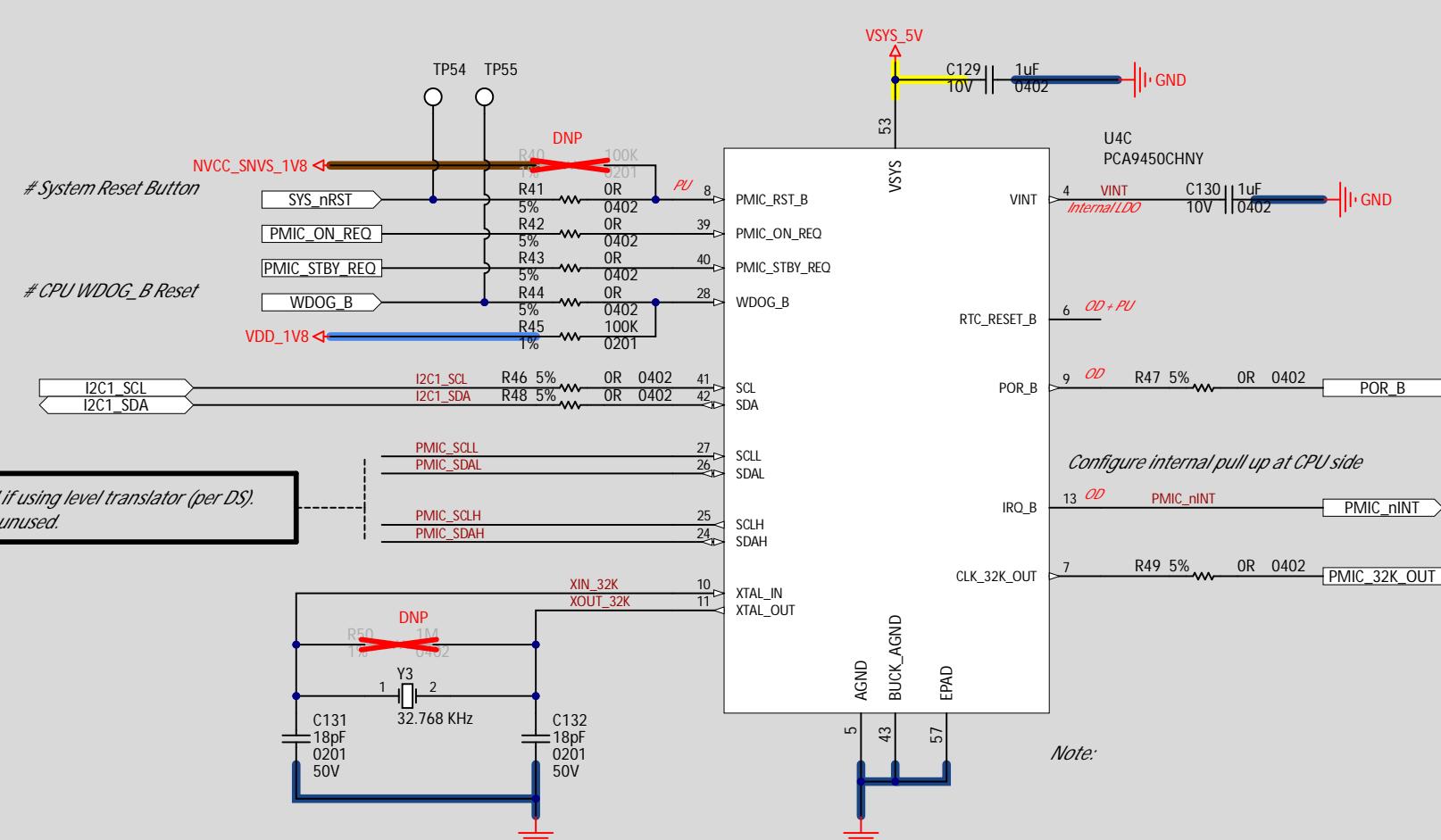
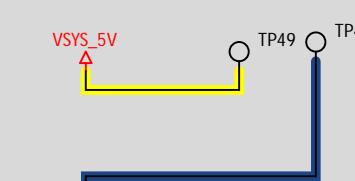


PCB Des :	ELIO F.	Sheet Title :	CPU POWER TREE
Approv By :	ELIO F.		
Project Title :	Dashcam CPU_V1.0_A.PriPcb	PCB Version :	1.0
Date :	4/19/2024	Size :	A2
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Power PMIC / Converter



Backup PWR Supply

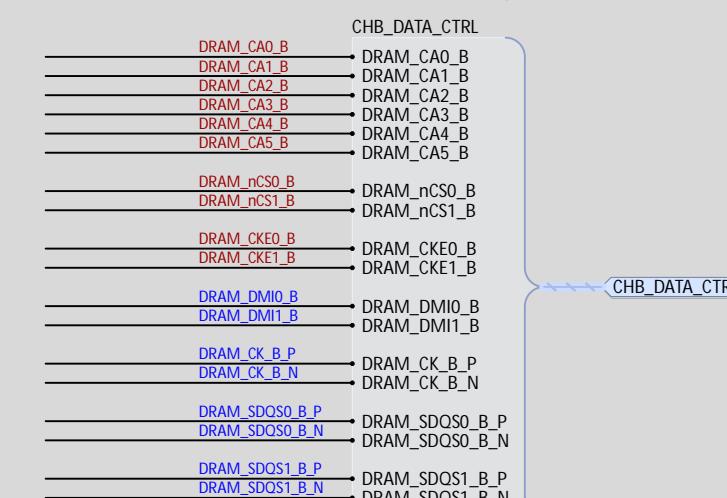
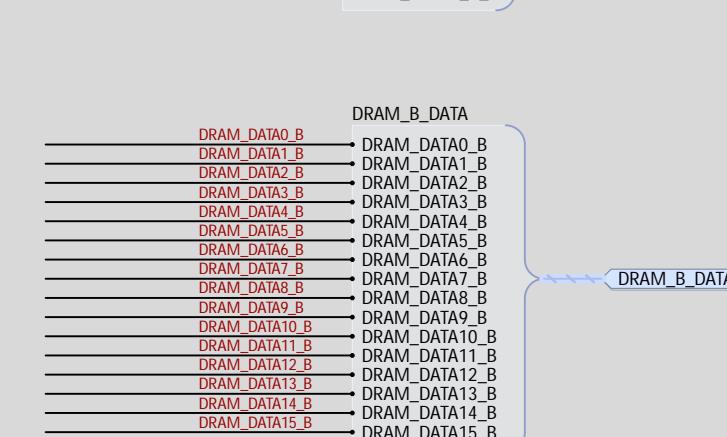
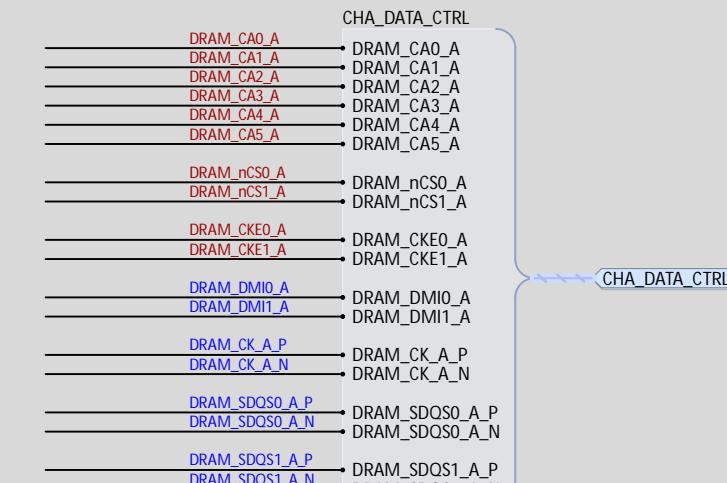
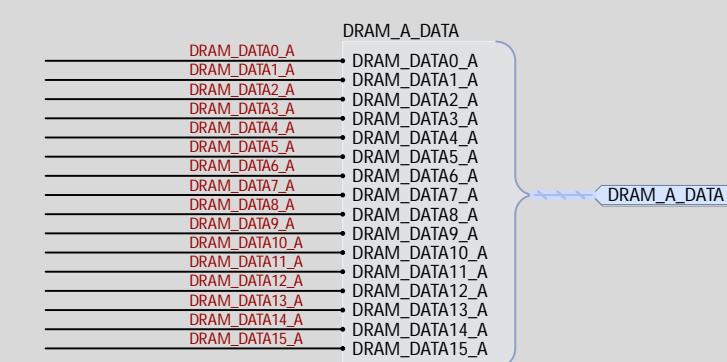
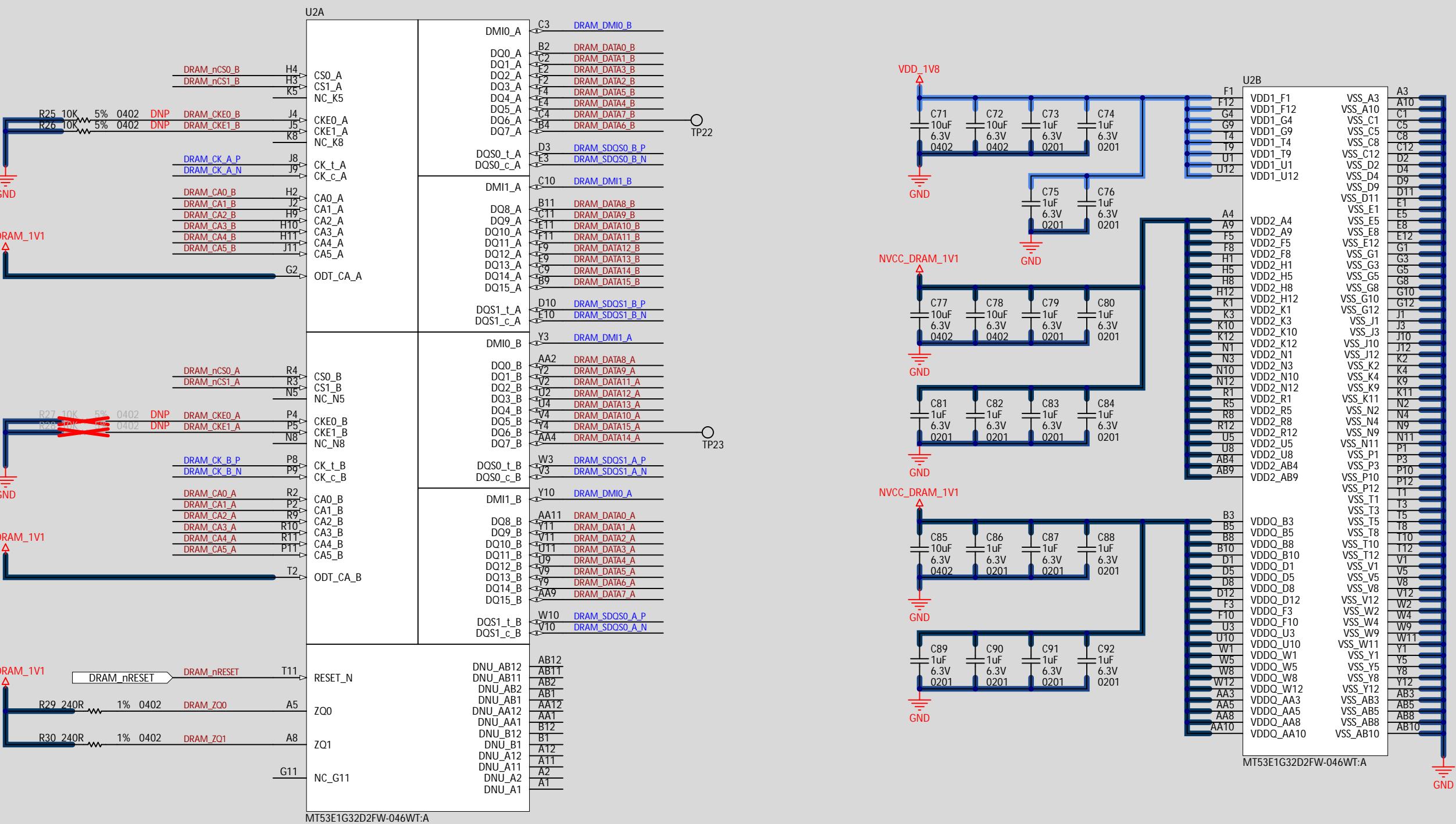


i.MX8M Plus LPDDR4 EVK Power Sequence and Operating Range

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNVS_1V8	LDO1	1.71	1.8	1.95	10
2	32K_INTERNAL	RTC_CLK	--	--	--	--
3	VDD_SOC	BUCK1/3	0.805/0.9	0.85/0.95	0.9/1.0	6000
4	VDD_ARM	BUCK2	0.805/0.9/0.95	0.85/0.95/1.0	0.9/1.0/1.05	3000
5	VDDA_1V8	LDO3	1.71	1.8	1.89	300
6	VDD_1V8/NVCC_xxx	BUCK5	1.65	1.8	1.95	2000
7	NVCC_DRAM_1V1	BUCK6	1.045	1.1	1.155	2000
8	VDD_3V3/NVCC_xxx	BUCK4	3	3.3	3.6	3000
8	VSD_3V3	MUXSW	3	3.3	3.6	400
9	NVCC_SD2	LDO5	3.0/1.65	3.3/1.8	3.6/1.95	150
10	POR_B	POR_B	--	--	--	--

PCB Des :	ELIO F.
Approv By :	ELIO F.
Project Title :	Dashcam CPU_V1.0 A.PrjPcb
Date :	4/19/2024
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LPDDR4



Note:

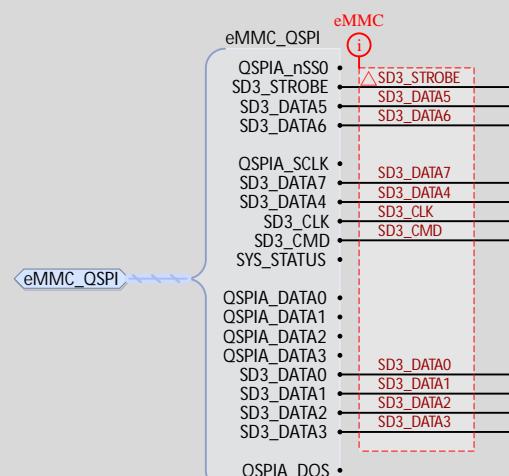
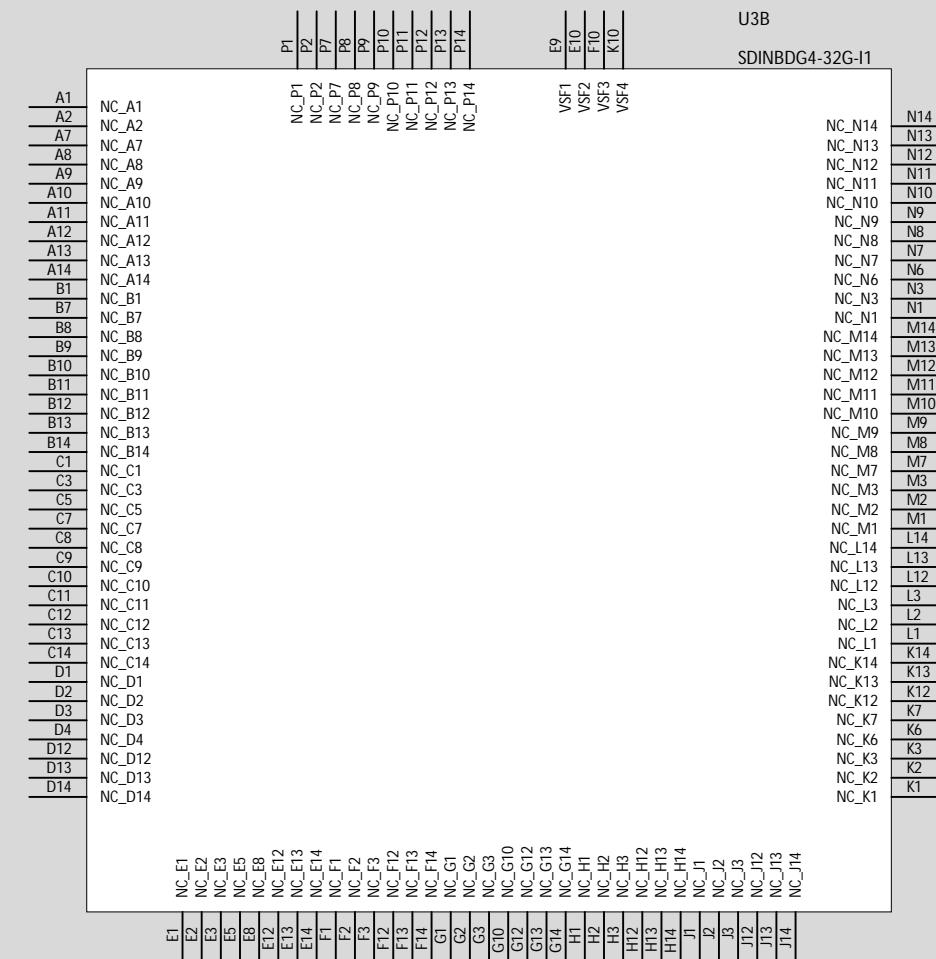
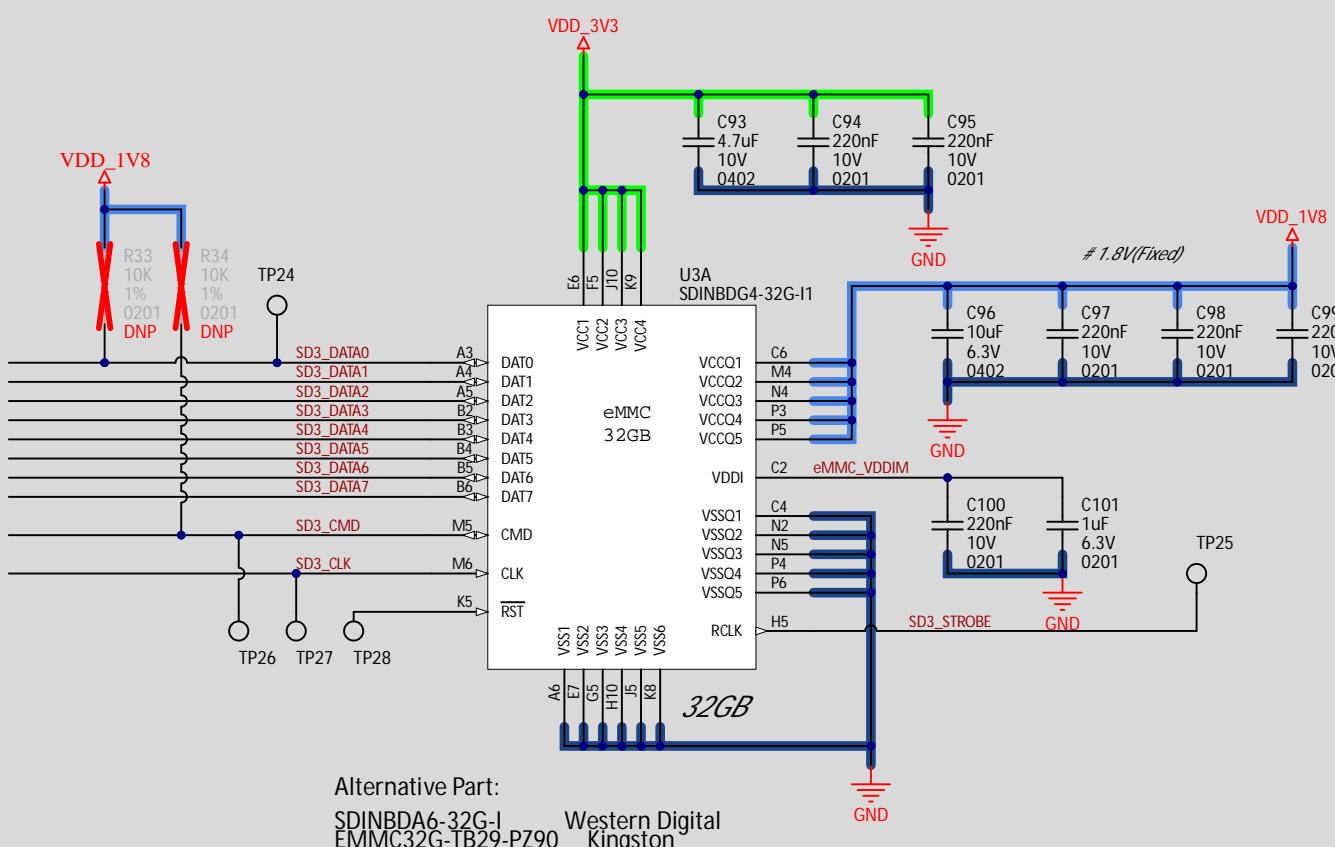
LPDDR4 ODT on i.MX 8M Plus is command-based, ODT_CA_A/B of LPDDR4 part should be connected directly to VDD2.

Data Bus			Command/Address		
Pin Name	LPDDR4	DDR4	Pin Name	LPDDR4	DDR4
DRAM_D0\$0_P	D0\$0_L_A	D0\$0_L_A	DRAM_RESET_N	RESET_N	RESET_N
DRAM_D0\$0_N	D0\$0_C_A	D0\$0_C_A	DRAM_ALERT_N	MTEST1	ALERT_N / MTEST1
DRAM_DM0	DM0_A	DM0_n_A / DBIL_n_A	DRAM_AC00	CKE0_A	CKE0
DRAM_D000	D00_A	D00_A	DRAM_AC01	CKE1_A	CKE1
DRAM_D001	D01_A	D01_A	DRAM_AC02	CS0_A	CS0_n
DRAM_D002	D02_A	D02_A	DRAM_AC03	CS1_A	CS1
DRAM_D003	D03_A	D03_A	DRAM_AC04	CK_L_A	BG0
DRAM_D004	D04_A	D04_A	DRAM_AC05	CK_C_A	BG1
DRAM_D005	D05_A	D05_A	DRAM_AC06	/	ACT_n
DRAM_D006	D06_A	D06_A	DRAM_AC07	/	A9
DRAM_D007	D07_A	D07_A	DRAM_AC08	CA0_A	A12
DRAM_D0\$1_P	D0\$1_L_A	D0\$1_L_A	DRAM_AC09	CA1_A	A11
DRAM_D0\$1_N	D0\$1_C_A	D0\$1_C_A	DRAM_AC10	CA2_A	A7
DRAM_DM1	DM1_A	DM1_n_A / DBIL_n_A	DRAM_AC11	CA3_A	A8
DRAM_D008	D008_A	D008_A	DRAM_AC12	CA4_A	A6
DRAM_D009	D009_A	D009_A	DRAM_AC13	CA5_A	A5
DRAM_D010	D010_A	D010_A	DRAM_AC14	/	A4
DRAM_D011	D011_A	D011_A	DRAM_AC15	/	A3
DRAM_D012	D012_A	D012_A	DRAM_AC16	/	CK_L_A
DRAM_D013	D013_A	D013_A	DRAM_AC17	/	CK_C_A
DRAM_D014	D014_A	D014_A	DRAM_AC19	MTEST	MTEST
DRAM_D015	D015_A	D015_A	DRAM_AC20	CKE0_B	CK_L_B
DRAM_D0\$2_P	D0\$0_L_B	D0\$0_L_B	DRAM_AC21	CKE1_B	CK_C_B
DRAM_D0\$2_N	D0\$0_C_B	D0\$0_C_B	DRAM_AC22	CS1_B	/
DRAM_DM2	DM0_B	DM0_n_B / DBIL_n_B	DRAM_AC23	CS0_B	/
DRAM_D016	D00_B	D00_B	DRAM_AC24	CK_L_B	A2
DRAM_D017	D01_B	D01_B	DRAM_AC25	CK_C_B	A1
DRAM_D018	D02_B	D02_B	DRAM_AC26	/	BAT
DRAM_D019	D03_B	D03_B	DRAM_AC27	/	PARITY
DRAM_D020	D04_B	D04_B	DRAM_AC28	CA0_B	A13
DRAM_D021	D05_B	D05_B	DRAM_AC29	CA1_B	BA0
DRAM_D022	D06_B	D06_B	DRAM_AC30	CA2_B	A10 / AP
DRAM_D023	D07_B	D07_B	DRAM_AC31	CA3_B	A0
DRAM_D0\$3_P	D0\$1_L_B	D0\$1_L_B	DRAM_AC32	CA4_B	C2
DRAM_D0\$3_N	D0\$1_C_B	D0\$1_C_B	DRAM_AC33	CA5_B	CAS_n / A15
DRAM_DM3	DM1_B	DM1_n_B / DBIL_n_B	DRAM_AC34	/	WE_n / A14
DRAM_D024	D008_B	D008_B	DRAM_AC35	/	RAS_n / A16
DRAM_D025	D009_B	D009_B	DRAM_AC36	/	ODD0
DRAM_D026	D010_B	D010_B	DRAM_AC37	/	ODT1
DRAM_D027	D011_B	D011_B	DRAM_AC38	/	CS1_n
DRAM_D028	D012_B	D012_B	DRAM_ZN	Z0	Z0
DRAM_D029	D013_B	D013_B	DRAM_VREF	VREF	VREF
DRAM_D030	D014_B	D014_B			
DRAM_D031	D015_B	D015_B			
	D0U7_B				

PCB Des :	
ELIO F.	
Approv By :	
ELIO F.	
Project Title :	Sheet Title :
Dashcam CPU_V1.0 A.PrjPcb	'LPDDR4
Date : 4/19/2024	PCB Version : 1.0
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Storage

eMMC5.1



PCB Des :	
ELIO F.	
Approv By :	
ELIO F.	
Project Title :	Sheet Title :
Dashcam CPU_V1.0.A.PrjPcb	'eMMC
Date : 4/19/2024	PCB Version : 1.0
Page : 13 16	PCB Revision : -
	Size : A3

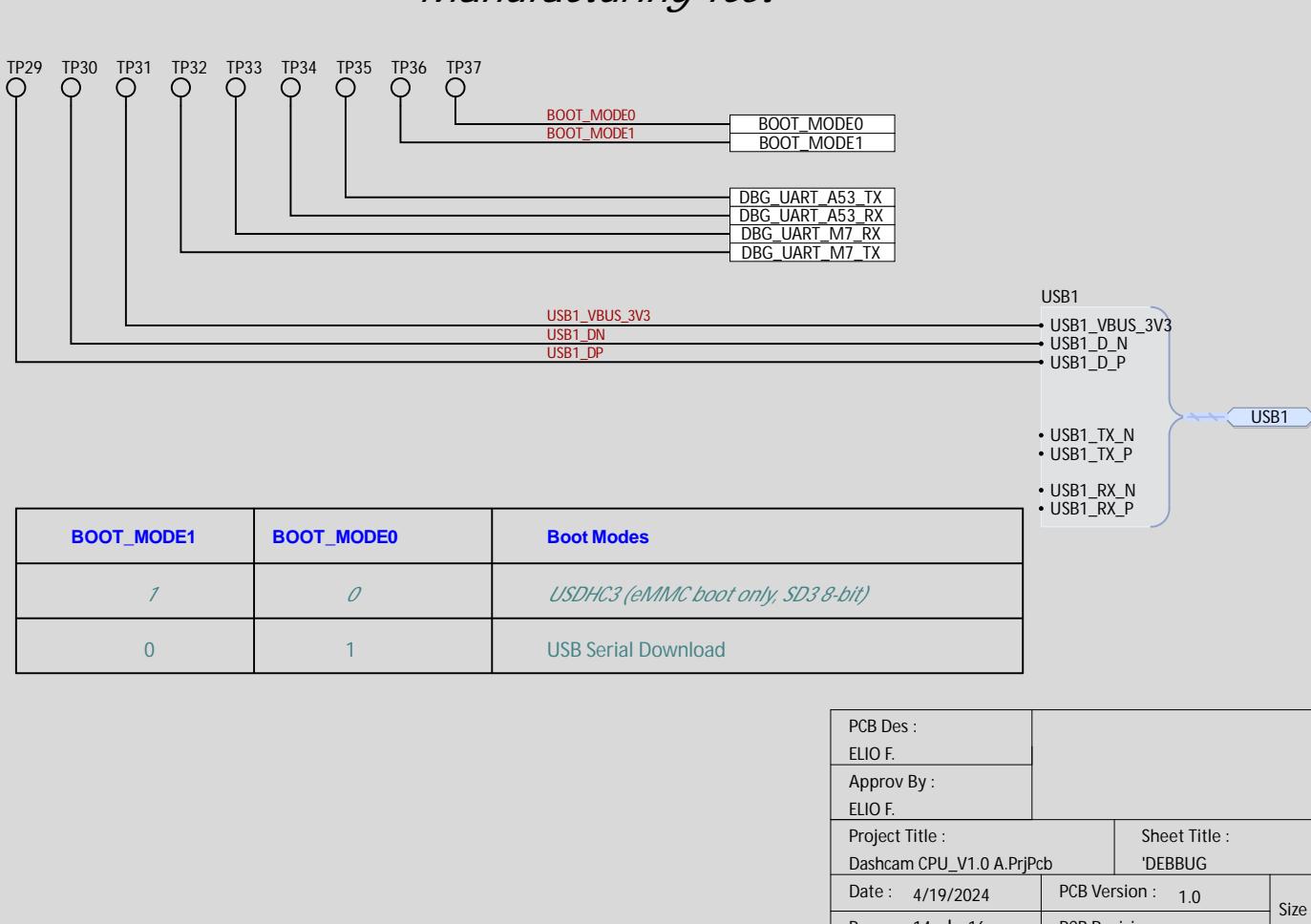
1	2	3	4	5	6	7	Full Line Address	Physical Address	0	1	2	3	4	5	6	7	8		
Boot Mode and CFG Switch																			
A	0x470[15:0]	0x470[7:0]		OVERRIDE_NAND_PG_PER_BLK_VAL 00 - 32 pages 01 - 64 pages 10 - 128 pages 11 - 32 pages	OVERRIDE_FLEXSPI_BT_SEL 0 - Do not override 1 - Override		OVERRIDE_FLEXSPI_BT_SEL_VAL 00 - FlexSPI (Hyperflash 1.8V) 01 - FlexSPI (Flash with 4B READ 1x13 default supported) 10 - Default Octal mode (Micron, supported on 80XP B0 already) 11 - Default Octal mode (Mic, Nice to have)	FLEXSPI_AUTO_PROBE_EN		FLEXSPI_AUTO_PROBE_TYPE 00 - QuadSPI NOR 01 - MixOctal 10 - MicronOctal 11 - AdestoOctal									
	0x480[15:0]	0x480[7:0]	Reserved				FLEXSPI_DUMMY_CYCLE_SEL			FLEXSPI_FEQ_SEL 000 - 100 MHz 001 - 100 MHz 010 - 160 MHz 011 - 200 MHz 100 - 80 MHz 101 - 20 MHz									
	0x480[31:16]	0x480[23:16]	NOC_ID_REMAP_BYPASS	ROM_NO_LOG if blown, ROM will not log event to log buffer	SDP_DISABLE Disable USB serial download	FORCE_BT_FROM_FUSE Boot from programmed fuses, not Boot Mode Pins		FLEXSPI_HOLD_TIME_SEL 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		WDOG_TIMEOUT_SELECT 00 - 2.0s 01 - 1.5s 10 - 1.0s 11 - 0.5s									
	0x490[15:0]	0x490[7:0]	USDHCI_PWR_EN 0 - No power cycle 1 - Enabled via	EMMC_FAST_BT 0 - Regular 1 - Fast Boot		SDMMC_BUS_WIDTH 00 - 8-bit 01 - 4-bit 10 - 8-bit DDR (MMC 4.4) 11 - 4-bit DDR (MMC 4.4)		SD_SPEED: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104	EMMC_SPEED: 00 - Normal 01 - High	USDHCI_VOL_SEL For Normal Boot Mode IO Voltage 0 - 3.3V 1 - 1.8V	USDHCI_MFG_VOL_SEL For Mfg Mode IO Voltage 0 - 3.3V 1 - 1.8V								
	0x490[31:16]	0x490[23:16]	RECOVERY_SDMMC_BOOT_DIS 0 - Enable 1 - Disable			IMG_CNTN_SET1_OFFSET			USDHCI_PAD_SION_EN 0 - Disable 1 - Enable		BT_RDC_DISABLE		USDHCI_DLL_EN 0 - Disable DLL for SD/dMMC 1 - Enable DLL for SD/dMMC						
	0x4A0[15:0]	0x4A0[7:0]	SD_CAU_STEP '00' - 1 TBD		USDHCI_PWR_INTERVAL 00 - 20ms 01 - 10ms 10 - 5ms 11 - 2.5ms		USDHCI_PWR_DELAY 0 - 5ms 1 - 2.5ms	USDHCI_PWR_POLARITY 0 - Low 1 - High		USDHCI_OVRD_PAD_SETTING_UP1		EMMC_FAST_BT_ACK 0 - Boot Ack Disabled 1 - Boot Ack Enabled							
	0x4A0[31:16]	0x4A0[23:16]				Reserved													
	0x4B0[15:0]	0x4B0[7:0]	Reserved			NAND_GPMI_DDR_DLL_VAL (GPMI Read DDR DLL Target Value) 0000 - 0 0001 - 1 0111 - 0 1111 - 15				USB_SS_ENABLE			NAND_CS_NUM (Nand Number Of Devices) 00 - 1 01 - 2 10 - 4 11 - Reserved						
	0x4B0[31:16]	0x4B0[23:16]	Reserved		FlexSPI NAND Busy Bit Offset Override			NAND_CS_SEL Interval 00-100ns 01-200ns 10-400ns 11-50ns				FlexSPI NAND Column Address Width 00-12 01-13 10-14 11-15							
B	0x470[15:0]	0x470[15:8]		BOOT_MODE_FUSES		BootRom will retrieve boot mode from these fuses instead of BOOT_MODE pins if * BOOT_MODE_PINS=0x0 or * BT_FUSE_SEL blown		OVERRIDE_USDHCI_BT_SEL 0 - Do not override 1 - Override		OVERRIDE_USDHCI_BT_SEL_VAL 00 - usdhci1_sd 01 - usdhci1_mmci 10 - usdhci2_sdmmc 11 - usdhci3_sd		OVERRIDE_NAND_PG_PER_BLK 0 - Do not override 1 - Override							
	0x480[15:0]	0x480[15:8]		BT_LP_B (Core/DDR/Bus) '00' - LPB Disable '10' - Div by 2 '11' - Div by 4		BT_LP_B_Polarity (GPIO polarity)	I CACHE_D5 L1 Cache DISABLE	TZASC_EN	WDOG_EN 0 - Disabled 1 - Enabled	BT_FREQ_SEL (ARM/DDR) 0 - 800 / 800 MHz 1 - 400 / 400 MHz		DCACHE_DIS	Disable L1 and L2 D-Cache						
	0x480[31:16]	0x480[31:24]		ECSP1_PORT_SEL 000 - eCSP1 001 - eCSP2 010 - eCSP3		ECSP1_ADDR_SEL 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)		ECSP1_CS_SEL(SPI only) 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		RECOVER_ESPI_BOOT_EN 0 - Disabled 1 - Enabled		DCACHE_BY_PASS_DIS							
	0x490[15:0]	0x490[15:8]	USDHCI_DLL_SEL 0 - DLL Slave Mode for 1 - DLL Override Mode			SDMMC_DLL_SEL(6:0)													
	0x490[31:16]	0x490[31:24]				USDHCI_OVRD_PAD_SETTING_LOWB[7:0]													
	0x4A0[15:0]	0x4A0[15:8]	BT_TOGGLE_MODE		NAND_FCB_SEARCH_COUNT 00 - 2 01 - 4 10 - 8 11 - 16			NAND_TG_PREAMBLE_RD_LATENCY (Toggle Mode 33MHz Preamble Delay, Read Latency) '000' - 16 GMICLK cycles. '001' - 1 GMICLK cycles. '010' - 2 GMICLK cycles. '011' - 3 GMICLK cycles. '100' - 4 GMICLK cycles. '101' - 5 GMICLK cycles. '110' - 6 GMICLK cycles. '111' - 7 GMICLK cycles. '1111' - 15 GMICLK cycles.			NAND_RST_TIME								
	0x4A0[31:16]	0x4A0[31:24]				NAND_OVERRIDE_PAD_SETTING[7:0]													
	0x4B0[15:0]	0x4B0[15:8]		NAND_READ_RETRY_SEQ_ID[0:0]		0000 - don't use read retry/RW sequence embedded in ROM 0001 - Micron 20nm RR sequence 0010 - Toshiba A19nm RR sequence 0011 - Toshiba 19nm RR sequence 0100 - SanDisk 19nm sequence 0101 - SanDisk 19nm sequence 0110 - Hynix 20nm RR sequence 0111 - Hynix 20nm RR sequence 1000 - Hynix 20nm B Die RR sequence 1001 - Hynix 20nm C Die RR sequence Others - Reserved			NAND_ROW_ADDR_BYTES 00 - 3 01 - 2 10 - 4 11 - 5										
	0x4B0[31:16]	0x4B0[31:24]				RNG_TRIM[7:0]													
C	0x470[15:0]	0x470[15:8]																	
	0x480[15:0]	0x480[15:8]																	
	0x480[31:16]	0x480[31:24]																	
	0x490[15:0]	0x490[15:8]																	
	0x490[31:16]	0x490[31:24]																	
	0x4A0[15:0]	0x4A0[15:8]																	
	0x4A0[31:16]	0x4A0[31:24]																	
	0x4B0[15:0]	0x4B0[15:8]																	
	0x4B0[31:16]	0x4B0[31:24]																	
	0x4C0[15:0]	0x4C0[15:8]																	
D	0x4C0[15:0]	0x4C0[15:8]																	
	0x4C0[31:16]	0x4C0[31:24]																	
	0x4D0[15:0]	0x4D0[15:8]																	
	0x4D0[31:16]	0x4D0[31:24]																	
	0x4E0[15:0]	0x4E0[15:8]																	
	0x4E0[31:16]	0x4E0[31:24]																	
	0x4F0[15:0]	0x4F0[15:8]																	
	0x4F0[31:16]	0x4F0[31:24]																	
	0x500[15:0]	0x500[15:8]																	
	0x500[31:16]	0x500[31:24]																	

i.MX8M Plus ROM Fuse

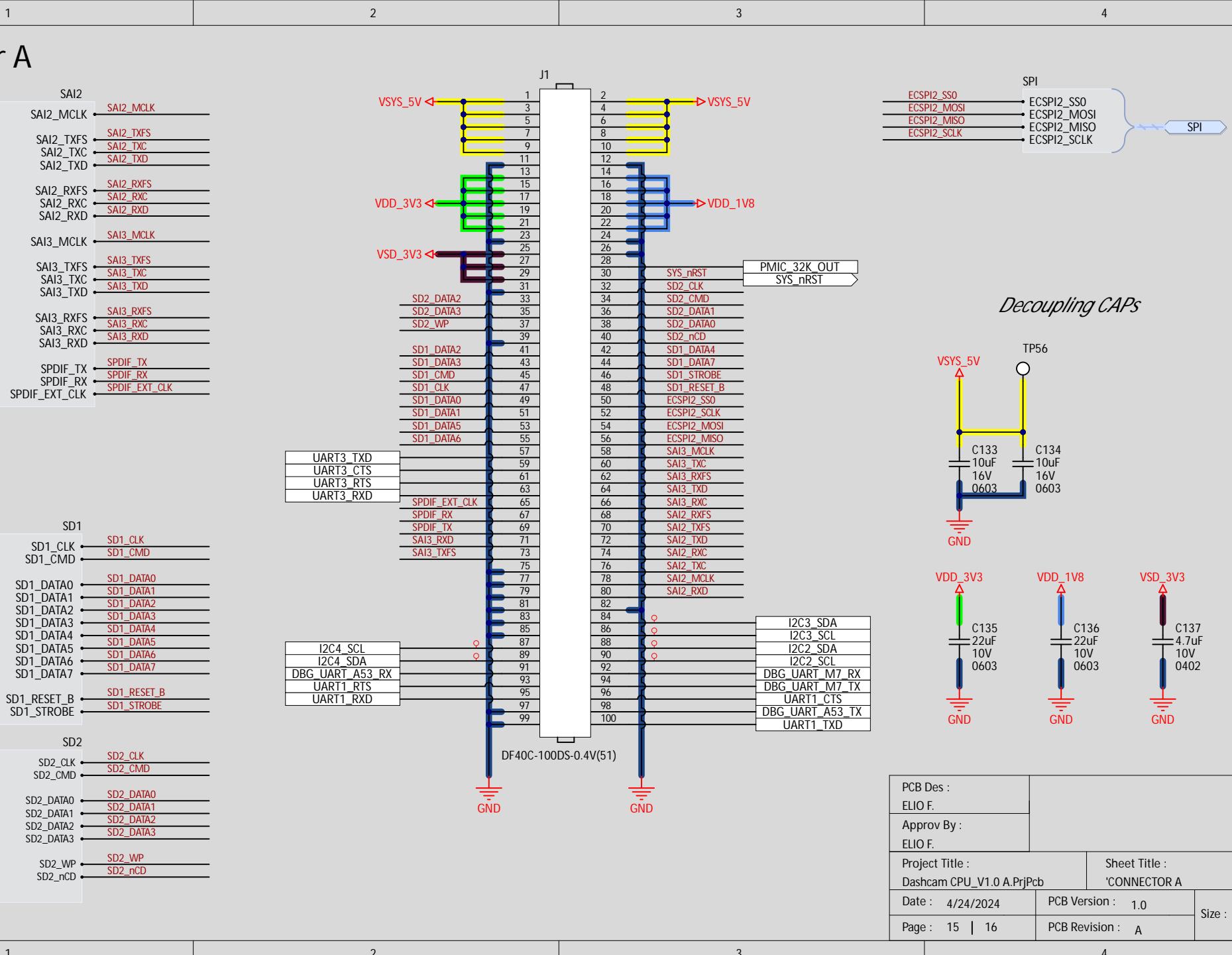
i.MX8M Plus Boot Mode

BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	0	1	0	USDHC3 (eMMC boot only, SD3 8-bit) Default
0	0	1	1	USDHC2 (SD boot only, SD2)
0	1	0	0	NAND 8-bit single device 256 page
0	1	0	1	NAND 8-bit single device 512 page
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI Hyperflash 3.3V
1	0	0	0	ecSPI Boot
1	0	0	1	Reserved
1	0	1	0	FLEXSPI Serial NAND 2k page
1	0	1	1	FLEXSPI Serial NAND 4k page
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

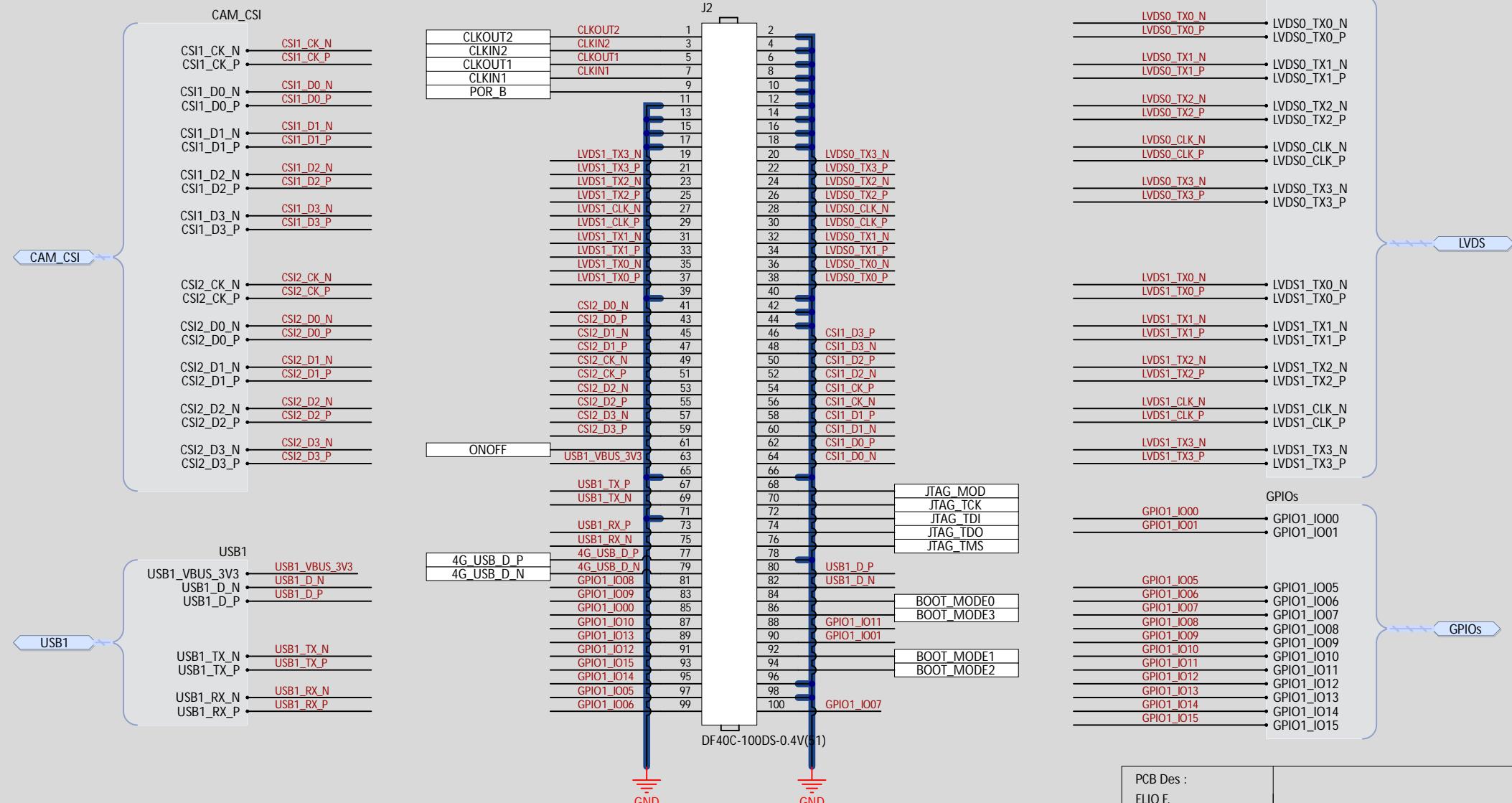
Manufacturing Test



Connector A



Connector B



PCB Des :
FLIO E.

Approv By :
FLIO E.

Project Title :
Dashcam CPU_V1.0 A.PrjPcb

Sheet Title :
'CONNECTOR B'

Date : 4/26/2024

Version : 1.0 | Size : A4