NEC

Design Manual

CB-9 Family VX/VM Type Core Library

0.35 μm CMOS Cell-Based IC (CBIC)

CPU Core, Memory Controller

78K/0 Core
V851™ Core
V853™ Core
V30MX™
V30MZ™
NB85E
NB85E901
NB85ET
NB85E500
NU85E500
NU85E502

Document No. A13195EJ5V1DM00 (5th edition)
Date Published January 2002 NS CP(N)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
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Major Revisions in This Edition

Pages	Description
p.17	Addition of **1.3 Timing Verification**
p.91	Addition of **5.3.7 Timing Verification**
p.105	Addition of **6.2.2 Timing Verification**
p.108	Modification of **6.5.2 Recommended operation range**
p.134	Modification of **7.4.4 (3) VSB arbitration timing**
p.144	Modification of **7.4.4 (8) VFB access timing**
p.175	Modification of **9.4.2 Recommended operation range**
p.176	Modification of **9.4.4 (1) Clock timing**
p.177	Modification of **9.4.4 (3) VSB arbitration timing**
p.186	Modification of **9.4.4 (8) VFB access timing**
p.262	Modification of **12.4.4 (1) SDRAM read timing**
p.264	Modification of **12.4.4 (2) SDRAM write timing**
p.267	Modification of **12.4.4 (4) VSB timing**
pp.268 to 270	Addition of **APPENDIX REVISION HISTORY**

The mark ⋆ shows major revised points.

INTRODUCTION

Readers This manual is intended for users who will design ASIC employing the CB-9 Family VX/VM Type of NEC's high-speed, highly integrated CMOS CBIC.

Purpose The purpose of this manual is to help the user understand the outlines and electrical specifications of the following CPU cores, run control unit (RCU), and memory controllers (MEMC) necessary for designing the system.

<CPU core>
- 78K/0 core
- V851 core
- V853 core
- V30MX
- V30MZ
- NB85E
- NB85ET

<RCU>
- NB85E901

<MEMC>
- NB85E500
- NU85E500
- NU85E502

Organization This manual is generally divided into the following sections.

CHAPTER 1 COMMON PART

Explains information which is common to the above CPU cores.
Be sure to read this chapter when you use any of the CPU cores listed above.

CHAPTER 2 78K/0 CORE or later chapters

Explains information peculiar to each CPU core, RCU, and MEMC.
Read the chapter explaining the CPU core, RCU, and MEMC to be used.

How To Read This Manual

It is assumed that the readers of this manual have general knowledge on electric engineering, logic circuits, and microcontrollers.
Before using this manual, be sure to read the related manual **CB-9 Family VX/VM Type Design Manual (A12745E).**

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	xxxB or xxxZ ("B" or "Z" is appended to the pin name or signal name)
Note:	Footnote for item marked with Note in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH

Prefix indicating power of 2 (in address space or memory capacity):

K (kilo) … $2^{10} = 1024$
M (mega) … $2^{20} = 1024^2$
G (giga) … $2^{30} = 1024^3$

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- CB-9 Family VX/VM Type Design Manual (A12745E)
- CB-9 Family VX/VM Type Design Manual 78K/0 Core User's Manual (A13688E)
- CB-9 Family VX/VM Type V851 Core, V853 Core Design Manual User's Manual (A13602E)
- CB-9 Family VX/VM Type NB85E, NB85ET Design Manual (A14335E)
- 78K/0 Core User's Manual (A13142E)
- V851 Core Hardware User's Manual (A12757E)
- V853 Core Hardware User's Manual (A13141E)
- V30MX Hardware User's Manual (A11897E)
- V30MZ Hardware User's Manual (A13761E)
- NB85E Hardware User's Manual (A13971E)
- NB85ET Hardware User's Manual (A14342E)
- Memory Controller NB85E, NB85ET User's Manual (A14206E)

The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

CONTENTS

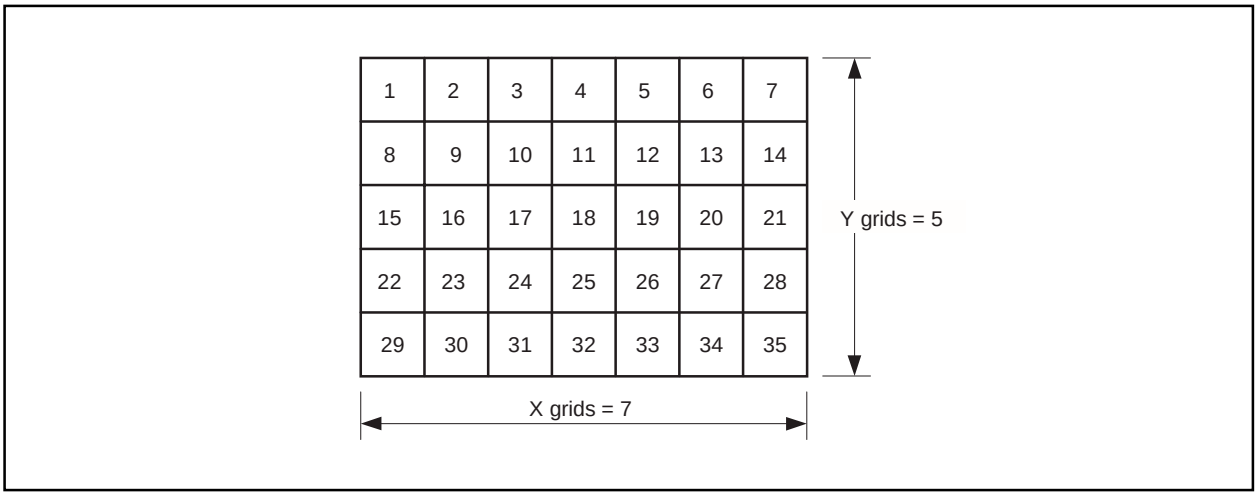
LIST OF FIGURES

1. 1 Macro Area

The area of a macro is expressed as a number of grids.
The number of grids is an index that indicates the area of the circuit of a cell-based IC.

Number of grids = X grids (size in X direction) × Y grids (size in Y direction)

For example, the circuit shown below consists of 35 grids.



1. 2 Test Design

Test design is very important when designing the circuit of an ASIC.

This section explains the test functions of a CPU core. These test functions are necessary when designing the CB-9 family VX/VM type using any of the CPU cores explained in this manual.

1. 2. 1 Test pattern

When developing a CB-9 family VX/VM type product including a CPU core, simulation is implemented for each internal block in the following three stages, unlike when the circuit consists of only user logic.

(1) User logic separation simulation

Checks the functions of the user logic in detail.

(2) Test circuit check simulation

Checks the path (test bus) that tests the internal functions of the CPU core.

The test patterns for the internal functions of the CPU cores have been created by NEC.

(3) Total chip simulation

Checks mutual connection between the CPU core, user logic, and interface block.

Theoretically, it is possible to check the circuit operation in (1) through (3) with one test pattern, but it is more efficient to use the above three stages for the following reasons:

(a) To avoid creating test pattern for checking CPU core functions in detail

The internal circuits of the CPU core are very complicated and in effect a kind of black box.

Therefore, it is extremely difficult to create a simulation test pattern that can check the internal functions taking delicate timing into consideration, and it is practically impossible for the user to create a test pattern that tests all the internal functions of the CPU core.

For this reason, separate the simulation process to check the internal circuits of the CPU core from the user logic block, and insert a test circuit. NEC offers ready-made test patterns.

(b) To mitigate the simulation load of the CPU core, and to avoid the limitations of using a CAD tool that can simulate the CPU core

Some CPU cores have several 10,000 of gates and therefore have a heavy simulation load.

Consequently, the types of machines that can execute simulation of these CPU cores are limited and the execution time is very long.

The user logic separation simulation in (1) above can mitigate the simulation load of the user logic block where a mistake is most likely to occur, by creating a model, called a dummy macro, of only the CPU core cut-out section. Consequently, the design period can be shortened. In addition, a wider range of CAD tools can be used. Note, however, that the kinds of tools that can use a dummy macro are also limited.

1. 2. 2 Test program for total chip simulation

A test program that is executed by the CPU core is also necessary for executing total chip simulation. When using an external memory instead of the internal memory of the CB-9 family VX/VM type, simulation is easier if a circuit in which an external memory is connected to the circuit of the CB-9 family VX/VM type is created and if total chip simulation is executed in the same manner as above, rather than if instructions are given in the form of a test pattern. In this case, the test pattern for the actual chip can be created if the signals at the cut-out section of the circuit block of the original CB-9 family VX/VM type is dumped.

For details, refer to **Design Manual** of each CPU core.

1. 2. 3 Test pins

(1) TBO (n:0), TBI (m:0)

These are test pins for simulation to check the test circuit.

The pins of a CPU core can be broadly divided into test pins and normal pins used for application circuit design.

The signals input to or output from the test pins are separated from those input to or output from the normal pins.

The number of test pins differs depending on the CPU core.

(2) BUNRI, TEST

These pins select the modes of the test pins and normal pins.

Depending on the combination of the signals input to these pins, the CPU core operates as follows:

BUNRI	TEST	Operation Mode
0	0	Normal mode
	1	
1	0	Test mode (standby test)
	1	Test mode (unit test)

(a) Normal mode

This mode is used to perform normal operations such as during total chip simulation. In this mode, the normal pins are valid.

(b) Test mode (standby test)

This mode is used when the CPU core is not tested during test circuit check simulation or user logic separation simulation.

(c) Test mode (unit test)

This mode is used when the CPU core is tested during test circuit check simulation.

Each pin is in the following status in each operation mode.

Mode	Normal Pins				Test Pins	
	Input	Output	3-State Output	Bidirectional	Input (TBIx)	Output (TBOx)
Normal mode	Valid	Valid	Valid	Valid	Input ignored	High impedance
Test mode (standby test)	Input ignored	Undefined	High impedance	Input ignored		
Test mode (unit test)					Valid	Valid

For details on circuit design, refer to **CB-9 Family VX/VM Type Design Manual (A12745E)**.

1. 2. 4 Initialize

The steps for initialization are explained in below. Initialize each CPU core by following these steps.

(1) Input an initialization pattern from the normal pins

(a) Apply a reset pulse

Apply a pulse with a specified width or more.

Some CPUs require operation of the clock signal while the reset pulse is input.

(b) Write initial values to the internal registers

Some registers, such as the stack pointer of the CPU, require that initial values be set in advance.

(2) Input an initialization pattern from a test pin

This step is used to initialize a CPU core for which NEC has already created an initialization pattern because the test pattern is very complicated.

In this case, the initialization pattern is input in the same test mode as for test circuit check simulation, and then the mode is changed back to that of total chip simulation.

Although this step allows you to ignore the details of the pattern, it requires care when changing the mode from test to normal, so that a malfunction does not occur.

1. 2. 5 Prohibition on spike input

It is necessary to take care not to input a spike to input pins that operate at the edge of an input signal, such as interrupt and clock input pins.

★ 1. 3 Timing Verification

Verify that the input timing is satisfied at the boundary between the CPU core and memory controller using a delay analysis tool.

Observe the description on timing verification for each CPU core and memory controller if described in this manual (refer to the design manual of each CPU core).

CHAPTER 2 78K/0 CORE

The 78K/0 core is a CPU core containing many peripheral functions such as timers, serial interfaces, and an interrupt controller. The instruction set of the 78K/0 core is common to that of the 78K/0 Series 8-bit single-chip microcontrollers.

2. 1 Outline

- CPU function: 78K/0 Series standard
- Minimum instruction execution time: 0.24 μs (maximum input frequency: 8.38 MHz)
- Internal memory

Part Number	ROM Capacity	RAM Capacity
NAK0HM0	0 (ROMless)	1 KB
NAK0HM4	32 KB (mask ROM)	
NAK0HM8	60 KB (mask ROM)	

- Port
  Up to 128 port pins can be used by using an I/O buffer.
  Input port: 64 pins
  Output port: 64 pins
- Timers/counters
  16-bit timer/event counter: 1 ch
  8-bit timer/event counter: 2 chs
  Watch timer: 1 ch
  Watchdog timer: 1 ch
- Serial interface
  3-wire serial I/O mode: 2 chs
  UART mode: 2 chs
  I^2C bus mode: 2 chs
- Vectored interrupt source: 29 (internal : 17, external : 12)
- External memory expansion space: 64 KB (address/DIN/DOUT separation)
- Standby function: HALT/STOP mode (can be released by interrupt)
- Supply voltage: V_{DD} = 3.0 to 3.6 V

2. 1. 1 Symbol diagram

(1) NAK0HM0

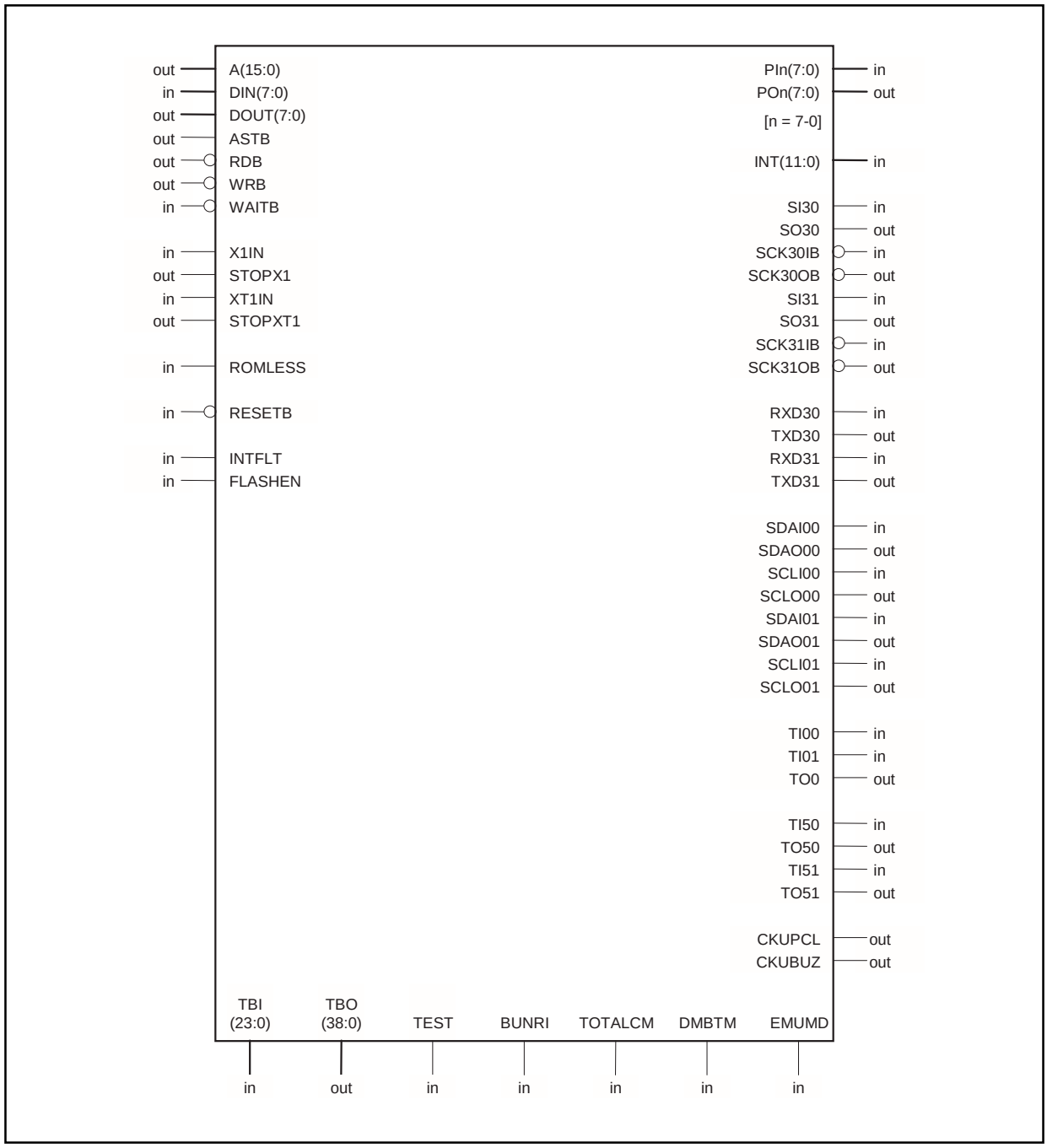
Number of grids

147k grids

192k grids (value including wiring area)

Number of separation simulation patterns

165k



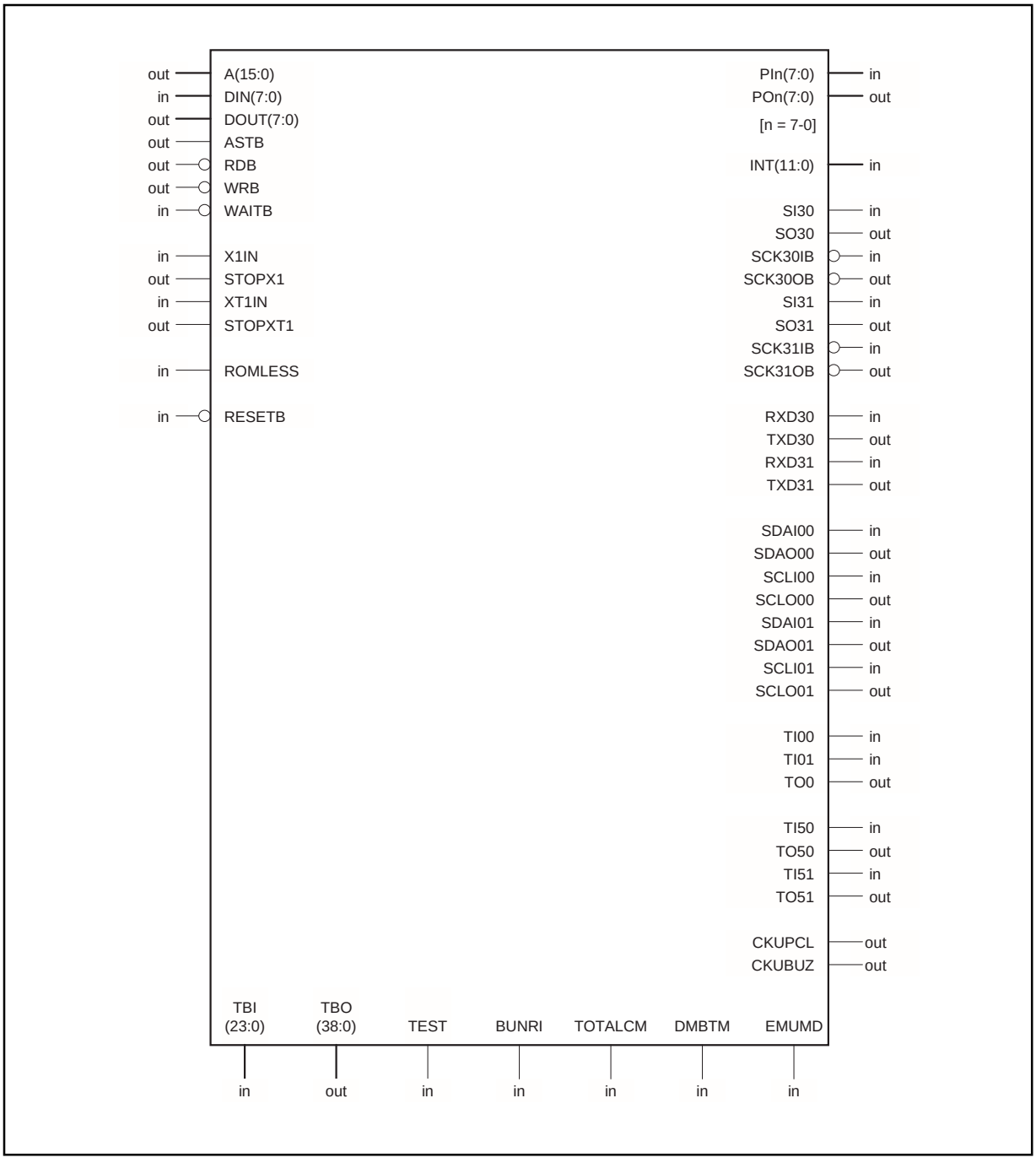
(2) NAK0HM4, NAK0HM8

Number of grids

- NAK0HM4: 193k grids
  243k grids (value including wiring area)
- NAK0HM8: 217k grids
  270k grids (value including wiring area)

Number of separation simulation patterns

- NAK0HM4: 230k
- NAK0HM8: 285k



2. 1. 2 Pin capacitance

Remark C_{IN}: Capacitance of only input pin

C_{inewl}: Value of C_{IN} with wiring capacitance (estimated wire length capacitance) taken into consideration (l = 10 mm)

(1) NAK0HM0

(a) Input pins

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
DIN7 to DIN0	0.102	2.002	SCLI00	0.233	2.133
WAITB	0.059	1.959	SDAI01	0.067	1.967
X1IN	0.059	1.959	SCLI01	0.065	1.965
XT1IN	0.046	1.946	TI00	0.056	1.956
ROMLESS	0.630	2.530	TI01	0.075	1.975
RESETB	0.109	2.009	TI50	0.045	1.945
PIn7 to PIn0 (n = 7 to 0)	0.153	2.053	TI51	0.050	1.950
INT11 to INT0	0.210	2.110	TBI23 to TBI0	1.019	2.919
SI30	0.062	1.962	TEST	3.983	5.883
SCK30IB	0.068	1.968	BUNRI	4.455	6.355
SI31	0.081	1.981	TOTALCM	1.544	3.444
SCK31IB	0.168	2.068	DMBTM	0.859	2.759
RXD30	0.087	1.987	EMUMD	0.747	2.647
RXD31	0.152	2.052	INTFLT	0.373	2.273
SDAI00	0.082	1.982	FLASHEN	0.629	2.529

(b) Output pins

Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)
A15 to A0	6.459	SO30	6.561	SDAO01	6.567
DOUT7 to DOUT0	6.501	SCK30OB	6.561	SCLO01	6.562
ASTB	6.452	SO31	6.545	TO0	6.566
RDB	6.415	SCK31OB	6.523	TO50	6.567
WRB	6.500	TXD30	6.555	TO51	6.566
STOPX1	6.564	TXD31	6.522	CKUPCL	6.550
STOPXT1	6.555	SDAO00	6.496	CKUBUZ	6.545
POn7 to POn0 (n = 7 to 0)	6.496	SCLO00	6.527	TBO38 to TBO0	6.322

(2) NAK0HM4

(a) Input pins

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
DIN7 to DIN0	0.090	1.990	SDAI00	0.057	1.957
WAITB	0.061	1.961	SCLI00	0.042	1.942
X1IN	0.049	1.949	SDAI01	0.043	1.943
XT1IN	0.045	1.945	SCLI01	0.046	1.946
ROMLESS	0.569	2.469	TI00	0.056	1.956
RESETB	0.047	1.947	TI01	0.073	1.973
PIn7 to PIn0 (n = 7 to 0)	0.178	2.078	TI50	0.081	1.981
INT11 to INT0	0.258	2.158	TI51	0.050	1.950
SI30	0.049	1.949	TBI23 to TBI0	0.925	2.825
SCK30IB	0.043	1.943	TEST	4.125	6.025
SI31	0.084	1.984	BUNRI	4.493	6.393
SCK31IB	0.068	1.968	TOTALCM	1.434	3.334
RXD30	0.058	1.958	DMBTM	0.794	2.694
RXD31	0.064	1.964	EMUMD	0.779	2.679

(b) Output pins

Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)
A15 to A0	6.445	SO30	6.568	SDAO01	6.568
DOUT7 to DOUT0	6.542	SCK30OB	6.568	SCLO01	6.567
ASTB	6.529	SO31	6.563	TO0	6.554
RDB	6.564	SCK31OB	6.559	TO50	6.528
WRB	6.562	TXD30	6.557	TO51	6.568
STOPX1	6.557	TXD31	6.566	CKUPCL	6.528
STOPXT1	6.540	SDAO00	6.530	CKUBUZ	6.561
POn7 to POn0 (n = 7 to 0)	6.347	SCLO00	6.564	TBO38 to TBO0	6.322

(3) NAK0HM8

(a) Input pins

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
DIN7 to DIN0	0.090	1.990	SDAI00	0.057	1.957
WAITB	0.061	1.961	SCLI00	0.042	1.942
X1IN	0.049	1.949	SDAI01	0.043	1.943
XT1IN	0.045	1.945	SCLI01	0.046	1.946
ROMLESS	0.569	2.469	TI00	0.056	1.956
RESETB	0.047	1.947	TI01	0.073	1.973
PIn7 to PIn0 (n = 7 to 0)	0.178	2.078	TI50	0.081	1.981
INT11 to INT0	0.258	2.158	TI51	0.051	1.951
SI30	0.049	1.949	TBI23 to TBI0	0.925	2.825
SCK30IB	0.043	1.943	TEST	4.123	6.023
SI31	0.084	1.984	BUNRI	4.493	6.393
SCK31IB	0.068	1.968	TOTALCM	1.434	3.334
RXD30	0.058	1.958	DMBTM	0.794	2.694
RXD31	0.064	1.964	EMUMD	0.779	2.679

(b) Output pins

Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)
A15 to A0	6.445	SO30	6.568	SDAO01	6.567
DOUT7 to DOUT0	6.542	SCK30OB	6.568	SCLO01	6.567
ASTB	6.529	SO31	6.563	TO0	6.554
RDB	6.564	SCK31OB	6.559	TO50	6.528
WRB	6.562	TXD30	6.557	TO51	6.568
STOPX1	6.557	TXD31	6.566	CKUPCL	6.528
STOPXT1	6.540	SDAO00	6.530	CKUBUZ	6.561
POn7 to POn0 (n = 7 to 0)	6.347	SCLO00	6.564	TBO38 to TBO0	6.322

2. 2 Pin Functions

(1/2)

Pin Name	I/O	Function
A15 to A0	Output	Output address output for external access.
DIN7 to DIN0	Input	Input data input for external access.
DOUT7 to DOUT0	Output	Output data output for external access.
ASTB	Output	External address strobe signal.
RDB	Output	External read strobe signal.
WRB	Output	External write strobe signal.
WAITB	Input	Control signal input to insert wait to external bus cycle.
X1IN	Input	Main system clock oscillator input.
STOPX1	Output	Main system clock oscillator stop signal.
XT1IN	Input	Subsystem clock oscillator input.
STOPXT1	Output	Subsystem clock oscillator stop signal.
ROMLESS	Input	ROMless mode select signal.
RESETB	Input	System reset input.
PIn7 to PIn0 (n = 7 to 0)	Input	8-bit input port.
POn7 to POn0 (n = 7 to 0)	Output	8-bit output port.
INT11 to INT0	Input	External interrupt request input.
SI30	Input	Serial interface (SIO30) serial data input.
SO30	Output	Serial interface (SIO30) serial data output.
SCK30IB	Input	Serial interface (SIO30) serial clock input.
SCK30OB	Output	Serial interface (SIO30) serial clock output.
SI31	Input	Serial interface (SIO31) serial data input.
SO31	Output	Serial interface (SIO31) serial data output.
SCK31IB	Input	Serial interface (SIO31) serial clock input.
SCK31OB	Output	Serial interface (SIO31) serial clock output.
RXD30	Input	Asynchronous serial interface (UART30) serial data input.
TXD30	Output	Asynchronous serial interface (UART30) serial data output.
RXD31	Input	Asynchronous serial interface (UART31) serial data input.
TXD31	Output	Asynchronous serial interface (UART31) serial data output.
SDAI00	Input	Serial interface (IIC00) serial data input.
SDAO00	Output	Serial interface (IIC00) serial data output.
SCLI00	Input	Serial interface (IIC00) serial clock input.
SCLO00	Output	Serial interface (IIC00) serial clock output.
SDAI01	Input	Serial interface (IIC01) serial data input.
SDAO01	Output	Serial interface (IIC01) serial data output.
SCLI01	Input	Serial interface (IIC01) serial clock input.
SCLO01	Output	Serial interface (IIC01) serial clock output.
TI00	Input	Capture trigger input 1 to capture register of 16-bit timer (TM0).
TI01	Input	Capture trigger input 2 to capture register of 16-bit timer (TM0).

(2/2)

Pin Name	I/O	Function
TO0	Output	16-bit timer (TM0) PWM output.
TI50	Input	External count clock input to 8-bit timer (TM50).
TO50	Output	8-bit timer (TM50) output.
TI51	Input	External count clock input to 8-bit timer (TM51).
TO51	Output	8-bit timer (TM51) output.
CKUPCL	Output	Clock output.
CKUBUZ	Output	Buzzer output.
TBI23 to TBI0	Input	Test bus input signal.
TBO38 to TBO0	Output	Test bus output signal.
TEST	Input	Test bus control signal input.
BUNRI	Input	Normal test mode select signal input.
TOTALCM	Input	Test mode select signal input.
DMBTM	Input	Test mode select signal input.
EMUMD	Input	Emulation mode.

2. 3 Electrical Specifications

The following specifications are for a single macro. An actual chip consists of two or more macros. Design the system so that all the specifications of the individual macros are satisfied when the chip is used.

2. 3. 1 Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

2. 3. 2 Recommended operation range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	–40		+85	°C

2. 3. 3 DC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1}	In normal operation mode		0.8	1.2	mA/MHz
	I_{DD2}	In HALT mode		0.2	0.3	mA/MHz
	I_{DD3}	In STOP mode		1.0	10	μA

2. 3. 4 AC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V, load capacitance of output pin C_L = 5 pF)

(1) Clock timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
CLKIN cycle time	<1>	t_{CYX}		120		ns
CLKIN input high-level width[Note]	<2>	t_{WXH}		50	64	ns
CLKIN input low-level width[Note]	<3>	t_{WXL}		50	64	ns
CPU operating frequency	–	ϕ		0	8.38	MHz

Note The slew rate clock is taken into consideration for the high-level and low-level widths of the clock, where the rate of change in the duty factor is 15% MAX.

(2) Fetch operation

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKIN to address	<4>	t_{DXA}	When divider is not used, CLKIN↓		25	ns
			When divider is used, CLKIN↑		25	ns
Delay time from CLKIN to ASTB	<5>	t_{DXST}			25	ns
Delay time from CLKIN to RDB↓↑	<6>	t_{DXR}			25	ns
Address hold time from CLKIN	<7>	t_{HXA}	When divider is not used, CLKIN↓	15		ns
			When divider is used, CLKIN↑	15		ns
Setup time from CLKIN to WAITB↓	<8>	t_{SXWT}	When divider is not used, CLKIN↑ $0.5t_{CYX}$ – 20 ns		40	ns
			When divider is used, CLKIN↓ $0.5t_{CYX}$ – 20 ns		40	ns
Hold time from CLKIN to WAITB↑	<9>	t_{HXWT}	When divider is not used, CLKIN↓	25		ns
			When divider is used, CLKIN↑	25		ns
Delay time from CLKIN to WAITB↑	<10>	t_{DXWT}	When divider is not used, CLKIN↑ $0.5t_{CYX}$ – 25 ns		35	ns
			When divider is used, CLKIN↓ $0.5t_{CYX}$ – 25 ns		35	ns
Delay time from address to ASTB↓	<15>	t_{DAST}	$0.5t_{CYK}$ – 30 ns	30		ns
ASTB high-level width	<16>	t_{WSTH}	$0.5t_{CYK}$ – 10 ns	50		ns
Setup time from address to data input*	<17>	t_{SAID}	$(1.5 + n)t_{CYK}$ – 50 ns		130	ns
Setup time from RDB↓ to data input*	<18>	t_{SRID}	$(1.0 + n)t_{CYK}$ – 50 ns		70	ns
RDB low-level width*	<19>	t_{WRL}	$(1.0 + n)t_{CYK}$ – 15 ns	105		ns
Read data hold time	<20>	t_{HRID}		0		ns
Delay time from RDB↑ to ASTB↑*	<21>	t_{DRSTL}	$0.5t_{CYK}$ – 20 ns	40		ns
Address hold time (from RDB↑)*	<22>	t_{HRA}	$0.5t_{CYK}$ – 20 ns	40		ns
Delay time from RDB↑ to ASTB↓*	<23>	t_{DRSTH}	t_{CYK} – 20 ns	100		ns
Setup time from ASTB↓ to data input*	<24>	t_{SSTID}	$(1.0 + n)t_{CYK}$ – 50 ns		70	ns
Setup time from address to WAITB↓*	<31>	t_{SAWT}	t_{CYK} – 40 ns		80	ns
Setup time from ASTB↓ to WAITB↓*	<32>	t_{SSTWT}	$0.5t_{CYK}$ – 30 ns		30	ns
Hold time from ASTB↓ to WAITB↑*	<33>	t_{HSTWT}	$(n – 0.5)t_{CYK}$ + 10 ns	70		ns
Delay time from ASTB↓ to WAITB↑*	<34>	t_{DSTWT}	$(0.5 + n)t_{CYK}$ – 40 ns		140	ns
Setup time from RDB↓ to WAITB↓*	<35>	t_{SRWT}	$0.5t_{CYK}$ – 30 ns		30	ns
Hold time from RDB↓ to WAITB↑*	<36>	t_{HRWT}	$(n – 0.5)t_{CYK}$ + 10 ns	70		ns
Setup time from WAITB↑ to data input	<38>	t_{SWTID}	$0.5t_{CYK}$ – 10 ns		50	ns
Delay time from WAITB↑ to RDB↑	<39>	t_{DWTR}	$0.5t_{CYK}$ + 40 ns	100		ns

Remarks 1. t_{CYX}: CLKIN cycle time (120 ns (MIN.))

2. t_{CYK}: CPU clock selected with processor clock control register (PCC) (120 ns (MIN.))

3. n: Number of wait cycles (software wait: n = 1, external wait input: n ≥ 1)

4. The minimum and maximum values are calculated where $t_{CYX} = t_{CYK}$ = 120 ns.

5. The values of the operations marked * differ from the calculated value during data access read.

(3) Data access read operation

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKIN to address	<4>	t_{DXA}	When divider is not used, CLKIN↓		25	ns
			When divider is used, CLKIN↑		25	ns
Delay time from CLKIN to ASTB	<5>	t_{DXST}			25	ns
Delay time from CLKIN to RDB↓↑	<6>	t_{DXR}			25	ns
Hold time from CLKIN to address	<7>	t_{HXA}	When divider is not used, CLKIN↓	15		ns
			When divider is used, CLKIN↑	15		ns
Setup time from CLKIN↓ to WAITB↓ input	<8>	t_{SXWT}	$0.5t_{CYX}$ – 20 ns		40	ns
Hold time from CLKIN↑ to WAITB↑	<9>	t_{HXWT}		25		ns
Delay time from CLKIN to WAITB↑	<10>	t_{DXWT}	When divider is not used, CLKIN↓ $0.5t_{CYX}$ – 25 ns		35	ns
			When divider is used, CLKIN↑ $0.5t_{CYX}$ – 25 ns		35	ns
Delay time from address to ASTB↓	<15>	t_{DAST}	$0.5t_{CYK}$ – 30 ns	30		ns
ASTB high-level width	<16>	t_{WSTH}	$0.5t_{CYK}$ – 10 ns	50		ns
Setup time from address to data input*	<17>	t_{SAID}	$(2 + n)t_{CYK}$ – 50 ns		190	ns
Setup time from RDB↓ to data input*	<18>	t_{SRID}	$(1.5 + n)t_{CYK}$ – 50 ns		130	ns
RDB low-level width*	<19>	t_{WRL}	$(1.5 + n)t_{CYK}$ – 15 ns	165		ns
Read data hold time	<20>	t_{HRID}		0		ns
Delay time from RDB↑ to ASTB↑*	<21>	t_{DRSTL}	t_{CYK} – 20 ns	100		ns
Address hold time (from RDB↑)*	<22>	t_{HRA}	t_{CYK} – 20 ns	100		ns
Delay time from RDB↑ to ASTB↓*	<23>	t_{DRSTH}	$1.5t_{CYK}$ – 20 ns	160		ns
Setup time from ASTB↓ to data input*	<24>	t_{SSTID}	$(1.5 + n)t_{CYK}$ – 50 ns		0	ns
Setup time from address to WAITB↓*	<31>	t_{SAWT}	$1.5t_{CYK}$ – 40 ns		140	ns
Setup time from ASTB↓ to WAITB↓*	<32>	t_{SSTWT}	t_{CYK} – 30 ns		90	ns
Hold time from ASTB↓ to WAITB↑*	<33>	t_{HSTWT}	nt_{CYK} + 10 ns	130		ns
Delay time from ASTB↓ to WAITB↑*	<34>	t_{DSTWT}	$(1 + n)t_{CYK}$ – 40 ns		200	ns
Setup time from RDB↓ to WAITB↓*	<35>	t_{SRWT}	t_{CYK} – 30 ns		90	ns
Hold time from RDB↓ to WAITB↑*	<36>	t_{HRWT}	nt_{CYK} + 10 ns	130		ns
Delay time from RDB↓ to WAITB↑	<37>	t_{DASWT}	$(1 + n)t_{CYK}$ – 40 ns		200	ns
Setup time from WAITB↑ to data input	<38>	t_{SWTID}	$0.5t_{CYK}$ – 10 ns		50	ns
Delay time from WAITB↑ to RDB↑	<39>	t_{DWTR}	$0.5t_{CYK}$ + 40 ns	100		ns

Remarks 1. t_{CYX}: CLKIN cycle time (120 ns (MIN.))

2. t_{CYK}: CPU clock selected with processor clock control register (PCC) (120 ns (MIN.))

3. n: Number of wait cycles (software wait: n = 1, external wait input: n ≥ 1)

4. The minimum and maximum values are calculated where $t_{CYX} = t_{CYK} = 120$ ns.

5. The values of the operations marked * differ from the calculated value during fetch.

(4) Data access write operation

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKIN to address	<4>	t_{DXA}	When divider is not used, CLKIN↓		25	ns
			When divider is used, CLKIN↑		25	ns
Delay time from CLKIN to ASTB	<5>	t_{DXST}			25	ns
Hold time from CLKIN to address	<7>	t_{HXA}	When divider is not used, CLKIN↓	15		ns
			When divider is used, CLKIN↑	15		ns
Setup time from CLKIN to WAITB↓	<8>	t_{SXWT}	When divider is not used, CLKIN↑ 0.5 t_{CYX} – 20 ns		40	ns
			When divider is used, CLKIN↓ 0.5t_{CYX} – 20 ns		40	ns
Hold time from CLKIN to WAITB↑	<9>	t_{HXWT}	When divider is not used, CLKIN↓	25		ns
			When divider is used, CLKIN↑	25		ns
Delay time from CLKIN to WAITB↑	<10>	t_{DXWT}	When divider is not used, CLKIN↑ 0.5t_{CYX} – 25 ns		35	ns
			When divider is used, CLKIN↓ 0.5t_{CYX} – 25 ns		35	ns
Delay time from CLKIN↑ to WRB↓↑	<11>	t_{DXW}			25	ns
Delay time from CLKIN↑ to data output	<12>	t_{DKOD}			75	ns
Write data hold time (from CLKIN)	<13>	t_{HKOD}		15		ns
Delay time from WRB↑ to ASTB↑	<14>	t_{DWST}	t_{CYK} – 20 ns	100		ns
Delay time from address to ASTB↓	<15>	t_{DAST}	0.5t_{CYK} – 30 ns	30		ns
ASTB high-level width	<16>	t_{WSTH}	0.5t_{CYK} – 10 ns	50		ns
Delay time from ASTB↓ to WRB↓	<25>	t_{DSTW}	t_{CYK} – 15 ns	105		ns
WRB low-level width	<26>	t_{WWL}	(1.0 + n)t_{CYK} – 15 ns	105		ns
Delay time from WRB↓ to data output	<27>	t_{DWOD}			50	ns
Data setup time (to WRB↑)	<28>	t_{SODW}	(1.0 + n)t_{CYK} – 50 ns	70		ns
Data hold time (from WRB↑)	<29>	t_{HODW}	0.5t_{CYK} – 15 ns	45		ns
Address hold time (from WRB↑)	<30>	t_{HAW}	0.5t_{CYK} – 20 ns	40		ns
Setup time from address to WAITB↓	<31>	t_{SAWT}	2t_{CYK} – 40 ns		200	ns
Setup time from ASTB↓ to WAITB↓	<32>	t_{SSTWT}	1.5t_{CYK} – 30 ns		150	ns
Hold time from ASTB↓ to WAITB↑	<33>	t_{HSTWT}	(0.5 + n)t_{CYK} + 10 ns	190		ns
Delay time from ASTB↓ to WAITB↑	<34>	t_{DSTWT}	(1.5 + n)t_{CYK} – 40 ns		260	ns
Delay time from WAITB↑ to WRB↑	<40>	t_{DWTW}	0.5t_{CYK} + 40 ns	100		ns
Setup time from WRB↓ to WAITB↓	<41>	t_{SWWT}	0.5t_{CYK} – 30 ns		30	ns
Hold time from WRB↓ to WAITB↑	<42>	t_{HWWT}	(n – 0.5)t_{CYK} + 10 ns	70		ns
Delay time from WRB↓ to WAITB↑	<43>	t_{DWWT}	(0.5 + n)t_{CYK} – 40 ns		140	ns

Remarks 1. t_{CYX}: CLKIN cycle time (120 ns (MIN.))

2. t_{CYK}: CPU clock selected with processor clock control register (PCC) (120 ns (MIN.))

3. n: Number of wait cycles (software wait: n = 1, external wait input: n ≥ 1)

4. The minimum and maximum values are calculated where t_{CYX} = t_{CYK} = 120 ns.

(5) Basic operation

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	–	T_{CY}	Operates with main system clock	0.24		32	μs
			Operates with subsystem clock	40	122	125	μs
TI01, TI00 input high-/low-level width	<44>	t_{TIH0}		$2/f_{sam}$ +0.1 Note			μs
	<45>	t_{TIL0}					
TI51, TI50 input frequency	<46>	f_{TI5}		0		10	MHz
TI51, TI50 input high-/low-level width	<47>	t_{TIH5}		40			ns
	<48>	t_{TIL5}					
Interrupt request input high-level width	<49>	t_{INTH}	INT11 to INT0	1			μs
RESETB low-level width	<50>	t_{RSL}		10			μs

Note f_{sam} = fx, fx/4, or fx/64 can be selected by using bits 0 and 1 (PRM00 and PRM01) of the prescaler mode register 0 (PRM0). However, if the TI00 valid edge is selected as the count clock, f_{sam} = fx/8.

(6) Serial interface

(a) 3-wire serial I/O mode (SCK31OB, SCK30OB ... internal clock output)

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
SCK31OB, SCK30OB cycle time	<51>	t_{KCY1}		954			ns
SCK31OB, SCK30OB high-/low-level width	<52>	t_{KH1}		$t_{KCY1}/2$ –20			ns
	<53>	t_{KL1}					
SI31, SI30 setup time (to SCK31OB, SCK30OB↑)	<54>	t_{SIK1}		50			ns
SI31, SI30 hold time (from SCK31OB, SCK30OB↑)	<55>	t_{KSI1}		70			ns
Delay time from SCK31OB, SCK30OB↓ to SO31, SO30 output	<56>	t_{KSO1}				70	ns

(b) 3-wire serial I/O mode (SCK31IB, SCK30IB ... external clock input)

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
SCK31IB, SCK30IB cycle time	<57>	t_{KCY2}		800			ns
SCK31IB, SCK30IB high-/low-level width	<58>	t_{KH2}		380			ns
	<59>	t_{KL1}					
SI31, SI30 setup time (to SCK31IB, SCK30IB↑)	<60>	t_{SIK2}		50			ns
SI31, SI30 hold time (from SCK31IB, SCK30IB↑)	<61>	t_{KSI2}		70			ns
Delay time from SCK31IB, SCK30IB↓ to SO31, SO30 output	<62>	t_{KSO2}				70	ns

(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate	–				262144	bps

(d) UART mode (infrared data transfer mode)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate	–			115200	bps
Permissible bit rate error	–			±0.87	%
Number of output pulses	–		1.2	0.24/fbr	μs
Number of input pulses	–		4/f_X		μs

Remark fbr: set baud rate

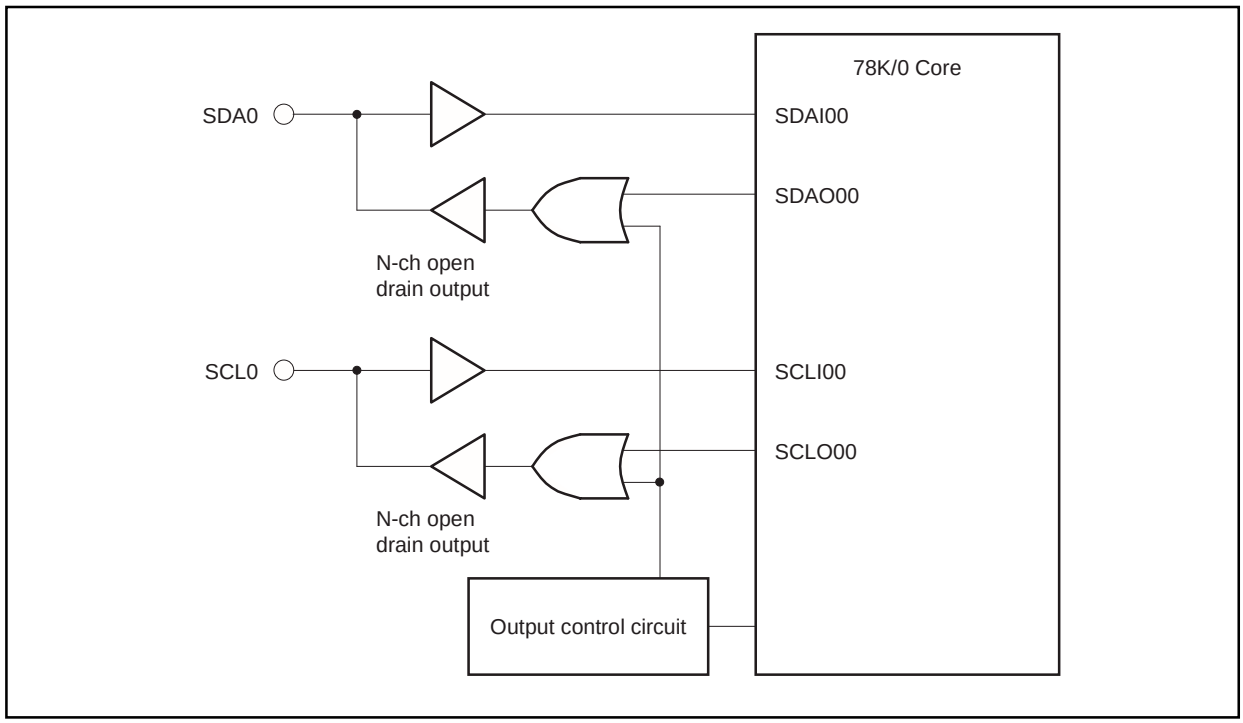
(e) I^2C bus mode

Parameter	Symbol		Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency	<63>	f_{CLK}	0	100	0	400	kHz
Bus free time (between stop and start conditions)	<64>	t_{BUF}	4.8		1.4		μs
Hold time[Note]	<65>	t_{HD} : STA	4.1		0.7		μs
Low-level width of SCL0 clock	<66>	t_{LOW}	5.0		1.25		μs
High-level width of SCL0 clock	<67>	t_{HIGH}	5.0		1.25		μs
Setup time of start/restart condition	<68>	t_{SU} : STA	4.8		0.7		μs
Data setup time (reception)	<69>	t_{SU} : DAT	0		0		ns
Data hold time (transmission)	<70>	t_{HD} : DAT	0.72	3.5	0.48	1.0	μs

Note The first clock pulse is created after this period in the start condition.

Caution The serial data line (SDA0) and serial clock line (SCL0) pins of serial interface (IIC0) incorporated in the 78K/0 core are separated to input pins (SDAI00, SCLI00) and output pins (SDAO00, SCLO00). Therefore, when the configuration consists of external device and I^2C bus, the circuit should be as shown in Figure 2-1 (for details, refer to 78K/0 Core User's Manual (A13142E)).

Figure 2-1. Example of Circuit Construction of Serial Interface (IIC0) Input/Output Pin



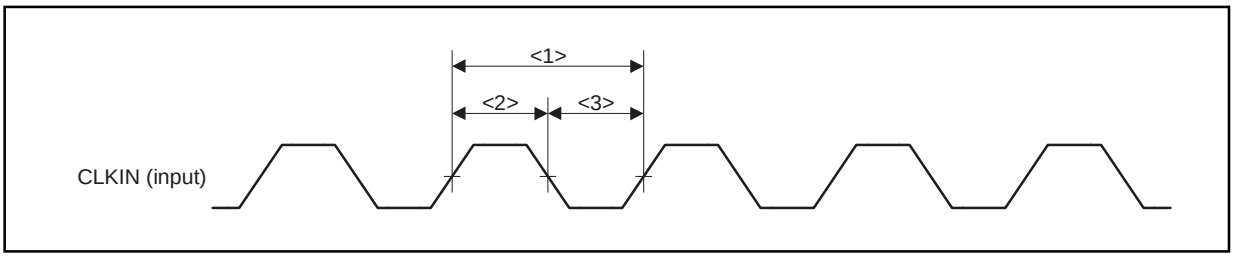
2. 3. 5 Low-voltage data retention characteristics of data memory in STOP mode (T_A = –40 to +85°C)

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
Release signal set time	<72>	t_{SREL}		0			μs
Oscillation stabilization wait time[Note]	<73>	t_{WAIT}	Released by RESETB		0		ms
			Released by interrupt request		0		ms

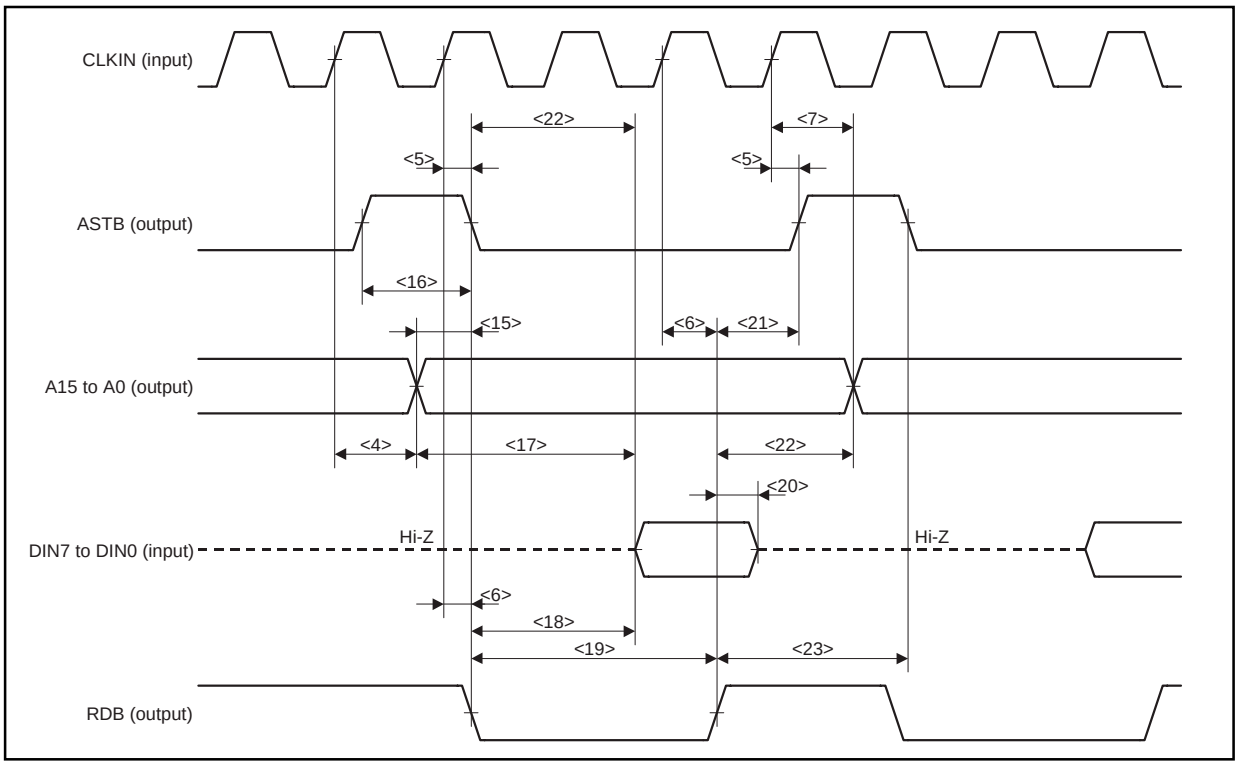
Note The user should ensure the lapse of the oscillation stabilization time if necessary.

2. 4 Timing Chart

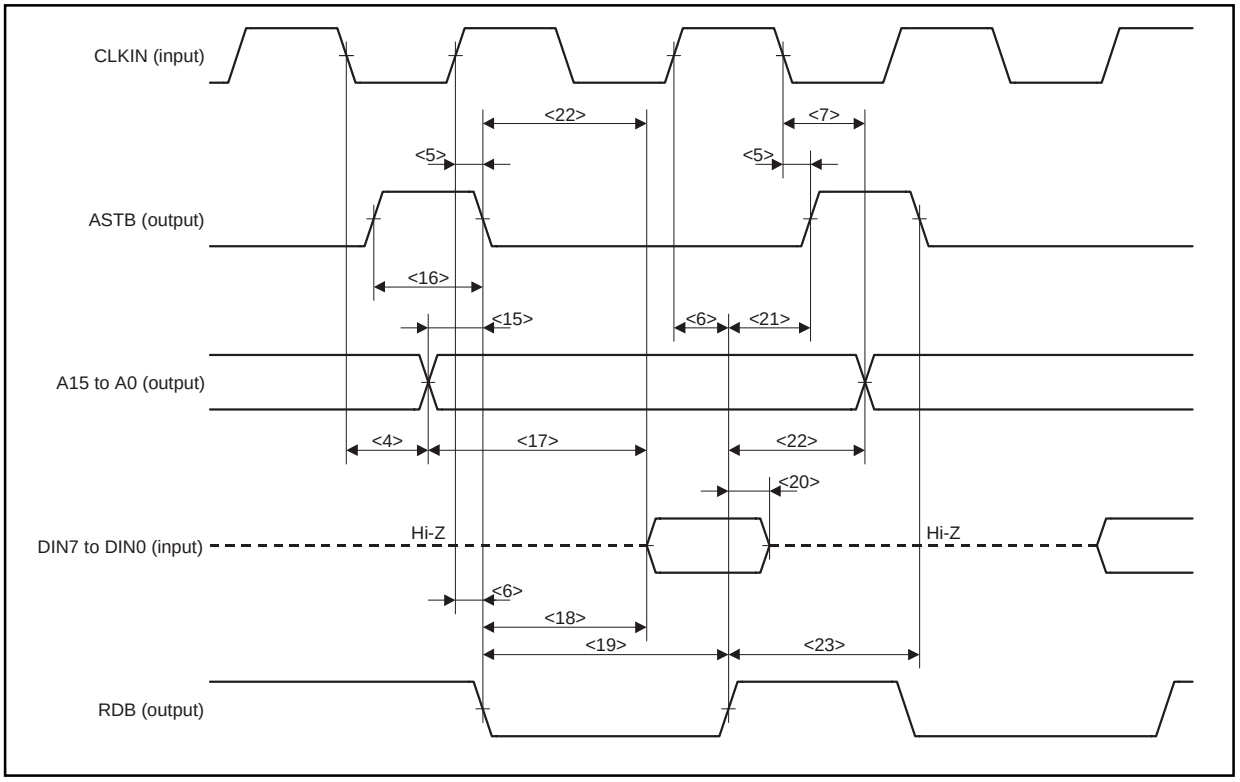
(1) Clock timing



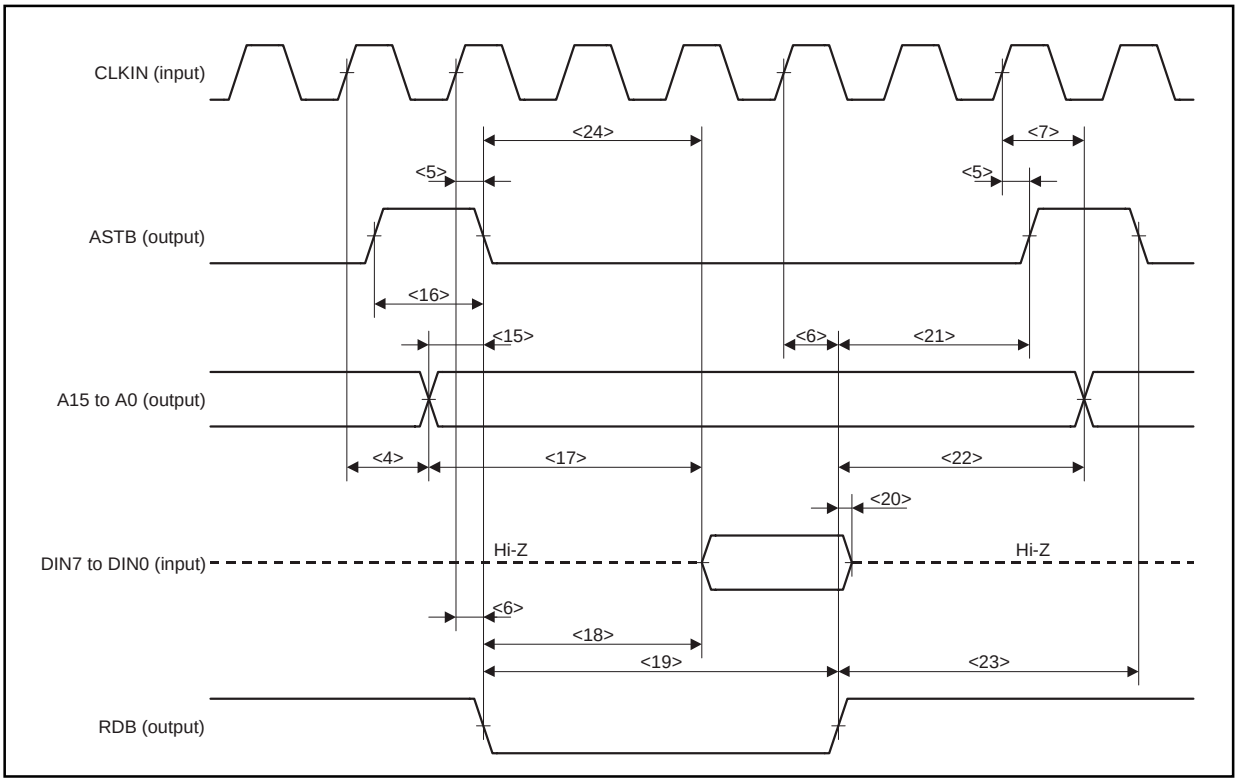
(2) Fetch timing 1 (when divider (fx/2) is used, no wait)



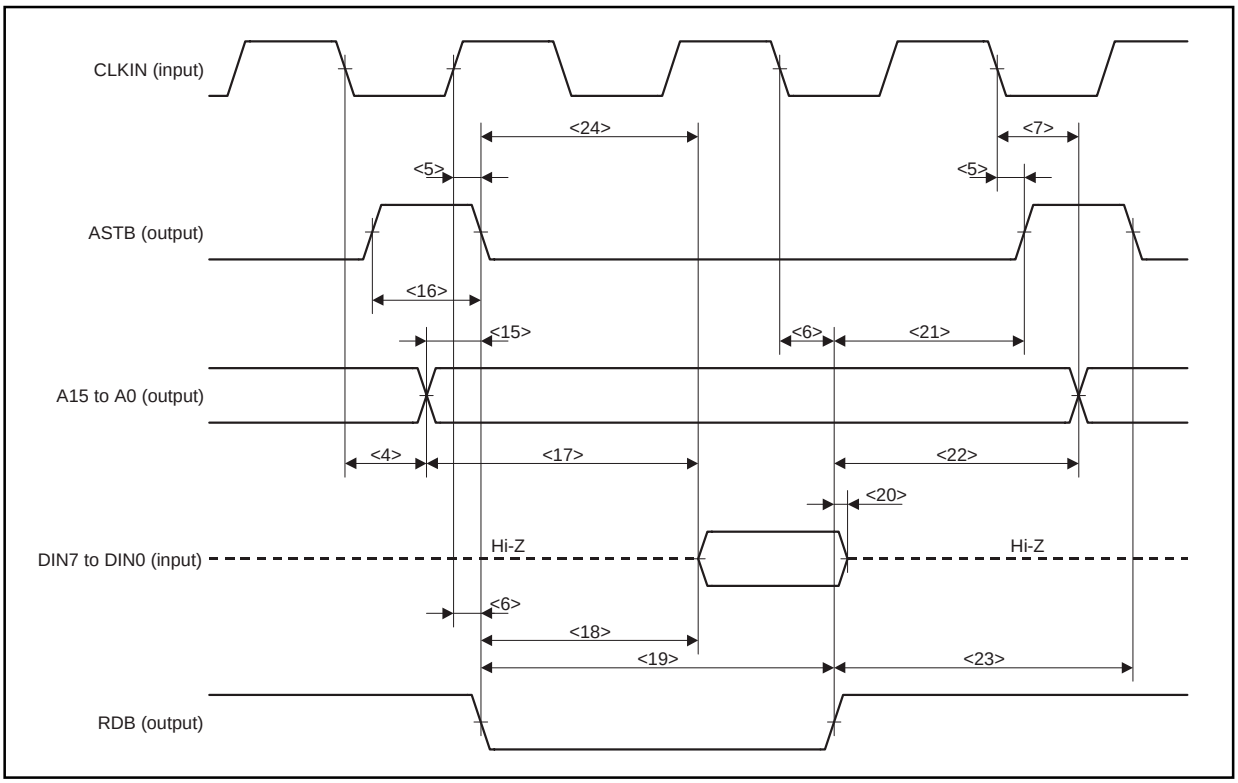
(3) Fetch timing 2 (when divider is not used, no wait)



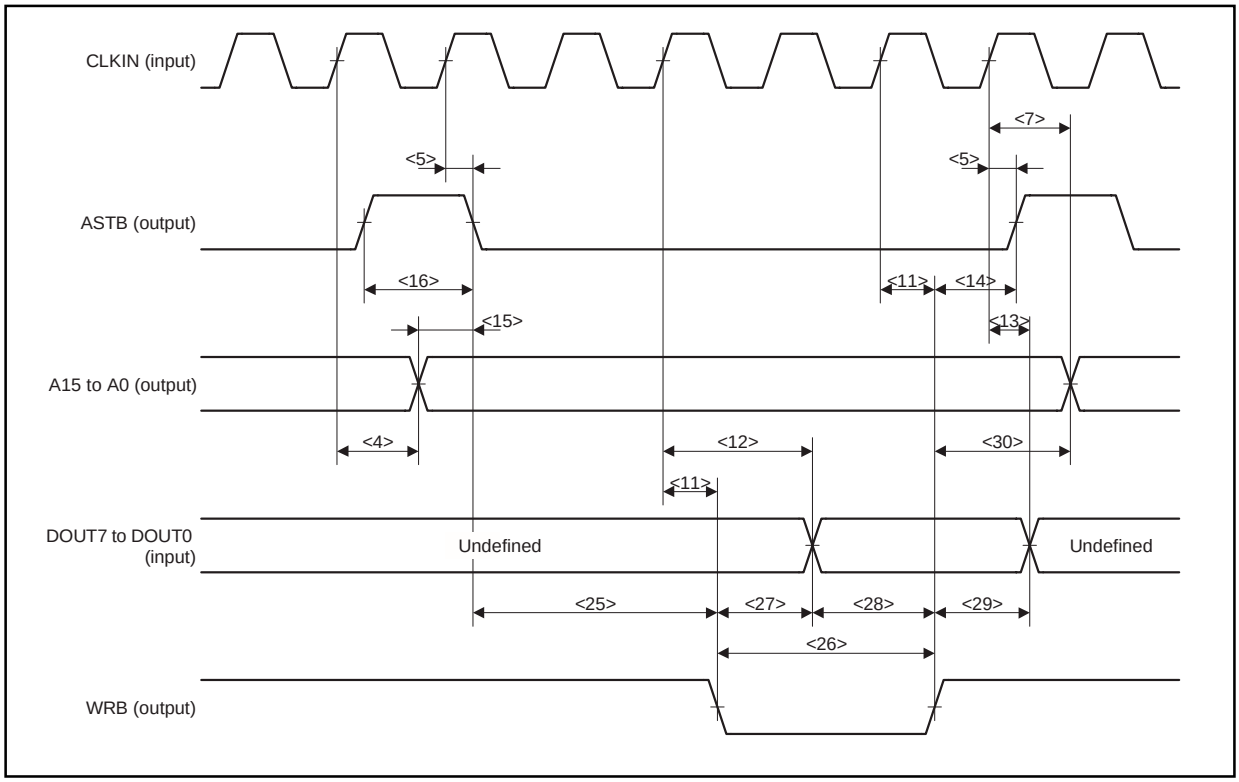
(4) Read timing 1 (when data is accessed and when divider is used, no wait)



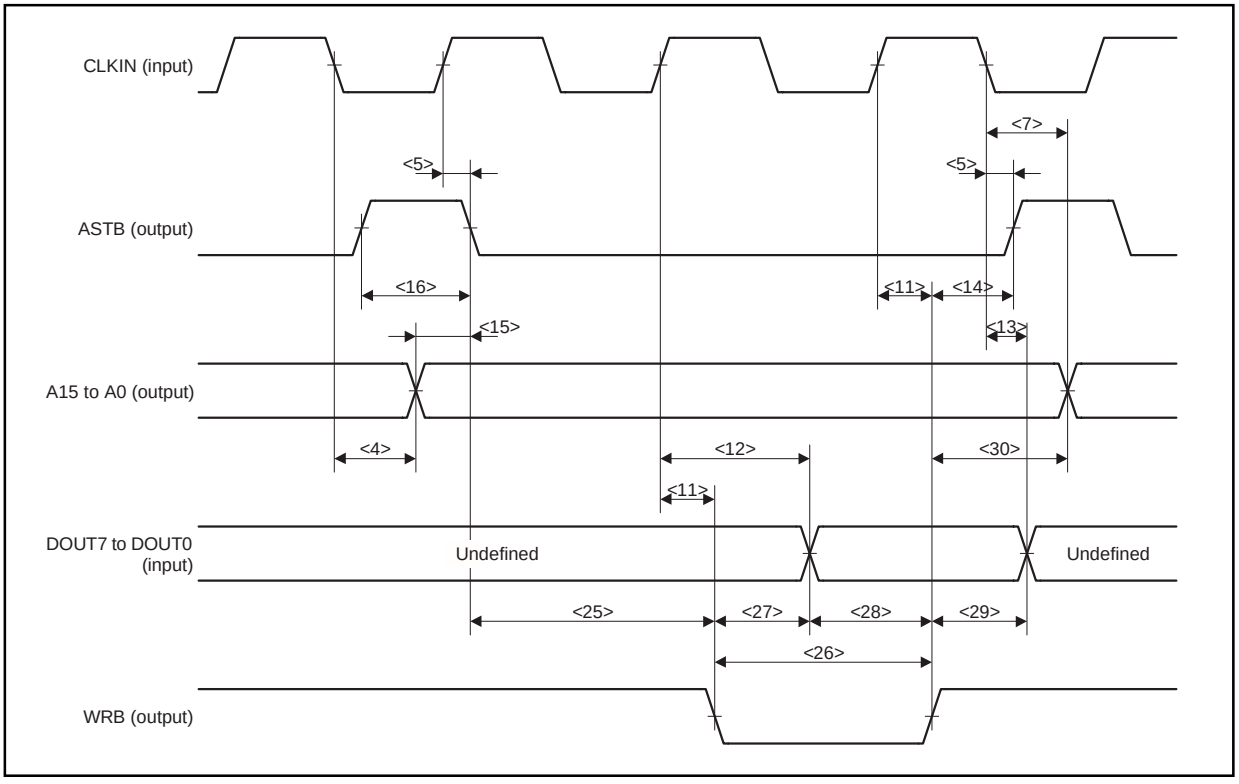
(5) Read timing 2 (when data is accessed and when divider is not used, no wait)



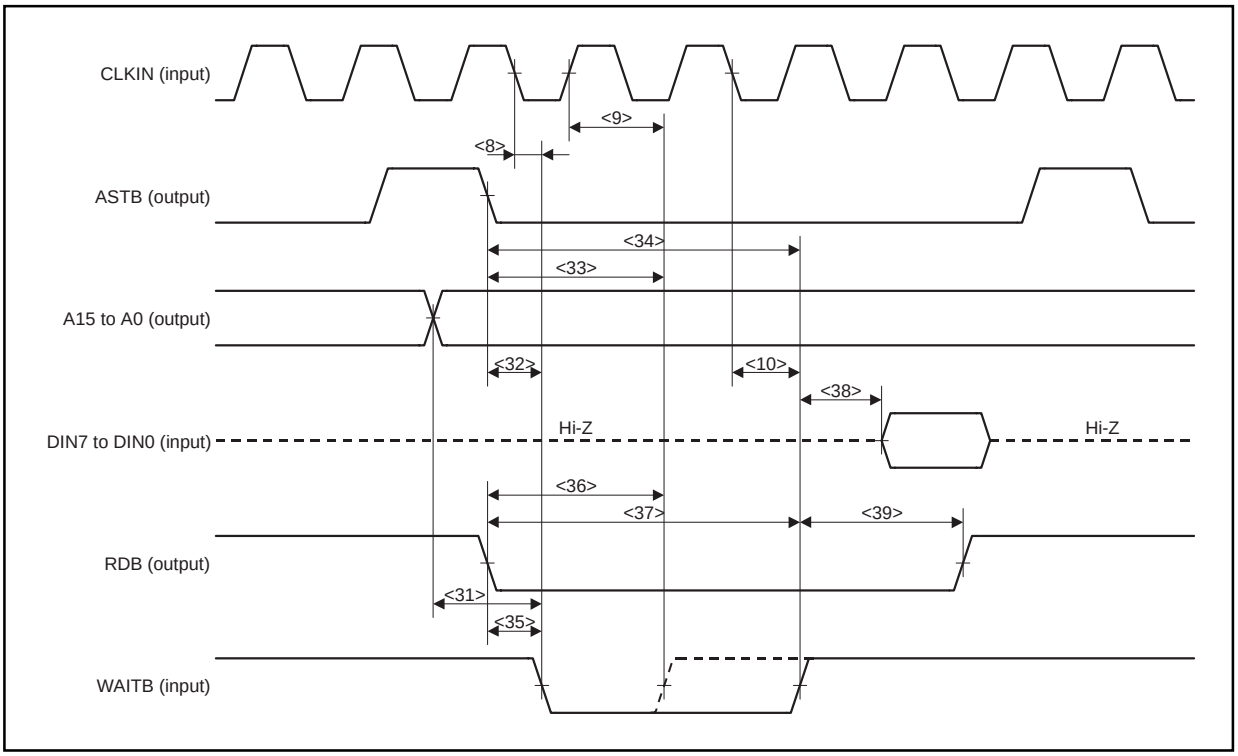
(6) Write timing 1 (when data is accessed and when divider is used, no wait)



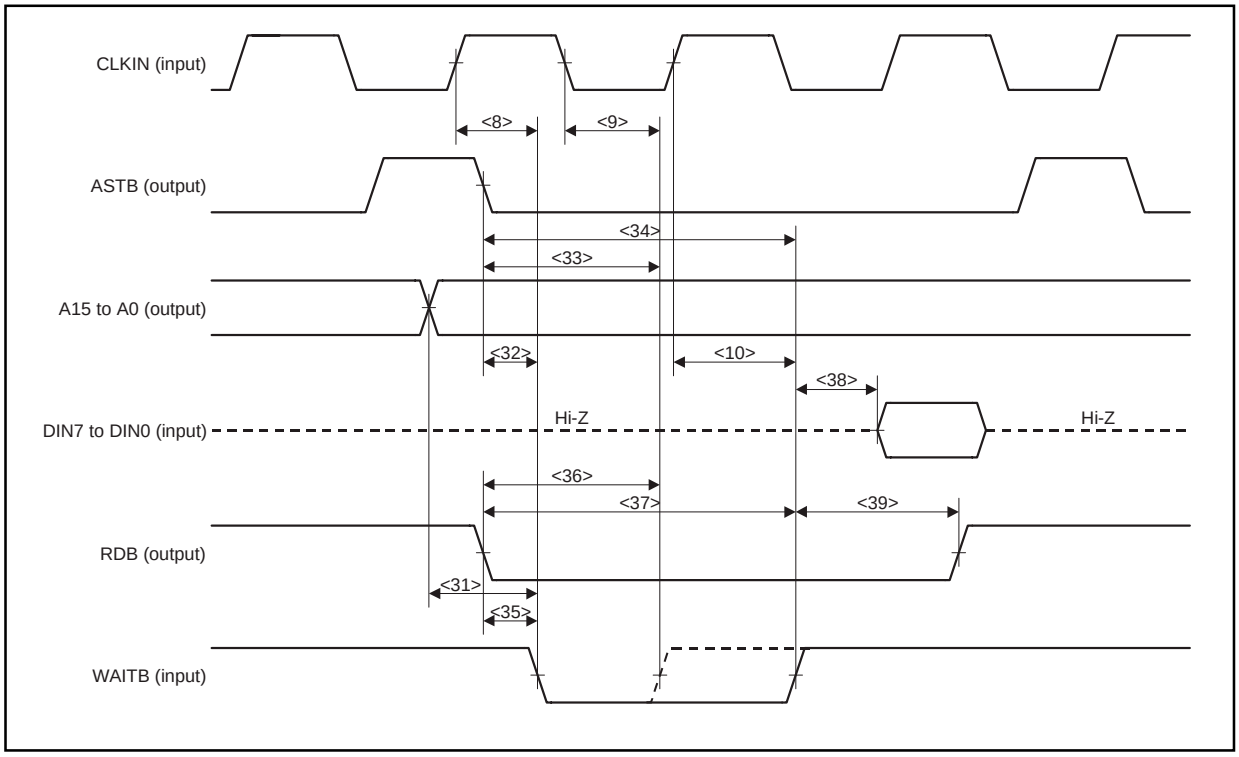
(7) Write timing 2 (when data is accessed and when divider is not used, no wait)



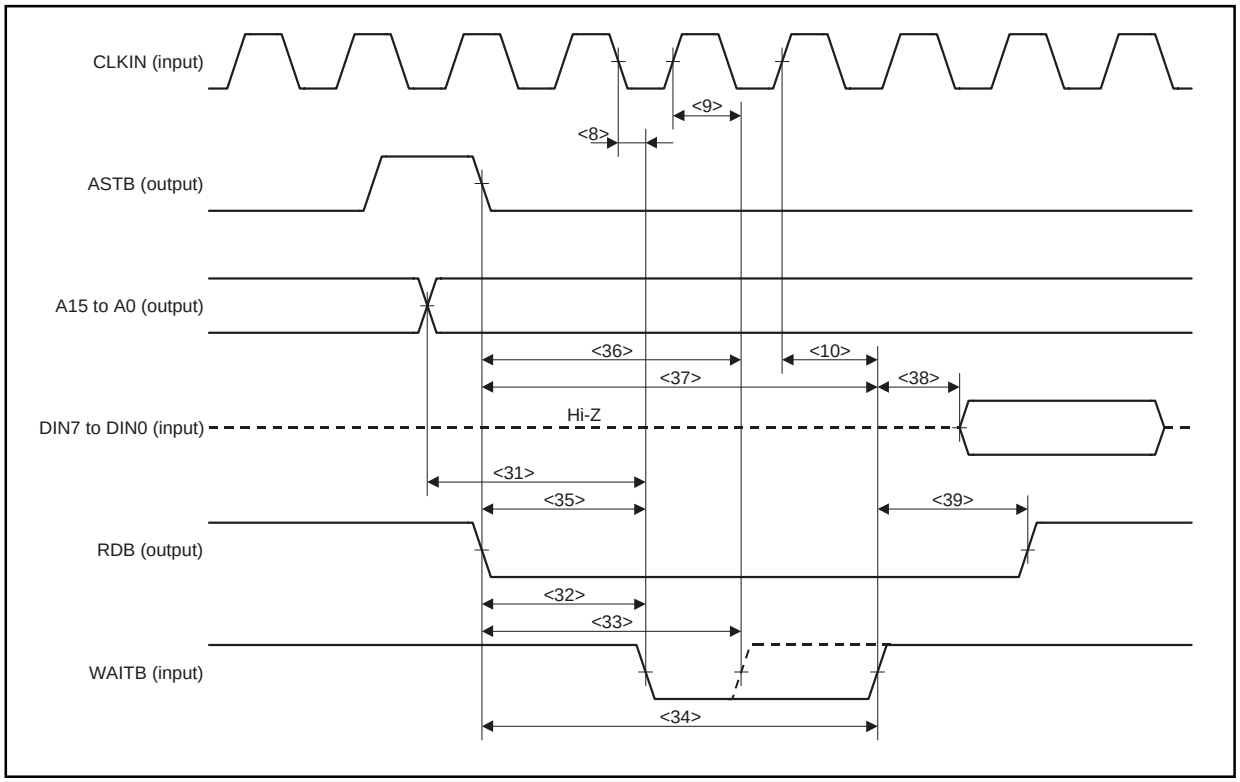
(8) External wait input fetch timing 1 (when divider is used, 1 wait)



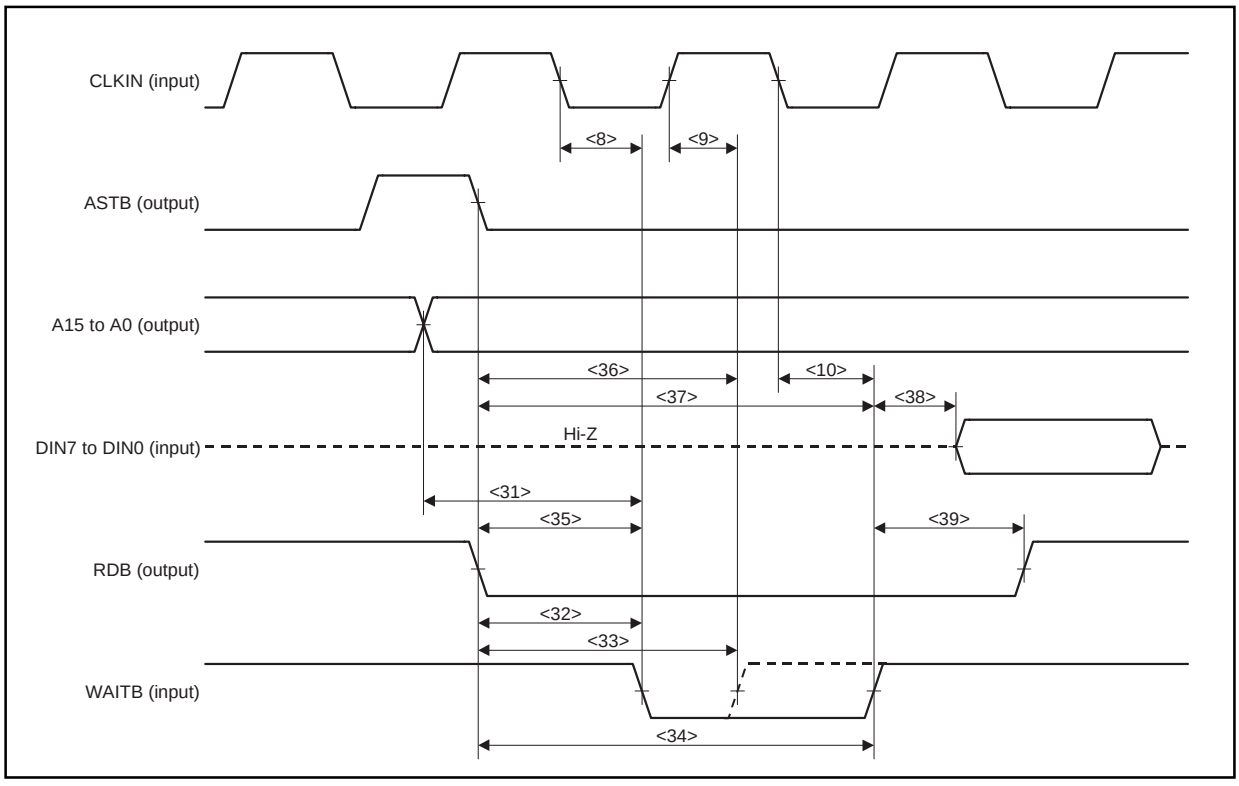
(9) External wait input fetch timing 2 (when divider is not used, 1 wait)



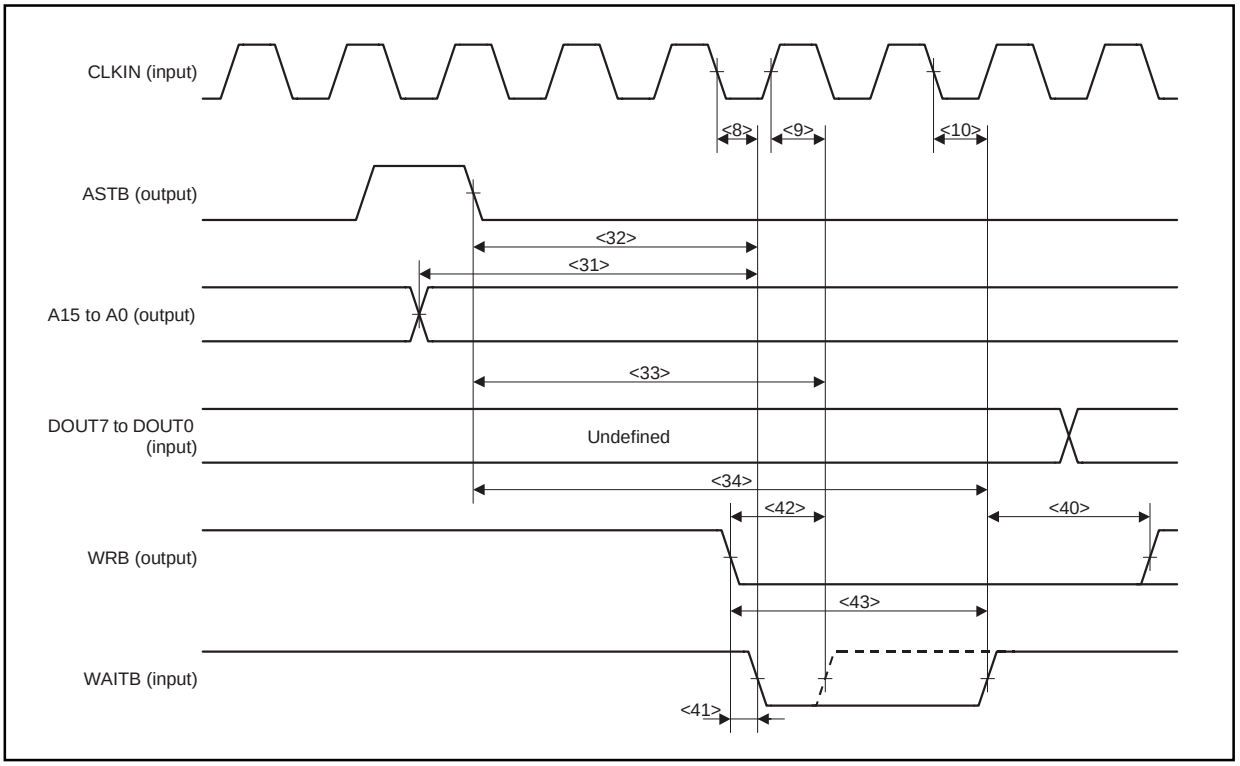
(10) External wait input read timing 1 (when data is accessed and when divider is used, 1 wait)



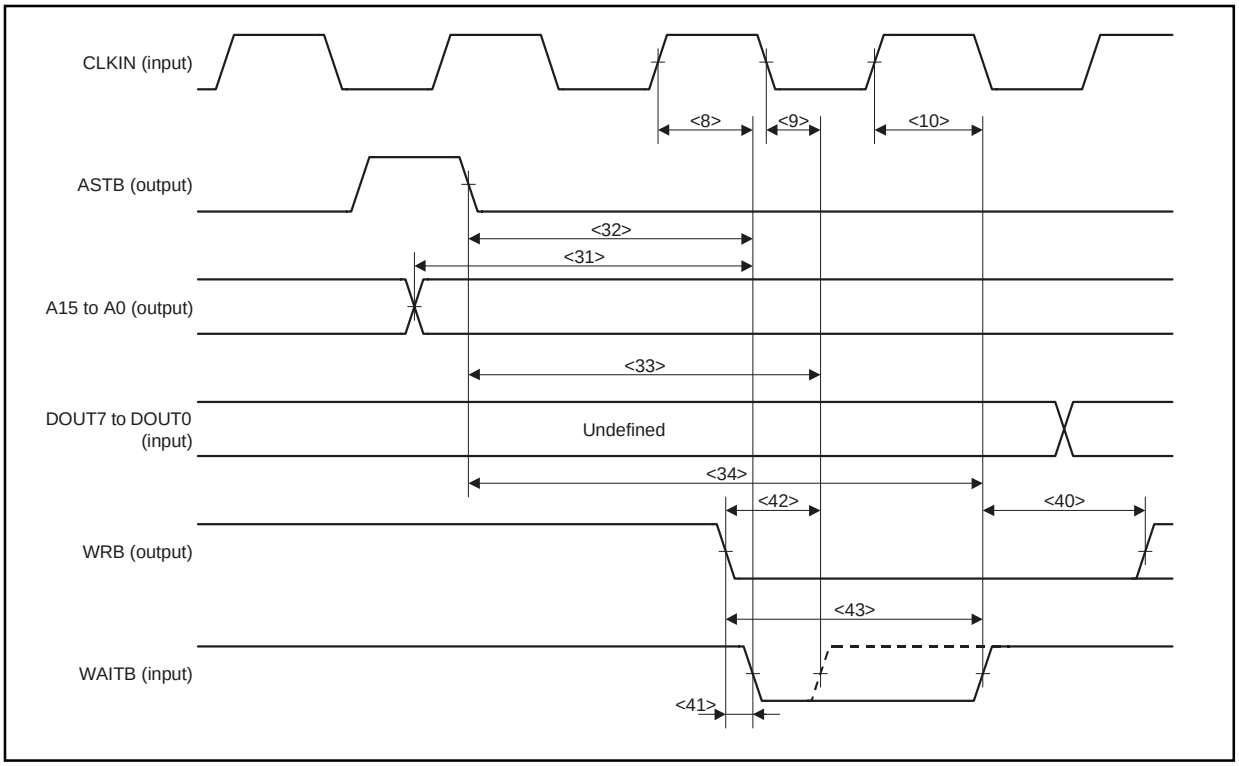
(11) External wait input read timing 2 (when data is accessed and when divider is not used, 1 wait)



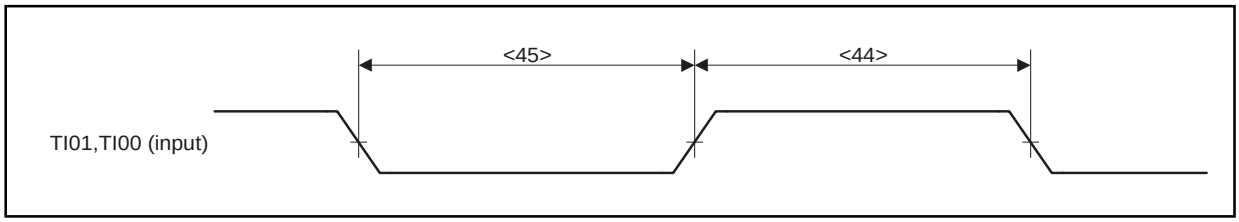
(12) External wait input write timing 1 (when data is accessed and when divider is used, 1 wait)

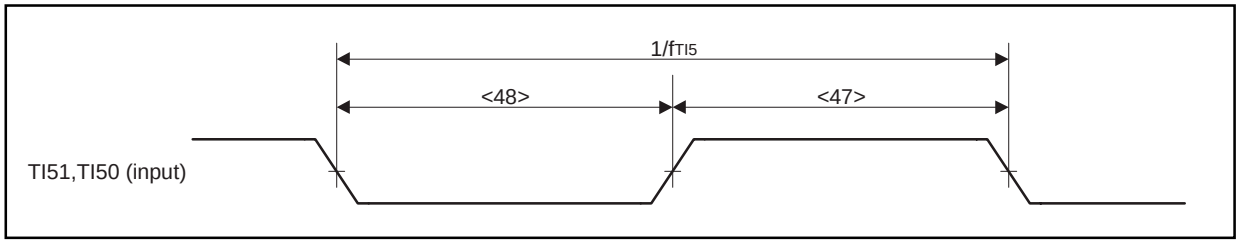


(13) External wait input write timing 2 (when data is accessed and when divider is not used, 1 wait)

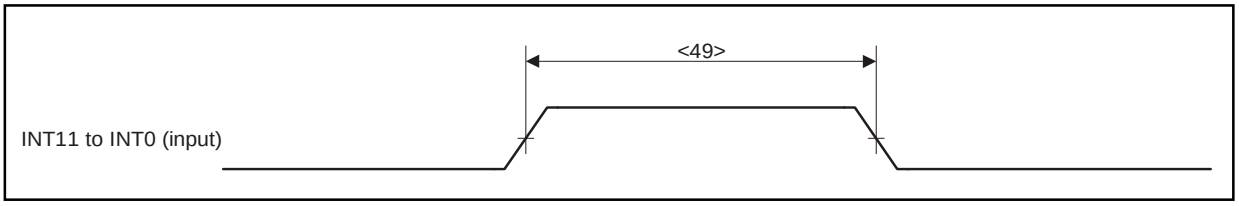


(14) TI timing

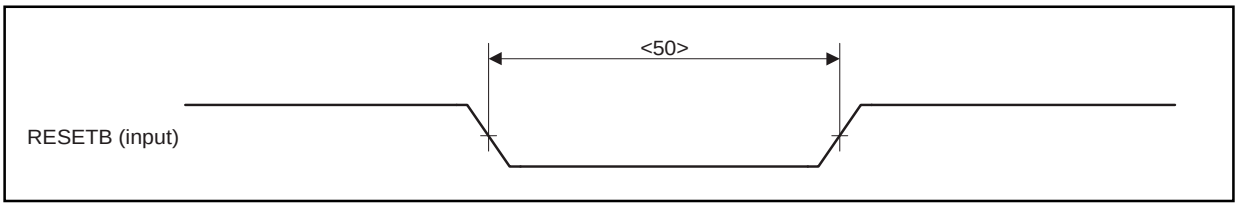




(15) Interrupt request input timing

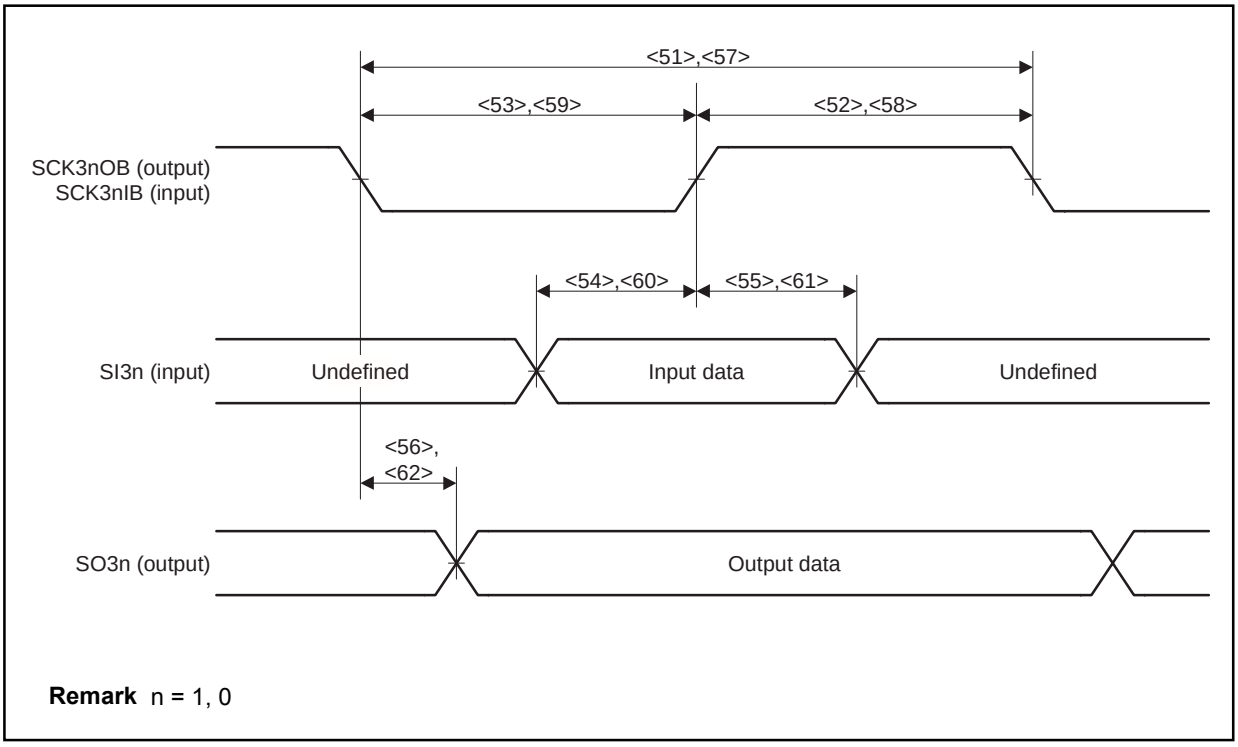


(16) RESETB input timing



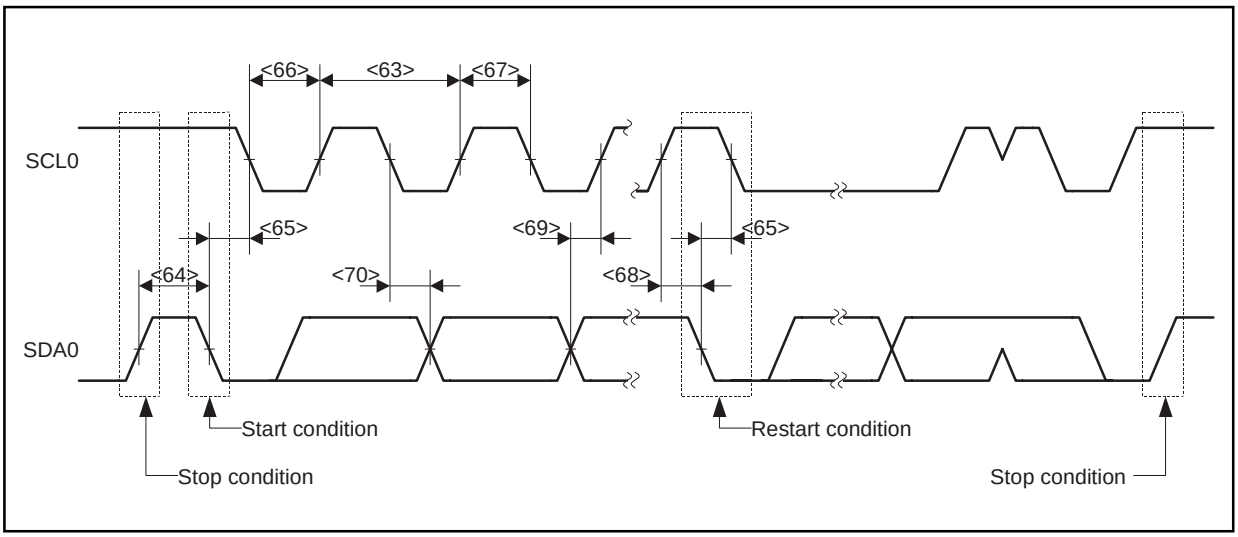
(17) Serial transfer timing

(a) 3-wire serial I/O mode

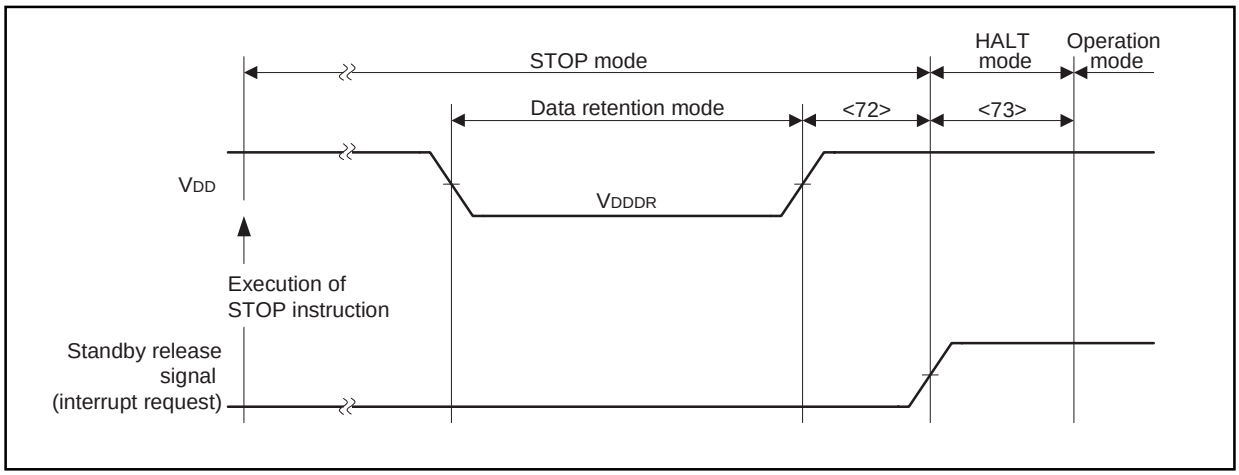


Remark n = 1, 0

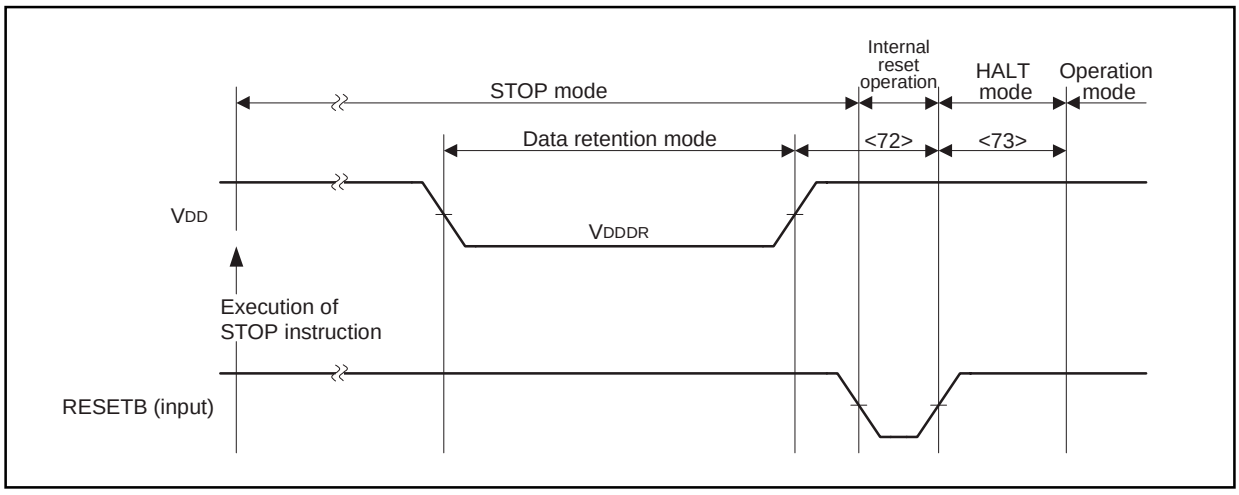
(b) I^2C bus mode



(18) Data retention timing (standby release signal: STOP mode is released by interrupt request signal)



(19) Data retention timing (STOP mode is released by RESETB)



CHAPTER 3 V851 CORE

The V851 core is a CPU core having peripheral functions such as a real-time pulse unit and serial interfaces. The instruction set of the V851 core is common to that of the V850 Family™ 32-bit single-chip microcontrollers.

3. 1 Outline

- CPU performance: 38 MIPS (@ 33 MHz operation)
- Internal memory (ROM can be removed.)
  Mask ROM: 48, 64, 96, 128, and 256 KB
  RAM: 4, 8, 16, and 24 KB
- Minimum instruction execution time: 30 ns (@ 33 MHz operation)
- External bus interface
  16-bit data bus (DIN/DOUT separated)
  24-bit address bus
- Interrupt/exception
  External interrupt: 9 (including NMI)
  Internal interrupt: 14 sources
  Software exception: 32 sources
  Exception trap: 1 source
  Eight priority levels can be specified.
- Real-time pulse unit
  16-bit timer/event counter: 1 ch
  16-bit interval timer: 1 ch
- Serial interface
  Asynchronous serial interface (UART): 1 ch
  Clocked serial interface (CSI): 1 ch
- Power save function
  HALT, STOP, IDLE mode
  Clock output stop function

3. 1. 1 Symbol diagram

Number of grids

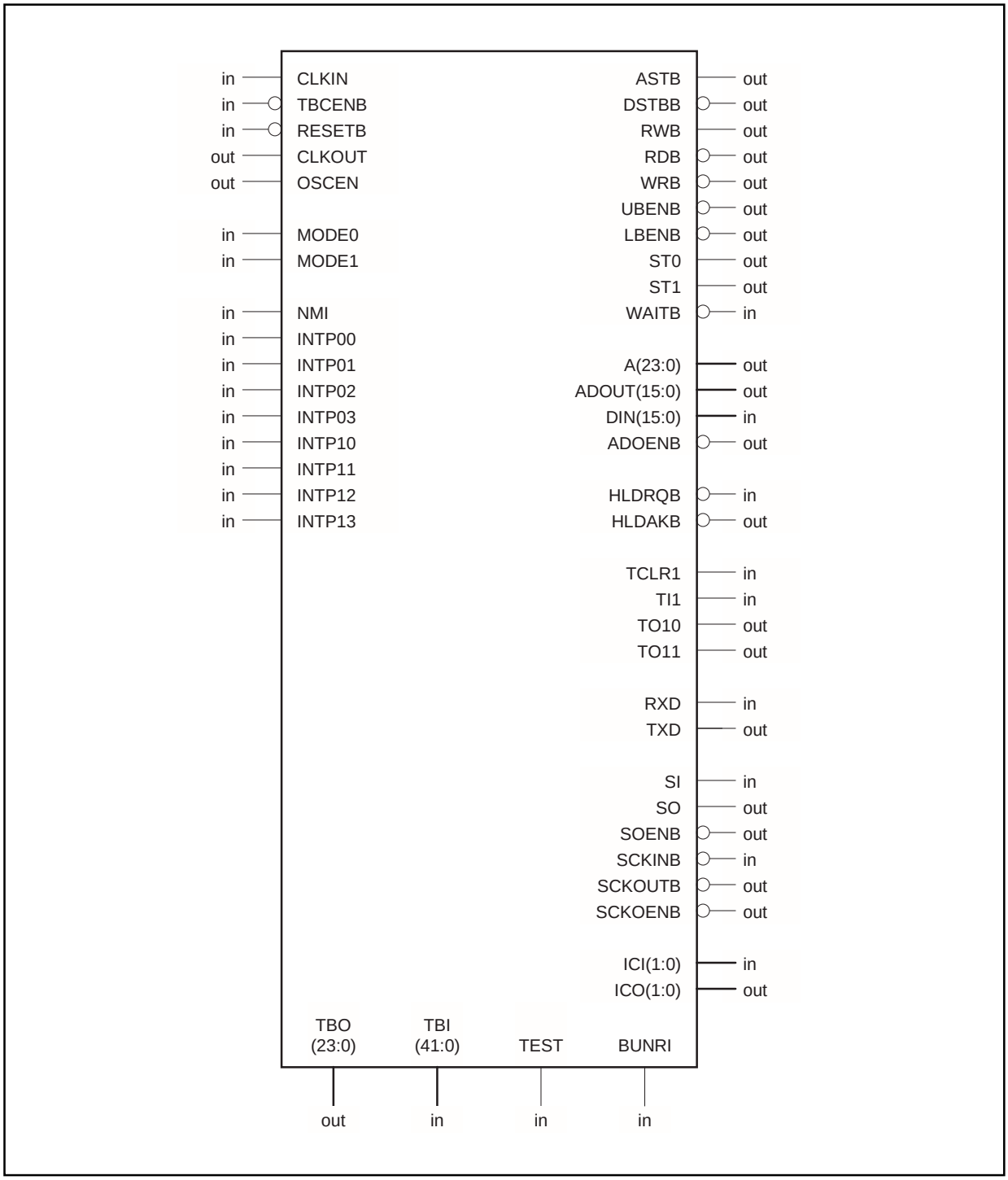
139k grids

156k grids (including wiring area)

Number of separation simulation patterns

ROM Size / RAM Size	0 byte (ROMless)	48 KB	64 KB	96 KB	128 KB	256 KB
4 KB	NA851M02 258.5k	NA851M32 270.6k	NA851M42 278.8k	NA851M62 295.2k	NA851M82 311.5k	NA851MG2 377.1k
8 KB	NA851M04 258.5k	NA851M34 270.6k	NA851M44 278.8k	NA851M64 295.2k	NA851M84 311.5k	NA851MG4 377.1k
16 KB	NA851M08 266.1k	NA851M38 278.2k	NA851M48 286.4k	NA851M68 302.8k	NA851M88 319.2k	NA851MG8 384.7k
24 KB	NA851M0C 266.1k	NA851M3C 278.2k	NA851M4C 286.4k	NA851M6C 302.8k	NA851M8C 319.2k	NA851MGC 384.7k

Remark The upper figure in each column of the above table indicates the part number and the lower figure indicates the total number of patterns.


in CLKIN
in TBCENB
in RESETB
out CLKOUT
out OSCEN
in MODE0
in MODE1
in NMI
in INTP00
in INTP01
in INTP02
in INTP03
in INTP10
in INTP11
in INTP12
in INTP13
ASTB out
DSTBB out
RWB out
RDB out
WRB out
UBENB out
LBENB out
ST0 out
ST1 out
WAITB in
A(23:0) out
ADOUT(15:0) out
DIN(15:0) in
ADOENB out
HLDRQB in
HLDAKB out
TCLR1 in
TI1 in
TO10 out
TO11 out
RXD in
TXD out
SI in
SO out
SOENB out
SCKINB in
SCKOUTB out
SCKOENB out
ICI(1:0) in
ICO(1:0) out
TBO (23:0) out
TBI (41:0) in
TEST in
BUNRI in

3. 1. 2 Pin capacitance

(1) Input pins

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
DIN15	0.025	1.925	SCKINB	0.015	1.915	TBI24	0.023	1.923
DIN14	0.020	1.920	SI	0.019	1.919	TBI23	0.024	1.924
DIN13	0.016	1.916	TBCENB	0.017	1.917	TBI22	0.015	1.915
DIN12	0.022	1.922	TI1	0.021	1.921	TBI21	0.017	1.917
DIN11	0.021	1.921	TCLR1	0.028	1.928	TBI20	0.015	1.915
DIN10	0.021	1.921	RXD	0.013	1.913	TBI19	0.020	1.920
DIN9	0.024	1.924	WAITB	0.171	2.071	TBI18	0.019	1.919
DIN8	0.018	1.918	NMI	0.015	1.915	TBI17	0.027	1.927
DIN7	0.015	1.915	RESETB	0.027	1.927	TBI16	0.019	1.919
DIN6	0.021	1.921	ICI1	0.013	1.913	TBI15	0.018	1.918
DIN5	0.016	1.916	ICI0	0.013	1.913	TBI14	0.016	1.916
DIN4	0.014	1.914	TBI41	0.064	1.964	TBI13	0.018	1.918
DIN3	0.014	1.914	TBI40	0.023	1.923	TBI12	0.015	1.915
DIN2	0.014	1.914	TBI39	0.022	1.922	TBI11	0.014	1.914
DIN1	0.015	1.915	TBI38	0.016	1.916	TBI10	0.013	1.913
DIN0	0.033	1.933	TBI37	0.011	1.911	TBI9	0.014	1.914
CLKIN	0.020	1.920	TBI36	0.022	1.922	TBI8	0.016	1.916
HLDRQB	0.137	2.037	TBI35	0.014	1.914	TBI7	0.019	1.919
INTP13	0.014	1.914	TBI34	0.022	1.922	TBI6	0.013	1.913
INTP12	0.013	1.913	TBI33	0.014	1.914	TBI5	0.017	1.917
INTP11	0.014	1.914	TBI32	0.014	1.914	TBI4	0.019	1.919
INTP10	0.014	1.914	TBI31	0.156	2.056	TBI3	0.020	1.920
INTP03	0.016	1.916	TBI30	0.147	2.047	TBI2	0.019	1.919
INTP02	0.014	1.914	TBI29	0.018	1.918	TBI1	0.020	1.920
INTP01	0.021	1.921	TBI28	0.024	1.924	TBI0	0.038	1.938
INTP00	0.014	1.914	TBI27	0.015	1.915	BUNRI	1.433	3.333
MODE1	0.017	1.917	TBI26	0.022	1.922	TEST	1.740	3.640
MODE0	0.017	1.917	TBI25	0.016	1.916			

Remark C_{IN}: Capacitance of only input pin

C_{inewl}: Value of C_{IN} with wiring capacitance (estimated wire length capacitance) taken into consideration (l = 10 mm)

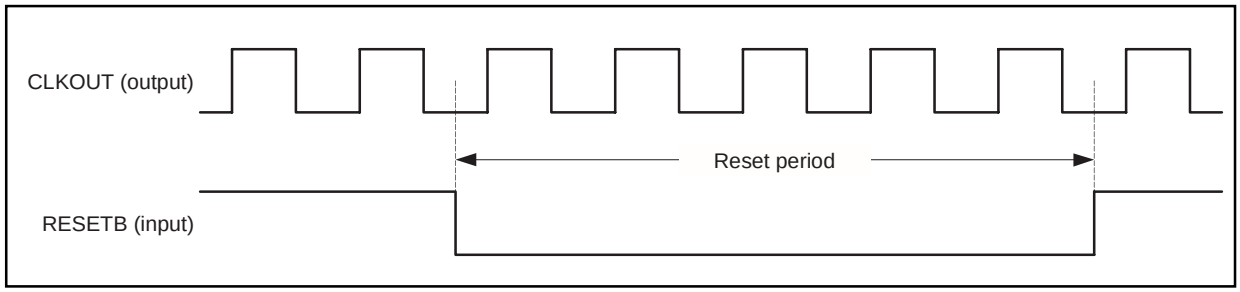
(2) Output pins

Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)
A23 to A0	6.570	OSCEN	13.340	ST1	6.587
ADOENB	13.072	RDB	6.570	ST0	6.587
ADOUT15 to ADOUT0	6.570	RWB	6.570	TO11	4.993
		SCKOENB	4.993	TO10	4.993
DSTBB	6.570	SCKOUTB	3.300	TXD	4.993
HLDAKB	6.570	SO	4.775	ICO1	6.587
ASTB	3.300	SOENB	6.587	ICO0	6.570
CLKOUT	13.072	UBENB	6.587	TBO23 to TBO0	6.536
LBENB	6.587	WRB	6.570		

3. 2 RESETB Signal

In view of the evaluations performed by NEC, when the RESETB signal is changed, do not synchronize it with the system clock's rising and falling edges (See **Figure 3-1**).

Figure 3-1. RESETB Signal Input Example



3. 3 Initialization of Internal Registers

Before executing the test program, be sure to execute an instruction to assign initial values to the internal registers used in test program execution. Failure to do this will result in the propagation of undefined values.

3. 4 Pin Functions

(1/2)

Pin Name	I/O	Function
TO11, TO10	Output	Pulse signal output from timer 1.
TCLR1	Input	External clear signal input to timer 1.
TI1	Input	External count clock input to timer 1.
INTP13 to INTP10	Input	External capture trigger input to timer 1/External maskable interrupt request input.
INTP03 to INTP00	Input	External maskable interrupt request input.
NMI	Input	Non-maskable interrupt request input.
SO	Output	Serial transmit data output from CSI.
SI	Input	Serial receive data input to CSI.
SOENB	Output	SO pin control signal output.
SCKINB	Input	Serial clock input to CSI.
SCKOUTB	Output	Serial clock output from CSI.
SCKOENB	Output	Signal output indicating input/output direction of serial clock of CSI.
TXD	Output	Serial transmit data output from UART.
RXD	Input	Serial receive data input to UART
ADOUT15 to ADOUT0	Output	Timer-division output of address/data when accessing external device.
ADOENB	Output	ADOUT15 to ADOUT0 pins control signal output.
DIN15 to DIN0	Input	Data input when accessing external device.
A23 to A0	Output	Address output when accessing external device.
LBENB	Output	Lower byte enable signal output of external data bus.
UBENB	Output	Upper byte enable signal output of external data bus.
RWB	Output	External read/write status output.
RDB	Output	External read strobe output.
WRB	Output	External write strobe output.
DSTBB	Output	External data strobe signal output.
ASTB	Output	External address strobe signal output.
ST1, ST0	Output	External bus cycle status output.
HLDAKB	Output	Bus hold acknowledge output.
HLDRQB	Input	Bus hold request input.
WAITB	Input	Inputs control signal that inserts wait states to bus cycle.
RESETB	Input	System reset input.
CLKIN	Input	External clock input.
CLKOUT	Output	Internal system clock output.
TBCENB	Input	Inputs control signal to time base counter (TBC).
OSCEN	Output	Specifies operation of external OSC.
MODE1, MODE0	Input	Specifies operation mode of V851 core.
TBI41 to TBI0	Input	Pin for test using test bus.
TBO23 to TBO0	Output	
TEST	Input	

(2/2)

Pin Name	I/O	Function
BUNRI	Input	Pin for test using test bus.
ICO1, ICO0	Output	NEC reserved pin.
ICI1, ICI0	Input	

3. 5 Electrical Specifications

The following specifications are for a single macro. An actual chip consists of two or more macros. Design the system so that all the specifications of the individual macros are satisfied when the chip is used.

3. 5. 1 Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

3. 5. 2 Recommended operation range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	–40		+85	°C
Clock cycle	t_{CYK}	30			ns

3. 5. 3 DC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1a}	In normal operation mode	Without ROM, RAM		0.4	0.5	mA/MHz
	I_{DD1b}		Other than the above	See **(1) How to calculate the current consumption value of the V851 core**			
	I_{DD2}	In HALT mode			0.2	0.3	mA/MHz
	I_{DD3}	In STOP mode			1.0	15	μA

Remark The TYP. value is a reference value for when T_A = 25°C, V_{DD} = 3.3 V.

Caution The current flow to the internal ROM in the reset interval is a maximum 5 mA.

(1) How to calculate the current consumption value of the V851 core

The current consumption value (TYP.) of the V851 core with internal ROM and RAM is defined by the following expression.

$$I_{DD1b} = I_{DD1a} + I_{DDROM} + I_{DDRAM}$$

- I_{DDROM}: the current consumption value of internal ROM
- I_{DDRAM}: the current consumption value of internal RAM

The following is an example of how to calculate the current consumption value of the NA851M82 (Internal ROM: 128 KB/Internal RAM: 4 KB).

Caution This current consumption calculation is for reference only; the values calculated herein are not guaranteed.

Conditions: V_{DD} = 3.3 V
ϕ = 33 MHz
Operation percentage of internal ROM = 80%
Operation percentage of internal RAM = 20% (the ratio of read operation to write operation = 1:1)
Internal RAM read operation frequency (f_R) = 33 MHz
Internal RAM write operation frequency (f_W) = 33 MHz

The current consumption value when an operation is performed under the above conditions is calculated by the following expression.

$I_{DD1a} = 0.4 \times \phi = 0.4 \times 33 = 13.2$ [mA] …<1>

I_{DDROM} Note 1 = ((2.2 + (V_{DD} – 2.7) × 3.0) + (0.05 × V_{DD} × ϕ)) × operating ratio %
= ((2.2 + (3.3 – 2.7) × 3.0) + (0.05 × 3.3 × 33)) × 0.8
= 7.556 [mA] …<2>

$I_{DDRAM\ (READ)}$ Note 2 = 0.82 × f_R × operating ratio % = 0.82 × 33 × 0.2 × 0.5 = 2.706 [mA] …<3>

$I_{DDRAM\ (WRITE)}$ Note 3 = 0.83 × f_W × operating ratio % = 0.83 × 33 × 0.2 × 0.5 = 2.739 [mA] …<4>

From <3> and <4>,

$I_{DDRAM} = (I_{DDRAM\ (READ)} + I_{DDRAM\ (WRITE)}) = 2.706 + 2.739 = 5.445$ [mA] …<5>

From <1>, <2>, and <5>,

$I_{DD1b} = 13.2 + 7.556 + 5.445 = 26.201$ [mA]

Therefore, from the above, the current consumption (TYP.) of the NA851M82 is 26.201 mA.

Notes 1. Use the following expression regardless of the internal ROM size (excepting ROMless versions).
((2.2 + (V_{DD} – 2.7) × 3.0) + (0.05 × V_{DD} × ϕ)) × operating ratio %

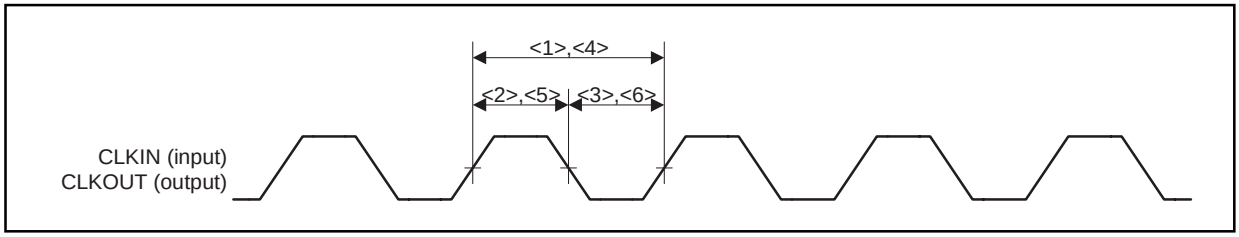
2. Use the following expressions for 8 KB, 16 KB, and 24 KB internal RAM sizes respectively.
8 KB: 2.55 × f_R × operating ratio %
16 KB: 3.02 × f_R × operating ratio %
24 KB: 3.34 × f_R × operating ratio %

3. Use the following expressions for 8 KB, 16 KB, and 24 KB internal RAM sizes respectively.
8 KB: 2.41 × f_W × operating ratio %
16 KB: 2.41 × f_W × operating ratio %
24 KB: 2.62 × f_W × operating ratio %

3. 5. 4 AC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

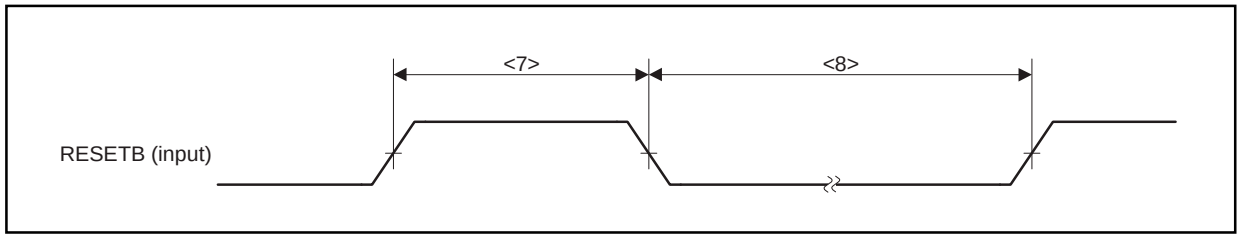
(1) Clock timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
CLKIN input cycle	<1>	t_{CYX}		30		ns
CLKIN input high-level width	<2>	t_{WXH}		14		ns
CLKIN input low-level width	<3>	t_{WXL}		14		ns
CPU operating frequency	–	ϕ		0	33	MHz
CLKOUT output cycle	<4>	t_{CYK}		30		ns
CLKOUT high-level width	<5>	t_{WKH}		$0.5t_{CYK}$–5		ns
CLKOUT low-level width	<6>	t_{WKL}		$0.5t_{CYK}$–5		ns



(2) Reset timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
RESETB high-level width	<7>	t_{WRSH}		500		ns
RESETB low-level width	<8>	t_{WRSL}	On power application	500		ns



(3) Read timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<9>	t_{DKA}			3	ns
Delay time from CLKOUT↓ to ASTB	<11>	t_{DKST}			4	ns
Delay time from CLKOUT↑ to DSTBB	<12>	t_{DKD}			3	ns
Delay time from CLKOUT↑ to status	<13>	t_{DKS}			3	ns
Data input setup time (to CLKOUT↑)	<14>	t_{SIDK}		2		ns
Data input hold time (from CLKOUT↑)	<15>	t_{HKID}		2		ns
WAITB setup time (to CLKOUT↓)	<16>	t_{SWTK}		2		ns
WAITB hold time (from CLKOUT↓)	<17>	t_{HKWT}		2		ns
Address setup time (to ASTB↓)	<19>	t_{SAST}		0.5T – 6		ns
Address hold time (from ASTB↓)	<20>	t_{HSTA}		0.5T – 6		ns
Delay time from CLKOUT↑ to LBENB	<22>	t_{DKLB}			3	ns
Delay time from CLKOUT↑ to UBENB	<23>	t_{DKUB}			3	ns
Delay time from ASTB↓ to DSTBB↓	<24>	t_{DSTD}		0.5T – 6		ns
Data input hold time (from DSTBB↑)	<25>	t_{HDID}		0		ns
Delay time from DSTBB↑ to address output	<26>	t_{DDA}		(1 + i)T		ns
Delay time from DSTBB↑ to ASTB↑	<27>	t_{DDSTH}		0.5T – 6		ns
Delay time from DSTBB↑ to ASTB↓	<28>	t_{DDSTL}		(1.5 + i)T – 6		ns
Status setup time (to ASTB↓)	<29>	t_{SSST}		0.5T – 6		ns
Status hold time (from ASTB↑)	<30>	t_{HSTS}		0.5T – 6		ns
DSTBB low-level width	<31>	t_{WDL}		(1 + n)T – 5		ns
ASTB high-level width	<32>	t_{WSTH}		T – 5		ns
WAITB setup time (to address)	<33>	t_{SAWT1}	n ≥ 1		1.5T – 11	ns
	<34>	t_{SAWT2}			(1.5 + n)T – 11	ns
WAITB hold time (from address)	<35>	t_{HAWT1}	n ≥ 1	1.5T + 6		ns
	<36>	t_{HAWT2}		(1.5 + n)T + 6		ns
WAITB setup time (to ASTB↓)	<37>	t_{SSTWT1}	n ≥ 1		T – 10	ns
	<38>	t_{SSTWT2}			(1 + n)T – 10	ns
WAITB hold time (from ASTB↓)	<39>	t_{HSTWT1}	n ≥ 1	NT + 5		ns
	<40>	t_{HSTWT2}		(1 + n)T + 5		ns
Delay time from CLKOUT↑ to ADOENB	<41>	t_{DKADEN}			3	ns
Delay time from CLKOUT↑ to address/data output	<42>	t_{DKAD}			5	ns

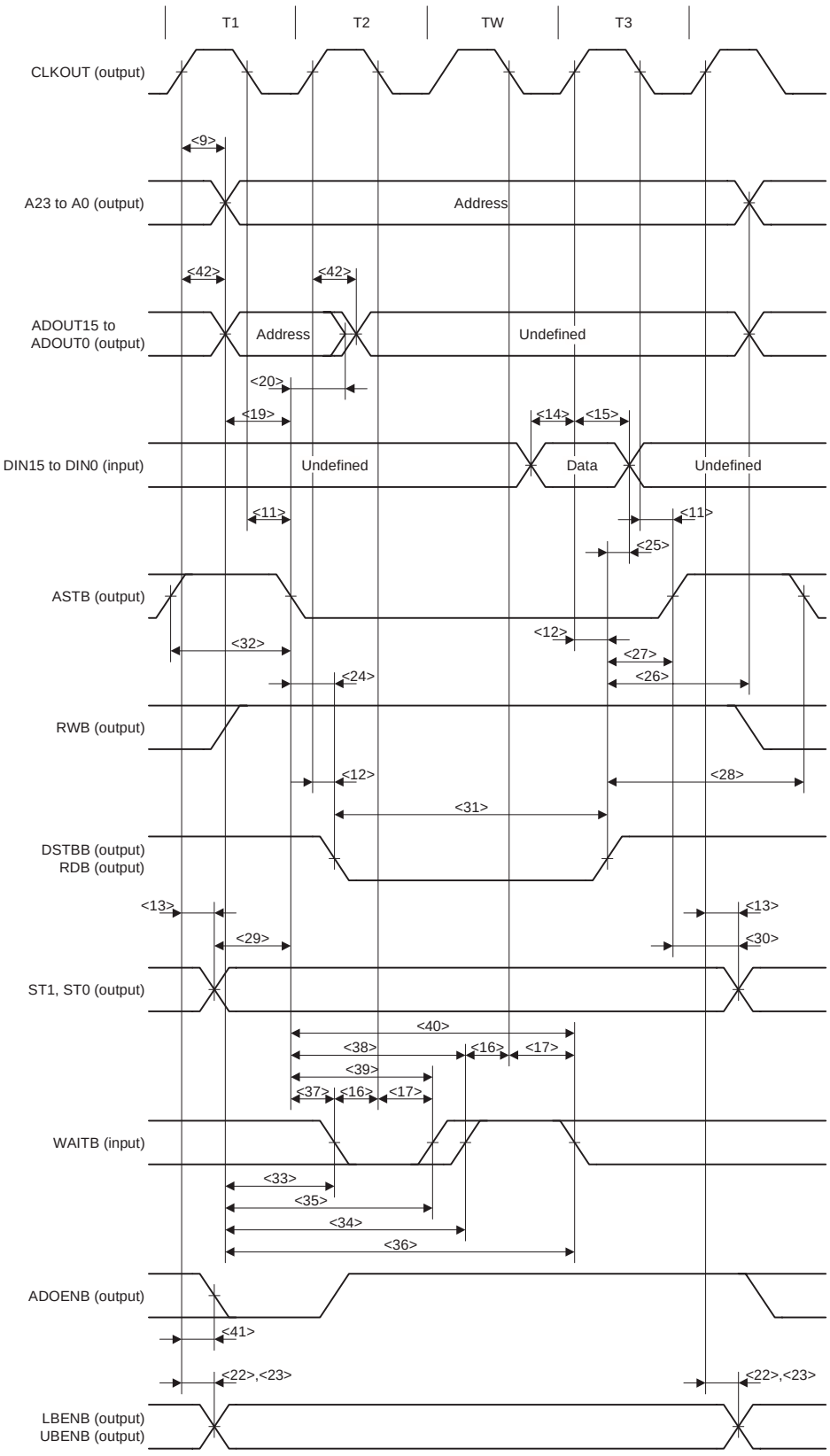
Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing changes when programmable wait cycles are inserted.

3. i indicates the number of idle states (0 or 1) inserted after read cycle.

4. Be sure to satisfy at least one of data input hold times t_{HKID} and t_{HDID}.

(3) Read timing (2/2)



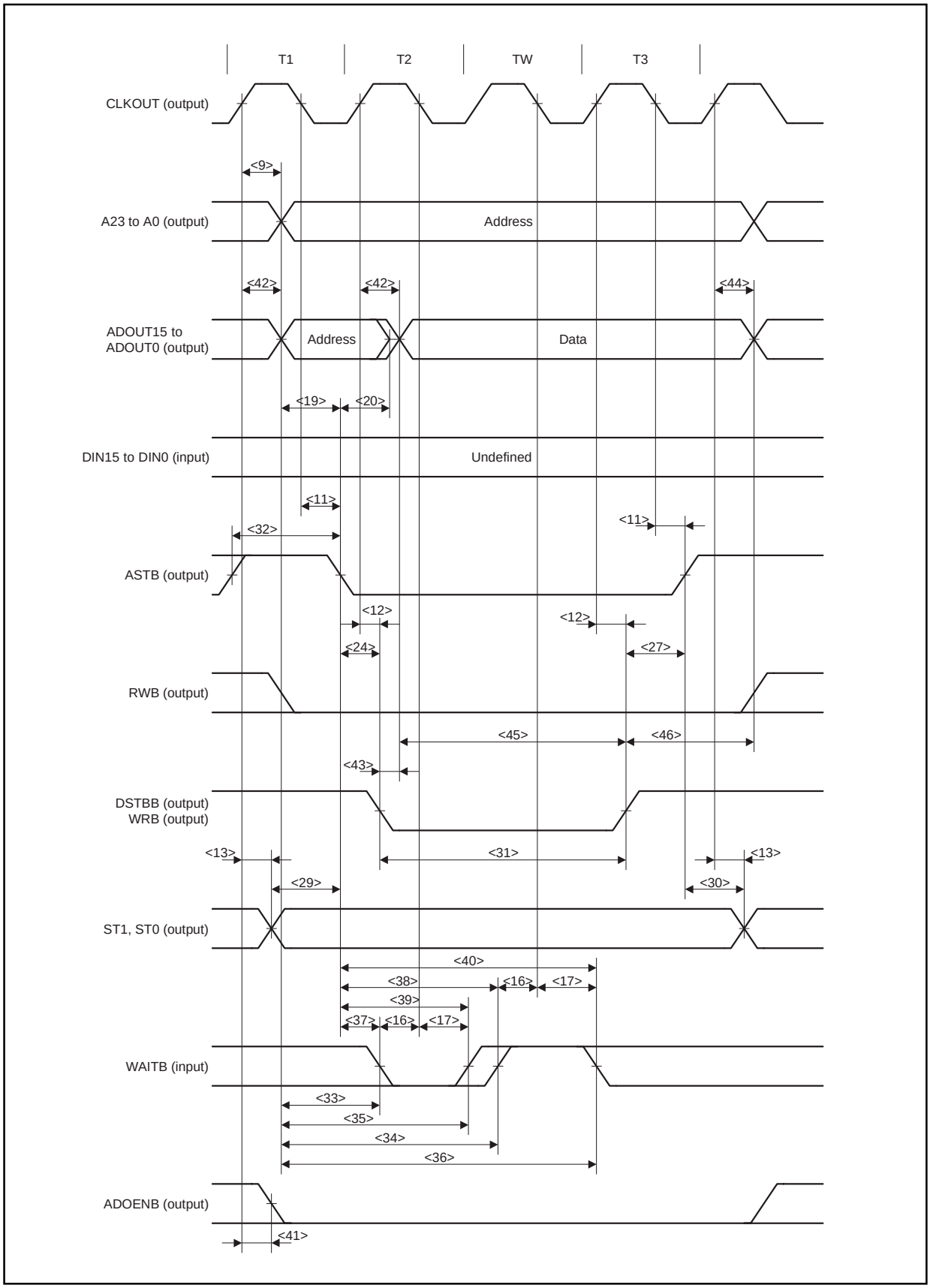
(4) Write timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<9>	t_{DKA}			3	ns
Delay time from CLKOUT↓ to ASTB	<11>	t_{DKST}			4	ns
Delay time from CLKOUT↑ to DSTBB	<12>	t_{DKD}			3	ns
Delay time from CLKOUT↑ to status	<13>	t_{DKS}			3	ns
WAITB setup time (to CLKOUT↓)	<16>	t_{SWTK}		2		ns
WAITB hold time (from CLKOUT↓)	<17>	t_{HKWT}		2		ns
Address setup time (to ASTB↓)	<19>	t_{SAST}		0.5T – 6		ns
Address hold time (from ASTB↓)	<20>	t_{HSTA}		0.5T – 6		ns
Delay time from ASTB↓ to DSTBB↓	<24>	t_{DSTD}		0.5T – 6		ns
Delay time from DSTBB↑ to ASTB↑	<27>	t_{DDSTH}		0.5T – 6		ns
Status setup time (to ASTB↓)	<29>	t_{SSST}		0.5T – 6		ns
Status hold time (from ASTB↑)	<30>	t_{HSTS}		0.5T – 6		ns
DSTBB low-level width	<31>	t_{WDL}		(1+n)T – 5		ns
ASTB high-level width	<32>	t_{WSTH}		T – 5		ns
WAITB setup time (to address)	<33>	t_{SAWT1}	n ≥ 1		1.5T – 11	ns
	<34>	t_{SAWT2}			(1.5 + n)T – 11	ns
WAITB hold time (from address)	<35>	t_{HAWT1}	n ≥ 1	1.5T + 6		ns
	<36>	t_{HAWT2}		(1.5 + n)T + 6		ns
WAITB setup time (to ASTB↓)	<37>	t_{SSTWT1}	n ≥ 1		T – 10	ns
	<38>	t_{SSTWT2}			(1 + n)T – 10	ns
WAITB hold time (from ASTB↓)	<39>	t_{HSTWT1}	n ≥ 1	NT + 5		ns
	<40>	t_{HSTWT2}		(1 + n)T + 5		ns
Delay time from CLKOUT↑ to ADOENB	<41>	t_{DKADEN}			3	ns
Delay time from CLKOUT↑ to address/data output	<42>	t_{DKAD}			5	ns
Delay time from DSTBB↓ to data output	<43>	t_{DDOD}			5	ns
Data output hold time (from CLKOUT↑)	<44>	t_{HKOD}			5	ns
Data output setup time (to DSTBB↑)	<45>	t_{SODD}		(1 + n)T – 5		ns
Data output hold time (from DSTBB↑)	<46>	t_{HDOD}		T – 5		ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing changes when programmable wait cycles are inserted.

(4) Write timing (2/2)



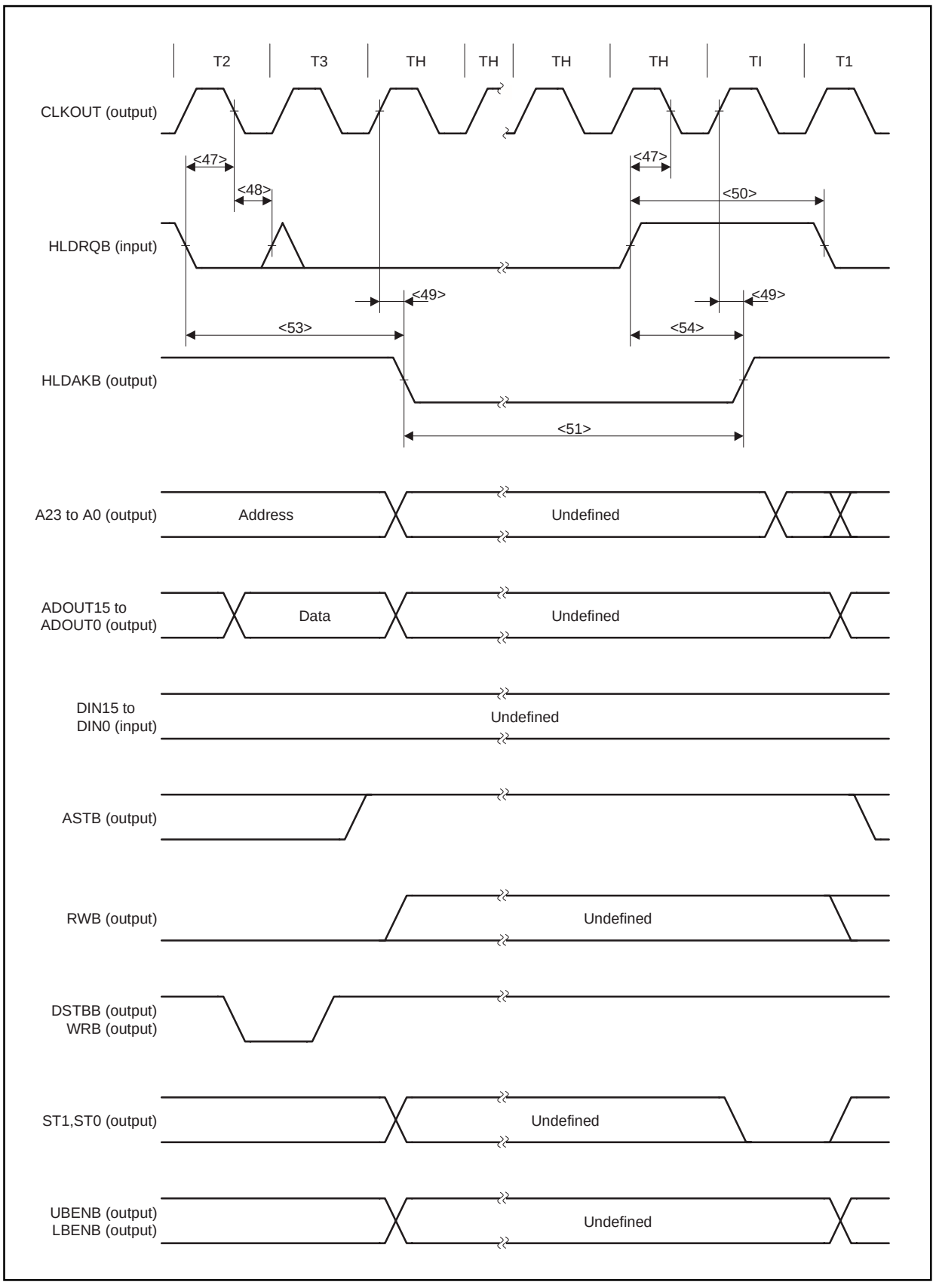
(5) Bus hold timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
HLDRQB setup time (to CLKOUT↓)	<47>	t_{SHQK}		2		ns
HLDRQB hold time (from CLKOUT↓)	<48>	t_{HKHQ}		2		ns
Delay time from CLKOUT↑ to HLDAKB	<49>	t_{DKHA}			3	ns
HLDRQB high-level width	<50>	t_{WHQH}		T + 5		ns
HLDAKB low-level width	<51>	t_{WHAL}		T − 5		ns
Delay time from HLDRQB↓ to HLDAKB↓	<53>	t_{DHQHA1}			(2n + 7.5)T + 11	ns
Delay time from HLDRQB↑ to HLDAKB↑	<54>	t_{DHQHA2}			1.5T + 11	ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing changes when programmable wait cycles are inserted.

(5) Bus hold timing (2/2)



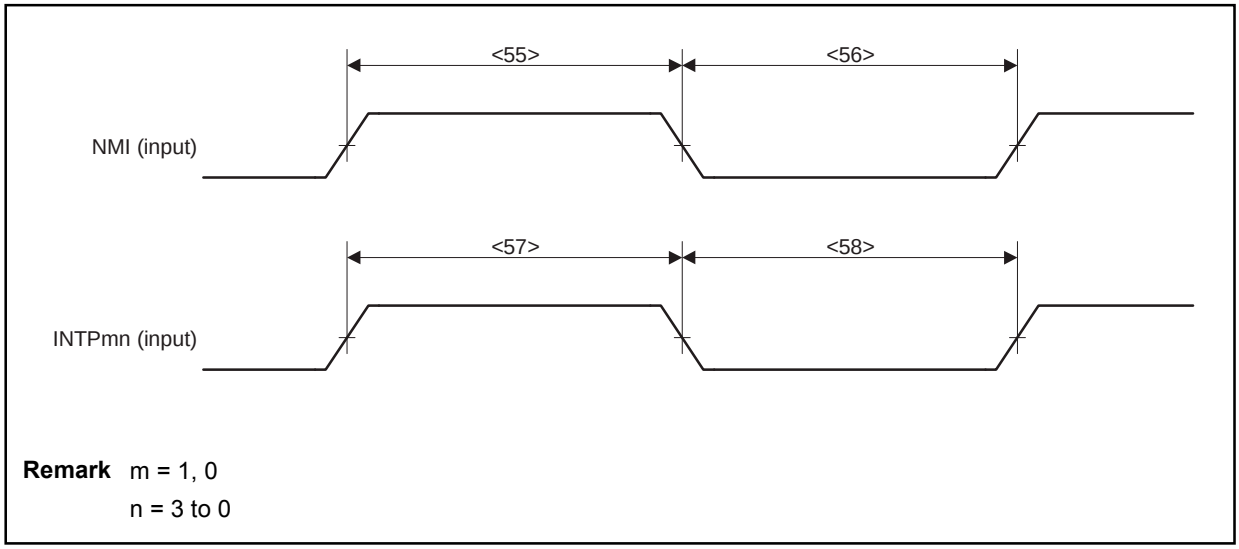
(6) Interrupt timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
NMI high-level width	<55>	t_{WNIH}		500		ns
NMI low-level width	<56>	t_{WNIL}		500		ns
INTPmn high-level width	<57>	t_{WITH}		3T + 10		ns
INTPmn low-level width	<58>	t_{WITL}		3T + 10		ns

Remarks 1. T = t_{CYK}

2. m = 1, 0

n = 3 to 0



Remark m = 1, 0

n = 3 to 0

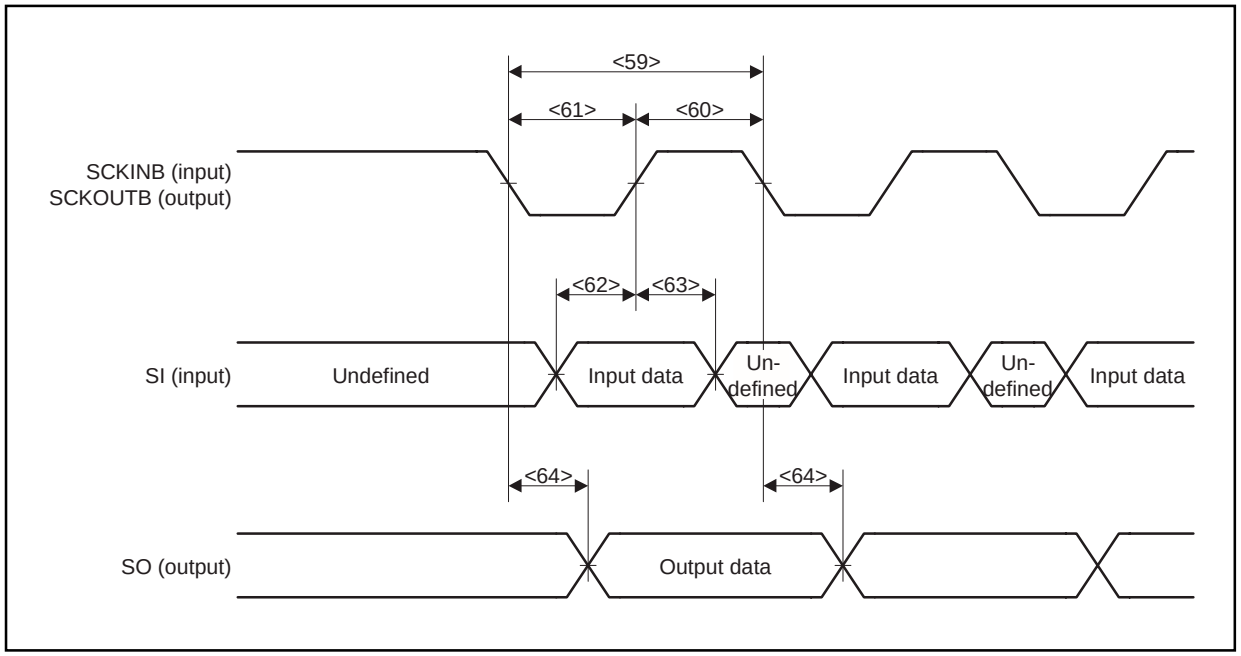
(7) CSI timing

(a) Master mode

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
SCKOUTB cycle	<59>	t_{CYSK}	Output	120		ns
SCKOUTB high-level width	<60>	t_{WSKH}	Output	0.5 t_{CYSK} – 10		ns
SCKOUTB low-level width	<61>	t_{WSKL}	Output	0.5 t_{CYSK} – 10		ns
SI setup time (to SCKOUTB↑)	<62>	t_{SSISK}		5		ns
SI hold time (from SCKOUTB↑)	<63>	t_{HSKSI}		5		ns
SO delay time (from SCKOUTB↓)	<64>	t_{DSKSO}			5	ns

(b) Slave mode

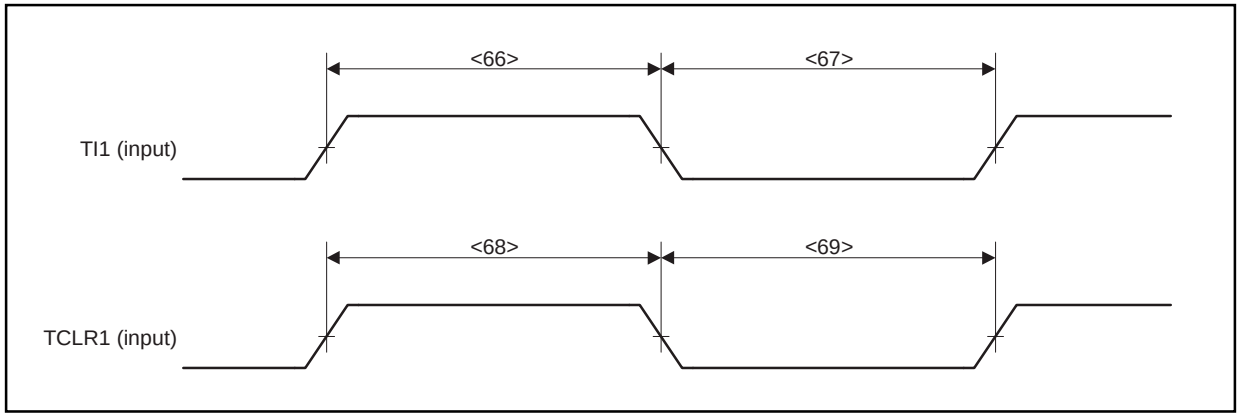
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
SCKINB cycle	<59>	t_{CYSK}	Input	120		ns
SCKINB high-level width	<60>	t_{WSKH}	Input	30		ns
SCKINB low-level width	<61>	t_{WSKL}	Input	30		ns
SI setup time (to SCKINB↑)	<62>	t_{SSISK}		5		ns
SI hold time (from SCKINB↑)	<63>	t_{HSKSI}		5		ns
SO delay time (from SCKINB↓)	<64>	t_{DSKSO}			5	ns

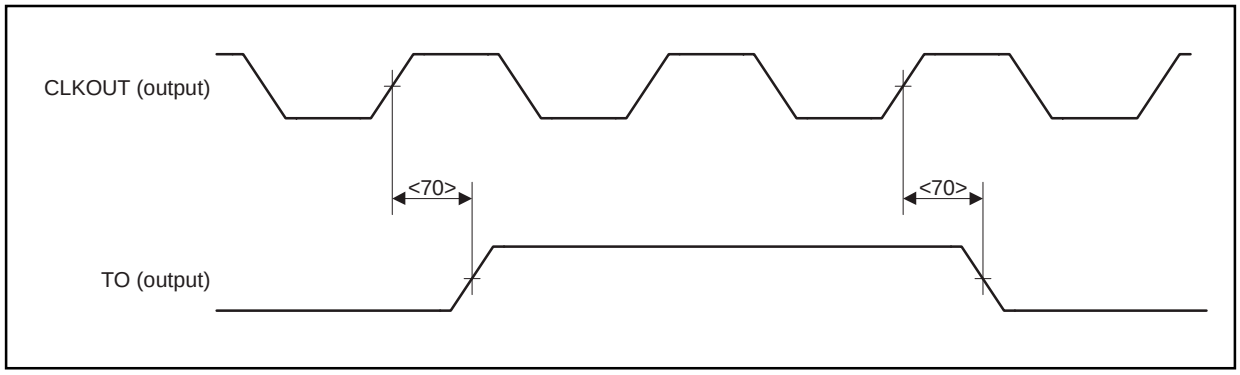


(8) RPU timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
TI1 high-level width	<66>	t_{WTIH}		3T + 10		ns
TI1 low-level width	<67>	t_{WTIL}		3T + 10		ns
TCLR1 high-level width	<68>	t_{WTCH}		3T + 10		ns
TCLR1 low-level width	<69>	t_{WTCL}		3T + 10		ns
Delay time from CLKOUT↑ to TO	<70>	t_{DKTO}			5	ns

Remark T = t_{CYK}





CHAPTER 4 V853 CORE

The V853 core is a CPU core having peripheral functions such as a real-time pulse unit, PWM output, and serial interfaces. The instruction set of the V853 core is common to that of the V850 Family 32-bit single-chip microcontrollers.

4. 1 Outline

- CPU performance: 38 MIPS (@ 33 MHz operation)
- Internal memory (ROM can be removed.)
  Mask ROM: 48, 64, 96, 128, and 256 KB
  RAM: 4, 8, 16, and 24 KB
- Minimum instruction execution time: 30 ns (@ 33 MHz operation)
- External bus interface
  16-bit data bus (DIN/DOUT separated)
  24-bit address bus
- Interrupt/exception
  External interrupt: 17 (including NMI)
  Internal interrupt: 31 sources
  Software exception: 32 sources
  Exception trap: 1 source
  Eight priority levels can be specified.
- Real-time pulse unit
  16-bit timer/event counter: 4 chs
  16-bit interval timer: 1 ch
- Serial interface
  Asynchronous serial interface (UART)
  Clocked serial interface (CSI)
  UART/CSI: 2 chs
  CSI: 2 chs
  Dedicated baud rate generator: 3 chs
- PWM (Pulse Width Modulation)
  8/9/10/12-bit resolution PWM: 2 chs
- Power save function
  HALT, STOP, IDLE mode
  Clock output stop function

4. 1. 1 Symbol diagram

Number of grids

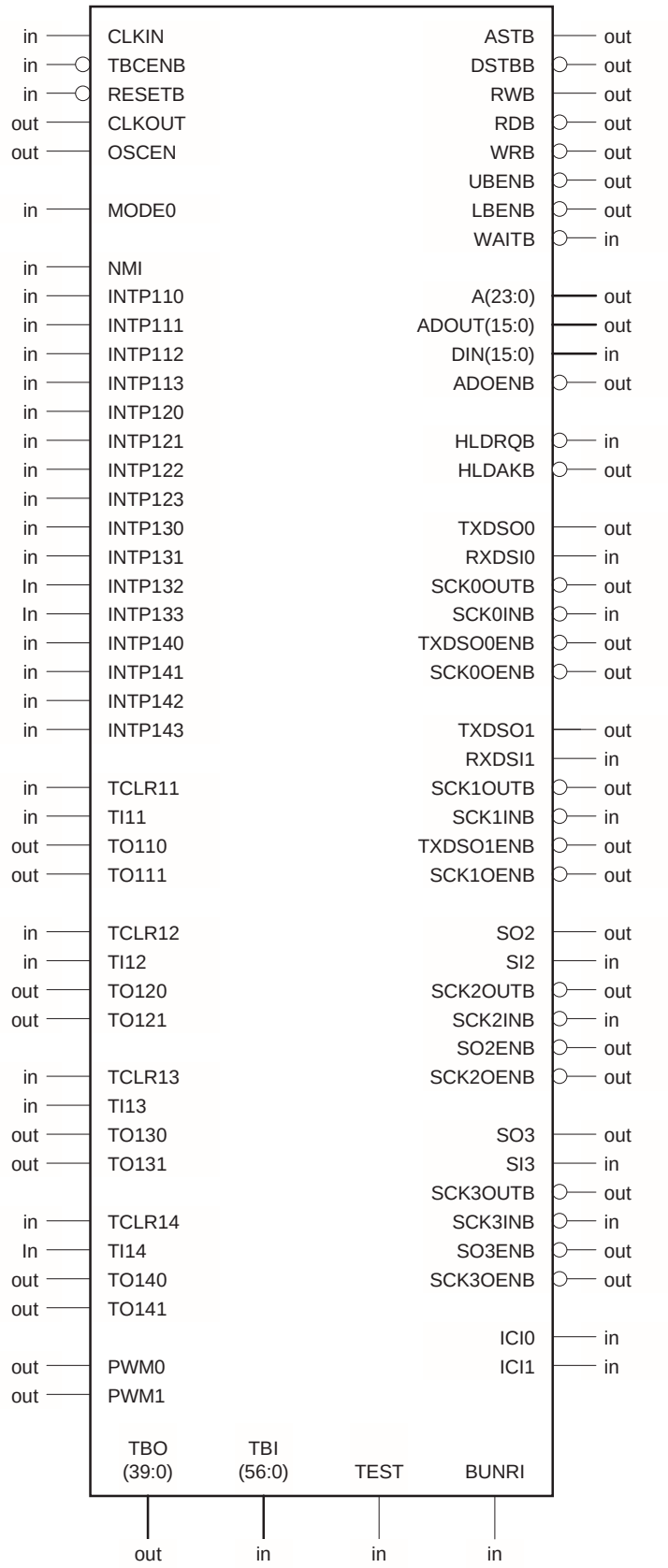
239k grids

262k grids (including wiring area)

Number of separation simulation patterns

ROM Size / RAM Size	0 byte (ROMless)	48 KB	64 KB	96 KB	128 KB	256 KB
4 KB	NA853M02 306.0k	NA853M32 318.4k	NA853M42 326.6k	NA853M62 342.9k	NA853M82 359.3k	NA853MG2 424.8k
8 KB	NA853M04 306.0k	NA853M34 318.4k	NA853M44 326.6k	NA853M64 342.9k	NA853M84 359.3k	NA853MG4 424.8k
16 KB	NA853M08 313.2k	NA853M38 325.6k	NA853M48 333.8k	NA853M68 350.1k	NA853M88 366.5k	NA853MG8 432.0k
24 KB	NA853M0C 313.2k	NA853M3C 325.6k	NA853M4C 333.8k	NA853M6C 350.1k	NA853M8C 366.5k	NA853GC 432.0k

Remark The upper figure in each column of the above table indicates the part number and the lower figure indicates the total number of patterns.


in CLKIN
in TBCENB
in RESETB
out CLKOUT
out OSCEN
in MODE0
in NMI
in INTP110
in INTP111
in INTP112
in INTP113
in INTP120
in INTP121
in INTP122
in INTP123
in INTP130
in INTP131
In INTP132
In INTP133
in INTP140
in INTP141
in INTP142
in INTP143
in TCLR11
in TI11
out TO110
out TO111
in TCLR12
in TI12
out TO120
out TO121
in TCLR13
in TI13
out TO130
out TO131
in TCLR14
In TI14
out TO140
out TO141
out PWM0
out PWM1
ASTB out
DSTBB out
RWB out
RDB out
WRB out
UBENB out
LBENB out
WAITB in
A(23:0) out
ADOUT(15:0) out
DIN(15:0) in
ADOENB out
HLDRQB in
HLDAKB out
TXDSO0 out
RXDSI0 in
SCK0OUTB out
SCK0INB in
TXDSO0ENB out
SCK0OENB out
TXDSO1 out
RXDSI1 in
SCK1OUTB out
SCK1INB in
TXDSO1ENB out
SCK1OENB out
SO2 out
SI2 in
SCK2OUTB out
SCK2INB in
SO2ENB out
SCK2OENB out
SO3 out
SI3 in
SCK3OUTB out
SCK3INB in
SO3ENB out
SCK3OENB out
ICI0 in
ICI1 in
TBO (39:0)
TBI (56:0)
TEST
BUNRI
out
in
in
in

4. 1. 2 Pin capacitance

(1) Input pins

(1/2)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
DIN15	0.067	1.967	TI12	0.013	1.913	TBI47	0.038	1.938
DIN14	0.094	1.994	TCLR12	0.047	1.947	TBI46	0.017	1.917
DIN13	0.075	1.975	INTP113	0.081	1.981	TBI45	0.085	1.985
DIN12	0.097	1.997	INTP112	0.082	1.982	TBI44	0.020	1.920
DIN11	0.068	1.968	INTP111	0.099	1.999	TBI43	0.068	1.968
DIN10	0.066	1.966	INTP110	0.110	2.010	TBI42	0.016	1.916
DIN9	0.066	1.966	TI11	0.051	1.951	TBI41	0.020	1.920
DIN8	0.066	1.966	TCLR11	0.072	1.972	TBI40	0.014	1.914
DIN7	0.067	1.967	SI3	0.017	1.917	TBI39	0.007	1.907
DIN6	0.068	1.968	SCK3INB	0.016	1.916	TBI38	0.016	1.916
DIN5	0.070	1.970	SI2	0.035	1.935	TBI37	0.018	1.918
DIN4	0.072	1.972	SCK2INB	0.044	1.944	TBI36	0.009	1.909
DIN3	0.094	1.994	RXDSI1	0.017	1.917	TBI35	0.013	1.913
DIN2	0.066	1.966	SCK1INB	0.027	1.927	TBI34	0.007	1.907
DIN1	0.068	1.968	RXDSI0	0.035	1.935	TBI33	0.008	1.908
DIN0	0.067	1.967	SCK0INB	0.017	1.917	TBI32	0.008	1.908
HLDRQB	0.267	2.167	NMI	0.034	1.934	TBI31	0.009	1.909
WAITB	0.139	2.039	RESETB	0.017	1.917	TBI30	0.046	1.946
INTP143	0.100	2.000	CLKIN	0.051	1.951	TBI29	0.041	1.941
INTP142	0.113	2.013	ICI1	0.017	1.917	TBI28	0.039	1.939
INTP141	0.115	2.015	ICI0	0.023	1.923	TBI27	0.018	1.918
INTP140	0.132	2.032	MODE	0.035	1.935	TBI26	0.016	1.916
TI14	0.015	1.915	TBCENB	0.025	1.925	TBI25	0.017	1.917
TCLR14	0.196	2.096	TEST	3.041	4.941	TBI24	0.052	1.952
INTP133	0.116	2.016	BUNRI	0.078	1.978	TBI23	0.203	2.103
INTP132	0.069	1.969	TBI56	0.015	1.915	TBI22	0.037	1.937
INTP131	0.100	2.000	TBI55	0.067	1.967	TBI21	0.052	1.952
INTP130	0.108	2.008	TBI54	0.019	1.919	TBI20	0.051	1.951
TI13	0.013	1.913	TBI53	0.055	1.955	TBI19	0.018	1.918
TCLR13	0.035	1.935	TBI52	0.019	1.919	TBI18	0.040	1.940
INTP123	0.057	1.957	TBI51	0.068	1.968	TBI17	0.023	1.923
INTP122	0.054	1.954	TBI50	0.142	2.042	TBI16	0.016	1.916
INTP121	0.043	1.943	TBI49	0.240	2.140	TBI15	0.069	1.969
INTP120	0.059	1.959	TBI48	0.016	1.916	TBI14	0.072	1.972

Remark C_{IN}: Capacitance of only input pin

C_{inewl}: Value of C_{IN} with wiring capacitance (estimated wire length capacitance) taken into consideration (l = 10 mm)

(2/2)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
TBI13	0.074	1.974	TBI8	0.066	1.966	TBI3	0.084	1.984
TBI12	0.100	2.000	TBI7	0.075	1.975	TBI2	0.067	1.967
TBI11	0.068	1.968	TBI6	0.067	1.967	TBI1	0.069	1.969
TBI10	0.067	1.967	TBI5	0.071	1.971	TBI0	0.068	1.968
TBI9	0.071	1.971	TBI4	0.068	1.968			

Remark C_{IN}: Capacitance of only input pin

C_{inewl}: Value of C_{IN} with wiring capacitance (estimated wire length capacitance) taken into consideration (l = 10 mm)

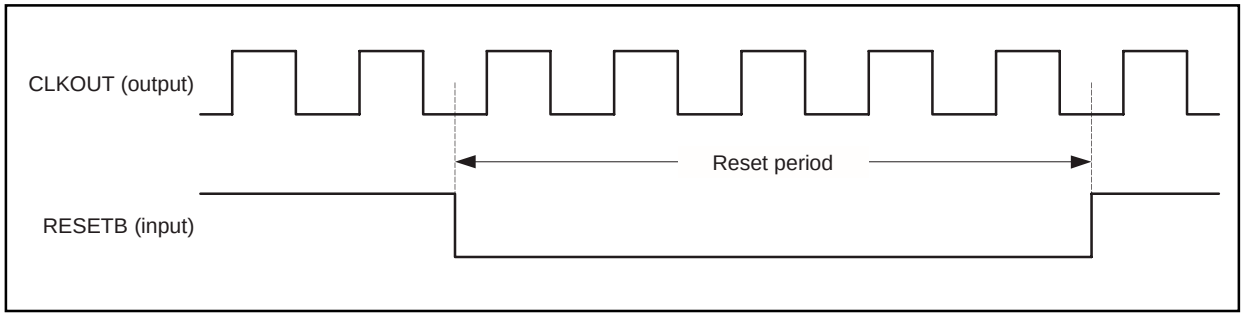
(2) Output pins

Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)
A23	6.565	ADOUT0	6.565	TBO38	6.516
A22	6.562	LBENB	6.461	TBO37	6.271
A21	6.563	UBENB	6.500	TBO36	6.516
A20	6.558	RWB	6.532	TBO35	6.535
A19	6.567	DSTBB	6.541	TBO34	6.531
A18	6.536	RDB	6.517	TBO33	6.534
A17	6.539	WRB	6.532	TBO32	6.530
A16	6.566	ASTB	6.553	TBO31	6.528
A15	6.512	ADOENB	6.553	TBO30	6.511
A14	6.561	HLDAKB	6.444	TBO29	6.533
A13	6.570	TO141	6.569	TBO28	6.513
A12	6.569	TO140	6.569	TBO27	3.301
A11	6.557	TO131	6.475	TBO26	6.452
A10	6.567	TO130	6.569	TBO25	6.404
A9	6.567	TO121	6.535	TBO24	6.501
A8	6.570	TO120	6.567	TBO23	6.489
A7	6.554	TO111	6.539	TBO22	6.443
A6	6.561	TO110	6.547	TBO21	6.433
A5	6.560	SO3	6.560	TBO20	6.523
A4	6.552	SO3ENB	6.568	TBO19	3.313
A3	6.536	SCK3OUTB	6.564	TBO18	3.295
A2	6.569	SCK3OENB	6.565	TBO17	3.313
A1	6.568	SO2	6.569	TBO16	3.295
A0	6.498	SO2ENB	6.569	TBO15	6.479
ADOUT15	6.519	SCK2OUTB	6.569	TBO14	6.526
ADOUT14	6.558	SCK2OENB	6.569	TBO13	6.448
ADOUT13	6.569	TXDSO1	6.568	TBO12	6.533
ADOUT12	6.557	TXDSO1ENB	6.567	TBO11	6.460
ADOUT11	6.560	SCK1OUTB	6.569	TBO10	6.487
ADOUT10	6.532	SCK1OENB	6.569	TBO9	6.513
ADOUT9	6.561	TXDSO0	6.548	TBO8	6.516
ADOUT8	6.570	TXDSO0ENB	6.563	TBO7	6.468
ADOUT7	6.568	SCK0OUTB	6.540	TBO6	6.535
ADOUT6	6.568	SCK0OENB	6.536	TBO5	6.535
ADOUT5	6.570	PWM1	6.569	TBO4	6.507
ADOUT4	6.544	PWM0	6.569	TBO3	6.533
ADOUT3	6.569	CLKOUT	13.063	TBO2	6.513
ADOUT2	6.569	OSCEN	6.337	TBO1	6.496
ADOUT1	6.568	TBO39	3.308	TBO0	6.509

4. 2 RESETB Signal

In view of the evaluations performed by NEC, when the RESETB signal is changed, do not synchronize it with the system clock's rising and falling edges (See **Figure 4-1**).

Figure 4-1. RESETB Signal Input Example



4. 3 Initialization of Internal Registers

Before executing the test program, be sure to execute an instruction to assign initial values to the internal registers used in test program execution. Failure to do this will result in the propagation of undefined values.

4. 4 Pin Functions

(1/2)

Pin Name	I/O	Function
TO141, TO140	Output	Pulse signal output from timer 1 (TM14).
TO131, TO130	Output	Pulse signal output from timer 1 (TM13).
TO121, TO120	Output	Pulse signal output from timer 1 (TM12).
TO111, TO110	Output	Pulse signal output from timer 1 (TM11).
TCLR14	Input	External clear signal input to timer 1 (TM14).
TCLR13	Input	External clear signal input to timer 1 (TM13).
TCLR12	Input	External clear signal input to timer 1 (TM12).
TCLR11	Input	External clear signal input to timer 1 (TM11).
TI14	Input	External count clock input to timer 1 (TM14).
TI13	Input	External count clock input to timer 1 (TM13).
TI12	Input	External count clock input to timer 1 (TM12).
TI11	Input	External count clock input to timer 1 (TM11).
INTP143 to INTP140	Input	External capture trigger input to timer 1 (TM14)/External maskable interrupt request input.
INTP133 to INTP130	Input	External capture trigger input to timer 1 (TM13)/External maskable interrupt request input.
INTP123 to INTP120	Input	External capture trigger input to timer 1 (TM12)/External maskable interrupt request input.
INTP113 to INTP110	Input	External capture trigger input to timer 1 (TM11)/External maskable interrupt request input.
NMI	Input	Non-maskable interrupt request input.
PWM1, PWM0	Output	Pulse output from PWM.
SO3	Output	Serial transmit data output from CSI3.
SO2	Output	Serial transmit data output from CSI2.
TXDSO1	Output	Serial transmit data output from UART1/Serial transmit data output from CSI1.
TXDSO0	Output	Serial transmit data output from UART0/Serial transmit data output from CSI0.
SI3	Input	Serial reception data input to CSI3.
SI2	Input	Serial reception data input to CSI2.
RXDSI1	Input	Serial reception data input to UART1/Serial reception data input to CSI1.
RXDSI0	Input	Serial reception data input to UART0/Serial reception data input to CSI0.
SO3ENB	Output	SO3 pin control signal output.
SO2ENB	Output	SO2 pin control signal output.
TXDSO1ENB	Output	TXDSO1 pin control signal output.
TXDSO0ENB	Output	TXDSO0 pin control signal output.
SCK3INB	Input	Serial clock input to CSI3.
SCK2INB	Input	Serial clock input to CSI2.
SCK1INB	Input	Serial clock input to CSI1.
SCK0INB	Input	Serial clock input to CSI0.
SCK3OUTB	Output	Serial clock output from CSI3.
SCK2OUTB	Output	Serial clock output from CSI2.

(2/2)

Pin Name	I/O	Function
SCK1OUTB	Output	Serial clock output from CSI1.
SCK0OUTB	Output	Serial clock output from CSI0.
SCK3OENB	Output	Signal output indicating input/output direction of serial clock of CSI3.
SCK2OENB	Output	Signal output indicating input/output direction of serial clock of CSI2.
SCK1OENB	Output	Signal output indicating input/output direction of serial clock of CSI1.
SCK0OENB	Output	Signal output indicating input/output direction of serial clock of CSI0.
ADOUT15 to ADOUT0	Output	Timer-division output of address/data when accessing external device.
ADOENB	Output	ADOUT15 to ADOUT0 pins control signal output.
DIN15 to DIN0	Input	Data input when accessing external device.
A23 to A0	Output	Address output when accessing external device.
LBENB	Output	Lower byte enable signal output of external data bus.
UBENB	Output	Upper byte enable signal output of external data bus.
RWB	Output	External read/write status output.
RDB	Output	External read strobe output.
WRB	Output	External write strobe output.
DSTBB	Output	External data strobe signal output.
ASTB	Output	External address strobe signal output.
HLDAKB	Output	Bus hold acknowledge output.
HLDRQB	Input	Bus hold request input.
WAITB	Input	Inputs control signal that inserts wait states to bus cycle.
RESETB	Input	System reset input.
CLKIN	Input	External clock input.
CLKOUT	Output	Internal system clock output.
TBCENB	Input	Inputs control signal to time base counter (TBC).
OSCEN	Output	Specifies operation of external OSC.
MODE	Input	Specifies operation mode of V853 core.
TBI56 to TBI0	Input	Pin for test using test bus.
TBO39 to TBO0	Output	
TEST	Input	
BUNRI	Input	
ICI1, ICI0	Output	NEC reserved pin.

4. 5 Electrical Specifications

The following specifications are for a single macro. An actual chip consists of two or more macros. Design the system so that all the specifications of the individual macros are satisfied when the chip is used.

4. 5. 1 Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to +4.6	V
Operating ambient temperature	T_A	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

4. 5. 2 Recommended operation range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	−40		+85	°C
Clock cycle	t_{CYK}	30			ns

4. 5. 3 DC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1a}	In normal operation mode	Without ROM, RAM		0.6	0.8	mA/MHz
	I_{DD1b}		Other than the above	See **(1) How to calculate the current consumption value of the V853 core**			
	I_{DD2}	In HALT mode			0.3	0.4	mA/MHz
	I_{DD3}	In STOP mode			1.0	30	μA

Remark The TYP. value is a reference value for when T_A = 25°C, V_{DD} = 3.3 V.

Caution The current flow to the internal ROM in the reset interval is a maximum 5 mA.

(1) How to calculate the current consumption value of the V853 core

The current consumption value (TYP.) of the V853 core with internal ROM and RAM is defined by the following expression.

$$I_{DD1b} = I_{DD1a} + I_{DDROM} + I_{DDRAM}$$

- I_{DDROM}: the current consumption value of internal ROM
- I_{DDRAM}: the current consumption value of internal RAM

The following is an example of how to calculate the current consumption value of the NA853M82 (Internal ROM: 128 KB/Internal RAM: 4KB).

Caution This current consumption calculation is for reference only; the values calculated herein are not guaranteed.

Conditions: V_{DD} = 3.3 V
ϕ = 33 MHz
Operation percentage of internal ROM = 80%
Operation percentage of internal RAM = 20% (the ratio of read operation to write operation = 1:1)
Internal RAM read operation frequency (f_R) = 33 MHz
Internal RAM write operation frequency (f_W) = 33 MHz

The current consumption value when an operation is performed under the above conditions is calculated by the following expression.

$I_{DD1a} = 0.6 \times \phi = 0.6 \times 33 = 19.8$ [mA] …<1>

I_{DDROM} Note 1 $= ((2.2 + (V_{DD} - 2.7) \times 3.0) + (0.05 \times V_{DD} \times \phi)) \times$ operating ratio %
$= ((2.2 + (3.3 - 2.7) \times 3.0) + (0.05 \times 3.3 \times 33)) \times 0.8$
$= 7.556$ [mA] …<2>

$I_{DDRAM\ (READ)}$ Note 2 $= 0.82 \times f_R \times$ operating ratio % $= 0.82 \times 33 \times 0.2 \times 0.5 = 2.706$ [mA] …<3>

$I_{DDRAM\ (WRITE)}$ Note 3 $= 0.83 \times f_W \times$ operating ratio % $= 0.83 \times 33 \times 0.2 \times 0.5 = 2.739$ [mA] …<4>

From <3> and <4>,

$I_{DDRAM} = (I_{DDRAM\ (READ)} + I_{DDRAM\ (WRITE)}) = 2.706 + 2.739 = 5.445$ [mA] …<5>

From <1>, <2>, and <5>,

$I_{DD1b} = 19.8 + 7.556 + 5.445 = 32.801$ [mA]

Therefore, from the above, the current consumption (TYP.) of the NA853M82 is 32.801 mA.

Notes 1. Use the following expression regardless of the internal ROM size (excepting ROMless versions).
$((2.2 + (V_{DD} - 2.7) \times 3.0) + (0.05 \times V_{DD} \times \phi)) \times$ operating ratio %

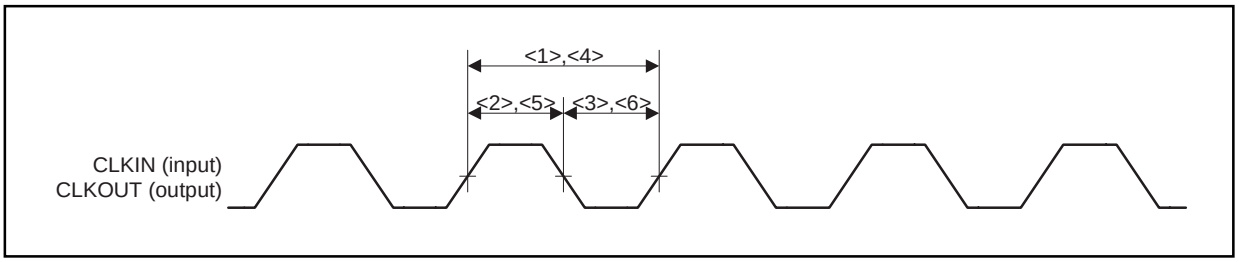
2. Use the following expressions for 8 KB, 16 KB, and 24 KB internal RAM sizes respectively.
8 KB: $2.55 \times f_R \times$ operating ratio %
16 KB: $3.02 \times f_R \times$ operating ratio %
24 KB: $3.34 \times f_R \times$ operating ratio %

3. Use the following expressions for 8 KB, 16 KB, and 24 KB internal RAM sizes respectively.
8 KB: $2.41 \times f_W \times$ operating ratio %
16 KB: $2.41 \times f_W \times$ operating ratio %
24 KB: $2.62 \times f_W \times$ operating ratio %

4. 5. 4 AC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

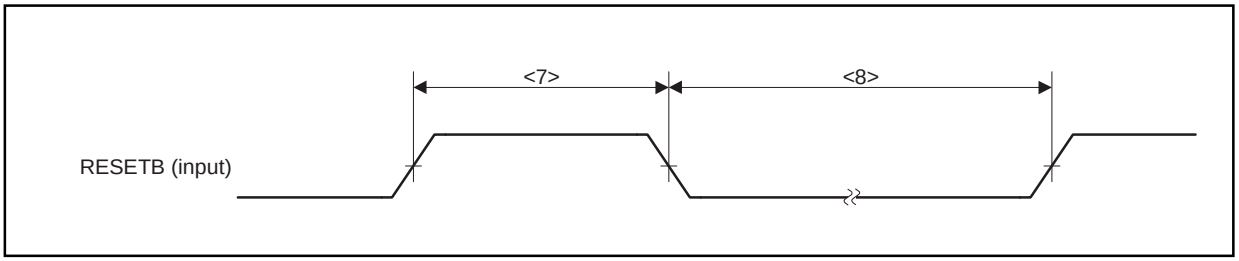
(1) Clock timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
CLKIN input cycle	<1>	t_{CYX}		30		ns
CLKIN input high-level width	<2>	t_{WXH}		14		ns
CLKIN input low-level width	<3>	t_{WXL}		14		ns
CPU operating frequency	–	ϕ		0	33	MHz
CLKOUT output cycle	<4>	t_{CYK}		30		ns
CLKOUT high-level width	<5>	t_{WKH}		$0.5t_{CYK}$–5		ns
CLKOUT low-level width	<6>	t_{WKL}		$0.5t_{CYK}$–5		ns



(2) Reset timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
RESETB high-level width	<7>	t_{WRSH}		500		ns
RESETB low-level width	<8>	t_{WRSL}	On power application	500		ns



(3) Read timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<9>	t_{DKA}			3	ns
Delay time from CLKOUT↓ to ASTB	<10>	t_{DKST}			4	ns
Delay time from CLKOUT↑ to DSTBB	<11>	t_{DKD}			3	ns
Data input setup time (to CLKOUT↑)	<12>	t_{SIDK}		2		ns
Data input hold time (from CLKOUT↑)	<13>	t_{HKID}		2		ns
WAITB setup time (to CLKOUT↓)	<14>	t_{SWTK}		2		ns
WAITB hold time (from CLKOUT↓)	<15>	t_{HKWT}		2		ns
Address setup time (to ASTB↓)	<17>	t_{SAST}		0.5T – 6		ns
Address hold time (from ASTB↓)	<18>	t_{HSTA}		0.5T – 6		ns
Delay time from CLKOUT↑ to LBENB	<19>	t_{DKLB}			3	ns
Delay time from CLKOUT↑ to UBENB	<20>	t_{DKUB}			3	ns
Delay time from ASTB↓ to DSTBB↓	<21>	t_{DSTD}		0.5T – 6		ns
Data input hold time (from DSTBB↑)	<22>	t_{HDID}		0		ns
Delay time from DSTBB↑ to address output	<23>	t_{DDA}		(1 + i)T		ns
Delay time from DSTBB↑ to ASTB↑	<24>	t_{DDSTH}		0.5T – 6		ns
Delay time from DSTBB↑ to ASTB↓	<25>	t_{DDSTL}		(1.5 + i)T – 6		ns
DSTBB low-level width	<26>	t_{WDL}		(1 + n)T – 5		ns
ASTB high-level width	<27>	t_{WSTH}		T – 5		ns
WAITB setup time (to address)	<28>	t_{SAWT1}	n ≥ 1		1.5T – 11	ns
	<29>	t_{SAWT2}			(1.5 + n)T – 11	ns
WAITB hold time (from address)	<30>	t_{HAWT1}	n ≥ 1	1.5T + 6		ns
	<31>	t_{HAWT2}		(1.5 + n)T + 6		ns
WAITB setup time (to ASTB↓)	<32>	t_{SSTWT1}	n ≥ 1		T – 10	ns
	<33>	t_{SSTWT2}			(1 + n)T – 10	ns
WAITB hold time (from ASTB↓)	<34>	t_{HSTWT1}	n ≥ 1	nT + 5		ns
	<35>	t_{HSTWT2}		(1 + n)T + 5		ns
Delay time from CLKOUT↑ to ADOENB	<36>	t_{DKADEN}			3	ns
Delay time from CLKOUT↑ to address/data output	<37>	t_{DKAD}			5	ns

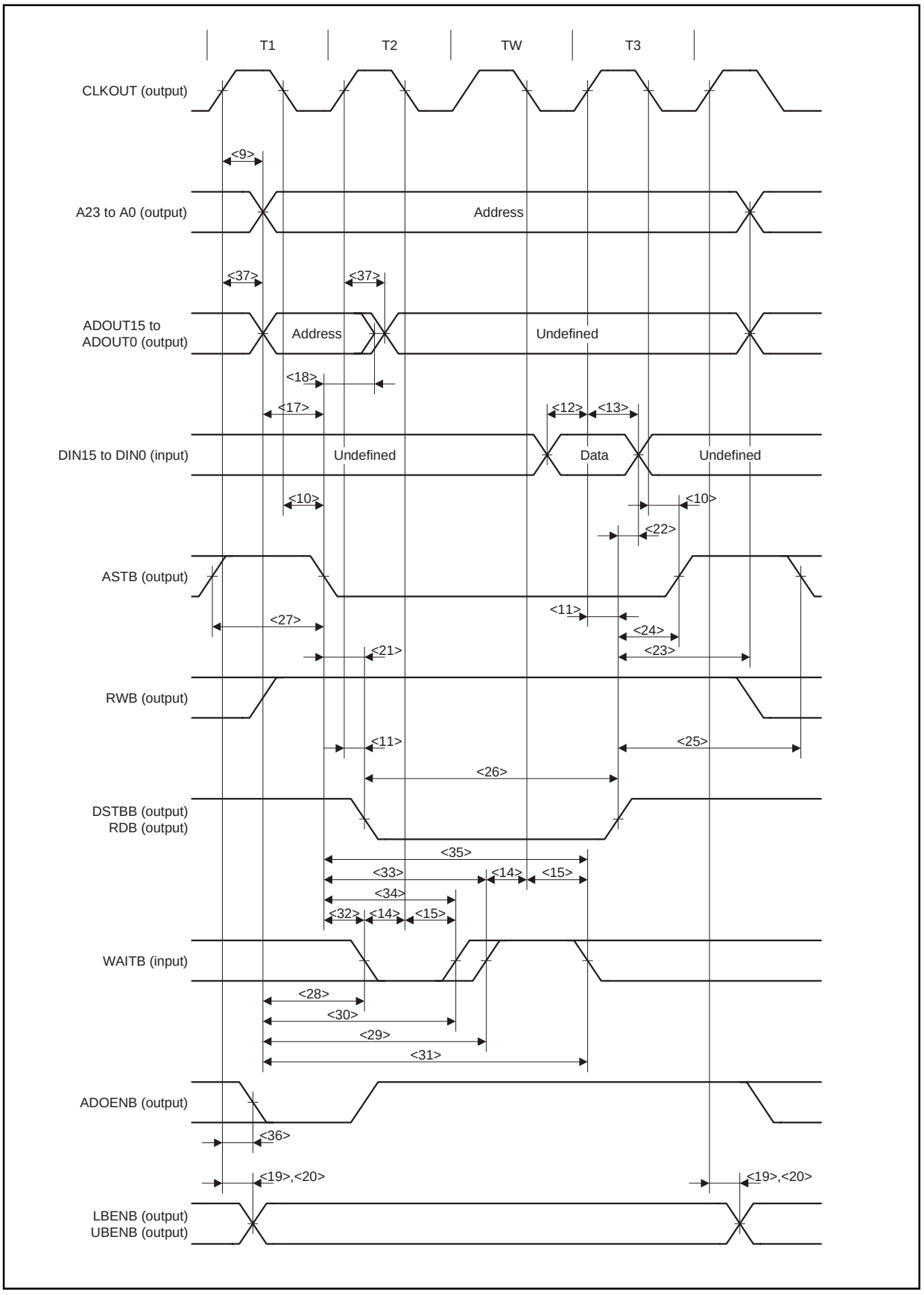
Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing changes when programmable wait cycles are inserted.

3. i indicates the number of idle states (0 or 1) inserted after read cycle.

4. Be sure to satisfy at least one of data input hold times t_{HKID} and t_{HDID}.

(3) Read timing (2/2)



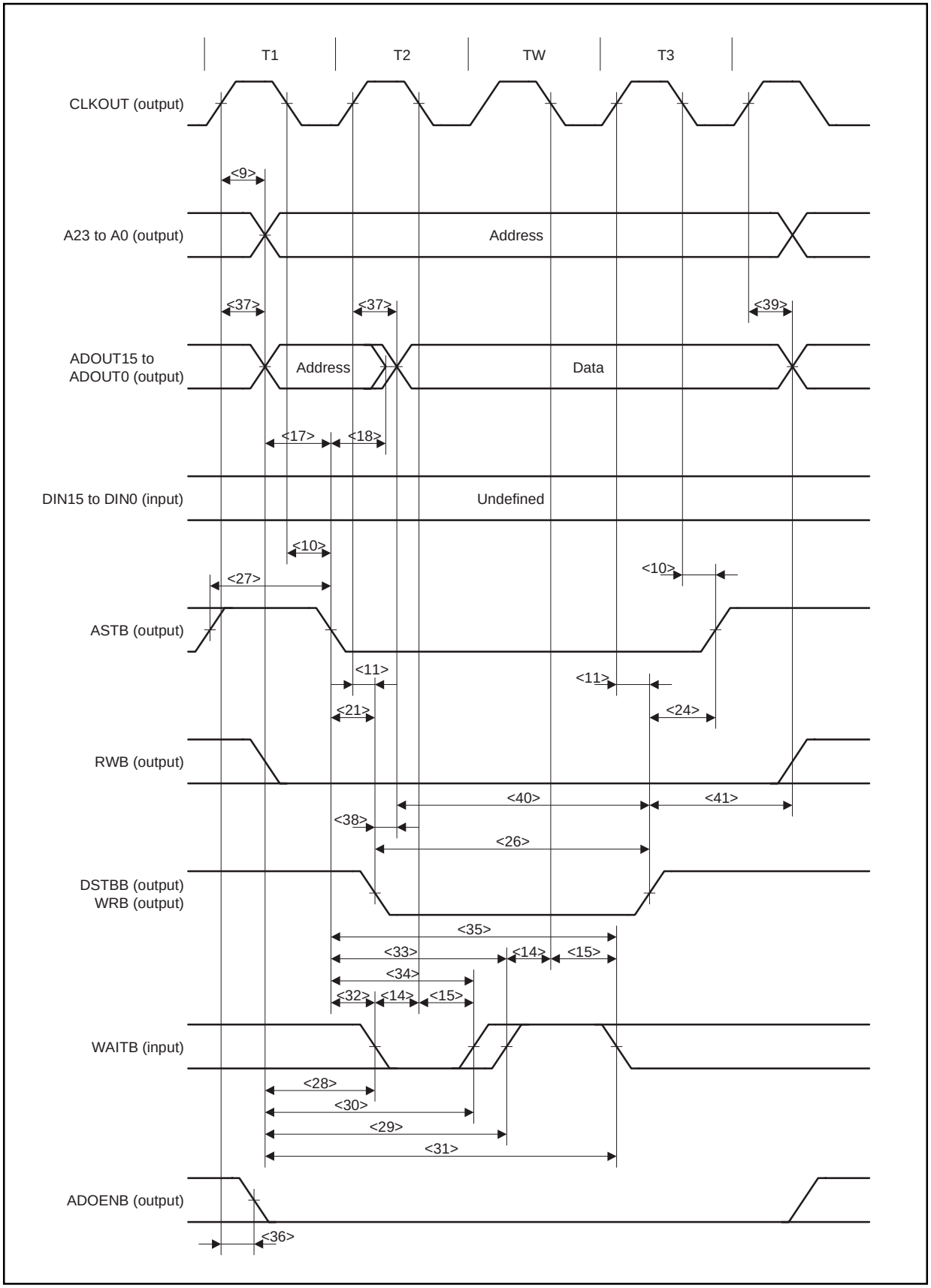
(4) Write timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<9>	t_{DKA}			3	ns
Delay time from CLKOUT↓ to ASTB	<10>	t_{DKST}			4	ns
Delay time from CLKOUT↑ to DSTBB	<11>	t_{DKD}			3	ns
WAITB setup time (to CLKOUT↓)	<14>	t_{SWTK}		2		ns
WAITB hold time (from CLKOUT↓)	<15>	t_{HKWT}		2		ns
Address setup time (to ASTB↓)	<17>	t_{SAST}		0.5T – 6		ns
Address hold time (from ASTB↓)	<18>	t_{HSTA}		0.5T – 6		ns
Delay time from ASTB↓ to DSTBB↓	<21>	t_{DSTD}		0.5T – 6		ns
Delay time from DSTBB↑ to ASTB↑	<24>	t_{DDSTH}		0.5T – 6		ns
DSTBB low-level width	<26>	t_{WDL}		(1 + n)T – 5		ns
ASTB high-level width	<27>	t_{WSTH}		T – 5		ns
WAITB setup time (to address)	<28>	t_{SAWT1}	n ≥ 1		1.5T – 11	ns
	<29>	t_{SAWT2}			(1.5 + n)T – 11	ns
WAITB hold time (from address)	<30>	t_{HAWT1}	n ≥ 1	1.5T + 6		ns
	<31>	t_{HAWT2}		(1.5 + n)T + 6		ns
WAITB setup time (to ASTB↓)	<32>	t_{SSTWT1}	n ≥ 1		T – 10	ns
	<33>	t_{SSTWT2}			(1 + n)T – 10	ns
WAITB hold time (from ASTB↓)	<34>	t_{HSTWT1}	n ≥ 1	nT + 5		ns
	<35>	t_{HSTWT2}		(1 + n)T + 5		ns
Delay time from CLKOUT↑ to ADOENB	<36>	t_{DKADEN}			3	ns
Delay time from CLKOUT↑ to address/data output	<37>	t_{DKAD}			5	ns
Delay time from DSTBB↓ to data output	<38>	t_{DDOD}			5	ns
Data output hold time (from CLKOUT↑)	<39>	t_{HKOD}			5	ns
Data output setup time (to DSTBB↑)	<40>	t_{SODD}		(1 + n)T – 5		ns
Data output hold time (from DSTBB↑)	<41>	t_{HDOD}		T – 5		ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing changes when programmable wait cycles are inserted.

(4) Write timing (2/2)



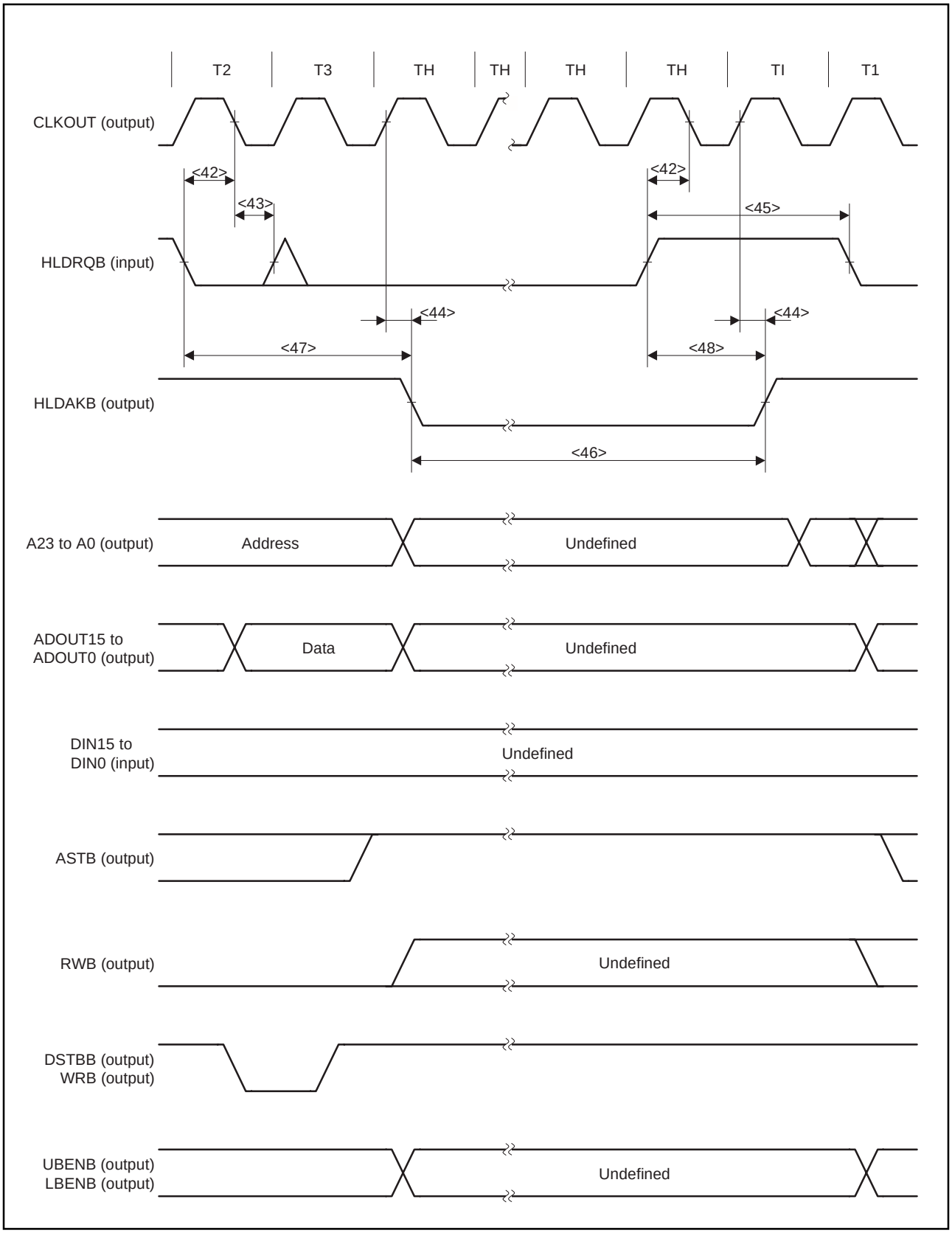
(5) Bus hold timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
HLDRQB setup time (to CLKOUT↓)	<42>	t_{SHQK}		2		ns
HLDRQB hold time (from CLKOUT↓)	<43>	t_{HKHQ}		2		ns
Delay time from CLKOUT↑ to HLDAKB	<44>	t_{DKHA}			3	ns
HLDRQB high-level width	<45>	t_{WHQH}		T + 5		ns
HLDAKB low-level width	<46>	t_{WHAL}		T − 5		ns
Delay time from HLDRQB↓ to HLDAKB↓	<47>	t_{DHQHA1}			(2n + 7.5)T + 11	ns
Delay time from HLDRQB↑ to HLDAKB↑	<48>	t_{DHQHA2}			1.5T + 11	ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing changes when programmable wait cycles are inserted.

(5) Bus hold timing (2/2)



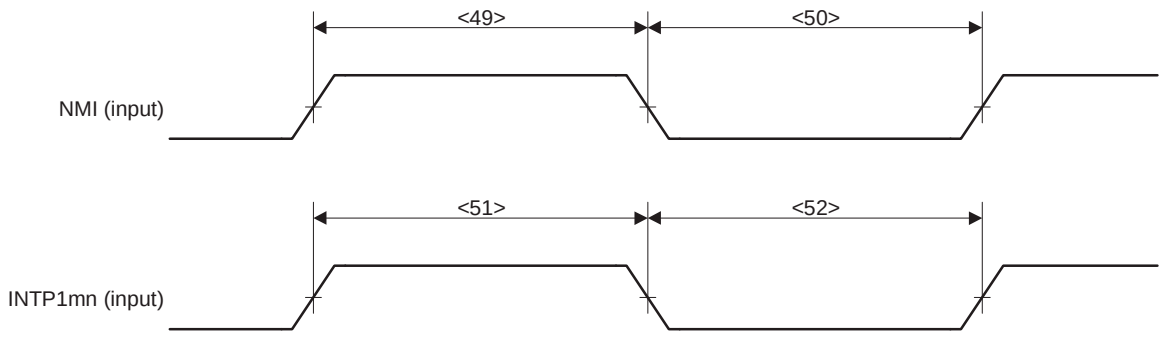
(6) Interrupt timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
NMI high-level width	<49>	t_{WNIH}		500		ns
NMI low-level width	<50>	t_{WNIL}		500		ns
INTP1mn high-level width	<51>	t_{WITH}		3T + 10		ns
INTP1mn low-level width	<52>	t_{WITL}		3T + 10		ns

Remarks 1. T = t_{CYK}

2. m = 4 to 1

n = 3 to 0



Remark m = 4 to 1

n = 3 to 0

[MEMO]

(7) CSI timing (1/2)

(a) Master mode

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
SCKnOUTB cycle	<53>	t_{CYSK}	Output	120		ns
SCKnOUTB high-level width	<54>	t_{WSKH}	Output	0.5 t_{CYSK}–10		ns
SCKnOUTB low-level width	<55>	t_{WSKL}	Output	0.5 t_{CYSK}–10		ns
SI3, SI2, RXDSI1, RXDSI0 setup time (to SCKnOUTB↑)	<56>	t_{SSISK}		5		ns
SI3, SI2, RXDSI1, RXDSI0 hold time (from SCKnOUTB↑)	<57>	t_{HSKSI}		5		ns
SO3, SO2, TXDSO1, TXDSO0 delay time (from SCKnOUTB↓)	<58>	t_{DSKSO}			5	ns

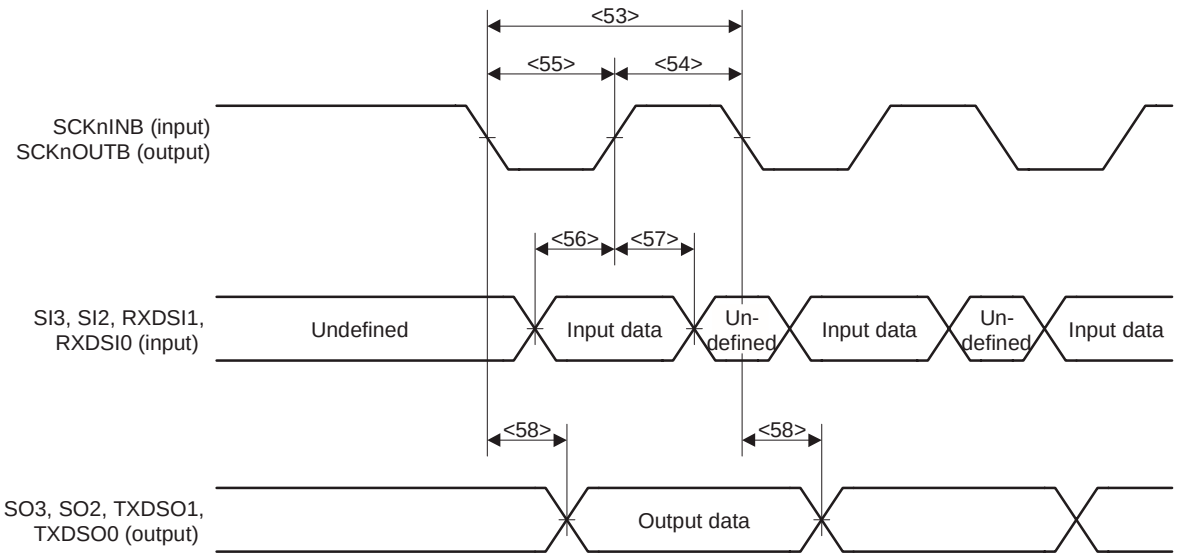
Remark n = 3 to 0

(b) Slave mode

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
SCKnINB cycle	<53>	t_{CYSK}	Input	120		ns
SCKnINB high-level width	<54>	t_{WSKH}	Input	30		ns
SCKnINB low-level width	<55>	t_{WSKL}	Input	30		ns
SI3, SI2, RXDSI1, RXDSI0 setup time (to SCKnINB↑)	<56>	t_{SSISK}		5		ns
SI3, SI2, RXDSI1, RXDSI0 hold time (from SCKnINB↑)	<57>	t_{HSKSI}		5		ns
SO3, SO2, TXDSO1, TXDSO0 delay time (from SCKnINB↓)	<58>	t_{DSKSO}			5	ns

Remark n = 3 to 0

(7) CSI timing (2/2)



Remark n = 3 to 0

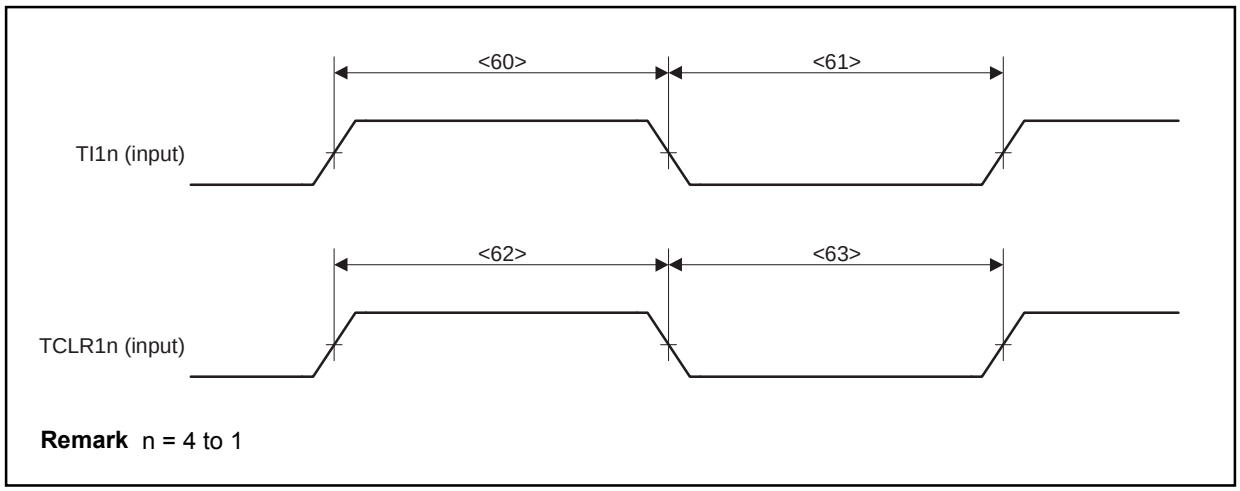
(8) RPU timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
TI1n high-level width	<60>	t_{WTIH}		3T + 10		ns
TI1n low-level width	<61>	t_{WTIL}		3T + 10		ns
TCLR1n high-level width	<62>	t_{WTCH}		3T + 10		ns
TCLR1n low-level width	<63>	t_{WTCL}		3T + 10		ns
Delay time from CLKOUT↑ to TO1nm	<64>	t_{DKTO}			5	ns

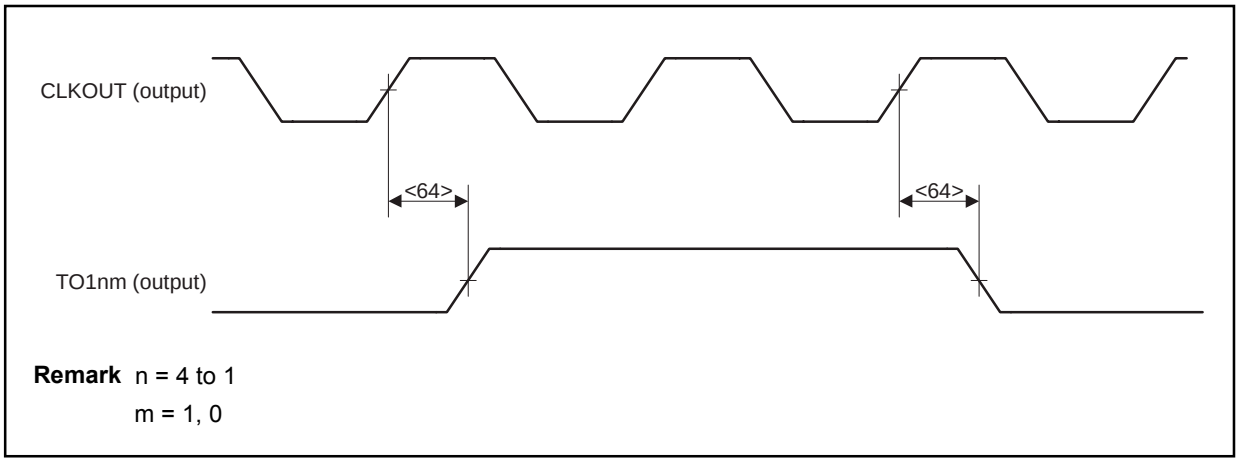
Remarks 1. T = t_{CYK}

2. n = 4 to 1

m = 1, 0



Remark n = 4 to 1



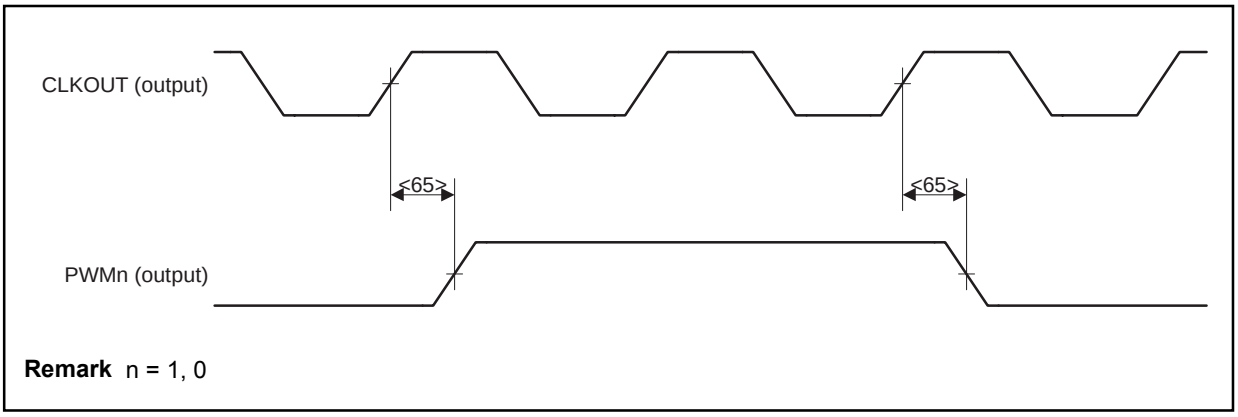
Remark n = 4 to 1

m = 1, 0

(9) PWM timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to PWMn	<65>	t_{DKPWM}			3	ns

Remark n = 1, 0



Remark n = 1, 0

CHAPTER 5 V30MX

The V30MX is an ASIC original CPU core that has improved the bus efficiency by separating the address and data buses of NEC's original microprocessor "μPD70116H" (commonly known as V30HL™). As the instruction set is the same as V30HL, V30MX can be used without making any program changes.

5. 1 Outline

- Complete static circuit configuration and simplified standby and clock stop.
- Low power consumption
- Minimum instruction execution time: 60 ns (33 MHz, 3.3 V)
- On-chip LIM EMS 4.0 supporting register
- Abundant memory addressing modes
- Fourteen 16-bit register sets
- 101 kinds of instruction sets (complete compatibility with μPD70116H)
- High speed execution of address calculation

5. 1. 1 Symbol diagram

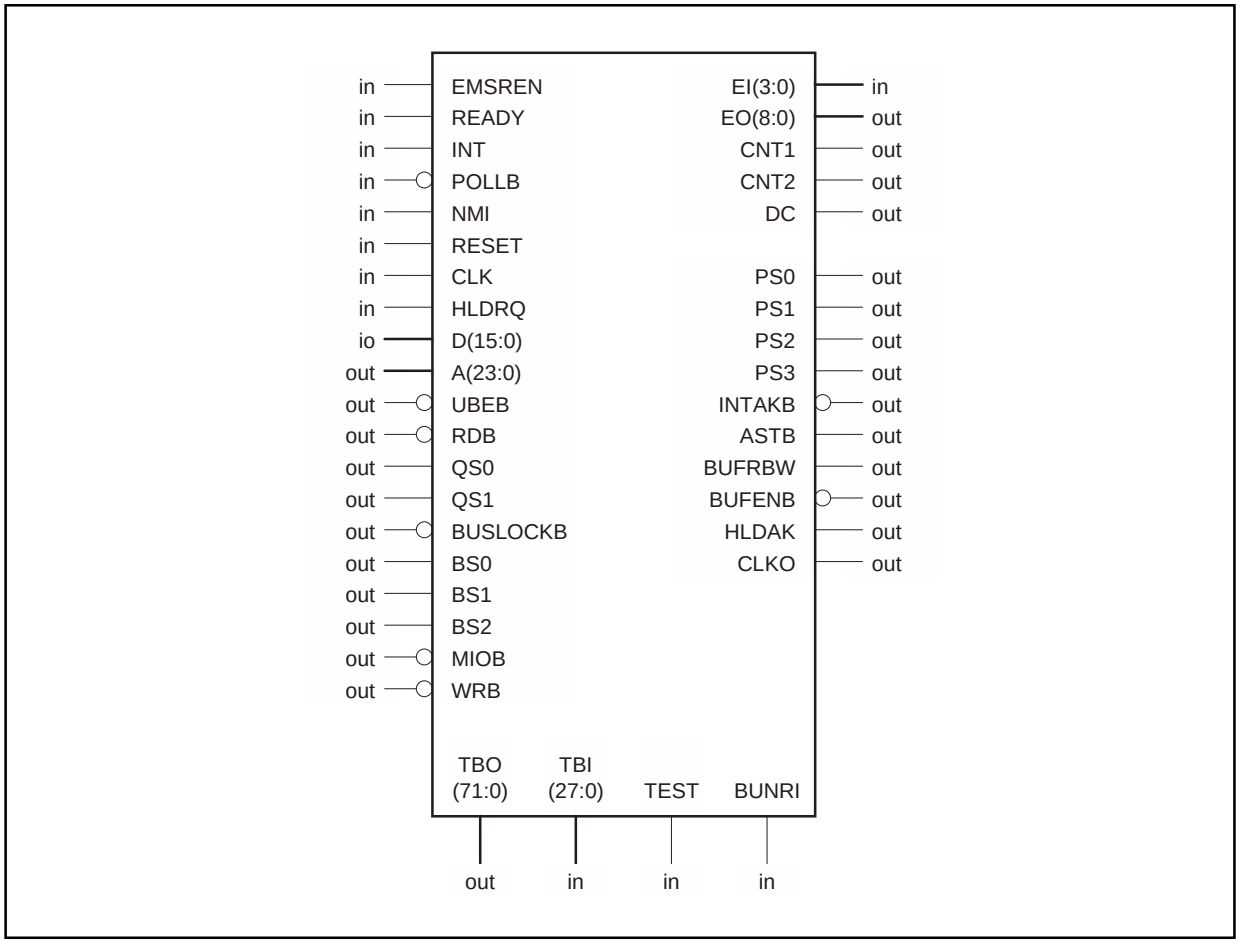
Number of grids

177k grids

228k grids (including wiring area)

Number of separation simulation patterns

80k



5. 1. 2 Pin capacitance

Remark C_{IN}: Capacitance of only input pin

C_{inewl}: Value of C_{IN} with wiring capacitance (estimated wire length capacitance) taken into consideration (l = 10 mm)

(1) Input pins

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
CLK	0.033	1.933	POLLB	0.033	1.933
EI3 to EI0	0.033	1.933	READY	0.033	1.933
EMSREN	0.033	1.933	RESET	0.033	1.933
HLDRQ	0.033	1.933	TBI27 to TBI0	0.033	1.932
INT	0.033	1.933	TEST	0.033	1.933
NMI	0.033	1.933	BUNRI	0.039	1.939

(2) Output pins

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
A23 to A0	4.001	0.063	1.963	EO8 to EO0	5.421	–	–
ASTB	5.421	–	–	HLDAK	5.421	–	–
BS2 to BS0	4.007	0.063	1.963	INTAKB	5.421	–	–
BUFENB	4.007	0.063	1.963	MIOB	4.007	0.063	1.963
BUFRBW	4.007	0.063	1.963	PS3 to PS0	5.421	–	–
BUSLOCKB	4.007	0.063	1.963	QS1, QS0	5.421	–	–
CLKO	5.421	–	–	RDB	4.007	0.063	1.963
CNT1	5.421	–	–	UBEB	4.007	0.063	1.963
CNT2	5.421	–	–	WRB	4.007	0.063	1.963
DC	5.421	–	–	TBO71 to TBO0	4.007	0.063	1.963

(3) Input/output pins

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
DO15 to DO0	4.007	0.096	1.996

5. 2 Notes for Initialization

(1) Internal gate initialization method

Although the initial state of flip-flops does not cause a problem in the actual product, it has been known to do so during simulation. To avoid such problems, portions that cannot be initialized at a usual reset are initialized using the following methods.

(a) Verilog-XL™

As initialization is carried out automatically during simulation, there is no special need to do anything.

(b) V.sim™

Input the following command when executing simulation.

Command>iv instance-name/_U248:N01 = 1

If this command is set in the additional-command file, it will save the necessity of re-typing it each time simulation is executed.

(2) Inputting the initialization pattern from the test pin is not necessary.

(3) The initialization pattern is input from the normal pin in the following manner.

(a) Hardware reset

Input logic 1 of at least four system clock (clock input to the CLK pin) cycles to the RESET pin.
The V30MX executes instructions from address 0FFFF0H when logic 0 is input to the RESET pin and the reset is released.

(b) Instruction input

Input instructions as necessary after the hardware reset is released.
Instructions tend to become long (from several hundred bytes to several KB) and the CPU instruction read timing is then difficult to catch, so use a method that will store the total chip simulation program in the memory.

5. 3 Notes for Pattern Generation and Circuit Designing

5. 3. 1 Handling 3-state outputs

3-state output pins such as RDB and WRB (refer to **5. 4 Pin Functions** for the 3-state output pins) become high impedance when the CPU is put on hold. If a floating level is supplied to a functional cell connected to a 3-state pin, errors and overlapping current due to a middle level input may occur. Use the CNT2 and CNT1 pins to avoid high impedance and ensure that a floating level is not input directly.

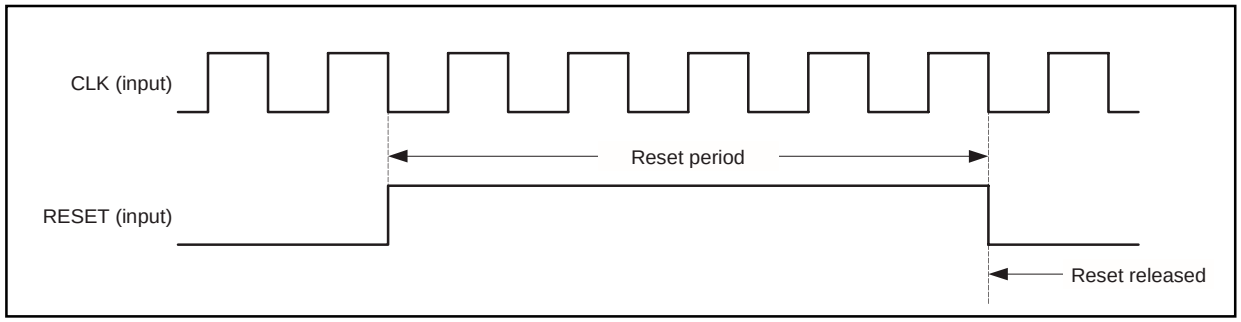
5. 3. 2 RESET signal

The RESET signal is executed from an instruction in the FFFF0H address after the high levels of at least four clocks have been input to the RESET pin, and upon the release of the reset following the input of the low levels.

Be aware that if the variable timing of the RESET signal conflicts with the clock rise, a timing error will be generated and the reset operation may not run normally.

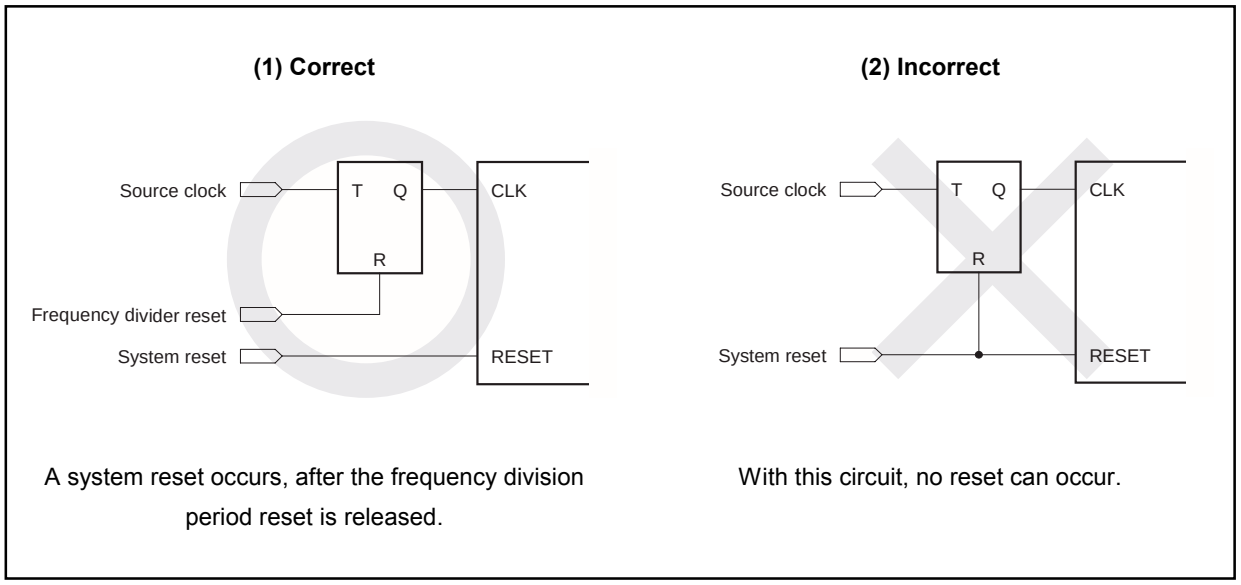
The RESET input must be set to low level when the reset is released.

Figure 5-1. RESET Signal Input Example



5. 3. 3 CLK input

A CPU reset occurs only when the CLK input toggles. Care should be taken when a frequency divider is inserted at the CLK input of the CPU.



5. 3. 4 Initialization of internal registers

Before executing the test program, be sure to execute an instruction to assign initial values to the internal registers used in test program execution.

Take particular care not to overlook the stack pointer (SP).

To minimize the execution time, avoid using subroutines as much as possible.

5. 3. 5 Restriction of test program size

The number of execution steps in the test program will ultimately determine the length of the test pattern, so try to reduce the number of these steps.

Make sure the number of patterns in the execution steps does not exceed 64000 (note that this is not the number of execution steps). To do this, ensure that the test program size is no more than 8 KB.

If the test program contains loops, however, the number of patterns in the execution steps can exceed 64000, even if the test program size is 8 KB or less. Note that the value of 8 KB is only a rough estimate.

5. 3. 6 Segment specification in the test program

The V30MX can use 16 MB of address space in the EMS mode. However, as it is necessary to load the test program in an address that consists of eight consecutive KB, code segment specification should be carried out once only.

For similar reasons, data and stack segment specification should also be carried out once only.

★ 5. 3. 7 Timing verification

Input timing verification methods vary depending on the simulator used.

For Verilog-XL, input timing verification is performed at execution, but for V.sim, no error message is output even if the input error ocurred at execution. For V.sim, be sure to verify by executing the OPENCAD™ menu “Megamacro Timing Check”.

If other simulators are used, contact NEC for verification methods.

5. 4 Pin Functions

Pin Name	I/O	Function
A23 to A0	3-state output	Address output
D15 to D0	Input/output	Data input/output
UBEB	3-state output	Upper byte enable signal output of data bus
RDB	3-state output	Read strobe output
READY	Input	Inputs control signal that inserts wait states to bus cycle
INT	Input	Maskable interrupt request input
POLLB	Input	Synchronized sense signal input from external system
NMI	Input	Non-maskable interrupt request input
RESET	Input	System reset input
CLK	Input	System clock input
QS1, QS0	Output	Queue status output
BUSLOCKB	3-state output	Bus lock output
BS2 to BS0	3-state output	Bus cycle status output
MIOB	3-state output	I/O access/memory access select output
PS3 to PS0	Output	Processor status output
WRB	3-state output	Write strobe output
INTAKB	Output	Interrupt acknowledge output
ASTB	Output	Address strobe output
BUFRBW	3-state output	Buffer read/write output
BUFENB	3-state output	Buffer enable output
HLDRQ	Input	Bus hold request input
HLDAK	Output	Bus hold acknowledge output
EMSREN	Input	EMS registers access enable input
CNT2, CNT1	Output	3-state output control output
DC	Output	D15 to D0 control output
BUNRI	Input	Pin for test using test bus
TEST	Input	
TBI27 to TBI0	Input	
TBO71 to TBO0	3-state output	
EI3 to EI0	Input	NEC reserved pin
EO8 to EO0	Output	
CLKO	Output	

5. 5 Electrical Specifications

The following specifications are for a single macro. An actual chip consists of two or more macros. Design the system so that all the specifications of the individual macros are satisfied when the chip is used.

5. 5. 1 Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to +4.6	V
Operating ambient temperature	T_A	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

5. 5. 2 Recommended operation range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	−40		+85	°C
Clock cycle	t_{CYK}	30			ns

5. 5. 3 DC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

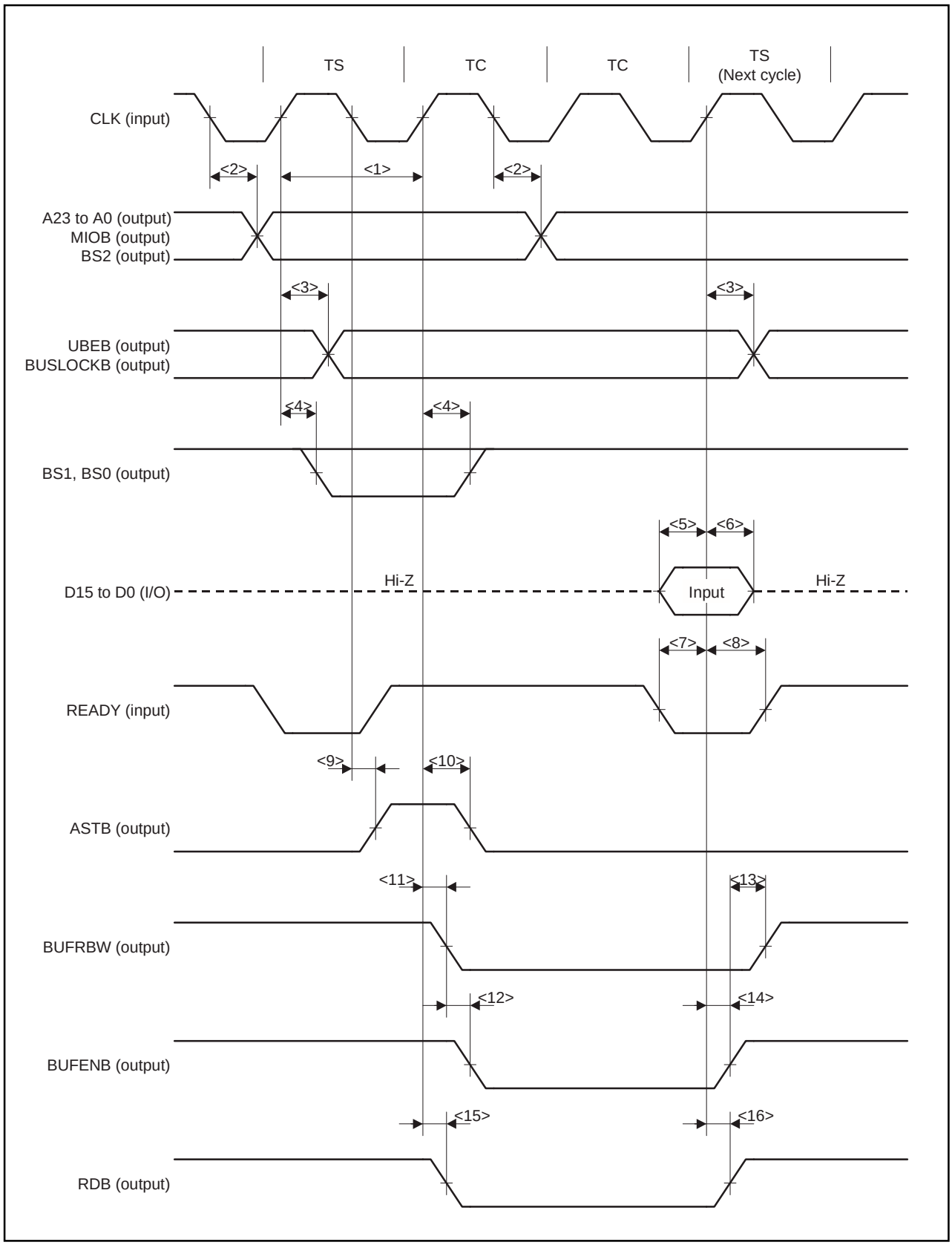
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD}	During normal operation		0.5	1.0	mA/MHz
		In standby (HALT) mode		0.05	0.10	mA/MHz
		When clock is stopped			30	μA

5. 5. 4 AC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

(1) Read timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Clock cycle	<1>	t_{CYK}		30		ns
Delay time from CLK↓ to address	<2>	t_{DKA}		2.4	11	ns
Delay time from CLK↑ to UBEB, BUSLOCKB	<3>	t_{DKUB}		2.4	11	ns
Delay time from CLK↑ to BS1, BS0	<4>	t_{DKB}		2.4	11	ns
Data setup time (to CLK↑)	<5>	t_{SDK}		3		ns
Data hold time (from CLK↑)	<6>	t_{HKD}		6		ns
READY setup time (to CLK↑)	<7>	t_{SRYK}		3		ns
READY hold time (from CLK↑)	<8>	t_{HKRY}		3		ns
Delay time from CLK↓ to ASTB↑	<9>	t_{DKSTH}		1.3	6	ns
Delay time from CLK↑ to ASTB↓	<10>	t_{DKSTL}		1.3	5.5	ns
Delay time from CLK↑ to BUFRBW↓	<11>	t_{DKCT}		1.9	9	ns
Delay time from BUFRBW↓ to BUFENB↓	<12>	t_{RWEN}		0	2	ns
Delay time from BUFENB↑ to BUFRBW↑	<13>	t_{DENRW}		0	2	ns
Delay time from CLK↑ to BUFENB↑ (Read cycle)	<14>	t_{DKENR}		1.9	9	ns
Delay time from CLK↑ to RDB↓, WRB↓	<15>	t_{DKCML}		1.8	8.4	ns
Delay time from CLK↑ to RDB↑, WRB↑	<16>	t_{DKCMH}		1.8	8.4	ns

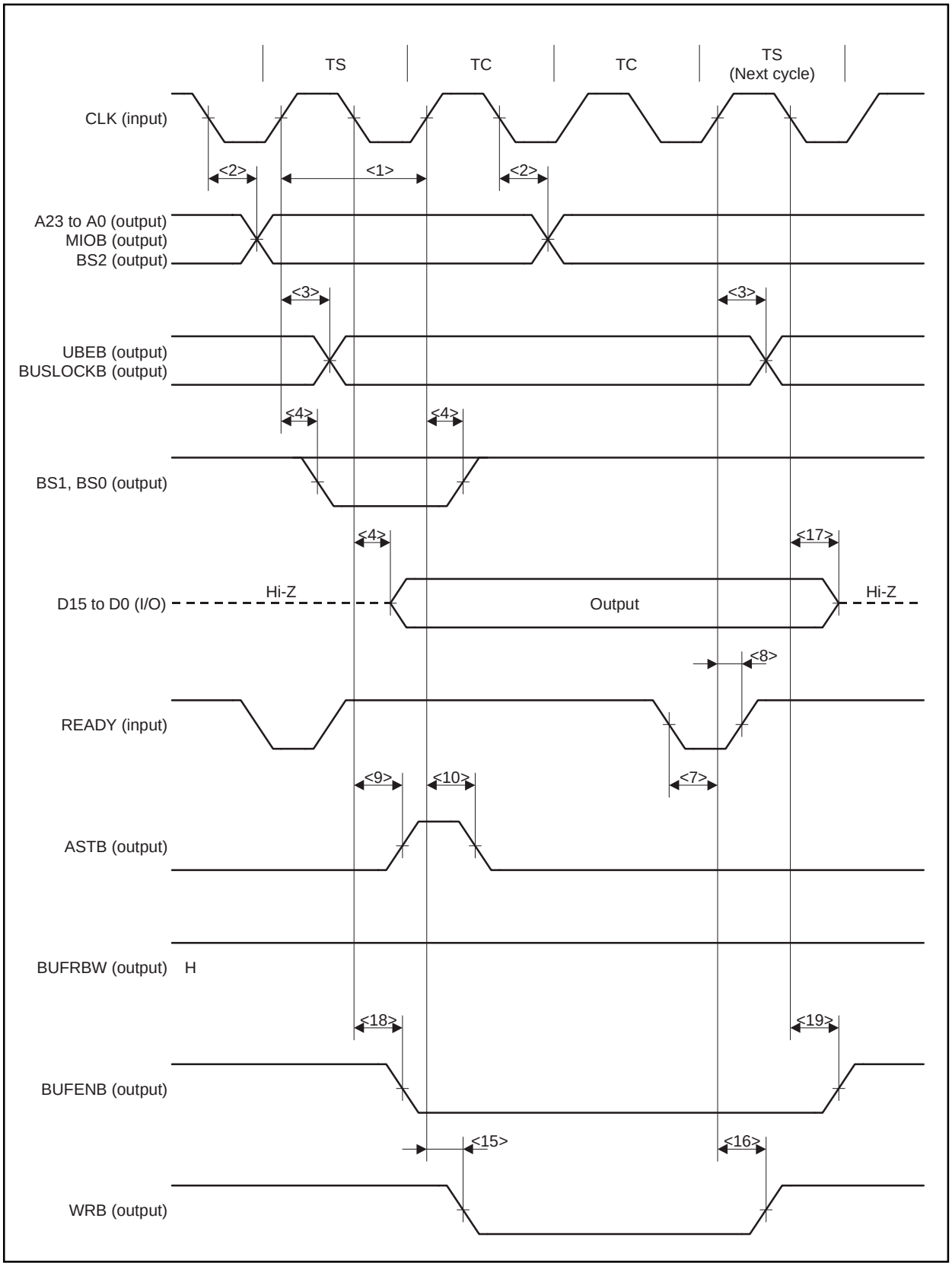
(1) Read timing (2/2)



(2) Write timing (1/2)

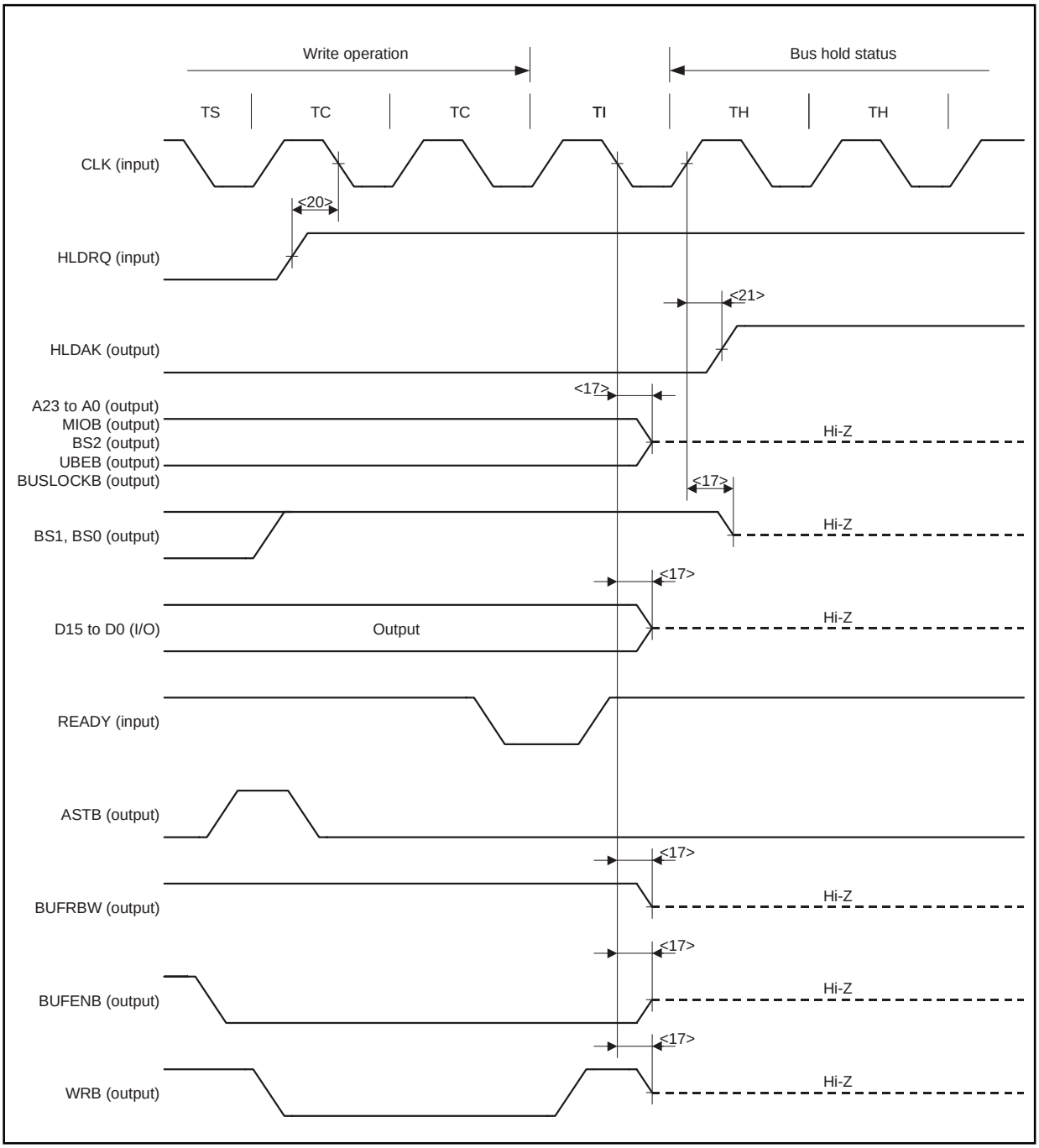
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Clock cycle	<1>	t_{CYK}		30		ns
Delay time from CLK↓ to address	<2>	t_{DKA}		2.4	11	ns
Delay time from CLK↑ to UBEB, BUSLOCKB	<3>	t_{DKUB}		2.4	11	ns
Delay time from CLK↑ to BS1, BS0	<4>	t_{DKB}		2.4	11	ns
READY setup time (to CLK↑)	<7>	t_{SRYK}		3		ns
READY hold time (from CLK↑)	<8>	t_{HKRY}		3		ns
Delay time from CLK↓ to ASTB↑	<9>	t_{DKSTH}		1.3	6	ns
Delay time from CLK↑ to ASTB↓	<10>	t_{DKSTL}		1.3	5.5	ns
Delay time from CLK↑ to RDB↓, WRB↓	<15>	t_{DKCML}		1.8	8.4	ns
Delay time from CLK↑ to RDB↑, WRB↑	<16>	t_{DKCMH}		1.8	8.4	ns
Delay time from CLK↓ to data float	<17>	t_{FKD}		2.3	10	ns
Delay time from CLK↓ to BUFENB↓ (Write cycle)	<18>	t_{DKENWH}		1.4	7	ns
Delay time from CLK↓ to BUFENB↑ (Write cycle)	<19>	t_{DKENWL}		1.4	7	ns

(2) Write timing (2/2)



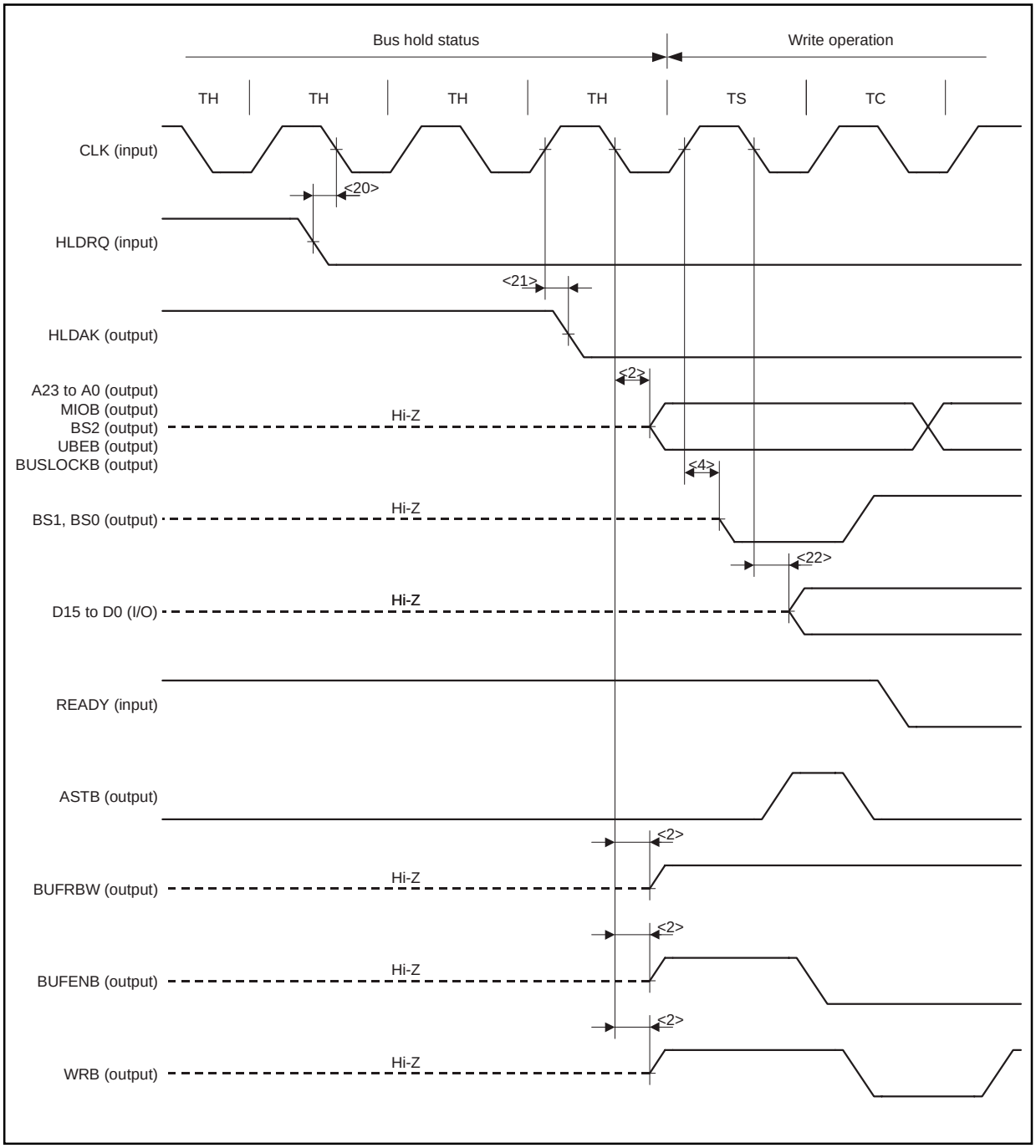
(3) Entering the bus hold status timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLK↓ to data float	<17>	t_{FKD}		2.3	10	ns
HLDRQ setup time (to CLK)	<20>	t_{SIK}		3		ns
Delay time from CLK↓ to HLDAK	<21>	t_{DKHA}		1.4	6	ns



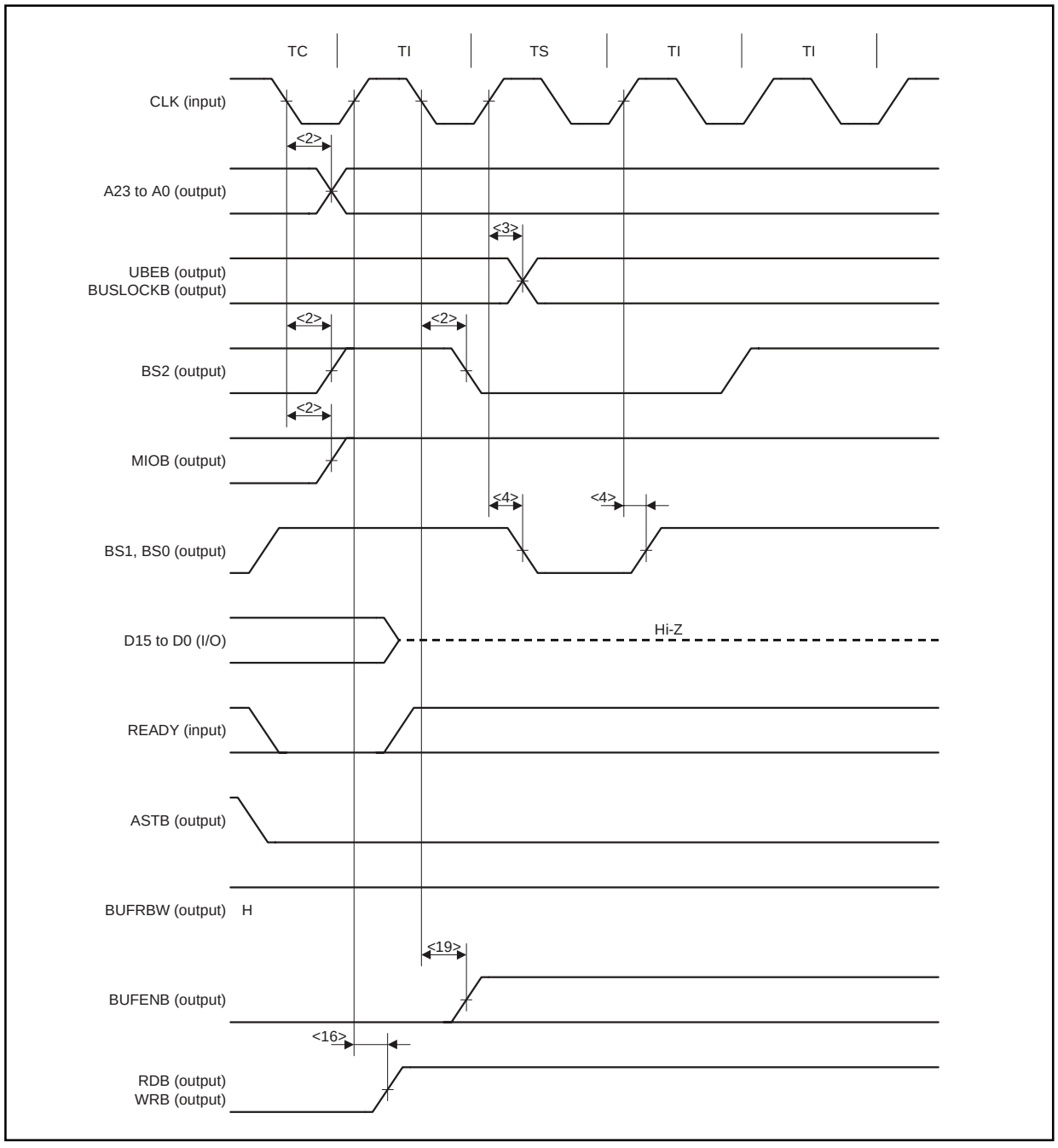
(4) Exiting the bus hold status timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLK↓ to address	<2>	t_{DKA}		2.4	11	ns
Delay time from CLK↑ to BS1, BS0	<4>	t_{DKB}		2.4	11	ns
HLDRQ setup time (to CLK)	<20>	t_{SIK}		3		ns
Delay time from CLK↓ to HLDAK	<21>	t_{DKHA}		1.4	6	ns
Delay time from CLK↓ to data output	<22>	t_{DKD}		2.2	10	ns



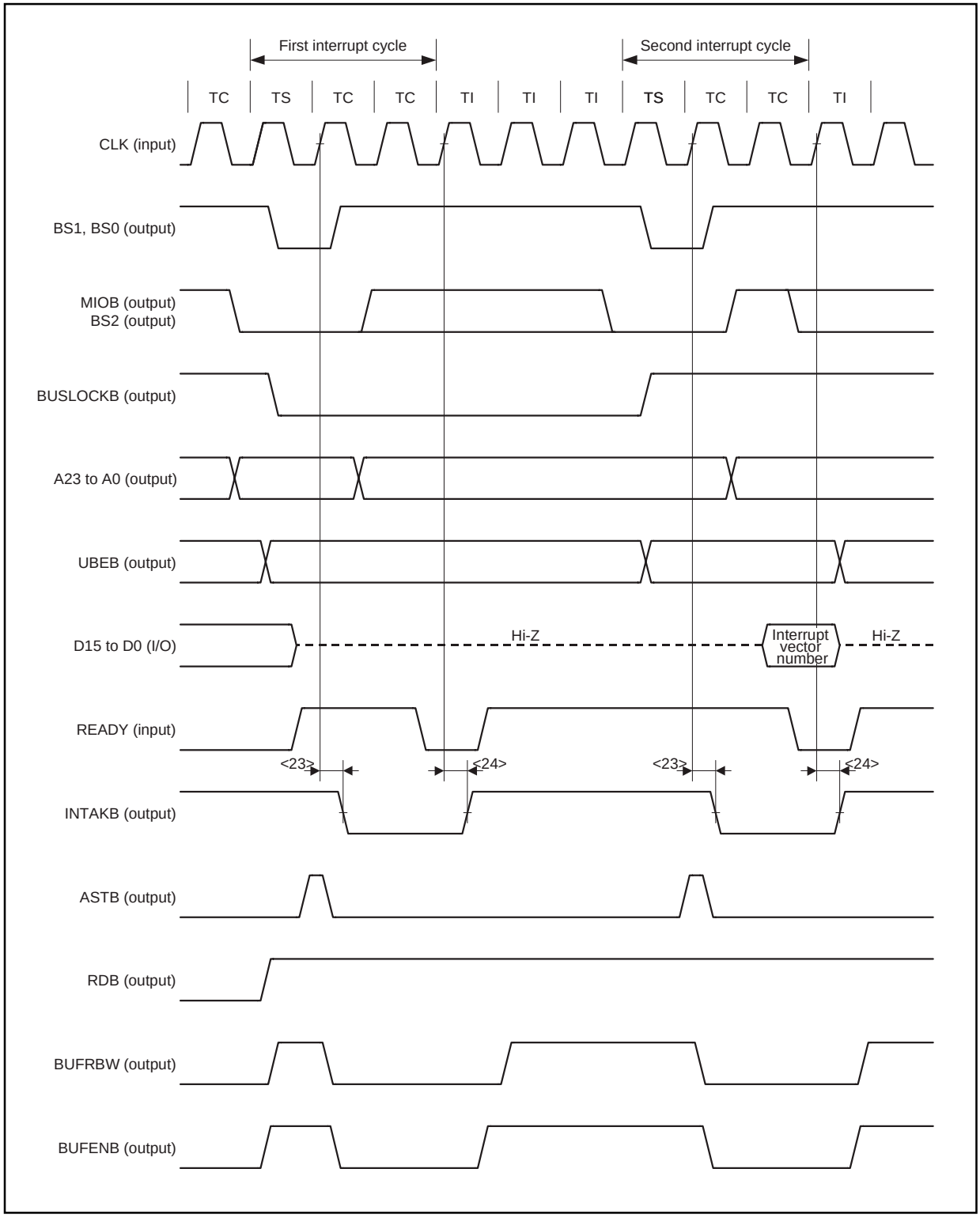
(5) Standby (HALT) mode setup timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLK↓ to address	<2>	t_{DKA}		2.4	11	ns
Delay time from CLK↑ to UBEB, BUSLOCKB	<3>	t_{DKUB}		2.4	11	ns
Delay time from CLK↑ to BS1, BS0	<4>	t_{DKB}		2.4	11	ns
Delay time from CLK↑ to RDB↑, WRB↑	<16>	t_{DKCMH}		1.8	8.4	ns
Delay time from CLK↓ to BUFENB↑ (Write cycle)	<19>	t_{DKENWL}		1.4	7	ns



(6) Interrupt acknowledge timing

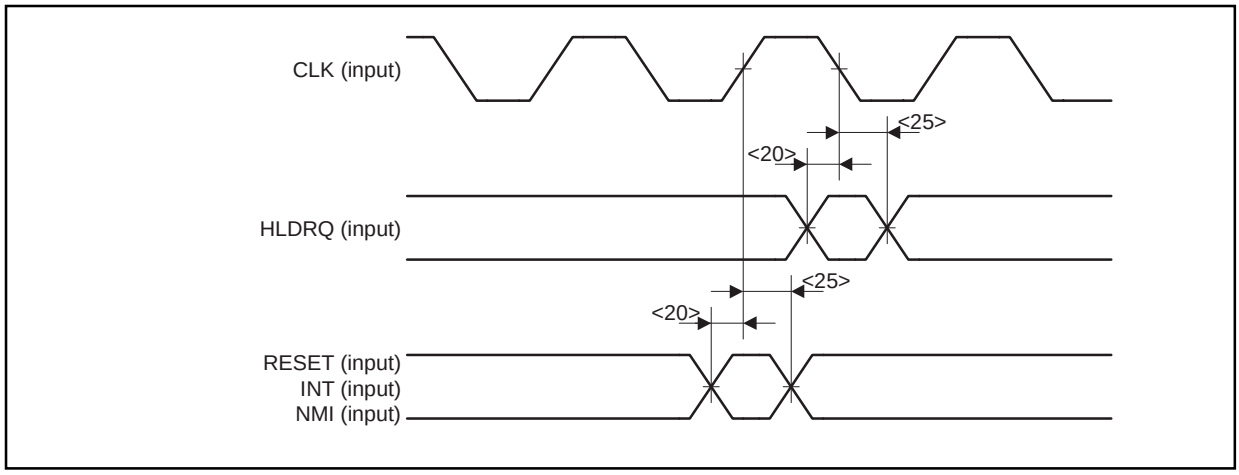
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLK↑ to INTAKB↓	<23>	t_{DKIF}		1.4	7	ns
Delay time from CLK↑ to INTAKB↑	<24>	t_{DKIR}		1.4	7	ns



(7) RESET, INT, NMI, HLDRQ input timing

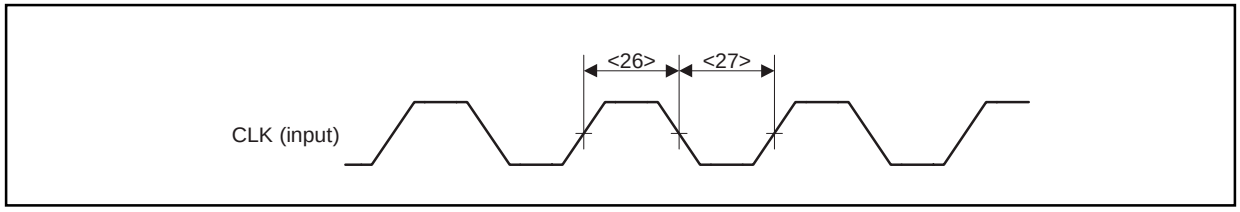
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Asynchronous signals[Note] setup time (to CLK)	<20>	t_{SIK}		3		ns
Asynchronous signals[Note] hold time (from CLK)	<25>	t_{HIK}		6		ns

Note Asynchronous signals: RESET, INT, NMI, HLDRQ



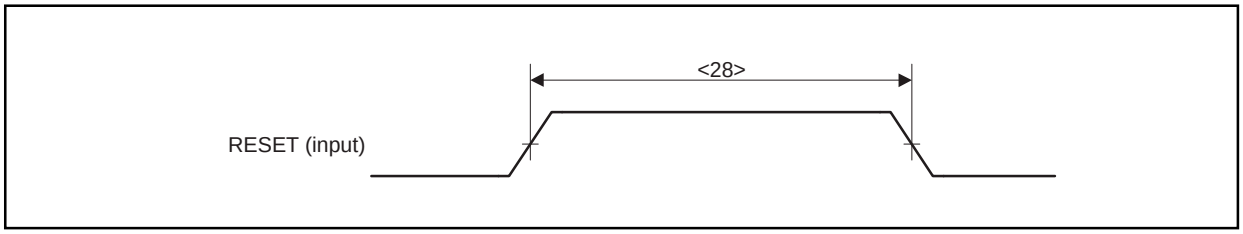
(8) CLK input timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Clock high-level width	<26>	t_{KKH}		10		ns
Clock low-level width	<27>	t_{KKL}		10		ns



(9) Reset timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
RESET high-level width	<28>	t_{WRSTH}		$4t_{CYK}$		ns



CHAPTER 6 V30MZ

(Under development)

The V30MZ is a CPU core that has further improved the CPU core “V30MX”, which has increased bus efficiency of the NEC original microprocessor “μPD70116H” (commonly known as V30HL).

High-speed processing at the speed of a RISC microprocessor has been made possible due to the raising of bus efficiency with the realization of a 1 clock/1 bus cycle, and the considerable increase in instruction execution speed through internal pipelining.

Compared to the 4.3 MIPS (at 33 MHz operation, no wait) of the V30MX, the V30MZ has realized a processing performance of 35 MIPS (at 66 MHz operation, no wait).

6. 1 Outline

- Processing performance: 35MIPS (@ 66 MHz operation, no wait)
- CMOS static design (capable of complete stop of the internal system clock)
- 1 clock/1 bus cycle
- External bus interface
  Address bus: 20 bits
  Data bus: 16 bits (I/O separate buses)
- Bus hold function
- Standby function (HALT mode)

6. 1. 1 Symbol diagram

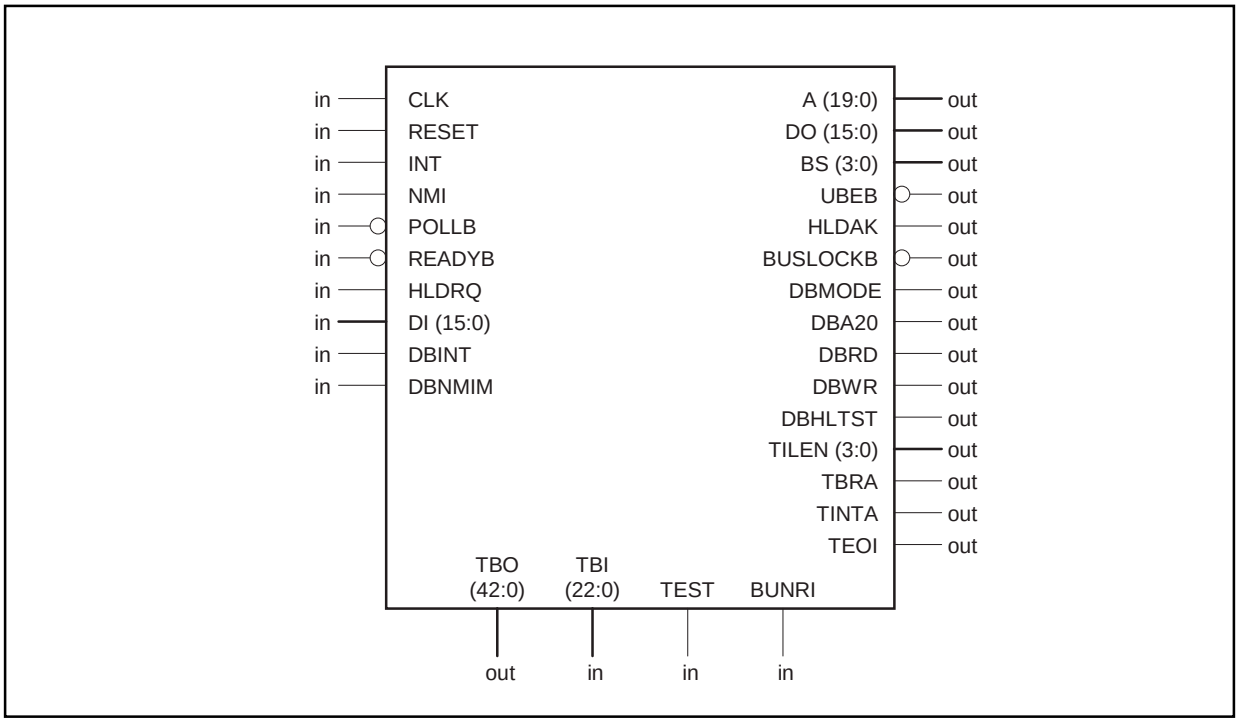
Number of grids

207k grids

251k grids (including wiring area)

Number of separation simulation patterns

52k



6. 1. 2 Pin capacitance

Remark C_{IN}: Capacitance of only input pin

C_{inewl}: Value of C_{IN} with wiring capacitance (estimated wire length capacitance) taken into consideration (l = 10 mm)

(1) Input pins

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
CLK	0.012	1.912	DI15 to DI0	0.012	1.912
RESET	0.012	1.912	BUNRI	0.037	1.937
NMI	0.012	1.912	TEST	0.010	1.910
INT	0.012	1.912	TBI22 to TBI0	0.011	1.911
HLDRQ	0.012	1.912	DBINT	0.008	1.908
POLLB	0.012	1.912	DBNMIM	0.008	1.908
READYB	0.012	1.912			

(2) Output pins

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
A19 to A0	13.072	–	–	DBA20	13.072	–	–
BS3 to BS0	13.072	–	–	DBRD	13.072	–	–
DO15 to DO0	13.072	–	–	DBWR	13.072	–	–
BUSLOCKB	13.072	–	–	DBHLTST	13.072	–	–
HLDAK	13.072	–	–	TEOI	13.072	–	–
UBEB	13.072	–	–	TILEN3 to TILEN0	13.072	–	–
TBO42 to TBO0	6.536	0.047	1.947	TBRA	13.072	–	–
DBMODE	13.072	–	–	TINTA	13.072	–	–

6. 2 Notes for Simulation Execution

6. 2. 1 Notes for V.sim simulation

When simulation is executed through V.sim, input the following command.

Command>mr instance-name/_NTMZROM NTMZROM NTMZROM.nincf

★ **6. 2. 2 Timing verification**

Input timing verification methods vary depending on the simulator used.

For Verilog-XL, input timing verification is performed at execution, but for V.sim, no error message is output even if the input error ocurred at execution. For V.sim, be sure to verify by executing the OPENCAD menu “Megamacro Timing Check”.

If other simulators are used, contact NEC for verification methods.

6. 3 Notes for Initialization

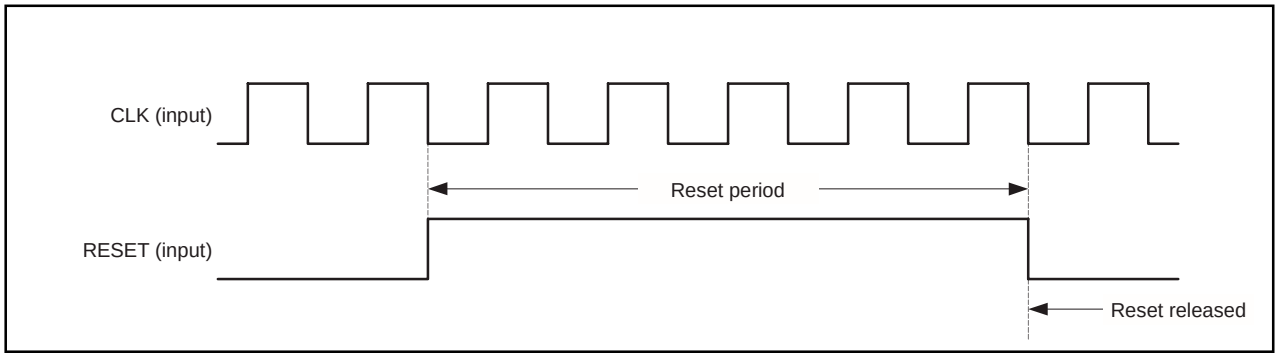
6. 3. 1 RESET signal

The RESET signal is executed from an instruction in the FFFF0H address after the high levels of at least four clocks have been input to the RESET pin, and upon the release of the reset following the input of the low levels.

Be aware that if the variable timing of the RESET signal conflicts with the clock rise, a timing error will be generated and the reset operation may not run normally.

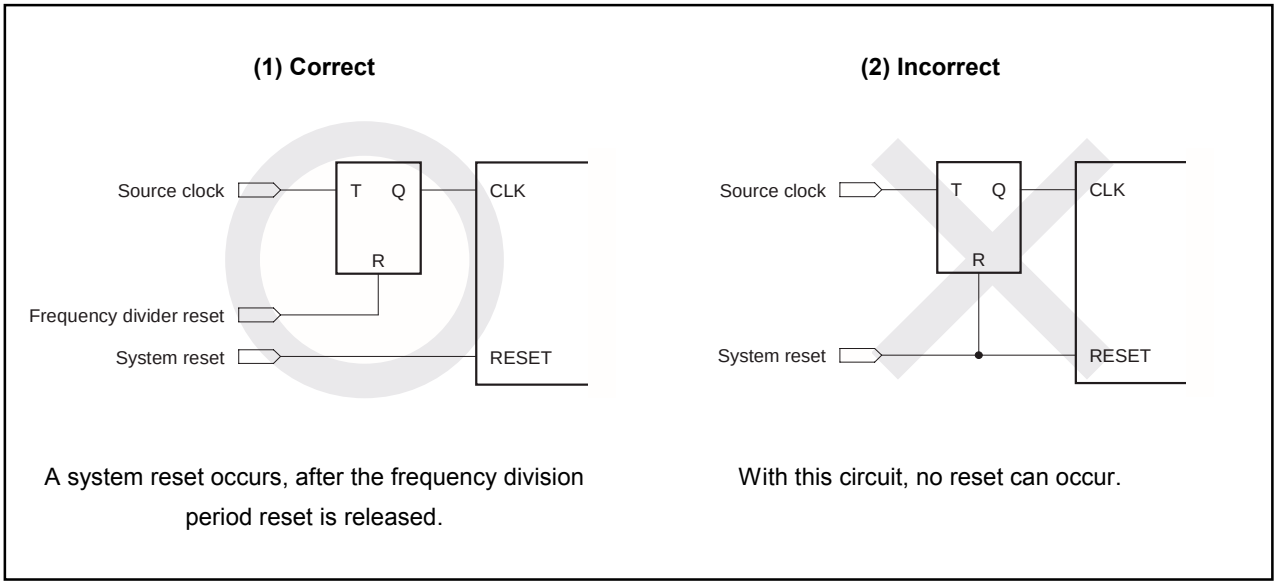
The RESET input must be set to low level when the reset is released.

Figure 6-1. RESET Signal Input Example



6. 3. 2 CLK input

A CPU reset occurs only when the CLK input toggles. Care should be taken when a frequency divider is inserted at the CLK input of the CPU.



6. 3. 3 Initialization of internal registers

Before executing the test program, be sure to execute an instruction to assign initial values to the internal registers used in test program execution.

6. 4 Pin Functions

Pin Name	I/O	Function
A19 to A0	Output	Address output
DI15 to DI0	Input	Data input
DO15 to DO0	Output	Data output
UBEB	Output	Upper byte enable signal output of data bus
BS3 to BS0	Output	Bus cycle status output
READYB	Input	Inputs control signal that inserts wait states to bus cycle
BUSLOCKB	Output	Bus lock output
POLLB	Input	Synchronized sense signal input from external system
RESET	Input	System reset input
HLDRQ	Input	Bus hold request input
HLDAK	Output	Bus hold acknowledge output
NMI	Input	Non-maskable interrupt request input
INT	Input	Maskable interrupt request input
CLK	Input	System clock input
BUNRI	Input	Pin for test using test bus
TEST	Input	
TBI22 to TBI0	Input	
TBO42 to TBO0	Output	
DBINT	Input	NEC reserved pin
DBMODE	Output	
DBA20	Output	
DBRD	Output	
DBWR	Output	
DBNMIM	Input	
DBHLTST	Output	
TEOI	Output	
TILEN3 to TILEN0	Output	
TBRA	Output	
TINTA	Output	

6. 5 Electrical Specifications (Preliminary)

The following specifications are for a single macro. An actual chip consists of two or more macros. Design the system so that all the specifications of the individual macros are satisfied when the chip is used.

6. 5. 1 Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

6. 5. 2 Recommended operation range

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Supply voltage	V_{DD}	At 2.0 V supply voltage	1.8	2.0	2.2	V
			At 3.3 V supply voltage	3.0	3.3	3.6	V
	Operating ambient temperature	T_A		–40		+85	°C
★	Clock cycle	t_{CYK}	At 2.0 V supply voltage	31			ns
★			At 3.3 V supply voltage	15			ns

6. 5. 3 DC characteristics (T_A = –40 to +85°C)

(1) At 2.0 V supply voltage (V_{DD} = 2.0 V ±0.2 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD}	During operation		0.4	0.8	mA/MHz
		In HALT mode		2	4	μA/MHz
		When clock is stopped			0	μA

(2) At 3.3 V supply voltage (V_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD}	During operation		0.6	1.2	mA/MHz
		In HALT mode		5	10	μA/MHz
		When clock is stopped			0	μA

6. 5. 4 AC characteristics (T_A = –40 to +85°C)

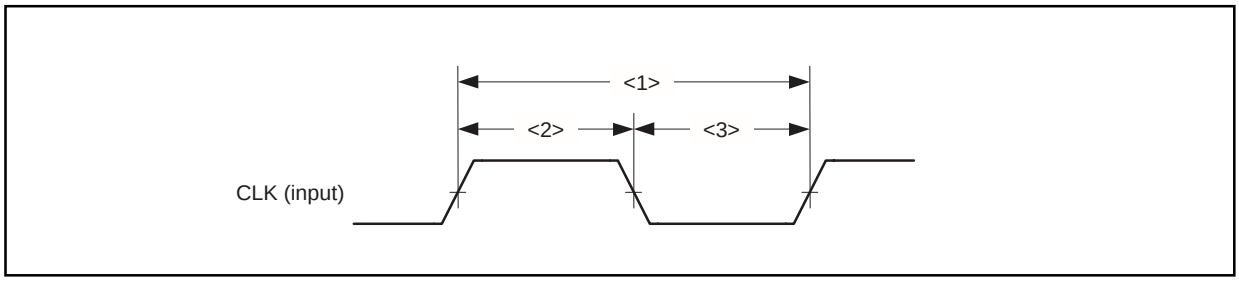
(1) CLK input timing

(a) At 2.0 V supply voltage (V_{DD} = 2.0 V ±0.2 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Operating frequency	ϕ				32	MHz
Clock cycle	<1>	t_{CYK}		31		ns
Clock high-level width	<2>	t_{KKH}		15.5		ns
Clock low-level width	<3>	t_{KKL}		15.5		ns

(b) At 3.3 V supply voltage (V_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Operating frequency	ϕ				66	MHz
Clock cycle	<1>	t_{CYK}		15		ns
Clock high-level width	<2>	t_{KKH}		7		ns
Clock low-level width	<3>	t_{KKL}		7		ns



(2) RESET, INT, NMI, HLDRQ, POLLB input timing

(a) At 2.0 V supply voltage (V_{DD} = 2.0 V ±0.2 V)

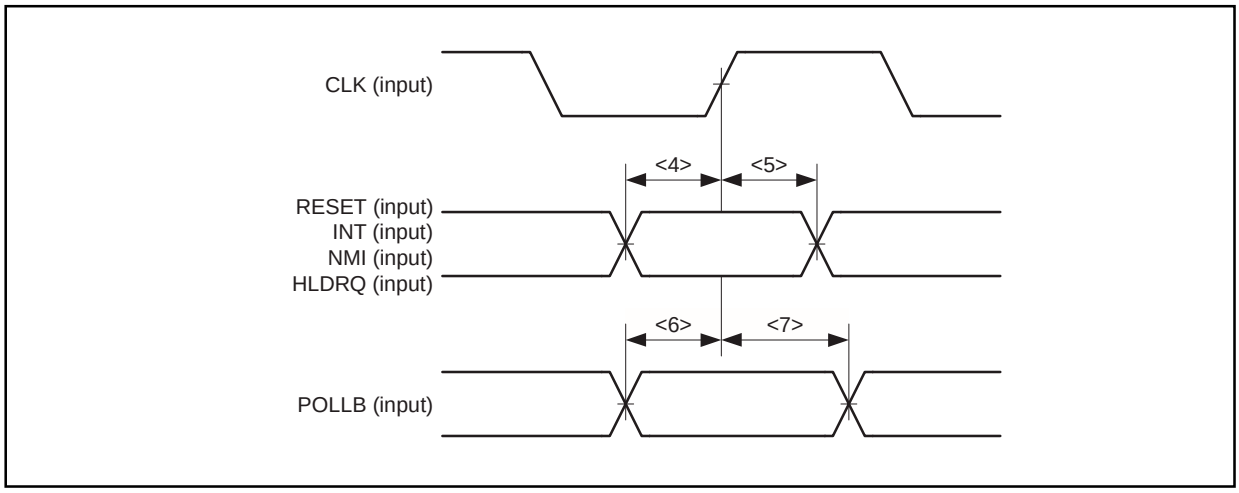
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Asynchronous signals[Note] setup time	<4>	t_{SIK}		2		ns
Asynchronous signals[Note] hold time	<5>	t_{HKI}		2		ns
POLLB setup time	<6>	t_{SPK}		2		ns
POLLB hold time	<7>	t_{HKP}		6		ns

Note Asynchronous signals: RESET, INT, NMI, HLDRQ

(b) At 3.3 V supply voltage (V_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Asynchronous signals[Note] setup time	<4>	t_{SIK}		2		ns
Asynchronous signals[Note] hold time	<5>	t_{HKI}		2		ns
POLLB setup time	<6>	t_{SPK}		2		ns
POLLB hold time	<7>	t_{HKP}		4		ns

Note Asynchronous signals: RESET, INT, NMI, HLDRQ



[MEMO]

(3) Timings of signals related to bus cycle (1/2)

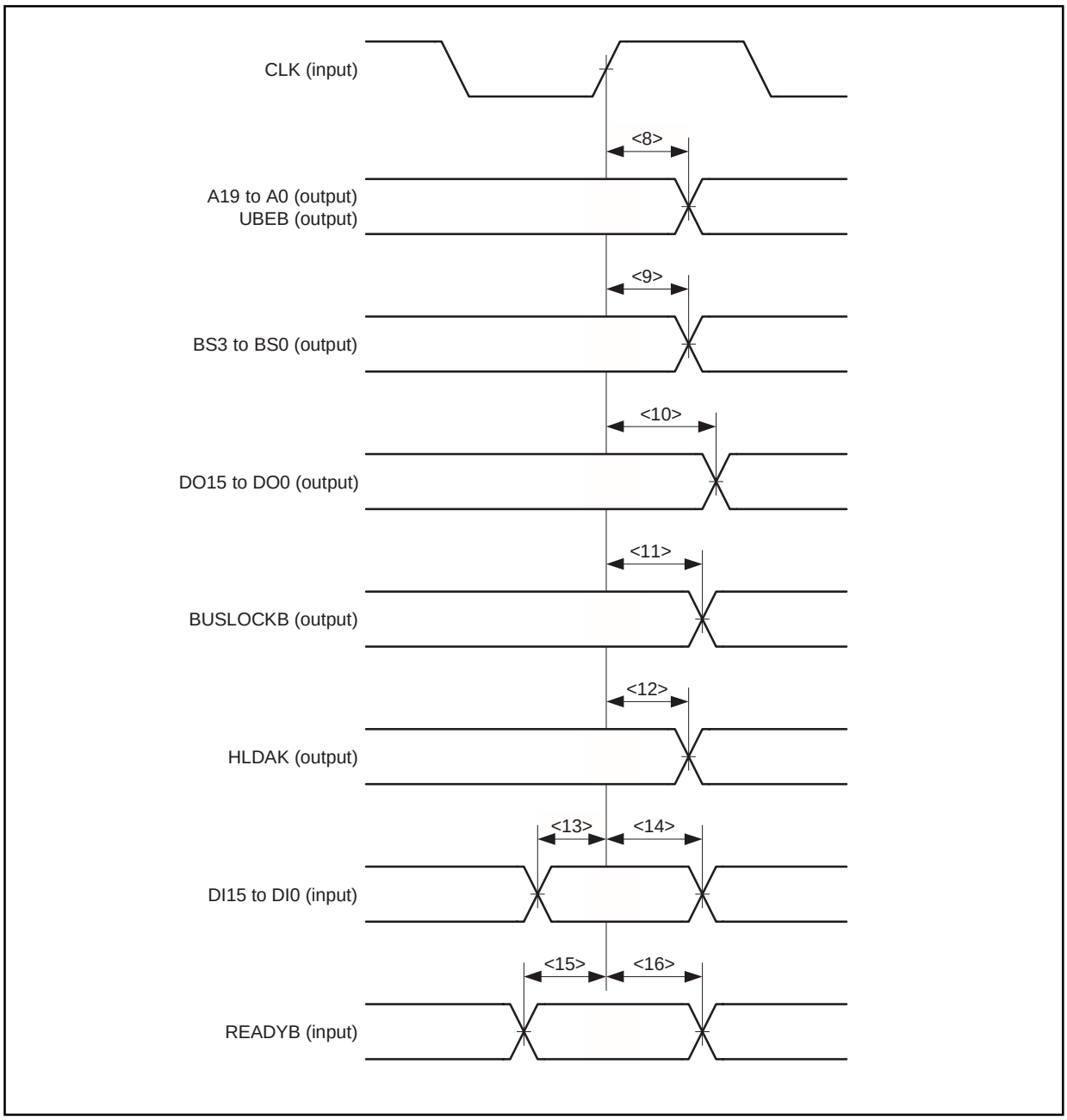
(a) At 2.0 V supply voltage (V_{DD} = 2.0 V ±0.2 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address bus output delay time	<8>	t_{DKA}		1	10	ns
Bus status output delay time	<9>	t_{DKB}		1	10	ns
Data output delay time	<10>	t_{DKD}		2	15	ns
BUSLOCKB delay time	<11>	t_{DKBL}		1	10	ns
HLDAK delay time	<12>	t_{DKHA}		1	10	ns
Data input setup time	<13>	t_{SDK}		2		ns
Data input hold time	<14>	t_{HKD}		6		ns
READYB setup time	<15>	t_{SRK}		7		ns
READYB hold time	<16>	t_{HKR}		4		ns

(b) At 3.3 V supply voltage (V_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address bus output delay time	<8>	t_{DKA}		1	5	ns
Bus status output delay time	<9>	t_{DKB}		1	5	ns
Data output delay time	<10>	t_{DKD}		2	7.5	ns
BUSLOCKB delay time	<11>	t_{DKBL}		1	5	ns
HLDAK delay time	<12>	t_{DKHA}		0.5	5	ns
Data input setup time	<13>	t_{SDK}		1		ns
Data input hold time	<14>	t_{HKD}		3		ns
READYB setup time	<15>	t_{SRK}		3		ns
READYB hold time	<16>	t_{HKR}		2		ns

(3) Timings of signals related to bus cycle (2/2)



CHAPTER 7 NB85E

(Under Development)

The NB85E is a CPU core provided for incorporation in ASICs and includes on chip the “V850E1” CPU, NEC’s 32-bit RISC microprocessor, as well as various peripheral I/O functions such as DMA and interrupt controllers.

7. 1 Outline

- Processing performance: 82 MIPS (@ 66 MHz operation)
- Memory space
  Program area: 64 MB linear
  Data area: 4 GB linear
  Memory bank division function: 2, 4, and 8 MB/bank
- Minimum instruction execution time: 15 ns (@ 66 MHz operation)
- External bus interface
  VSB (V850E System Bus)
  NPB (NEC Peripheral I/O Bus)
- Interrupt/exception control function
  Non-maskable interrupts: 3 sources
  Maskable interrupts: 64 sources
  Exceptions: 1 source
  8 priority levels specifiable (maskable interrupts)
- DMA control function
  4-channel structure
  Transfer unit: 8, 16, and 32 bits
  Maximum number of transfers: 65536 (2^{16})
  Transfer type: Flyby (1-cycle) transfer, 2-cycle transfer
  Transfer mode: Single transfer, single step transfer, line transfer, block transfer
  Terminal count output signals (DMTCO3 to DMTCO0)
- Power save function
  HALT, hardware/software STOP modes
- NB85E901 (RCU[Note]) interface function

Note RCU (Run Control Unit): A control unit for executing JTAG communication or debug processing.

7. 1. 1 Symbol diagram

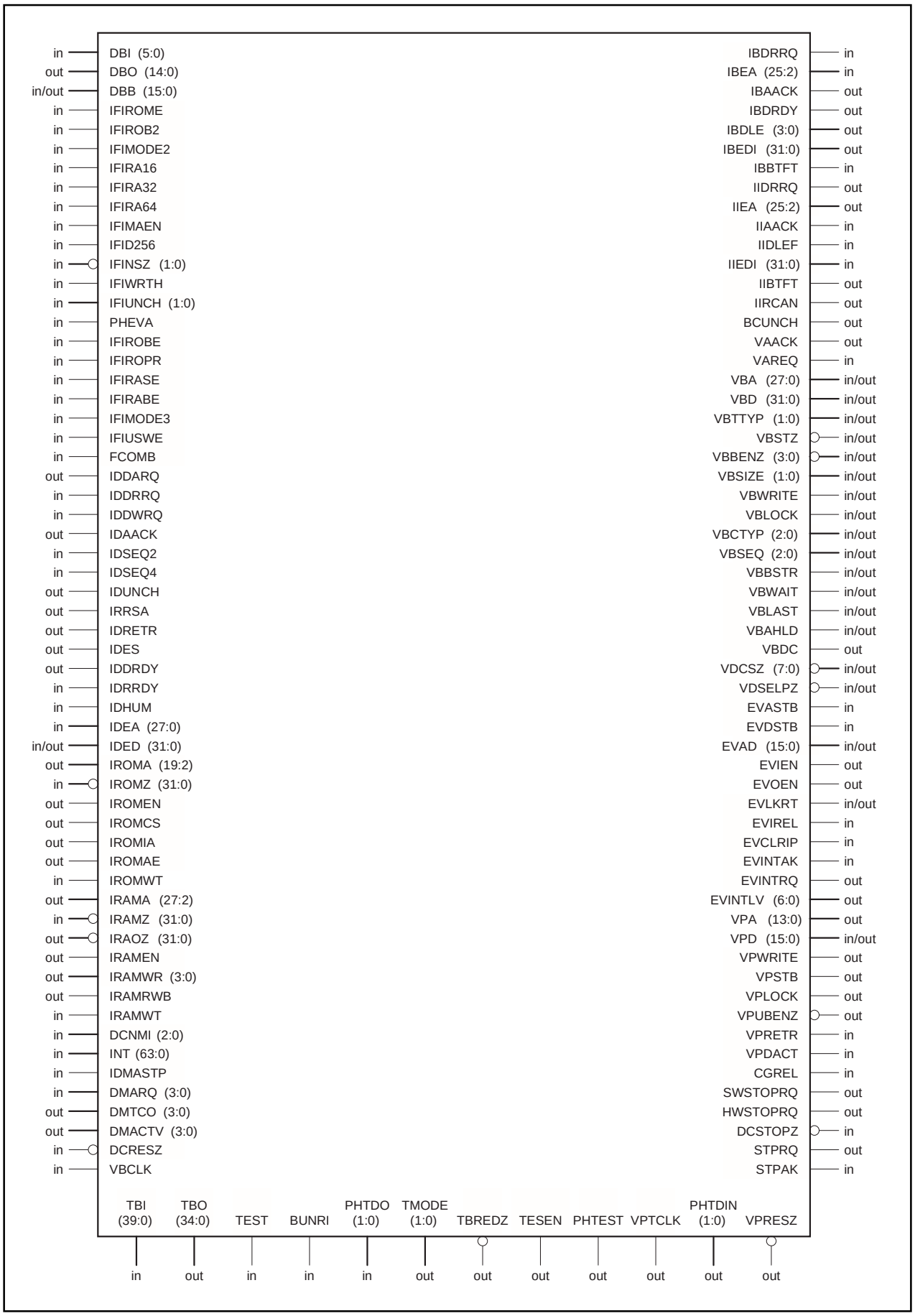
Number of grids

351.6k grids

574.4k grids (including wiring area)

Number of separation simulation patterns

194.7k


in DBI (5:0)
out DBO (14:0)
in/out DBB (15:0)
in IFIROME
in IFIROB2
in IFIMODE2
in IFIRA16
in IFIRA32
in IFIRA64
in IFIMAEN
in IFID256
in IFINSZ (1:0)
in IFIWRTH
in IFIUNCH (1:0)
in PHEVA
in IFIROBE
in IFIROPR
in IFIRASE
in IFIRABE
in IFIMODE3
in IFIUSWE
in FCOMB
out IDDARQ
in IDDRRQ
in IDDWRQ
out IDAACK
in IDSEQ2
in IDSEQ4
out IDUNCH
out IRRSA
out IDRETR
out IDES
out IDDRDY
in IDRRDY
in IDHUM
in IDEA (27:0)
in/out IDED (31:0)
out IROMA (19:2)
in IROMZ (31:0)
out IROMEN
out IROMCS
out IROMIA
out IROMAE
in IROMWT
out IRAMA (27:2)
in IRAMZ (31:0)
out IRAOZ (31:0)
out IRAMEN
out IRAMWR (3:0)
out IRAMRWB
in IRAMWT
in DCNMI (2:0)
in INT (63:0)
in IDMASTP
in DMARQ (3:0)
out DMTCO (3:0)
out DMACTV (3:0)
in DCRESZ
in VBCLK
IBDRRQ in
IBEA (25:2) in
IBAACK out
IBDRDY out
IBDLE (3:0) out
IBEDI (31:0) out
IBBTFT in
IIDRRQ out
IIEA (25:2) out
IIAACK in
IIDLEF in
IIEDI (31:0) in
IIBTFT out
IIRCAN out
BCUNCH out
VAACK out
VAREQ in
VBA (27:0) in/out
VBD (31:0) in/out
VBTTYP (1:0) in/out
VBSTZ in/out
VBBENZ (3:0) in/out
VBSIZE (1:0) in/out
VBWRITE in/out
VBLOCK in/out
VBCTYP (2:0) in/out
VBSEQ (2:0) in/out
VBBSTR in/out
VBWAIT in/out
VBLAST in/out
VBAHLD in/out
VBDC out
VDCSZ (7:0) in/out
VDSELPZ in/out
EVASTB in
EVDSTB in
EVAD (15:0) in/out
EVIEN out
EVOEN out
EVLKRT in/out
EVIREL in
EVCLRIP in
EVINTAK in
EVINTRQ out
EVINTLV (6:0) out
VPA (13:0) out
VPD (15:0) in/out
VPWRITE out
VPSTB out
VPLOCK out
VPUBENZ out
VPRETR in
VPDACT in
CGREL in
SWSTOPRQ out
HWSTOPRQ out
DCSTOPZ in
STPRQ out
STPAK in
TBI (39:0) in
TBO (34:0) out
TEST in
BUNRI in
PHTDO (1:0) in
TMODE (1:0) out
TBREDZ out
TESEN out
PHTEST out
VPTCLK out
PHTDIN (1:0) out
VPRESZ out

7. 1. 2 Pin capacitance

Remark C_{IN}: Capacitance of only input pin

C_{inewl}: Value of C_{IN} with wiring capacitance (estimated wire length capacitance) taken into consideration (l = 10 mm)

(1) Input pins (1/5)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
VPRETR	0.746	2.646	INT45	0.029	1.929
VPDACT	0.297	2.197	INT44	0.014	1.914
VAREQ	0.175	2.075	INT43	0.017	1.917
DCRESZ	0.166	2.066	INT42	0.041	1.941
VBCLK	0.480	2.380	INT41	0.014	1.914
CGREL	0.204	2.104	INT40	0.021	1.921
DCSTOPZ	0.260	2.160	INT39	0.018	1.918
STPAK	0.230	2.130	INT38	0.011	1.911
IDMASTP	0.178	2.078	INT37	0.008	1.908
DMARQ3	0.180	2.080	INT36	0.007	1.907
DMARQ2	0.189	2.089	INT35	0.009	1.909
DMARQ1	0.153	2.053	INT34	0.032	1.932
DMARQ0	0.177	2.077	INT33	0.068	1.968
DCNMI2	0.021	1.921	INT32	0.016	1.916
DCNMI1	0.015	1.915	INT31	0.012	1.912
DCNMI0	0.010	1.910	INT30	0.016	1.916
INT63	0.020	1.920	INT29	0.018	1.918
INT62	0.014	1.914	INT28	0.016	1.916
INT61	0.014	1.914	INT27	0.013	1.913
INT60	0.014	1.914	INT26	0.010	1.910
INT59	0.035	1.935	INT25	0.011	1.911
INT58	0.023	1.923	INT24	0.024	1.924
INT57	0.011	1.911	INT23	0.023	1.923
INT56	0.029	1.929	INT22	0.023	1.923
INT55	0.008	1.908	INT21	0.016	1.916
INT54	0.011	1.911	INT20	0.028	1.928
INT53	0.014	1.914	INT19	0.014	1.914
INT52	0.041	1.941	INT18	0.009	1.909
INT51	0.029	1.929	INT17	0.008	1.908
INT50	0.019	1.919	INT16	0.039	1.939
INT49	0.041	1.941	INT15	0.007	1.907
INT48	0.011	1.911	INT14	0.026	1.926
INT47	0.022	1.922	INT13	0.022	1.922
INT46	0.027	1.927	INT12	0.026	1.926

(1) Input pins (2/5)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
INT11	0.061	1.961	IROMZ4	0.726	2.626
INT10	0.051	1.951	IROMZ3	0.848	2.748
INT9	0.028	1.928	IROMZ2	0.731	2.631
INT8	0.025	1.925	IROMZ1	0.581	2.481
INT7	0.013	1.913	IROMZ0	0.717	2.617
INT6	0.027	1.927	IROMWT	0.070	1.970
INT5	0.023	1.923	IRAMZ31	0.274	2.174
INT4	0.018	1.918	IRAMZ30	0.159	2.059
INT3	0.012	1.912	IRAMZ29	0.255	2.155
INT2	0.022	1.922	IRAMZ28	0.298	2.198
INT1	0.030	1.930	IRAMZ27	0.280	2.180
INT0	0.012	1.912	IRAMZ26	0.275	2.175
IROMZ31	0.673	2.573	IRAMZ25	0.200	2.100
IROMZ30	1.383	3.283	IRAMZ24	0.281	2.181
IROMZ29	1.122	3.022	IRAMZ23	0.207	2.107
IROMZ28	0.754	2.654	IRAMZ22	0.189	2.089
IROMZ27	0.695	2.595	IRAMZ21	0.320	2.220
IROMZ26	1.017	2.917	IRAMZ20	0.290	2.190
IROMZ25	1.267	3.167	IRAMZ19	0.415	2.315
IROMZ24	1.203	3.103	IRAMZ18	0.295	2.195
IROMZ23	1.381	3.281	IRAMZ17	0.389	2.289
IROMZ22	0.860	2.760	IRAMZ16	0.322	2.222
IROMZ21	0.645	2.545	IRAMZ15	0.234	2.134
IROMZ20	1.473	3.373	IRAMZ14	0.202	2.102
IROMZ19	0.738	2.638	IRAMZ13	0.289	2.189
IROMZ18	0.751	2.651	IRAMZ12	0.296	2.196
IROMZ17	0.631	2.531	IRAMZ11	0.317	2.217
IROMZ16	0.653	2.553	IRAMZ10	0.254	2.154
IROMZ15	0.805	2.705	IRAMZ9	0.320	2.220
IROMZ14	0.662	2.562	IRAMZ8	0.344	2.244
IROMZ13	0.783	2.683	IRAMZ7	0.305	2.205
IROMZ12	0.757	2.657	IRAMZ6	0.225	2.125
IROMZ11	0.855	2.755	IRAMZ5	0.317	2.217
IROMZ10	0.712	2.612	IRAMZ4	0.495	2.395
IROMZ9	0.686	2.586	IRAMZ3	0.542	2.442
IROMZ8	0.769	2.669	IRAMZ2	0.418	2.318
IROMZ7	0.781	2.681	IRAMZ1	0.264	2.164
IROMZ6	0.775	2.675	IRAMZ0	0.289	2.189
IROMZ5	0.635	2.535	IRAMWT	0.463	2.363

(1) Input pins (3/5)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
IBDRRQ	0.166	2.066	IIEDI19	0.054	1.954
IBEA25	0.153	2.053	IIEDI18	0.067	1.967
IBEA24	0.050	1.950	IIEDI17	0.058	1.958
IBEA23	0.141	2.041	IIEDI16	0.017	1.917
IBEA22	0.171	2.071	IIEDI15	0.074	1.974
IBEA21	0.169	2.069	IIEDI14	0.055	1.955
IBEA20	0.196	2.096	IIEDI13	0.059	1.959
IBEA19	0.040	1.940	IIEDI12	0.074	1.974
IBEA18	0.101	2.001	IIEDI11	0.051	1.951
IBEA17	0.105	2.005	IIEDI10	0.066	1.966
IBEA16	0.129	2.029	IIEDI9	0.071	1.971
IBEA15	0.059	1.959	IIEDI8	0.059	1.959
IBEA14	0.082	1.982	IIEDI7	0.034	1.934
IBEA13	0.084	1.984	IIEDI6	0.057	1.957
IBEA12	0.058	1.958	IIEDI5	0.068	1.968
IBEA11	0.018	1.918	IIEDI4	0.061	1.961
IBEA10	0.114	2.014	IIEDI3	0.073	1.973
IBEA9	0.066	1.966	IIEDI2	0.060	1.960
IBEA8	0.131	2.031	IIEDI1	0.085	1.985
IBEA7	0.061	1.961	IIEDI0	0.088	1.988
IBEA6	0.041	1.941	IBBTFT	0.189	2.089
IBEA5	0.040	1.940	IDDRRQ	0.444	2.344
IBEA4	0.045	1.945	IDDWRQ	0.287	2.187
IBEA3	0.170	2.070	IDSEQ4	0.177	2.077
IBEA2	0.180	2.080	IDSEQ2	0.570	2.470
IIAACK	0.186	2.086	IDRRDY	0.495	2.395
IIDLEF	0.073	1.973	IDHUM	0.329	2.229
IIEDI31	0.062	1.962	IDEA27	0.425	2.325
IIEDI30	0.056	1.956	IDEA26	0.474	2.374
IIEDI29	0.103	2.003	IDEA25	0.401	2.301
IIEDI28	0.067	1.967	IDEA24	0.382	2.282
IIEDI27	0.053	1.953	IDEA23	0.345	2.245
IIEDI26	0.055	1.955	IDEA22	0.346	2.246
IIEDI25	0.077	1.977	IDEA21	0.399	2.299
IIEDI24	0.016	1.916	IDEA20	0.414	2.314
IIEDI23	0.064	1.964	IDEA19	0.283	2.183
IIEDI22	0.063	1.963	IDEA18	0.298	2.198
IIEDI21	0.065	1.965	IDEA17	0.303	2.203
IIEDI20	0.064	1.964	IDEA16	0.292	2.192

(1) Input pins (4/5)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
IDEA15	0.292	2.192	PHEVA	1.468	3.368
IDEA14	0.292	2.192	IFIROBE	0.470	2.370
IDEA13	0.270	2.170	IFIROPR	0.424	2.324
IDEA12	0.289	2.189	IFIRASE	0.715	2.615
IDEA11	0.277	2.177	IFIRABE	0.923	2.823
IDEA10	0.313	2.213	IFIMODE3	0.478	2.378
IDEA9	0.244	2.144	IFIMODE2	0.557	2.457
IDEA8	0.269	2.169	IFIUSWE	0.277	2.177
IDEA7	0.270	2.170	FCOMB	0.284	2.184
IDEA6	0.249	2.149	TBI39	0.022	1.922
IDEA5	0.273	2.173	TBI38	0.008	1.908
IDEA4	0.268	2.168	TBI37	0.009	1.909
IDEA3	0.290	2.190	TBI36	0.137	2.037
IDEA2	0.276	2.176	TBI35	0.497	2.397
IDEA1	0.331	2.231	TBI34	0.007	1.907
IDEA0	0.386	2.286	TBI33	0.146	2.046
DBI5	0.199	2.099	TBI32	0.134	2.034
DBI4	0.296	2.196	TBI31	0.011	1.911
DBI3	0.530	2.430	TBI30	0.012	1.912
DBI2	0.413	2.313	TBI29	0.009	1.909
DBI1	0.543	2.443	TBI28	0.009	1.909
DBI0	0.691	2.591	TBI27	0.011	1.911
EVASTB	0.459	2.359	TBI26	0.011	1.911
EVDSTB	0.091	1.991	TBI25	0.010	1.910
EVIREL	0.274	2.174	TBI24	0.009	1.909
EVCLRIP	0.035	1.935	TBI23	0.013	1.913
EVINTAK	0.150	2.050	TBI22	0.016	1.916
IFIROME	0.281	2.181	TBI21	0.011	1.911
IFIROB2	0.292	2.192	TBI20	0.051	1.951
IFIRA64	0.596	2.496	TBI19	0.043	1.943
IFIRA32	0.524	2.424	TBI18	0.169	2.069
IFIRA16	0.441	2.341	TBI17	0.035	1.935
IFIMAEN	0.363	2.263	TBI16	0.022	1.922
IFID256	0.424	2.324	TBI15	0.020	1.920
IFINSZ1	0.405	2.305	TBI14	0.017	1.917
IFINSZ0	0.573	2.473	TBI13	0.011	1.911
IFIWRTH	0.377	2.277	TBI12	0.039	1.939
IFIUNCH1	0.694	2.594	TBI11	0.035	1.935
IFIUNCH0	0.709	2.609	TBI10	0.027	1.927

(1) Input pins (5/5)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
TBI9	0.019	1.919	TBI2	0.007	1.907
TBI8	0.025	1.925	TBI1	0.008	1.908
TBI7	0.012	1.912	TBI0	0.013	1.913
TBI6	0.024	1.924	TEST	0.018	1.918
TBI5	0.045	1.945	BUNRI	0.371	2.271
TBI4	0.030	1.930	PHTDO1	0.535	2.435
TBI3	0.007	1.907	PHTDO0	0.535	2.435

(2) Output pins (1/4)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
VPA13	3.250	–	–	DMACTV2	3.168	–	–
VPA12	3.243	–	–	DMACTV1	3.006	–	–
VPA11	3.243	–	–	DMACTV0	2.949	–	–
VPA10	3.239	–	–	IROMA19	13.008	–	–
VPA9	3.234	–	–	IROMA18	3.191	–	–
VPA8	3.245	–	–	IROMA17	3.177	–	–
VPA7	3.238	–	–	IROMA16	3.195	–	–
VPA6	3.241	–	–	IROMA15	3.079	–	–
VPA5	3.239	–	–	IROMA14	3.177	–	–
VPA4	3.228	–	–	IROMA13	3.168	–	–
VPA3	3.294	–	–	IROMA12	3.189	–	–
VPA2	3.293	–	–	IROMA11	3.186	–	–
VPA1	3.292	–	–	IROMA10	3.092	–	–
VPA0	3.211	–	–	IROMA9	3.095	–	–
VPWRITE	3.176	–	–	IROMA8	13.001	–	–
VPSTB	3.174	–	–	IROMA7	3.102	–	–
VPLOCK	3.254	–	–	IROMA6	6.532	–	–
VPUBENZ	3.294	–	–	IROMA5	6.536	–	–
VAACK	13.316	–	–	IROMA4	6.564	–	–
VBDC	13.021	–	–	IROMA3	6.525	–	–
SWSTOPRQ	4.630	–	–	IROMA2	6.531	–	–
HWSTOPRQ	12.809	–	–	IROMEN	12.912	–	–
STPRQ	4.578	–	–	IROMCS	4.754	–	–
DMTCO3	3.159	–	–	IROMIA	6.503	–	–
DMTCO2	3.180	–	–	IROMAE	12.933	–	–
DMTCO1	3.141	–	–	IRAMA27	3.040	–	–
DMTCO0	3.135	–	–	IRAMA26	3.246	–	–
DMACTV3	3.044	–	–	IRAMA25	3.273	–	–

(2) Output pins (2/4)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
IRAMA24	3.020	–	–	IRAOZ15	3.159	–	–
IRAMA23	3.030	–	–	IRAOZ14	3.362	–	–
IRAMA22	3.241	–	–	IRAOZ13	3.360	–	–
IRAMA21	3.032	–	–	IRAOZ12	3.351	–	–
IRAMA20	3.049	–	–	IRAOZ11	3.354	–	–
IRAMA19	3.298	–	–	IRAOZ10	3.349	–	–
IRAMA18	2.969	–	–	IRAOZ9	3.055	–	–
IRAMA17	3.293	–	–	IRAOZ8	3.155	–	–
IRAMA16	3.256	–	–	IRAOZ7	3.295	–	–
IRAMA15	3.292	–	–	IRAOZ6	3.293	–	–
IRAMA14	3.279	–	–	IRAOZ5	3.290	–	–
IRAMA13	3.290	–	–	IRAOZ4	3.289	–	–
IRAMA12	3.292	–	–	IRAOZ3	3.296	–	–
IRAMA11	4.957	–	–	IRAOZ2	3.339	–	–
IRAMA10	3.291	–	–	IRAOZ1	3.134	–	–
IRAMA9	3.179	–	–	IRAOZ0	3.333	–	–
IRAMA8	3.290	–	–	IRAMEN	3.292	–	–
IRAMA7	3.176	–	–	IRAMWR3	3.284	–	–
IRAMA6	3.292	–	–	IRAMWR2	3.288	–	–
IRAMA5	3.256	–	–	IRAMWR1	13.068	–	–
IRAMA4	3.273	–	–	IRAMWR0	3.287	–	–
IRAMA3	13.067	–	–	IRAMRWB	3.288	–	–
IRAMA2	3.287	–	–	IBAACK	3.296	–	–
IRAOZ31	3.061	–	–	IBDRDY	3.293	–	–
IRAOZ30	3.360	–	–	IBDLE3	12.933	–	–
IRAOZ29	3.359	–	–	IBDLE2	4.799	–	–
IRAOZ28	3.360	–	–	IBDLE1	4.803	–	–
IRAOZ27	3.350	–	–	IBDLE0	4.679	–	–
IRAOZ26	3.352	–	–	IBEDI31	3.292	–	–
IRAOZ25	3.211	–	–	IBEDI30	3.293	–	–
IRAOZ24	3.353	–	–	IBEDI29	3.270	–	–
IRAOZ23	3.357	–	–	IBEDI28	3.285	–	–
IRAOZ22	2.998	–	–	IBEDI27	3.294	–	–
IRAOZ21	3.345	–	–	IBEDI26	3.290	–	–
IRAOZ20	3.151	–	–	IBEDI25	3.287	–	–
IRAOZ19	3.347	–	–	IBEDI24	3.292	–	–
IRAOZ18	3.170	–	–	IBEDI23	3.294	–	–
IRAOZ17	3.362	–	–	IBEDI22	3.289	–	–
IRAOZ16	3.362	–	–	IBEDI21	3.288	–	–

(2) Output pins (3/4)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
IBEDI20	3.295	–	–	IIEA8	4.874	–	–
IBEDI19	3.295	–	–	IIEA7	13.046	–	–
IBEDI18	3.291	–	–	IIEA6	13.066	–	–
IBEDI17	3.293	–	–	IIEA5	13.068	–	–
IBEDI16	3.294	–	–	IIEA4	13.055	–	–
IBEDI15	3.292	–	–	IIEA3	12.956	–	–
IBEDI14	3.292	–	–	IIEA2	12.956	–	–
IBEDI13	3.290	–	–	IIBTFT	3.242	–	–
IBEDI12	3.289	–	–	IIRCAN	3.292	–	–
IBEDI11	3.293	–	–	BCUNCH	12.990	–	–
IBEDI10	3.286	–	–	IDDARQ	3.214	–	–
IBEDI9	3.286	–	–	IDAACK	2.990	–	–
IBEDI8	3.280	–	–	IRRSA	13.001	–	–
IBEDI7	3.283	–	–	IDRETR	9.004	–	–
IBEDI6	3.288	–	–	IDUNCH	3.286	–	–
IBEDI5	3.290	–	–	IDDRDY	12.877	–	–
IBEDI4	3.289	–	–	IDES	12.836	–	–
IBEDI3	3.282	–	–	DBO14	7.685	–	–
IBEDI2	3.289	–	–	DBO13	2.793	–	–
IBEDI1	3.285	–	–	DBO12	2.868	–	–
IBEDI0	3.287	–	–	DBO11	3.105	–	–
IIDRRQ	12.951	–	–	DBO10	2.700	–	–
IIEA25	12.929	–	–	DBO9	2.745	–	–
IIEA24	4.989	–	–	DBO8	2.813	–	–
IIEA23	4.982	–	–	DBO7	2.882	–	–
IIEA22	4.857	–	–	DBO6	2.877	–	–
IIEA21	4.951	–	–	DBO5	2.883	–	–
IIEA20	4.953	–	–	DBO4	2.761	–	–
IIEA19	6.533	–	–	DBO3	12.566	–	–
IIEA18	4.911	–	–	DBO2	12.614	–	–
IIEA17	6.529	–	–	DBO1	2.777	–	–
IIEA16	12.996	–	–	DBO0	2.894	–	–
IIEA15	13.040	–	–	EVIEN	3.261	–	–
IIEA14	13.060	–	–	EVOEN	4.988	–	–
IIEA13	13.038	–	–	EVINTRQ	4.675	–	–
IIEA12	4.945	–	–	EVINTLV6	12.810	–	–
IIEA11	13.067	–	–	EVINTLV5	12.708	–	–
IIEA10	12.966	–	–	EVINTLV4	12.760	–	–
IIEA9	13.066	–	–	EVINTLV3	12.708	–	–

(2) Output pins (4/4)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
EVINTLV2	6.212	–	–	TBO13	6.511	0.071	1.971
EVINTLV1	12.687	–	–	TBO12	6.513	0.069	1.969
EVINTLV0	12.683	–	–	TBO11	6.524	0.059	1.959
TBO34	4.959	0.036	1.936	TBO10	6.516	0.067	1.967
TBO33	4.950	0.045	1.945	TBO9	6.501	0.081	1.981
TBO32	4.932	0.063	1.963	TBO8	6.511	0.072	1.972
TBO31	4.864	0.131	2.031	TBO7	6.507	0.075	1.975
TBO30	4.672	0.323	2.223	TBO6	6.527	0.055	1.955
TBO29	4.780	0.215	2.115	TBO5	6.532	0.050	1.950
TBO28	4.889	0.106	2.006	TBO4	6.502	0.080	1.980
TBO27	6.343	0.239	2.139	TBO3	6.528	0.054	1.954
TBO26	6.503	0.080	1.980	TBO2	6.509	0.073	1.973
TBO25	6.257	0.325	2.225	TBO1	6.519	0.063	1.963
TBO24	6.469	0.113	2.013	TBO0	6.518	0.065	1.965
TBO23	6.488	0.094	1.994	TESEN	3.174	–	–
TBO22	6.462	0.121	2.021	VPTCLK	3.250	–	–
TBO21	6.445	0.137	2.037	PHTDIN1	3.288	–	–
TBO20	6.500	0.083	1.983	PHTDIN0	3.290	–	–
TBO19	6.515	0.067	1.967	VPRESZ	4.731	–	–
TBO18	6.441	0.141	2.041	PHTEST	12.785	–	–
TBO17	6.485	0.097	1.997	TMODE1	2.483	–	–
TBO16	6.506	0.076	1.976	TMODE0	2.758	–	–
TBO15	4.937	0.058	1.958	TBREDZ	3.113	–	–
TBO14	6.480	0.103	2.003				

(3) I/O pins (1/3)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
VPD15	5.962	0.620	2.520	VPD4	5.962	0.620	2.520
VPD14	5.897	0.686	2.586	VPD3	5.936	0.646	2.546
VPD13	5.843	0.740	2.640	VPD2	5.908	0.675	2.575
VPD12	5.846	0.736	2.636	VPD1	5.906	0.676	2.576
VPD11	5.907	0.675	2.575	VPD0	5.912	0.670	2.570
VPD10	5.921	0.661	2.561	VBA27	4.343	0.652	2.552
VPD9	5.902	0.680	2.580	VBA26	4.252	0.743	2.643
VPD8	5.910	0.672	2.572	VBA25	2.661	0.678	2.578
VPD7	5.946	0.636	2.536	VBA24	4.336	0.659	2.559
VPD6	5.954	0.629	2.529	VBA23	4.352	0.643	2.543
VPD5	5.922	0.661	2.561	VBA22	4.302	0.693	2.593

(3) I/O pins (2/3)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
VBA21	4.316	0.679	2.579	VBD14	3.469	1.525	3.425
VBA20	4.307	0.687	2.587	VBD13	3.563	1.432	3.332
VBA19	4.304	0.691	2.591	VBD12	3.537	1.458	3.358
VBA18	4.236	0.758	2.658	VBD11	3.500	1.494	3.394
VBA17	4.195	0.800	2.700	VBD10	3.444	1.551	3.451
VBA16	2.614	0.724	2.624	VBD9	3.596	1.399	3.299
VBA15	4.235	0.760	2.660	VBD8	3.389	1.606	3.506
VBA14	4.291	0.704	2.604	VBD7	3.267	1.728	3.628
VBA13	4.201	0.794	2.694	VBD6	3.133	1.862	3.762
VBA12	4.181	0.814	2.714	VBD5	3.250	1.745	3.645
VBA11	4.201	0.794	2.694	VBD4	3.205	1.790	3.690
VBA10	4.196	0.799	2.699	VBD3	3.186	1.808	3.708
VBA9	4.220	0.775	2.675	VBD2	3.173	1.822	3.722
VBA8	4.229	0.766	2.666	VBD1	3.211	1.784	3.684
VBA7	4.174	0.821	2.721	VBD0	3.215	1.780	3.680
VBA6	4.186	0.809	2.709	VBTTYP1	5.827	0.756	2.656
VBA5	4.255	0.740	2.640	VBTTYP0	5.809	0.773	2.673
VBA4	4.219	0.776	2.676	VBSTZ	2.596	0.742	2.642
VBA3	4.191	0.804	2.704	VBBENZ3	5.737	0.845	2.745
VBA2	4.212	0.783	2.683	VBBENZ2	5.783	0.799	2.699
VBA1	4.179	0.816	2.716	VBBENZ1	5.689	0.894	2.794
VBA0	4.161	0.834	2.734	VBBENZ0	5.599	0.983	2.883
VBD31	3.720	1.275	3.175	VBSIZE1	4.081	0.914	2.814
VBD30	3.419	1.576	3.476	VBSIZE0	4.208	0.787	2.687
VBD29	3.733	1.262	3.162	VBWRITE	2.543	0.796	2.696
VBD28	3.690	1.304	3.204	VBLOCK	4.130	0.865	2.765
VBD27	3.823	1.172	3.072	VBCTYP2	4.176	0.819	2.719
VBD26	3.651	1.344	3.244	VBCTYP1	2.612	0.727	2.627
VBD25	3.760	1.235	3.135	VBCTYP0	2.564	0.775	2.675
VBD24	3.737	1.258	3.158	VBSEQ2	4.204	0.791	2.691
VBD23	3.724	1.271	3.171	VBSEQ1	4.174	0.821	2.721
VBD22	3.706	1.289	3.189	VBSEQ0	4.199	0.796	2.696
VBD21	3.699	1.296	3.196	VBBSTR	2.595	0.744	2.644
VBD20	3.705	1.290	3.190	VBWAIT	5.742	0.840	2.740
VBD19	3.751	1.244	3.144	VBLAST	5.785	0.797	2.697
VBD18	3.668	1.327	3.227	VBAHLD	5.811	0.771	2.671
VBD17	3.741	1.254	3.154	VDCSZ7	4.336	0.659	2.559
VBD16	3.617	1.377	3.277	VDCSZ6	4.347	0.648	2.548
VBD15	3.458	1.537	3.437	VDCSZ5	4.344	0.651	2.551

(3) I/O pins (3/3)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
VDCSZ4	4.291	0.704	2.604	IDED1	5.912	0.670	2.570
VDCSZ3	4.369	0.626	2.526	IDED0	5.895	0.688	2.588
VDCSZ2	4.336	0.659	2.559	DBB15	4.055	0.940	2.840
VDCSZ1	4.357	0.637	2.537	DBB14	4.023	0.972	2.872
VDCSZ0	4.347	0.648	2.548	DBB13	4.031	0.964	2.864
VDSELPZ	4.180	0.815	2.715	DBB12	4.012	0.983	2.883
IDED31	5.749	0.833	2.733	DBB11	3.993	1.002	2.902
IDED30	4.419	0.576	2.476	DBB10	3.999	0.996	2.896
IDED29	5.798	0.785	2.685	DBB9	3.971	1.024	2.924
IDED28	5.798	0.784	2.684	DBB8	4.019	0.976	2.876
IDED27	4.424	0.571	2.471	DBB7	4.012	0.982	2.882
IDED26	5.819	0.763	2.663	DBB6	4.028	0.967	2.867
IDED25	5.809	0.774	2.674	DBB5	3.949	1.046	2.946
IDED24	5.767	0.815	2.715	DBB4	4.002	0.993	2.893
IDED23	5.726	0.856	2.756	DBB3	3.863	1.131	3.031
IDED22	5.764	0.818	2.718	DBB2	3.952	1.043	2.943
IDED21	5.833	0.750	2.650	DBB1	4.051	0.944	2.844
IDED20	5.786	0.797	2.697	DBB0	4.048	0.947	2.847
IDED19	5.751	0.831	2.731	EVAD15	5.971	0.611	2.511
IDED18	4.236	0.759	2.659	EVAD14	5.886	0.696	2.596
IDED17	4.229	0.766	2.666	EVAD13	5.659	0.923	2.823
IDED16	4.275	0.720	2.620	EVAD12	5.842	0.740	2.640
IDED15	5.815	0.767	2.667	EVAD11	5.852	0.731	2.631
IDED14	5.832	0.750	2.650	EVAD10	5.927	0.655	2.555
IDED13	5.866	0.717	2.617	EVAD9	5.914	0.668	2.568
IDED12	5.829	0.754	2.654	EVAD8	5.923	0.660	2.560
IDED11	5.834	0.748	2.648	EVAD7	5.981	0.606	2.506
IDED10	5.861	0.721	2.621	EVAD6	5.992	0.595	2.495
IDED9	5.817	0.765	2.665	EVAD5	5.917	0.666	2.566
IDED8	5.853	0.729	2.629	EVAD4	5.965	0.618	2.518
IDED7	5.843	0.739	2.639	EVAD3	5.949	0.639	2.539
IDED6	5.841	0.741	2.641	EVAD2	5.730	0.852	2.752
IDED5	5.898	0.684	2.584	EVAD1	5.942	0.641	2.541
IDED4	5.892	0.690	2.590	EVAD0	5.799	0.783	2.683
IDED3	5.856	0.726	2.626	EVLKRT	6.013	0.569	2.469
IDED2	5.856	0.727	2.627				

7. 2 Initialization of Internal Registers

Before executing the test program, be sure to execute an instruction to assign initial values to the internal registers used in test program execution. Failure to do this will result in the propagation of undefined values.

7. 3 Pin Functions

(1/4)

Pin Name		I/O	Function
NPB pins	VPA13 to VPA0	Output	Address output for peripheral macro connected to NPB
	VPD15 to VPD0[Note]	I/O	Data I/O for peripheral macro connected to NPB
	VPWRITE	Output	Write access strobe output of signals VPD15 to VPD0
	VPSTB	Output	Data strobe output of signals VPD15 to VPD0
	VPLOCK	Output	Bus lock output
	VPUBENZ	Output	Upper byte enable output
	VPRETR[Note]	Input	Retry request input from peripheral macro connected to NPB
	VPDACT	Input	Retry function control input
VSB pins	VAREQ	Input	Bus access right request input
	VAACK	Output	Bus access right acknowledge output
	VBA27 to VBA0[Note]	I/O	Address I/O for peripheral macro connected to VSB
	VBD31 to VBD0[Note]	I/O	Data I/O for peripheral macro connected to VSB
	VBTTYP1, VBTTYP0[Note]	I/O	Bus transfer type I/O
	VBSTZ[Note]	I/O	Transfer start I/O
	VBBENZ3 to VBBENZ0[Note]	I/O	Byte enable I/O
	VBSIZE1, VBSIZE0[Note]	I/O	Transfer size I/O
	VBWRITE[Note]	I/O	Read/write status I/O
	VBLOCK[Note]	I/O	Bus lock I/O
	VBCTYP2 to VBCTYP0[Note]	I/O	Bus cycle status I/O
	VBSEQ2 to VBSEQ0[Note]	I/O	Sequential status I/O
	VBBSTR[Note]	I/O	Burst read status I/O
	VBWAIT[Note]	I/O	Wait response I/O
	VBLAST[Note]	I/O	Last response I/O
	VBAHLD[Note]	I/O	Address hold response I/O
	VBDC	Output	Data bus direction control output
	VDCSZ7 to VDCSZ0[Note]	I/O	Chip select I/O
	VDSELPZ[Note]	I/O	Peripheral I/O area access status I/O
System control pins	DCRESZ	Input	System reset input
	VBCLK	Input	Internal system clock input
	CGREL	Input	Clock generator release input
	SWSTOPRQ	Output	Software STOP mode request output to clock generator
	HWSTOPRQ	Output	Hardware STOP mode request output to clock generator
	DCSTOPZ	Input	Hardware STOP mode request input
	STPRQ	Output	Hardware/software STOP mode request output to MEMC
	STPAK	Input	Acknowledge input for input of STPRQ of MEMC

Note Connected internally to the bus holder.

(2/4)

Pin Name		I/O	Function
DMAC pins	IDMASTP	Input	DMA transfer terminate input
	DMARQ3 to DMARQ0	Input	DMA transfer request input
	DMTCO3 to DMTCO0	Output	Terminal count (DMA transfer completed) output
	DMACTV3 to DMACTV0	Output	DMA acknowledge output
INTC pins	DCNMI2 to DCNMI0	Input	Non-maskable interrupt request (NMI) input
	INT63 to INT0	Input	Maskable interrupt request input
VFB pins	IROMA19 to IROMA2	Output	Address output for ROM
	IROMZ31 to IROMZ0	Input	Data input for ROM
	IROMEN	Output	Access enable output for ROM
	IROMWT	Input	Wait input for ROM
	IROMCS	Output	NEC reserved pin (leave open)
	IROMIA	Output	
	IROMAE	Output	
VDB pins	IRAMA27 to IRAMA2	Output	Address output for RAM
	IRAMZ31 to IRAMZ0	Input	Data input for RAM
	IRAOZ31 to IRAOZ0	Output	Data output for RAM
	IRAMEN	Output	Access enable output for RAM
	IRAMWR3 to IRAMWR0	Output	Write enable output for RAM
	IRAMRWB	Output	Read/write status output for RAM
	IRAMWT	Input	Wait input for RAM
Instruction cache pins	IBDRRQ	Input	Fetch request input from instruction cache
	IBEA25 to IBEA2	Input	Fetch address input from instruction cache
	IBAACK	Output	Address acknowledge output to instruction cache
	IBDRDY	Output	Data ready output to instruction cache
	IBDLE3 to IBDLE0	Output	Data latch enable output to instruction cache
	IBEDI31 to IBEDI0	Output	Data output to instruction cache
	IIDRRQ	Output	Fetch request output to instruction cache
	IIEA25 to IIEA2	Output	Fetch address output to instruction cache
	IIAACK	Input	Address acknowledge input from instruction cache
	IIDLEF	Input	Data latch enable input from instruction cache
	IIEDI31 to IIEDI0	Input	Data input from instruction cache
	IIBTFT	Output	Branch target fetch status output to instruction cache
	IIRCAN	Output	Code cancel status output to instruction cache
	BCUNCH	Output	Uncache status output to instruction cache
	IBBTFT	Input	NEC reserved pin (input a low level)

Remark VFB: V850E Fetch Bus
VDB: V850E Data Bus

(3/4)

Pin Name		I/O	Function
Data cache pins	IDDARQ	Output	Read/write access request output to data cache
	IDAACK	Output	Acknowledge output
	IDDRRQ	Input	VSB read operation request input to BCU
	IDDWRQ	Input	VSB write operation request input to BCU
	IDSEQ4	Input	Read/write operation type setting input
	IDSEQ2	Input	Read/write operation type setting input
	IRRSA	Output	VDB hold status output
	IDRETR	Output	Read retry request output
	IDUNCH	Output	Uncache status output
	IDDRDY	Output	Read data ready output
	IDRRDY	Input	Read data ready input from data cache
	IDHUM	Input	Hit under miss-hit read input
	IDEA27 to IDEA0	Input	Address input
	IDED31 to IDED0[Note 1]	I/O	Data I/O
	IDES	Output	NEC reserved pin[Note 2]
RCU pins	DBI5 to DBI0	Input	Debug control input
	DBO14 to DBO0	Output	Debug control output
	DBB15 to DBB0[Note 1]	I/O	Debug control I/O
Peripheral EVA chip mode pins	EVASTB	Input	Address strobe input
	EVDSTB	Input	Data strobe input
	EVAD15 to EVAD0[Note 1]	I/O	Address/data I/O
	EVIEN	Output	EVADn input enable output (n = 15 to 0)
	EVOEN	Output	EVADn output enable output (n = 15 to 0)
	EVLKRT[Note 1]	I/O	Lock/retry I/O
	EVIREL	Input	Standby release input
	EVCLRIP	Input	ISPR clear input
	EVINTAK	Input	Interrupt acknowledge input
	EVINTRQ	Output	Interrupt request output
	EVINTLV6 to EVINTLV0	Output	Interrupt vector output
Operation mode setting pins	IFIROME	Input	ROM mapping enable input
	IFIROB2	Input	Location setting input of ROM area
	IFIRA64	Input	RAM area size selection input
	IFIRA32	Input	RAM area size selection input
	IFIRA16	Input	RAM area size selection input
	IFIMAEN	Input	Misalign access setting input

Notes 1. Connected internally to the bus holder.

2. When using the data cache, always connect this pin to the IDES pin of the data cache. Leave open when unused.

(4/4)

Pin Name		I/O	Function
Operation mode setting pins	IFID256	Input	Data area setting input
	IFINSZ1, IFINSZ0	Input	VSB data bus size selection input
	IFIWRTH	Input	Data cache write-back/write-through mode selection input
	IFIUNCH1	Input	Data cache setting input
	IFIUNCH0	Input	Instruction cache setting input
	PHEVA	Input	Peripheral EVA chip mode setting input
	IFIROBE	Input	NEC reserved pin (input a low level)
	IFIROPR	Input	
	IFIRASE	Input	
	IFIRABE	Input	
	IFIMODE3	Input	
	IFIMODE2	Input	
	IFIUSWE	Input	
	FCOMB	Input	
Test mode pins	TBI39 to TBI0	Input	Input test bus
	TBO34 to TBO0	Output	Output test bus
	TEST	Input	Test bus control input
	BUNRI	Input	Normal/test mode selection input
	PHTDO1, PHTDO0[Note]	Input	Peripheral macro test input
	TESEN	Output	Peripheral macro test enable output
	VPTCLK	Output	Clock output for peripheral macro test
	PHTDIN1, PHTDIN0	Output	Peripheral macro test output
	VPRESZ	Output	Peripheral macro reset output
	PHTEST	Output	Peripheral test mode status output
	TMODE1	Output	Test mode selection output
	TMODE0	Output	NEC reserved pin (leave open)
	TBREDZ	Output	

Note Connected internally to the bus holder.

7. 4 Electrical Specifications (Preliminary)

The following specifications are for a single macro. An actual chip consists of two or more macros. Design the system so that all the specifications of the individual macros are satisfied when the chip is used.

7. 4. 1 Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to +4.6	V
Operating ambient temperature	T_A	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

7. 4. 2 Recommended operation range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	−40		+85	°C
Clock cycle	t_{CYK}	15.0			ns

7. 4. 3 DC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

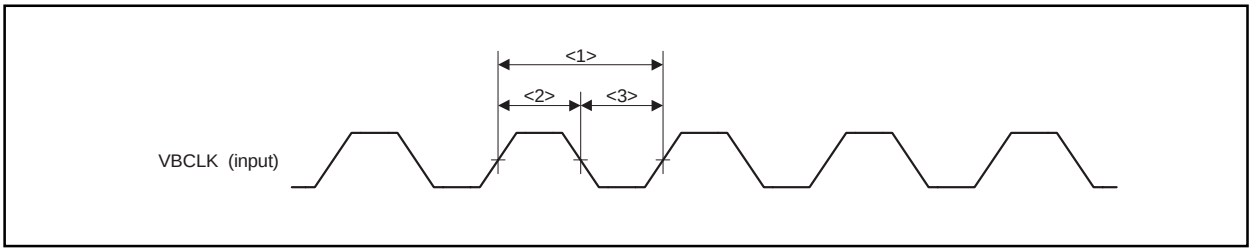
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1}	In normal operation mode		0.5	0.6	mA/MHz
	I_{DD2}	In HALT mode (when DMAC is not operating)		0.17	0.2	mA/MHz
	I_{DD3}	In STOP mode		0	1.0	μA

Remark The TYP. value is a reference value for when T_A = 25°C, V_{DD} = 3.3 V.

7. 4. 4 AC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

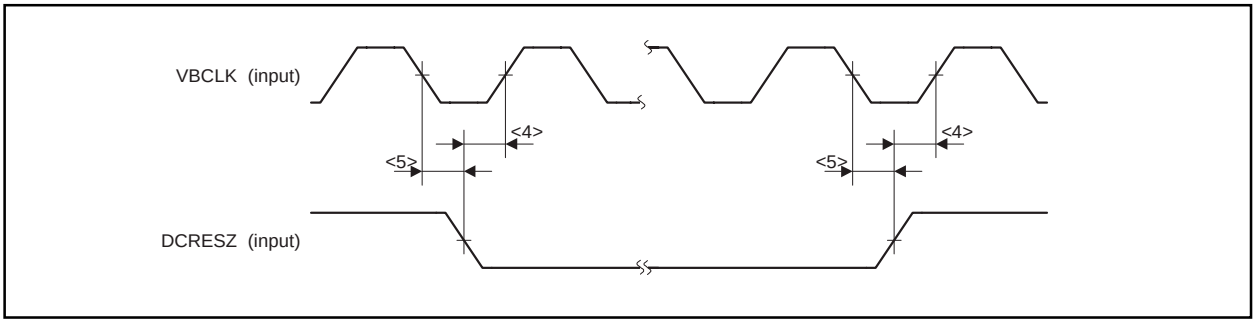
(1) Clock timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VBCLK input cycle	<1>	t_{CYK}		15.0		ns
VBCLK input high-level width	<2>	t_{KKH}		7.5		ns
VBCLK input low-level width	<3>	t_{KKL}		7.5		ns
CPU operating frequency	–	ϕ		0	66	MHz



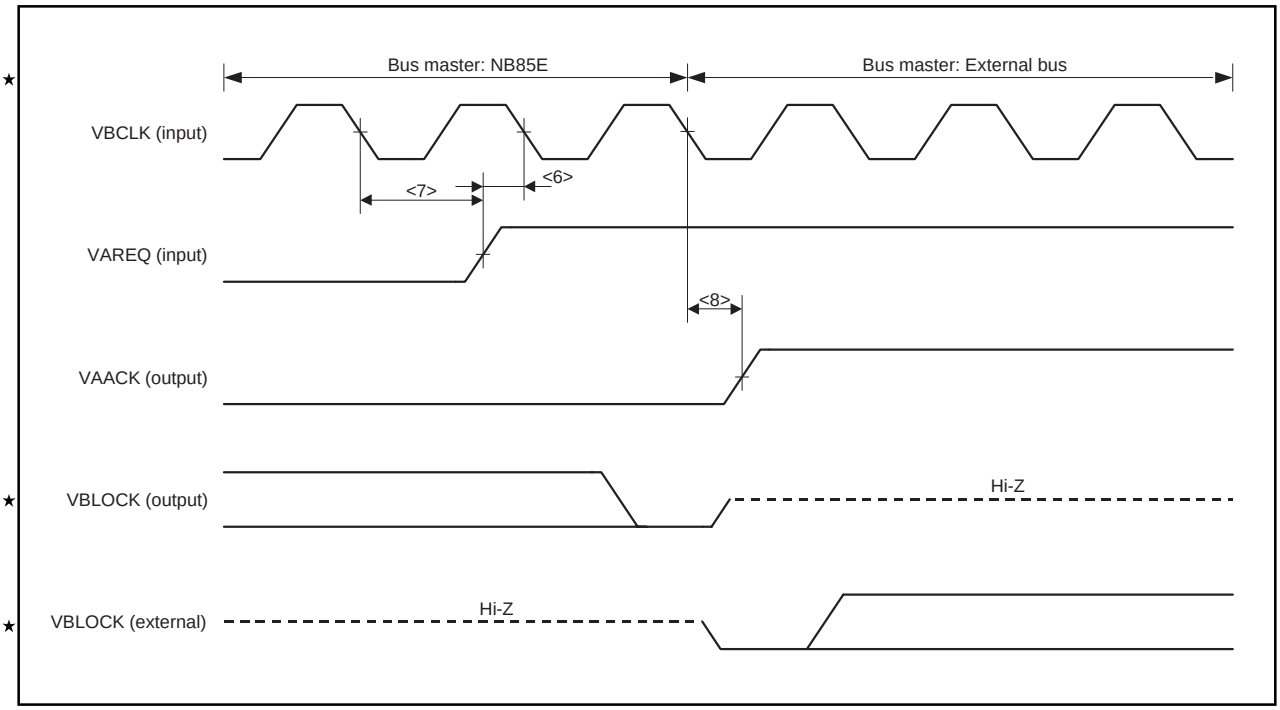
(2) Reset timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
DCRESZ setup time (to VBCLK↑)	<4>	t_{SKR}		2.0		ns
DCRESZ hold time (from VBCLK↓)	<5>	t_{HKR}		1.9		ns
Delay time from DCRESZ to VPRESZ	–	t_{DRPR}		1	2.5	ns



(3) VSB arbitration timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VAREQ setup time (to VBCLK↓)	<6>	t_{SKQ}		0		ns
VAREQ hold time (from VBCLK↓)	<7>	t_{HKQ}		3.4		ns
Delay time from VBCLK↓ to VAACK	<8>	t_{DKK}		1.3	4.7	ns

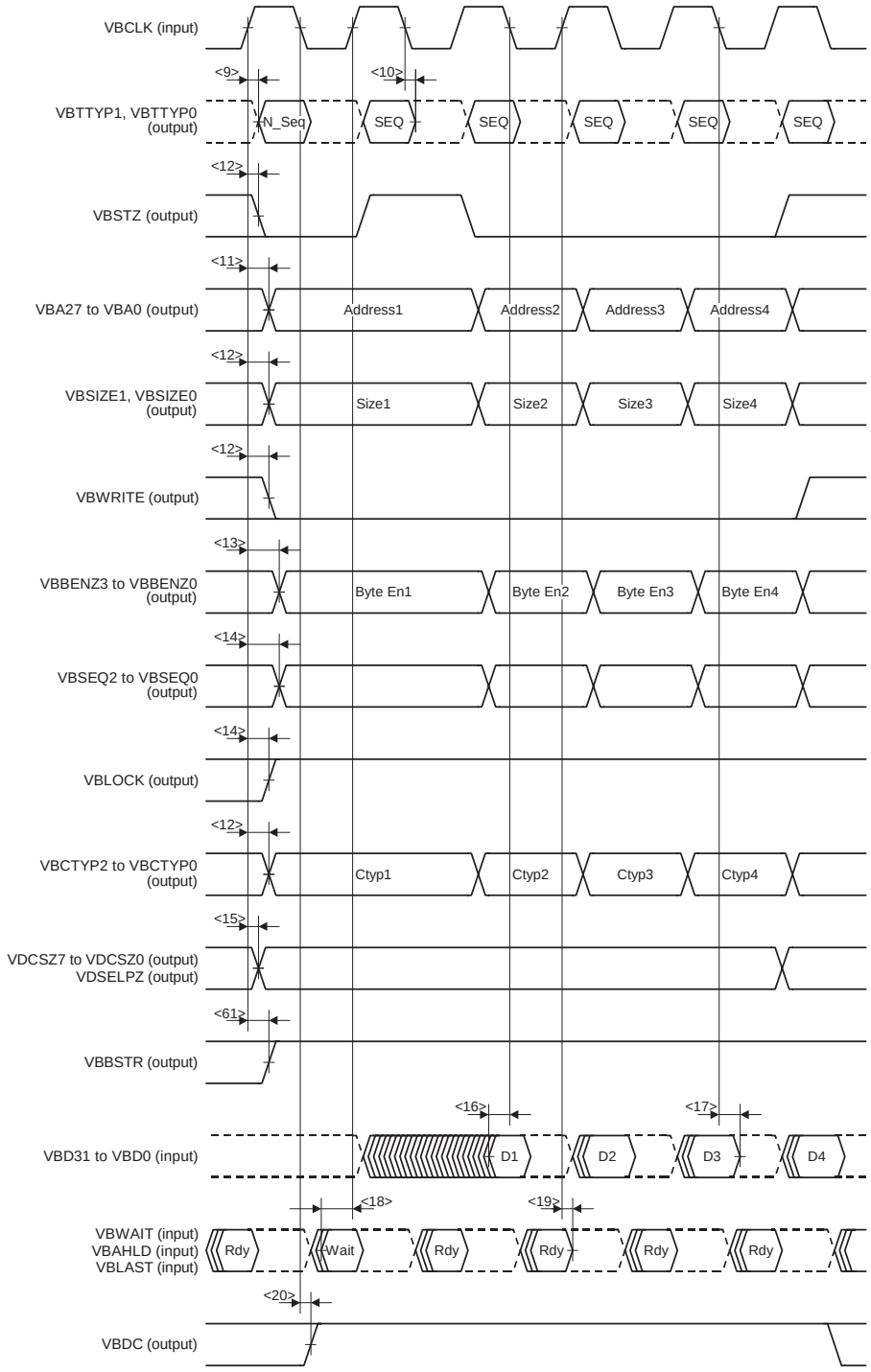


[MEMO]

(4) VSB master read timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to VBTTYP	<9>	t_{DKT}		1.3	4.1	ns
VBTTYP hold time (from VBCLK↓)	<10>	t_{HKT}		2.8		ns
Delay time from VBCLK↑ to VBA	<11>	t_{DKA}		1.3	6.3	ns
Delay time from VBCLK↑ to VBSTZ, VBSIZE, VBWRITE, VBCTYP	<12>	t_{DKS1}		1.3	6.1	ns
Delay time from VBCLK↑ to VBBENZ	<13>	t_{DKS2}		1.3	6.7	ns
Delay time from VBCLK↑ to VBSEQ, VBLOCK	<14>	t_{DKS3}		1.3	6.6	ns
Delay time from VBCLK↑ to VDCSZ, VDSELPZ	<15>	t_{DKC}		1.3	5.6	ns
Delay time from VBCLK↑ to VBBSTR	<61>	t_{DKBSR}		1.3	5.5	ns
VBD data setup time (to VBCLK↓)	<16>	t_{SKD}		0		ns
VBD data hold time (from VBCLK↓)	<17>	t_{HKD}		2.8		ns
VBWAIT, VBAHLD, VBLAST setup time (to VBCLK↑)	<18>	t_{SKW}		0		ns
VBWAIT, VBAHLD, VBLAST hold time (from VBCLK↑)	<19>	t_{HKW}		2.9		ns
Delay time from VBCLK↓ to VBDC	<20>	t_{DKS4}		1.3	4.7	ns

(4) VSB master read timing (2/2)



Remarks 1. The level of the broken line portion indicates the undefined state (weak unknown) in which the bus holder in the NB85E is driving.

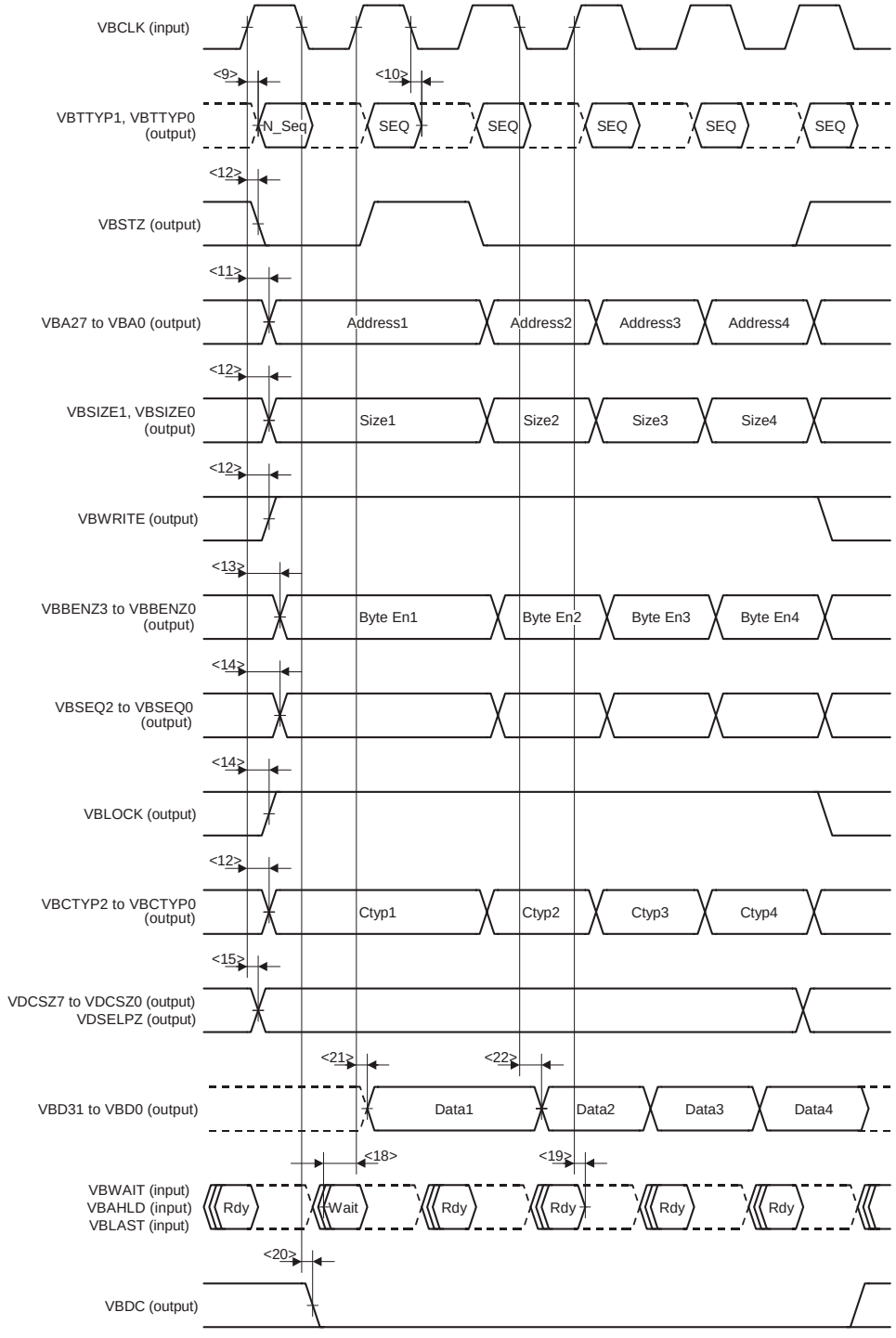
2. Rdy: When the VBWAIT, VBAHLD, and VBLAST signals are all low level

Wait: When the VBWAIT signal is high level, and the VBAHLD and VBLAST signals are low level

(5) VSB master write timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to VBTTYP	<9>	t_{DKT}		1.3	4.1	ns
VBTTYP hold time (from VBCLK↓)	<10>	t_{HKT}		2.8		ns
Delay time from VBCLK↑ to VBA	<11>	t_{DKA}		1.3	6.3	ns
Delay time from VBCLK↑ to VBSTZ, VBSIZE, VBWRITE, VBCTYP	<12>	t_{DKS1}		1.3	6.1	ns
Delay time from VBCLK↑ to VBBENZ	<13>	t_{DKS2}		1.3	6.7	ns
Delay time from VBCLK↑ to VBSEQ, VBLOCK	<14>	t_{DKS3}		1.3	6.6	ns
Delay time from VBCLK↑ to VDCSZ, VDSELPZ	<15>	t_{DKC}		1.3	5.6	ns
VBWAIT, VBAHLD, VBLAST setup time (to VBCLK↑)	<18>	t_{SKW}		0		ns
VBWAIT, VBAHLD, VBLAST hold time (from VBCLK↑)	<19>	t_{HKW}		2.9		ns
Delay time from VBCLK↓ to VBDC	<20>	t_{DKS4}		1.3	4.7	ns
Delay time from VBCLK↑ to VBD data	<21>	t_{DKD0}		0	5.5	ns
Delay time from VBCLK↓ to VBD data	<22>	t_{DKD1}		1.2	5.8	ns

(5) VSB master write timing (2/2)



Remarks 1. The level of the broken line portion indicates the undefined state (weak unknown) in which the bus holder in the NB85E is driving.

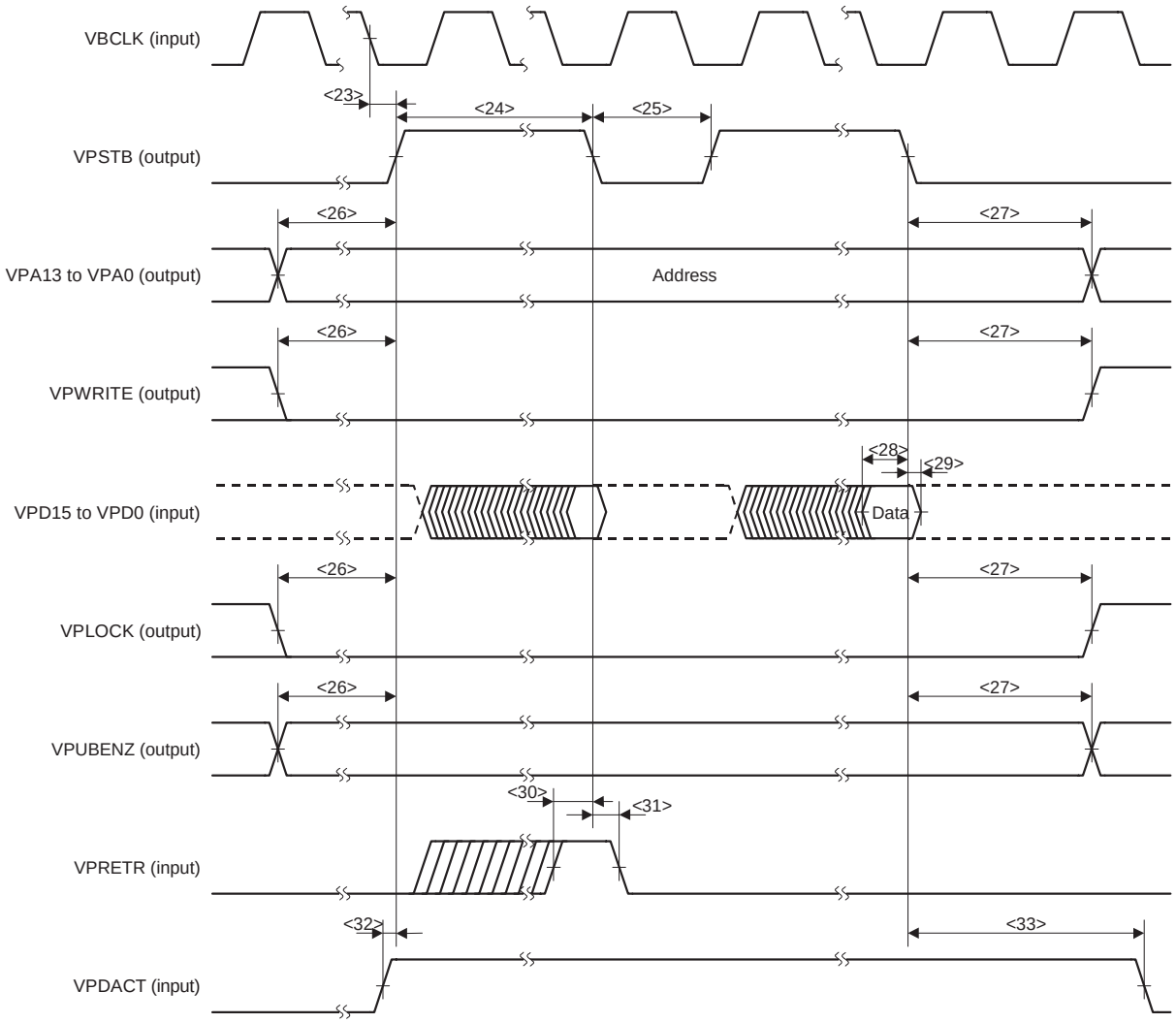
2. Rdy: When the VBWAIT, VBAHLD, and VBLAST signals are all low level

Wait: When the VBWAIT signal is high level, and the VBAHLD and VBLAST signals are low level

(6) NPB read timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↓ to VPSTB	<23>	t_{DKP}		2.5	7.8	ns
VPSTB output high-level width	<24>	t_{SSH}		60		ns
VPSTB output low-level width	<25>	t_{SSL}		20		ns
VPA address, VPWRITE, VPLOCK, VPUBENZ setup time (to VPSTB↑)	<26>	t_{SSA}		20		ns
VPA address, VPWRITE, VPLOCK, VPUBENZ hold time (from VPSTB↓)	<27>	t_{HSA}		20		ns
VPD read data setup time (to VPSTB↓)	<28>	t_{SSD}		20		ns
VPD read data hold time (from VPSTB↓)	<29>	t_{HSD}		0		ns
VPRETR setup time (to VPSTB↓)	<30>	t_{SSR}		20		ns
VPRETR hold time (from VPSTB↓)	<31>	t_{HSR}		0		ns
VPDACT setup time (to VPSTB↑)	<32>	t_{SSC}		20		ns
VPDACT hold time (from VPSTB↓)	<33>	t_{HSC}		20		ns

(6) NPB read timing (2/2)

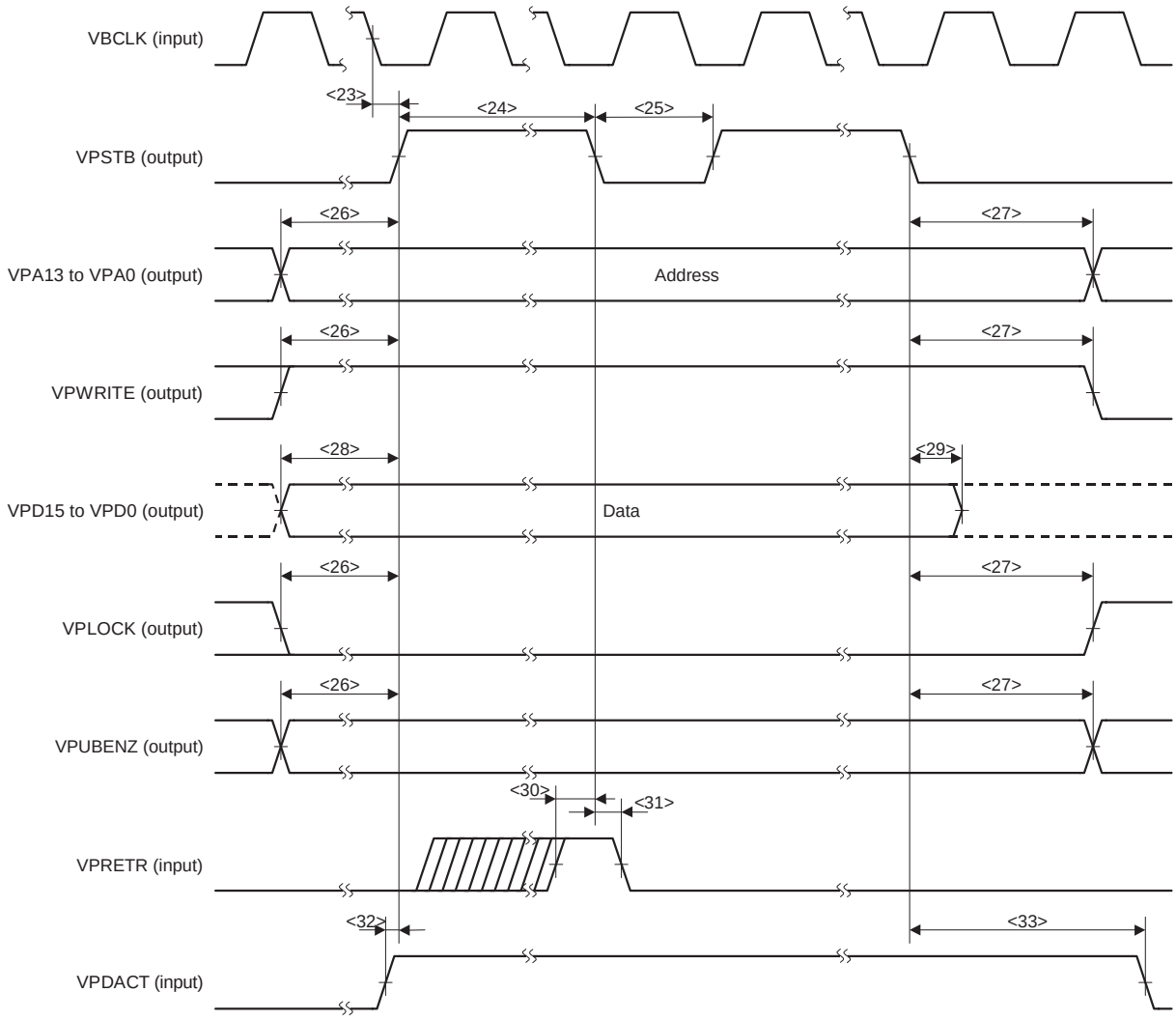


Remark The level of the broken line portion indicates the undefined state (weak unknown) in which the bus holder in the NB85E is driving.

(7) NPB write timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↓ to VPSTB	<23>	t_{DKP}		2.5	7.8	ns
VPSTB output high-level width	<24>	t_{SSH}		60		ns
VPSTB output low-level width	<25>	t_{SSL}		20		ns
VPA address, VPWRITE, VPLOCK, VPUBENZ setup time (to VPSTB↑)	<26>	t_{SSA}		20		ns
VPA address, VPWRITE, VPLOCK, VPUBENZ hold time (from VPSTB↓)	<27>	t_{HSA}		20		ns
VPD write data setup time (to VPSTB↑)	<28>	t_{SSD}		20		ns
VPD write data hold time (from VPSTB↓)	<29>	t_{HSD}		20		ns
VPRETR setup time (to VPSTB↓)	<30>	t_{SSR}		20		ns
VPRETR hold time (from VPSTB↓)	<31>	t_{HSR}		0		ns
VPDACT setup time (to VPSTB↑)	<32>	t_{SSC}		20		ns
VPDACT hold time (from VPSTB↓)	<33>	t_{HSC}		20		ns

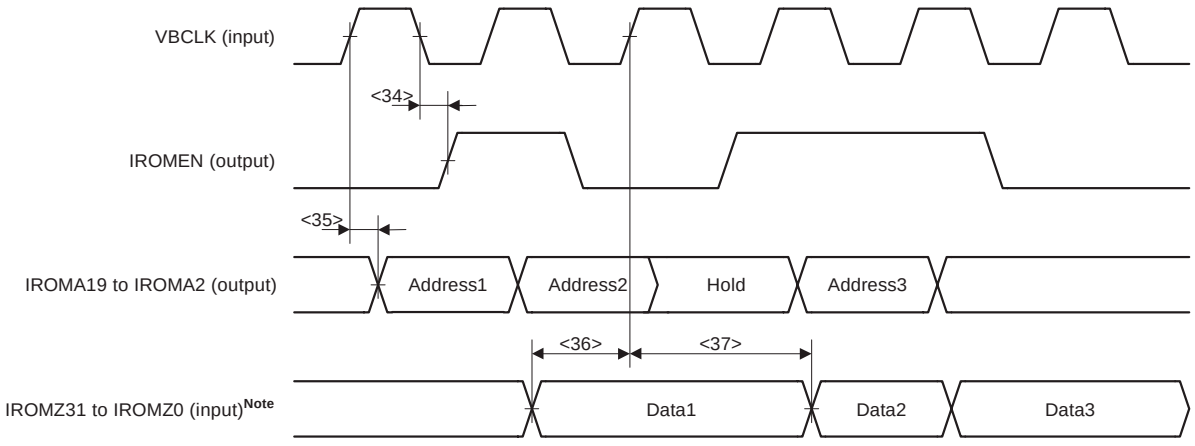
(7) NPB write timing (2/2)



Remark The level of the broken line portion indicates the undefined state (weak unknown) in which the bus holder in the NB85E is driving.

(8) VFB access timing

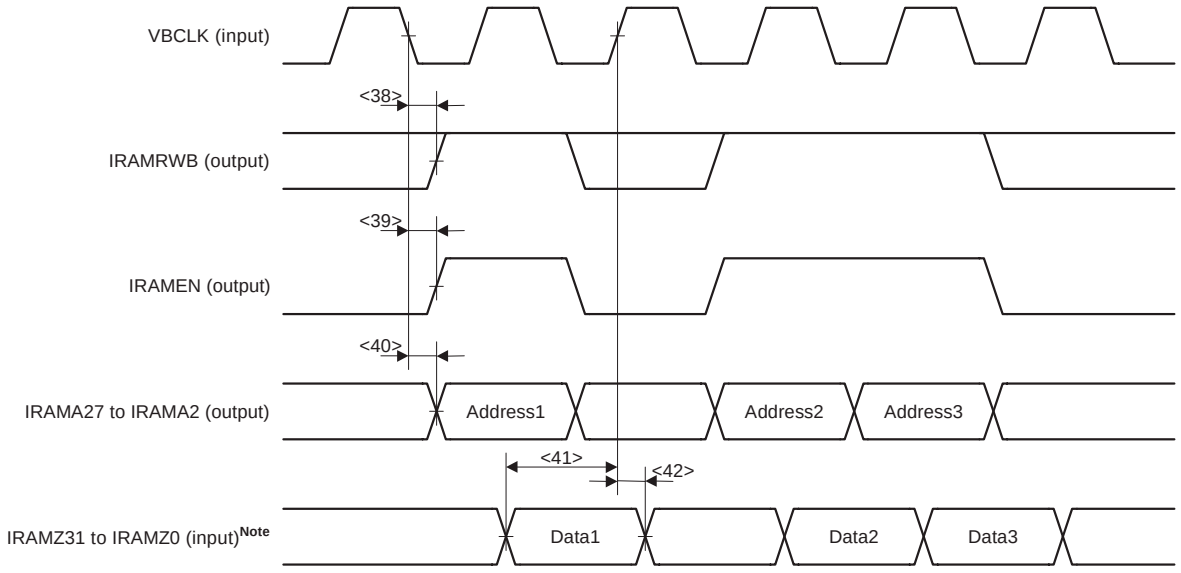
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↓ to IROMEN	<34>	t_{DKROE}		1.3	8.9	ns
Delay time from VBCLK↑ to IROMA	<35>	t_{DKROA}		1.3	11.8	ns
IROMZ setup time (to VBCLK↑)	<36>	t_{SKROZ}		3.4		ns
IROMZ hold time (from VBCLK↑)	<37>	t_{HKROZ}		3.2		ns



★ **Note** Hold data during the IROMEN signal is low level.

(9) VDB read timing

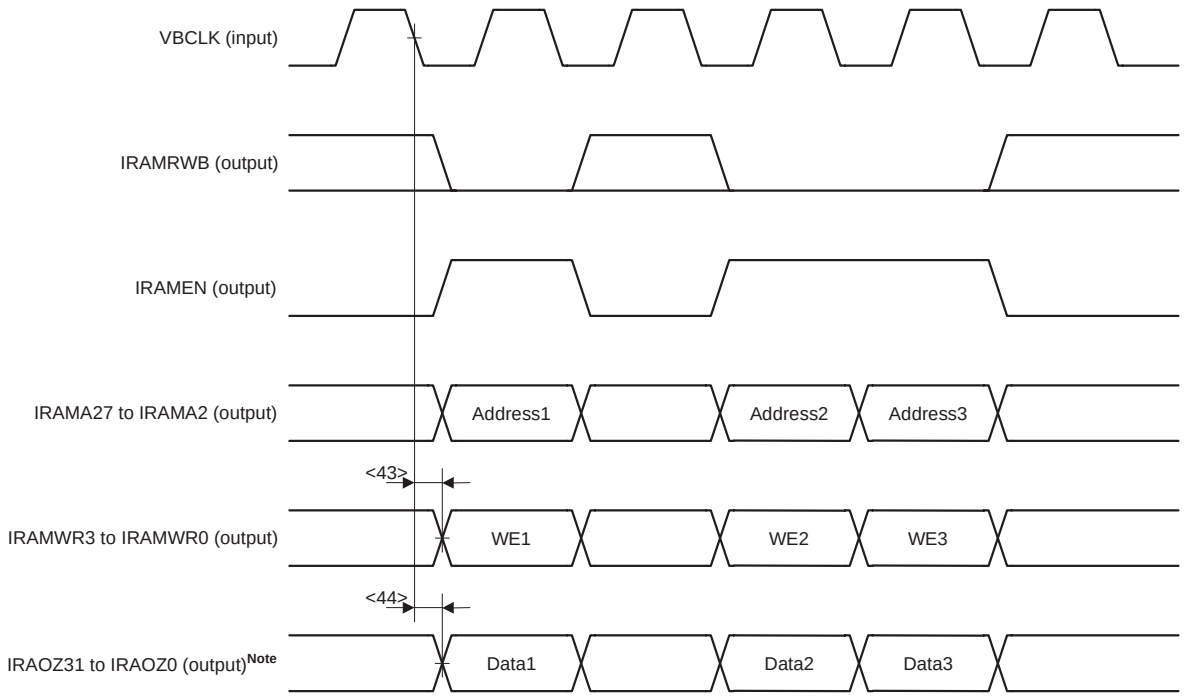
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↓ to IRAMRWB	<38>	t_{DKRAR}		1.3	8.4	ns
Delay time from VBCLK↓ to IRAMEN	<39>	t_{DKRAE}		1.3	8.9	ns
Delay time from VBCLK↓ to IRAMA	<40>	t_{DKRAA}		1.3	8.3	ns
IRAMZ setup time (to VBCLK↑)	<41>	t_{SKRAZ}		2.6		ns
IRAMZ hold time (from VBCLK↑)	<42>	t_{HKRAZ}		3.7		ns



Note Do not make signals IRAMZ31 to IRAMZ0 high impedance.

(10) VDB write timing

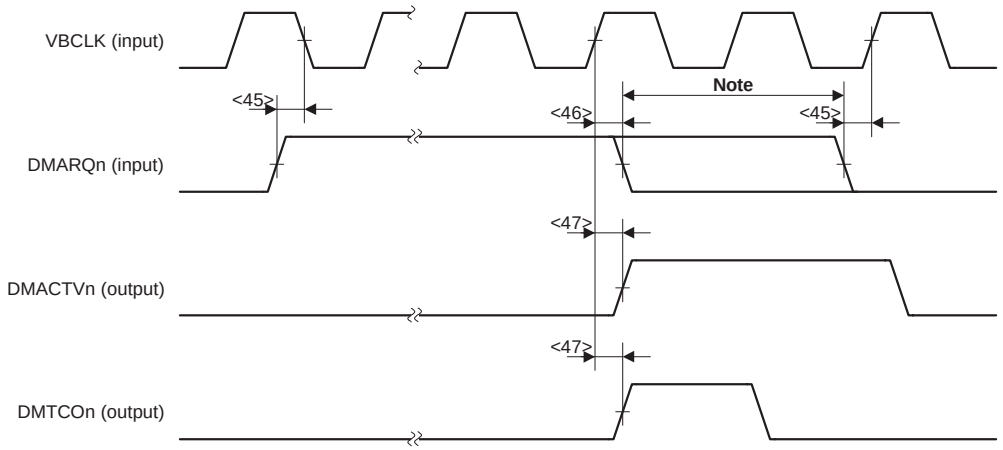
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↓ to IRAMWR	<43>	t_{DKRAW}		1.3	8.8	ns
Delay time from VBCLK↓ to IRAOZ	<44>	t_{DKRAZ}		1.3	9.1	ns



Note Signals IRAOZ31 to IRAOZ0 are always output and do not become high impedance.
Write operations are controlled by the IRAMEN signal and signals IRAMWR3 to IRAMWR0. Data cannot be written when the IRAMEN signal is low level.

(11) DMA transfer request, transfer completion timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
DMARQ setup time (to VBCLK↓)	<45>	t_{SKDQ}		0		ns
DMARQ hold time (from VBCLK↑)	<46>	t_{HKDQ}		0.8		ns
Delay time from VBCLK↑ to DMACTV, DMTCO	<47>	t_{DKDC}		1.3	6.5	ns

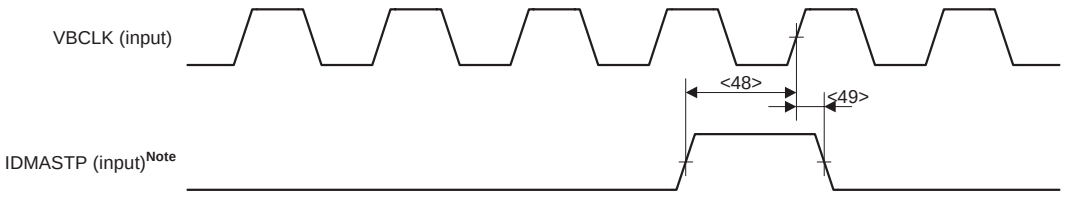


Note In order to avoid the generation of the next cycle, make the DMARQn signal low level in this cycle.

Remark n = 3 to 0

(12) DMA transfer abort timing

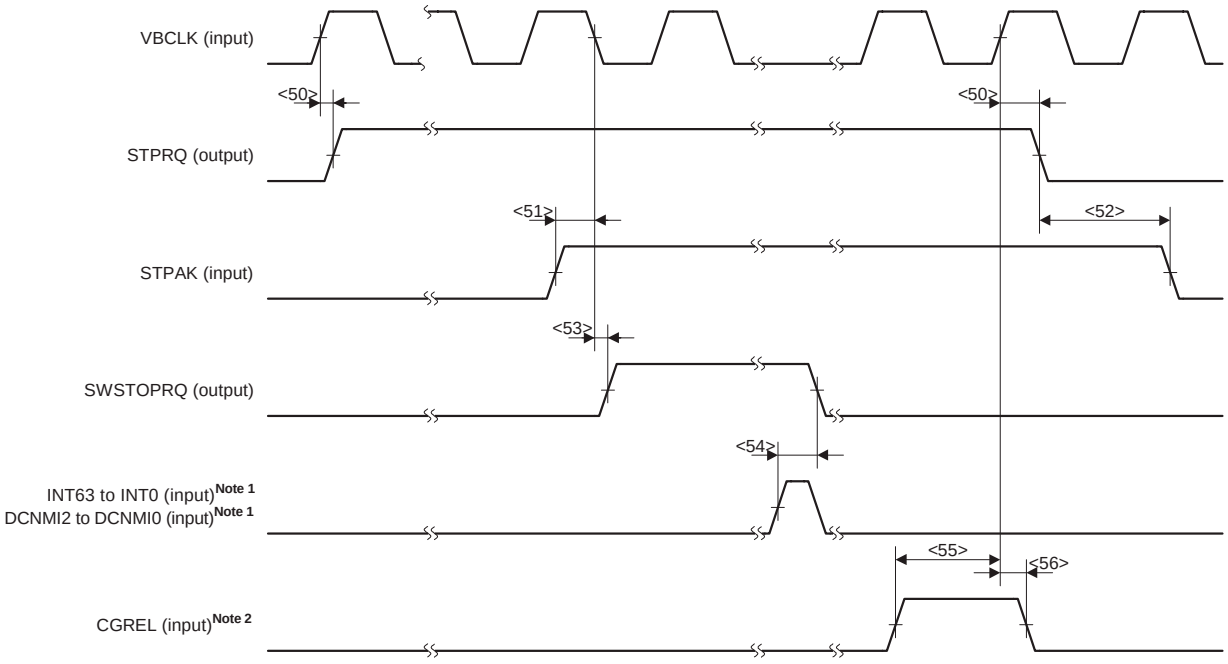
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
IDMASTP setup time (to VBCLK↑)	<48>	t_{SKDS}		3.5		ns
IDMASTP hold time (from VBCLK↑)	<49>	t_{HKDS}		1.7		ns



Note Input using a 1-clock pulse.

(13) Software STOP mode timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to STPRQ	<50>	t_{DKSQ}		1.3	4.6	ns
STPAK setup time (to VBCLK↓)	<51>	t_{SKSA}		0		ns
STPAK hold time (from STPRQ↓)	<52>	t_{HQSA}		7.0		ns
Delay time from VBCLK↓ to SWSTOPRQ↑	<53>	t_{DKSS}		1.3	4.7	ns
Delay time from INT, DCNMI to SWSTOPRQ↓	<54>	t_{DRSR}		0	15.0	ns
CGREL setup time (to VBCLK↑)	<55>	t_{SKSG}		0		ns
CGREL hold time (from VBCLK↑)	<56>	t_{HKSG}		2.5		ns

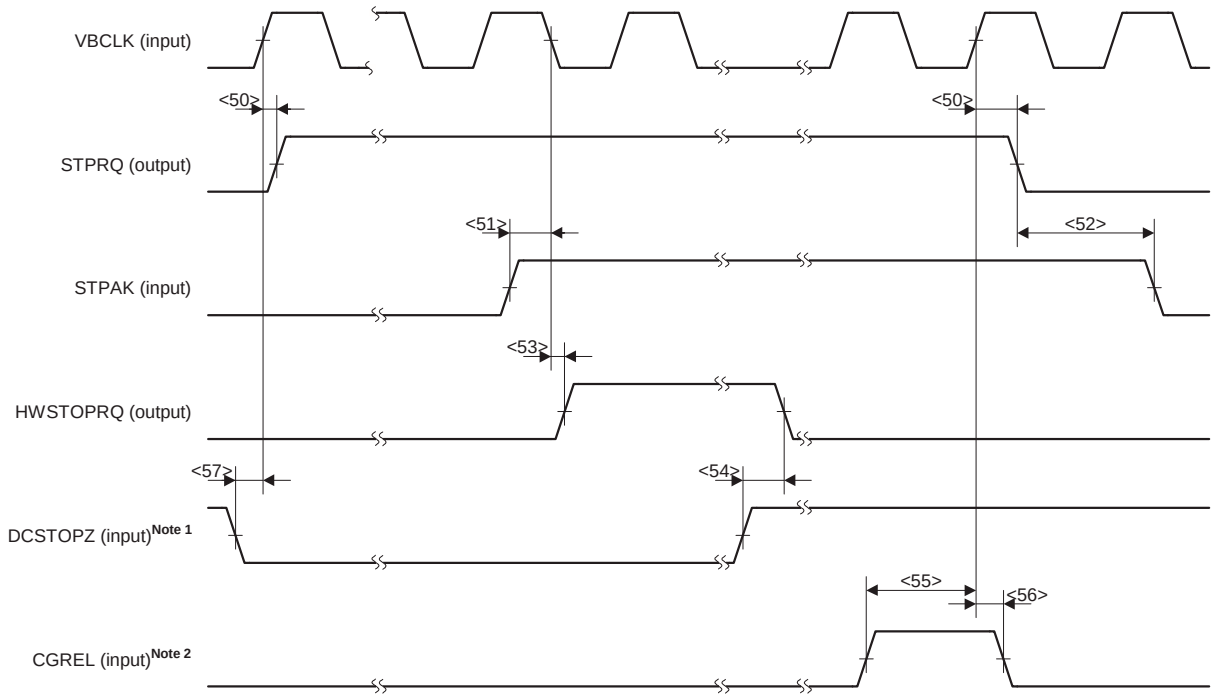


Notes 1. Software STOP mode is released upon detection of the rising edge of these signals.

2. Input an active level (high level) of 1 clock or more.

(14) Hardware STOP mode timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to STPRQ	<50>	t_{DKSQ}		1.3	4.6	ns
STPAK setup time (to VBCLK↓)	<51>	t_{SKSA}		0		ns
STPAK hold time (from STPRQ↓)	<52>	t_{HQSA}		7.0		ns
Delay time from VBCLK↓ to HWSTOPRQ↑	<53>	t_{DKSS}		1.3	4.7	ns
Delay time from DCSTOPZ to HWSTOPRQ↓	<54>	t_{DRSR}		0	15.0	ns
CGREL setup time (to VBCLK↑)	<55>	t_{SKSG}		0		ns
CGREL hold time (from VBCLK↑)	<56>	t_{HKSG}		2.5		ns
DCSTOPZ setup time (to VBCLK↑)	<57>	t_{SKST}		0		ns

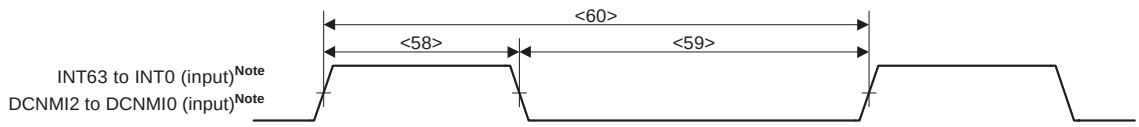


Notes 1. Hardware STOP mode is released upon detection of the rising edge of this signal.

2. Input an active level (high level) of 1 clock or more.

(15) Interrupt timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
INT, DCNMI high-level width	<58>	t_{WIH}		5.0		ns
INT, DCNMI low-level width	<59>	t_{WIL}		5.0		ns
INT, DCNMI interval time	<60>	t_{CYI}		$3 \times t_{CYK}$		ns



Note An interrupt is generated upon detection of the rising edge of these signals.

CHAPTER 8 NB85E901

(Under Development)

The NB85E901 is a run control unit (RCU) used by connecting to the NB85E.

8. 1 Outline

The NB85E901 (RCU) is a run control unit that realizes the execution of JTAG communication and debug processing. Connection of the NB85E901 with an N-Wire type in-circuit emulator (N-Wire type IE) makes it possible to perform on-chip debugging on the NB85E.

8. 1. 1 Symbol diagram

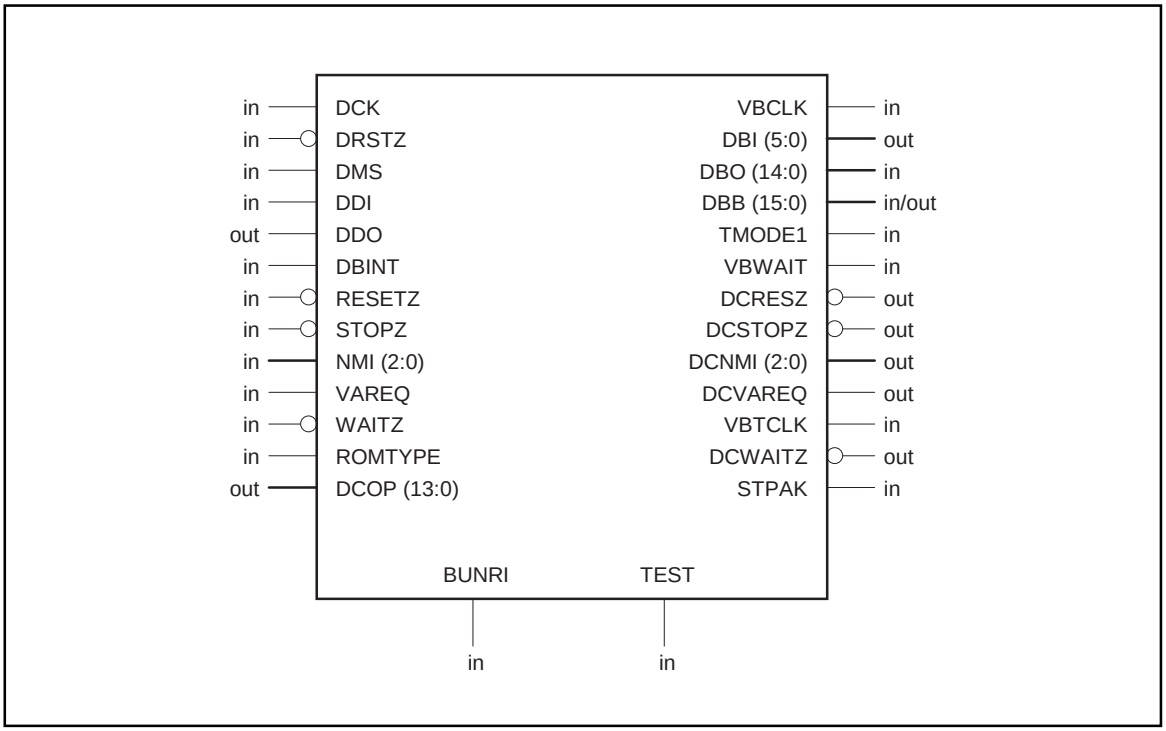
Number of grids

36.2k grids

46.4k grids (including wiring area)

Number of separation simulation patterns

41.8k



8. 1. 2 Pin capacitance

Remark C_{IN}: Capacitance of only input pin

C_{inewl}: Value of C_{IN} with wiring capacitance (estimated wire length capacitance) taken into consideration (l = 10 mm)

(1) Input pins

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
DCK	0.027	1.927	DBO10	0.020	1.920
DRSTZ	0.017	1.917	DBO9	0.054	1.954
DMS	0.088	1.988	DBO8	0.024	1.924
DDI	0.054	1.954	DBO7	0.062	1.962
DBINT	0.019	1.919	DBO6	0.077	1.977
RESETZ	0.069	1.969	DBO5	0.048	1.948
STOPZ	0.066	1.966	DBO4	0.057	1.957
NMI2	0.036	1.936	DBO3	0.065	1.965
NMI1	0.063	1.963	DBO2	0.090	1.990
NMI0	0.048	1.948	DBO1	0.009	1.909
VAREQ	0.021	1.921	DBO0	0.067	1.967
WAITZ	0.024	1.924	TMODE1	0.029	1.929
ROMTYPE	0.132	2.032	VBWAIT	0.050	1.950
VBCLK	0.035	1.935	VBTCLK	0.040	1.940
DBO14	0.057	1.957	STPAK	0.014	1.914
DBO13	0.062	1.962	BUNRI	0.096	1.996
DBO12	0.079	1.979	TEST	0.034	1.934
DBO11	0.065	1.965			

(2) Output pins

Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)
DDO	6.518	DCOP4	6.482	DBI0	12.901
DCOP13	6.399	DCOP3	6.474	DCRESZ	6.462
DCOP12	6.306	DCOP2	6.399	DCSTOPZ	4.884
DCOP11	6.404	DCOP1	6.560	DCNMI2	13.191
DCOP10	6.358	DCOP0	6.553	DCNMI1	13.319
DCOP9	12.922	DBI5	12.958	DCNMI0	13.308
DCOP8	12.855	DBI4	4.555	DCVAREQ	13.201
DCOP7	12.917	DBI3	6.435	DCWAITZ	13.306
DCOP6	12.818	DBI2	13.311		
DCOP5	12.850	DBI1	6.462		

(3) I/O pins

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
DBB15	6.487	0.095	1.995	DBB7	6.462	0.120	2.020
DBB14	6.420	0.163	2.063	DBB6	6.451	0.132	2.032
DBB13	6.492	0.091	1.991	DBB5	6.389	0.194	2.094
DBB12	6.432	0.150	2.050	DBB4	6.373	0.210	2.110
DBB11	6.517	0.066	1.966	DBB3	6.443	0.139	2.039
DBB10	6.524	0.059	1.959	DBB2	6.412	0.170	2.070
DBB9	6.487	0.096	1.996	DBB1	6.466	0.116	2.016
DBB8	6.496	0.087	1.987	DBB0	6.384	0.199	2.099

8. 2 Pin Functions

Pin Name		I/O	Function
N-Wire type IE connection pins	DCK	Input	Clock input for RCU
	DRSTZ	Input	Reset input for RCU
	DMS	Input	Debug mode selection input
	DDI	Input	Debug data input
	DDO	Output	Debug data output
	DBINT	Input	External debug interrupt input
System control pins	RESETZ	Input	System reset input
	STOPZ	Input	Hardware STOP mode request input
	NMI2 to NMI0	Input	Non-maskable interrupt input
	VAREQ	Input	Bus access right request input
	WAITZ	Input	Wait request input
	ROMTYPE	Input	NEC reserved pin (input a low level)
	DCOP13 to DCOP0	Output	NEC reserved pin (leave open)
NB85E connection pins	VBCLK	Input	System clock input
	DBI5 to DBI0	Output	Debug control output
	DBO14 to DBO0	Input	Debug control input
	DBB15 to DBB0	I/O	Debug control I/O
	TMODE1	Input	Test mode selection input
	VBWAIT	Input	Wait response input
	DCRESZ	Output	Reset output
	DCSTOPZ	Output	Hardware STOP mode request output
	DCNMI2 to DCNMI0	Output	Non-maskable interrupt output
	DCVAREQ	Output	Bus access right request output
	VBTCLK	Input	Clock input for testing
Peripheral connection pins	DCWAITZ	Output	Wait request output
	STPAK	Input	STOP mode request acknowledge input
Test mode pins	BUNRI	Input	Normal/test mode selection input
	TEST	Input	Test bus control input

8. 3 Electrical Specifications (Preliminary)

The following specifications are for a single macro. An actual chip consists of two or more macros. Design the system so that all the specifications of the individual macros are satisfied when the chip is used.

8. 3. 1 Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to +4.6	V
Operating ambient temperature	T_A	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

8. 3. 2 Recommended operation range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	−40		+85	°C
Clock cycle	t_{CYK}	15.0			ns

8. 3. 3 DC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1}	When operating		0.33	0.43	mA/MHz
	I_{DD2}	When not operating		0	1.0	μA

Remark The TYP. value is a reference value for when T_A = 25°C, V_{DD} = 3.3 V.

8. 3. 4 AC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay time from RESETZ to DCRESZ	t_{DDRES}			2.0	ns
Delay time from STOPZ to DCSTOPZ	t_{DDSTP}			2.0	ns
Delay time from NMI to DCNMI	t_{DDNMI}			2.0	ns
Delay time from WAITZ to DCWAITZ	t_{DDWT}			2.0	ns
Delay time from VAREQ to DCVAREQ	t_{DDVRQ}			2.0	ns

CHAPTER 9 NB85ET

(Under Development)

The NB85ET is a CPU core incorporating debug controller that realizes on-chip debugging using a single NB85ET, and includes on chip the “V850E1” CPU, NEC’s 32-bit RISC microprocessor, as well as various peripheral I/O functions such as DMA and interrupt controllers.

9. 1 Outline

- Processing performance: 62 MIPS (@ 50 MHz operation)
- Memory space
  Program area: 64 MB linear
  Data area: 4 GB linear
  Memory bank division function: 2, 4, and 8 MB/bank
- Minimum instruction execution time: 20 ns (@ 50 MHz operation)
- External bus interface
  VSB (V850E System Bus)
  NPB (NEC Peripheral I/O Bus)
- Interrupt/exception control function
  Non-maskable interrupts: 3 sources
  Maskable interrupts: 64 sources
  Exceptions: 1 source
  8 priority levels specifiable (maskable interrupts)
- DMA control function
  4-channel structure
  Transfer unit: 8, 16, and 32 bits
  Maximum number of transfers: 65536 (2^{16})
  Transfer type: Flyby (1-cycle) transfer, 2-cycle transfer
  Transfer mode: Single transfer, single step transfer, line transfer, block transfer
  Terminal count output signals (DMTCO3 to DMTCO0)
- Power save function
  HALT, hardware/software STOP modes
- Debug control function
  CPU break, trace, event detection

9. 1. 1 Symbol diagram

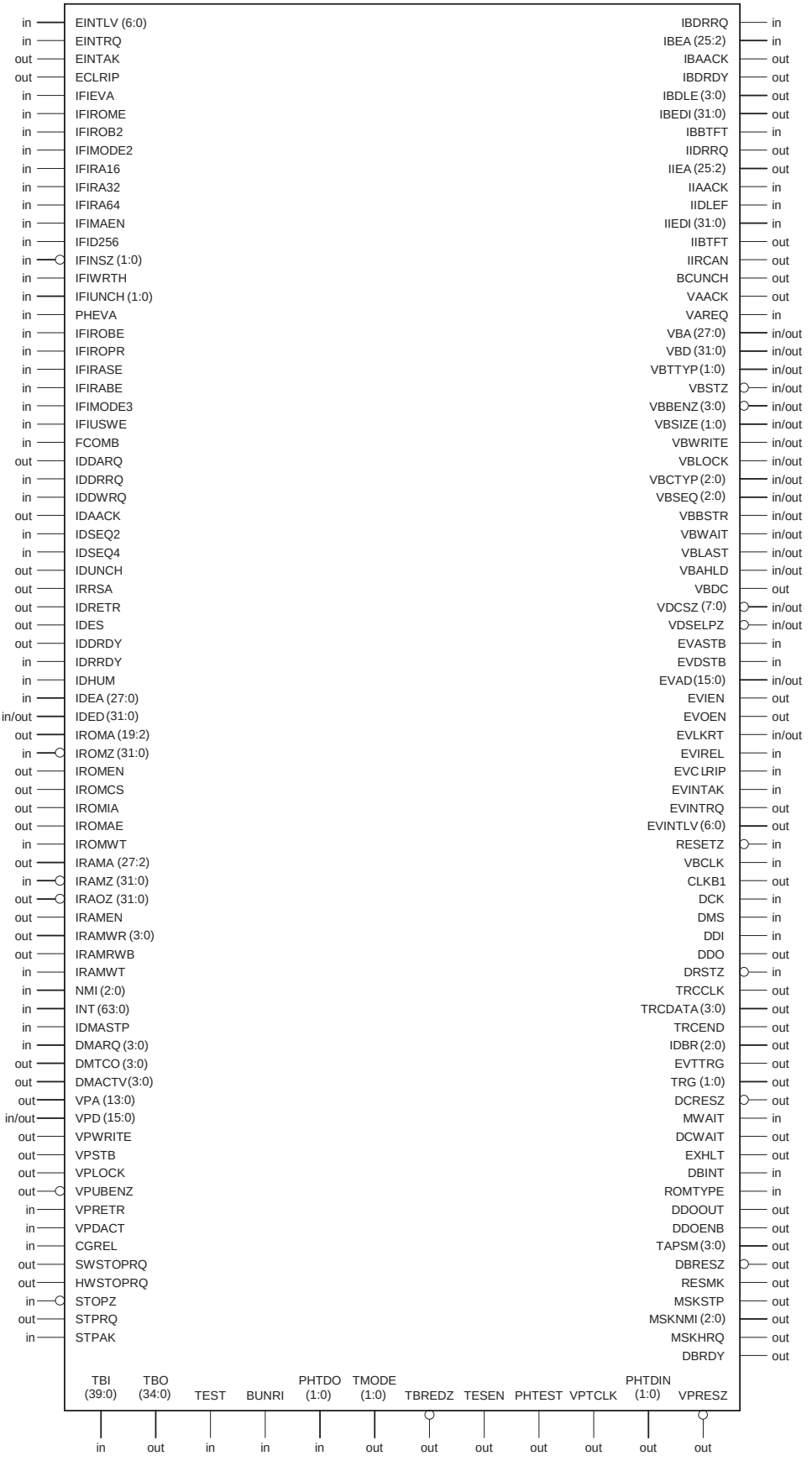
Number of grids

574.6k grids

857.4k grids (including wiring area)

Number of separation simulation patterns

498.5k


in EINTLV (6:0)
in EINTRQ
out EINTAK
out ECLRIP
in IFIEVA
in IFIROME
in IFIROB2
in IFIMODE2
in IFIRA16
in IFIRA32
in IFIRA64
in IFIMAEN
in IFID256
in IFINSZ (1:0)
in IFIWRTH
in IFIUNCH (1:0)
in PHEVA
in IFIROBE
in IFIROPR
in IFIRASE
in IFIRABE
in IFIMODE3
in IFIUSWE
in FCOMB
out IDDARQ
in IDDRRQ
in IDDWRQ
out IDAACK
in IDSEQ2
in IDSEQ4
out IDUNCH
out IRRSA
out IDRETR
out IDES
out IDDRDY
in IDRRDY
in IDHUM
in IDEA (27:0)
in/out IDED (31:0)
out IROMA (19:2)
in IROMZ (31:0)
out IROMEN
out IROMCS
out IROMIA
out IROMAE
in IROMWT
out IRAMA (27:2)
in IRAMZ (31:0)
out IRAOZ (31:0)
out IRAMEN
out IRAMWR (3:0)
out IRAMRWB
in IRAMWT
in NMI (2:0)
in INT (63:0)
in IDMASTP
in DMARQ (3:0)
out DMTCO (3:0)
out DMACTV (3:0)
out VPA (13:0)
in/out VPD (15:0)
out VPWRITE
out VPSTB
out VPLOCK
out VPUBENZ
in VPRETR
in VPDACT
in CGREL
out SWSTOPRQ
out HWSTOPRQ
in STOPZ
out STPRQ
in STPAK
IBDRRQ in
IBEA (25:2) in
IBAACK out
IBDRDY out
IBDLE (3:0) out
IBEDI (31:0) out
IBBTFT in
IIDRRQ out
IIEA (25:2) out
IIAACK in
IIDLEF in
IIEDI (31:0) in
IIBTFT out
IIRCAN out
BCUNCH out
VAACK out
VAREQ in
VBA (27:0) in/out
VBD (31:0) in/out
VBTTYP (1:0) in/out
VBSTZ in/out
VBBENZ (3:0) in/out
VBSIZE (1:0) in/out
VBWRITE in/out
VBLOCK in/out
VBCTYP (2:0) in/out
VBSEQ (2:0) in/out
VBBSTR in/out
VBWAIT in/out
VBLAST in/out
VBAHLD in/out
VBDC out
VDCSZ (7:0) in/out
VDSELPZ in/out
EVASTB in
EVDSTB in
EVAD (15:0) in/out
EVIEN out
EVOEN out
EVLKRT in/out
EVIREL in
EVCLRIP in
EVINTAK in
EVINTRQ out
EVINTLV (6:0) out
RESETZ in
VBCLK in
CLKB1 out
DCK in
DMS in
DDI in
DDO out
DRSTZ in
TRCCLK out
TRCDATA (3:0) out
TRCEND out
IDBR (2:0) out
EVTTRG out
TRG (1:0) out
DCRESZ out
MWAIT in
DCWAIT out
EXHLT out
DBINT in
ROMTYPE in
DDOOUT out
DDOENB out
TAPSM (3:0) out
DBRESZ out
RESMK out
MSKSTP out
MSKNMI (2:0) out
MSKHRQ out
DBRDY out
TBI (39:0) in
TBO (34:0) out
TEST in
BUNRI in
PHTDO (1:0) in
TMODE (1:0) out
TBREDZ out
TESEN out
PHTEST out
VPTCLK out
PHTDIN (1:0) out
VPRESZ out

9. 1. 2 Pin capacitance

Remark C_{IN}: Capacitance of only input pin

C_{inewl}: Value of C_{IN} with wiring capacitance (estimated wire length capacitance) taken into consideration (l = 10 mm)

(1) Input pins (1/5)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
VPRETR	0.663	2.563	INT45	0.032	1.932
VPDACT	0.205	2.105	INT44	0.052	1.952
VAREQ	0.248	2.148	INT43	0.032	1.932
RESETZ	0.196	2.096	INT42	0.023	1.923
VBCLK	0.070	1.970	INT41	0.051	1.951
CGREL	0.047	1.947	INT40	0.084	1.984
STOPZ	0.447	2.347	INT39	0.228	2.128
STPAK	0.263	2.163	INT38	0.070	1.970
IDMASTP	0.137	2.037	INT37	0.075	1.975
DMARQ3	0.020	1.920	INT36	0.088	1.988
DMARQ2	0.211	2.111	INT35	0.071	1.971
DMARQ1	0.169	2.069	INT34	0.033	1.933
DMARQ0	0.259	2.159	INT33	0.053	1.953
NMI2	0.390	2.290	INT32	0.031	1.931
NMI1	0.340	2.240	INT31	0.039	1.939
NMI0	0.363	2.263	INT30	0.050	1.950
INT63	0.022	1.922	INT29	0.024	1.924
INT62	0.031	1.931	INT28	0.042	1.942
INT61	0.013	1.913	INT27	0.013	1.913
INT60	0.023	1.923	INT26	0.044	1.944
INT59	0.034	1.934	INT25	0.012	1.912
INT58	0.032	1.932	INT24	0.017	1.917
INT57	0.046	1.946	INT23	0.053	1.953
INT56	0.024	1.924	INT22	0.058	1.958
INT55	0.016	1.916	INT21	0.019	1.919
INT54	0.057	1.957	INT20	0.019	1.919
INT53	0.016	1.916	INT19	0.034	1.934
INT52	0.033	1.933	INT18	0.019	1.919
INT51	0.054	1.954	INT17	0.045	1.945
INT50	0.043	1.943	INT16	0.023	1.923
INT49	0.015	1.915	INT15	0.027	1.927
INT48	0.025	1.925	INT14	0.016	1.916
INT47	0.020	1.920	INT13	0.044	1.944
INT46	0.057	1.957	INT12	0.034	1.934

(1) Input pins (2/5)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
INT11	0.034	1.934	IROMZ4	0.651	2.551
INT10	0.023	1.923	IROMZ3	0.612	2.512
INT9	0.037	1.937	IROMZ2	0.707	2.607
INT8	0.028	1.928	IROMZ1	0.599	2.499
INT7	0.024	1.924	IROMZ0	0.632	2.532
INT6	0.026	1.926	IROMWT	0.117	2.017
INT5	0.028	1.928	IRAMZ31	0.057	1.957
INT4	0.030	1.930	IRAMZ30	0.037	1.937
INT3	0.025	1.925	IRAMZ29	0.513	2.413
INT2	0.035	1.935	IRAMZ28	0.483	2.383
INT1	0.026	1.926	IRAMZ27	0.198	2.098
INT0	0.030	1.930	IRAMZ26	0.036	1.936
IROMZ31	0.318	2.218	IRAMZ25	0.051	1.951
IROMZ30	0.405	2.305	IRAMZ24	0.045	1.945
IROMZ29	0.313	2.213	IRAMZ23	0.036	1.936
IROMZ28	0.358	2.258	IRAMZ22	0.037	1.937
IROMZ27	0.534	2.434	IRAMZ21	0.152	2.052
IROMZ26	0.411	2.311	IRAMZ20	0.473	2.373
IROMZ25	0.352	2.252	IRAMZ19	0.380	2.280
IROMZ24	0.427	2.327	IRAMZ18	0.209	2.109
IROMZ23	0.373	2.273	IRAMZ17	0.233	2.133
IROMZ22	0.527	2.427	IRAMZ16	0.078	1.978
IROMZ21	0.544	2.444	IRAMZ15	0.075	1.975
IROMZ20	0.335	2.235	IRAMZ14	0.052	1.952
IROMZ19	0.406	2.306	IRAMZ13	0.239	2.139
IROMZ18	0.603	2.503	IRAMZ12	0.197	2.097
IROMZ17	0.400	2.300	IRAMZ11	0.234	2.134
IROMZ16	0.399	2.299	IRAMZ10	0.184	2.084
IROMZ15	0.388	2.288	IRAMZ9	0.407	2.307
IROMZ14	0.569	2.469	IRAMZ8	0.222	2.122
IROMZ13	0.559	2.459	IRAMZ7	0.322	2.222
IROMZ12	0.597	2.497	IRAMZ6	0.063	1.963
IROMZ11	0.612	2.512	IRAMZ5	0.278	2.178
IROMZ10	0.643	2.543	IRAMZ4	0.265	2.165
IROMZ9	0.375	2.275	IRAMZ3	0.241	2.141
IROMZ8	0.434	2.334	IRAMZ2	0.169	2.069
IROMZ7	0.602	2.502	IRAMZ1	0.050	1.950
IROMZ6	0.399	2.299	IRAMZ0	0.292	2.192
IROMZ5	0.537	2.437	IRAMWT	0.393	2.293

(1) Input pins (3/5)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
IBDRRQ	0.110	2.010	IIEDI19	0.043	1.943
IBEA25	0.168	2.068	IIEDI18	0.084	1.984
IBEA24	0.110	2.010	IIEDI17	0.075	1.975
IBEA23	0.014	1.914	IIEDI16	0.042	1.942
IBEA22	0.025	1.925	IIEDI15	0.067	1.967
IBEA21	0.074	1.974	IIEDI14	0.070	1.970
IBEA20	0.017	1.917	IIEDI13	0.049	1.949
IBEA19	0.050	1.950	IIEDI12	0.047	1.947
IBEA18	0.057	1.957	IIEDI11	0.054	1.954
IBEA17	0.014	1.914	IIEDI10	0.022	1.922
IBEA16	0.043	1.943	IIEDI9	0.056	1.956
IBEA15	0.016	1.916	IIEDI8	0.038	1.938
IBEA14	0.024	1.924	IIEDI7	0.049	1.949
IBEA13	0.139	2.039	IIEDI6	0.038	1.938
IBEA12	0.032	1.932	IIEDI5	0.029	1.929
IBEA11	0.109	2.009	IIEDI4	0.038	1.938
IBEA10	0.150	2.050	IIEDI3	0.029	1.929
IBEA9	0.082	1.982	IIEDI2	0.022	1.922
IBEA8	0.125	2.025	IIEDI1	0.030	1.930
IBEA7	0.133	2.033	IIEDI0	0.020	1.920
IBEA6	0.128	2.028	IBBTFT	0.175	2.075
IBEA5	0.117	2.017	IDDRRQ	0.549	2.449
IBEA4	0.089	1.989	IDDWRQ	0.522	2.422
IBEA3	0.168	2.068	IDSEQ4	0.373	2.273
IBEA2	0.180	2.080	IDSEQ2	0.568	2.468
IIAACK	0.069	1.969	IDRRDY	0.155	2.055
IIDLEF	0.090	1.990	IDHUM	0.361	2.261
IIEDI31	0.159	2.059	IDEA27	0.249	2.149
IIEDI30	0.143	2.043	IDEA26	0.264	2.164
IIEDI29	0.124	2.024	IDEA25	0.293	2.193
IIEDI28	0.110	2.010	IDEA24	0.375	2.275
IIEDI27	0.115	2.015	IDEA23	0.255	2.155
IIEDI26	0.094	1.994	IDEA22	0.260	2.160
IIEDI25	0.178	2.078	IDEA21	0.251	2.151
IIEDI24	0.124	2.024	IDEA20	0.356	2.256
IIEDI23	0.105	2.005	IDEA19	0.259	2.159
IIEDI22	0.081	1.981	IDEA18	0.333	2.233
IIEDI21	0.083	1.983	IDEA17	0.248	2.148
IIEDI20	0.066	1.966	IDEA16	0.273	2.173

(1) Input pins (4/5)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
IDEA15	0.328	2.228	IFIRA32	0.944	2.844
IDEA14	0.291	2.191	IFIRA16	0.831	2.731
IDEA13	0.303	2.203	IFIMAEN	0.430	2.330
IDEA12	0.325	2.225	IFID256	0.450	2.350
IDEA11	0.248	2.148	IFINSZ1	0.476	2.376
IDEA10	0.361	2.261	IFINSZ0	0.491	2.391
IDEA9	0.328	2.228	IFIWRTH	0.549	2.449
IDEA8	0.256	2.156	IFIUNCH1	0.657	2.557
IDEA7	0.249	2.149	IFIUNCH0	0.506	2.406
IDEA6	0.344	2.244	PHEVA	1.405	3.305
IDEA5	0.235	2.135	IFIEVA	0.311	2.211
IDEA4	0.244	2.144	IFIMODE2	0.586	2.486
IDEA3	0.235	2.135	IFIROBE	0.413	2.313
IDEA2	0.274	2.174	IFIROPR	0.523	2.423
IDEA1	0.259	2.159	IFIRASE	1.053	2.953
IDEA0	0.234	2.134	IFIRABE	0.610	2.510
EINTLV6	0.034	1.934	IFIMODE3	0.642	2.542
EINTLV5	0.062	1.962	IFIUSWE	0.377	2.277
EINTLV4	0.040	1.940	FCOMB	0.131	2.031
EINTLV3	0.013	1.913	TBI39	0.013	1.913
EINTLV2	0.066	1.966	TBI38	0.013	1.913
EINTLV1	0.046	1.946	TBI37	0.060	1.960
EINTLV0	0.055	1.955	TBI36	0.034	1.934
EINTRQ	0.048	1.948	TBI35	0.023	1.923
DCK	0.408	2.308	TBI34	0.007	1.907
DMS	0.196	2.096	TBI33	0.031	1.931
DDI	0.016	1.916	TBI32	0.014	1.914
DRSTZ	0.014	1.914	TBI31	0.017	1.917
MWAIT	0.065	1.965	TBI30	0.017	1.917
DBINT	0.074	1.974	TBI29	0.021	1.921
ROMTYPE	0.080	1.980	TBI28	0.011	1.911
EVASTB	0.410	2.310	TBI27	0.028	1.928
EVDSTB	0.181	2.081	TBI26	0.018	1.918
EVIREL	0.135	2.035	TBI25	0.010	1.910
EVCLRIP	0.225	2.125	TBI24	0.023	1.923
EVINTAK	0.133	2.033	TBI23	0.021	1.921
IFIROME	0.462	2.362	TBI22	0.034	1.934
IFIROB2	0.550	2.450	TBI21	0.158	2.058
IFIRA64	1.016	2.916	TBI20	0.168	2.068

(1) Input pins (5/5)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
TBI19	0.103	2.003	TBI7	0.022	1.922
TBI18	0.186	2.086	TBI6	0.047	1.947
TBI17	0.190	2.090	TBI5	0.032	1.932
TBI16	0.171	2.071	TBI4	0.013	1.913
TBI15	0.008	1.908	TBI3	0.016	1.916
TBI14	0.032	1.932	TBI2	0.007	1.907
TBI13	0.041	1.941	TBI1	0.043	1.943
TBI12	0.031	1.931	TBI0	0.025	1.925
TBI11	0.042	1.942	TEST	0.305	2.205
TBI10	0.041	1.941	BUNRI	0.459	2.359
TBI9	0.025	1.925	PHTDO1	0.545	2.445
TBI8	0.031	1.931	PHTDO0	0.540	2.440

(2) Output pins (1/4)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
VPA13	12.854	–	–	STPRQ	12.443	–	–
VPA12	12.877	–	–	DMTCO3	12.973	–	–
VPA11	12.799	–	–	DMTCO2	12.905	–	–
VPA10	13.300	–	–	DMTCO1	13.145	–	–
VPA9	12.852	–	–	DMTCO0	13.157	–	–
VPA8	12.801	–	–	DMACTV3	13.185	–	–
VPA7	13.284	–	–	DMACTV2	13.275	–	–
VPA6	13.272	–	–	DMACTV1	13.229	–	–
VPA5	13.242	–	–	DMACTV0	13.338	–	–
VPA4	13.102	–	–	IROMA19	13.056	–	–
VPA3	13.149	–	–	IROMA18	13.071	–	–
VPA2	13.192	–	–	IROMA17	13.069	–	–
VPA1	12.839	–	–	IROMA16	13.069	–	–
VPA0	13.188	–	–	IROMA15	13.068	–	–
VPWRITE	13.151	–	–	IROMA14	13.334	–	–
VPSTB	12.758	–	–	IROMA13	13.333	–	–
VPLOCK	13.025	–	–	IROMA12	13.332	–	–
VPUBENZ	13.191	–	–	IROMA11	13.055	–	–
VAACK	12.977	–	–	IROMA10	13.329	–	–
VBDC	13.018	–	–	IROMA9	13.064	–	–
CLKB1	13.071	–	–	IROMA8	13.328	–	–
SWSTOPRQ	12.778	–	–	IROMA7	13.338	–	–
HWSTOPRQ	12.945	–	–	IROMA6	13.062	–	–

(2) Output pins (2/4)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
IROMA5	13.071	–	–	IRAOZ26	13.291	–	–
IROMA4	13.059	–	–	IRAOZ25	13.331	–	–
IROMA3	13.046	–	–	IRAOZ24	13.286	–	–
IROMA2	13.052	–	–	IRAOZ23	13.326	–	–
IROMEN	13.056	–	–	IRAOZ22	13.334	–	–
IROMCS	13.055	–	–	IRAOZ21	13.336	–	–
IROMIA	12.985	–	–	IRAOZ20	13.336	–	–
IROMAE	13.006	–	–	IRAOZ19	13.327	–	–
IRAMA27	13.071	–	–	IRAOZ18	13.312	–	–
IRAMA26	13.291	–	–	IRAOZ17	13.269	–	–
IRAMA25	13.006	–	–	IRAOZ16	13.103	–	–
IRAMA24	13.322	–	–	IRAOZ15	13.260	–	–
IRAMA23	13.325	–	–	IRAOZ14	13.314	–	–
IRAMA22	13.332	–	–	IRAOZ13	13.335	–	–
IRAMA21	13.009	–	–	IRAOZ12	13.292	–	–
IRAMA20	13.325	–	–	IRAOZ11	13.118	–	–
IRAMA19	13.323	–	–	IRAOZ10	13.275	–	–
IRAMA18	13.297	–	–	IRAOZ9	13.333	–	–
IRAMA17	13.283	–	–	IRAOZ8	13.257	–	–
IRAMA16	13.303	–	–	IRAOZ7	13.338	–	–
IRAMA15	13.269	–	–	IRAOZ6	13.314	–	–
IRAMA14	13.324	–	–	IRAOZ5	13.334	–	–
IRAMA13	13.317	–	–	IRAOZ4	13.321	–	–
IRAMA12	13.323	–	–	IRAOZ3	13.194	–	–
IRAMA11	13.320	–	–	IRAOZ2	13.112	–	–
IRAMA10	13.272	–	–	IRAOZ1	13.331	–	–
IRAMA9	13.284	–	–	IRAOZ0	13.338	–	–
IRAMA8	13.311	–	–	IRAMEN	13.194	–	–
IRAMA7	13.270	–	–	IRAMWR3	13.139	–	–
IRAMA6	13.274	–	–	IRAMWR2	13.152	–	–
IRAMA5	13.270	–	–	IRAMWR1	13.202	–	–
IRAMA4	13.273	–	–	IRAMWR0	13.262	–	–
IRAMA3	13.329	–	–	IRAMRWB	13.191	–	–
IRAMA2	13.319	–	–	IBAACK	13.338	–	–
IRAOZ31	13.337	–	–	IBDRDY	13.338	–	–
IRAOZ30	13.334	–	–	IBDLE3	12.818	–	–
IRAOZ29	13.338	–	–	IBDLE2	12.785	–	–
IRAOZ28	13.333	–	–	IBDLE1	12.744	–	–
IRAOZ27	13.333	–	–	IBDLE0	12.620	–	–

(2) Output pins (3/4)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
IBEDI31	12.929	–	–	IIEA19	13.035	–	–
IBEDI30	12.948	–	–	IIEA18	13.061	–	–
IBEDI29	13.056	–	–	IIEA17	13.070	–	–
IBEDI28	12.980	–	–	IIEA16	13.048	–	–
IBEDI27	13.025	–	–	IIEA15	13.071	–	–
IBEDI26	13.017	–	–	IIEA14	13.070	–	–
IBEDI25	12.969	–	–	IIEA13	12.948	–	–
IBEDI24	13.000	–	–	IIEA12	13.057	–	–
IBEDI23	12.990	–	–	IIEA11	12.956	–	–
IBEDI22	13.039	–	–	IIEA10	12.981	–	–
IBEDI21	13.044	–	–	IIEA9	13.028	–	–
IBEDI20	13.051	–	–	IIEA8	13.005	–	–
IBEDI19	13.049	–	–	IIEA7	13.026	–	–
IBEDI18	13.041	–	–	IIEA6	13.067	–	–
IBEDI17	13.033	–	–	IIEA5	12.964	–	–
IBEDI16	13.067	–	–	IIEA4	12.999	–	–
IBEDI15	13.027	–	–	IIEA3	12.929	–	–
IBEDI14	13.024	–	–	IIEA2	12.948	–	–
IBEDI13	13.061	–	–	IIBTFT	12.924	–	–
IBEDI12	13.052	–	–	IIRCAN	12.889	–	–
IBEDI11	13.048	–	–	BCUNCH	13.062	–	–
IBEDI10	13.070	–	–	IDDARQ	13.037	–	–
IBEDI9	13.038	–	–	IDAACK	13.030	–	–
IBEDI8	13.059	–	–	IRRSA	13.287	–	–
IBEDI7	13.054	–	–	IDRETR	13.039	–	–
IBEDI6	13.046	–	–	IDUNCH	12.574	–	–
IBEDI5	13.067	–	–	IDDRDY	13.289	–	–
IBEDI4	13.066	–	–	IDES	13.049	–	–
IBEDI3	13.066	–	–	EINTAK	13.025	–	–
IBEDI2	13.066	–	–	ECLRIP	13.049	–	–
IBEDI1	13.060	–	–	DDO	13.007	–	–
IBEDI0	13.065	–	–	TRCCLK	12.885	–	–
IIDRRQ	13.019	–	–	TRCDATA3	12.803	–	–
IIEA25	12.985	–	–	TRCDATA2	12.796	–	–
IIEA24	12.972	–	–	TRCDATA1	12.683	–	–
IIEA23	13.070	–	–	TRCDATA0	12.852	–	–
IIEA22	13.067	–	–	TRCEND	12.736	–	–
IIEA21	13.020	–	–	IDBR2	12.638	–	–
IIEA20	13.056	–	–	IDBR1	12.206	–	–

(2) Output pins (4/4)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
IDBR0	12.673	–	–	TBO27	6.493	0.137	2.037
EVTTRG	13.238	–	–	TBO26	6.276	0.353	2.253
DCRESZ	13.071	–	–	TBO25	6.396	0.233	2.133
DCWAIT	12.844	–	–	TBO24	6.470	0.159	2.059
EXHLT	12.343	–	–	TBO23	6.575	0.055	1.955
DDOOUT	12.869	–	–	TBO22	6.484	0.145	2.045
DDOENB	12.829	–	–	TBO21	6.578	0.051	1.951
TAPSM3	12.942	–	–	TBO20	6.576	0.053	1.953
TAPSM2	12.851	–	–	TBO19	6.496	0.133	2.033
TAPSM1	12.885	–	–	TBO18	6.515	0.114	2.014
TAPSM0	12.857	–	–	TBO17	6.487	0.142	2.042
TRG1	12.976	–	–	TBO16	6.505	0.124	2.024
TRG0	12.610	–	–	TBO15	6.571	0.058	1.958
DBRESZ	13.149	–	–	TBO14	6.578	0.052	1.952
RESMK	13.316	–	–	TBO13	6.577	0.052	1.952
MSKSTP	13.011	–	–	TBO12	6.579	0.050	1.950
MSKNMI2	12.807	–	–	TBO11	6.581	0.048	1.948
MSKNMI1	12.691	–	–	TBO10	6.565	0.064	1.964
MSKNMI0	12.690	–	–	TBO9	6.576	0.053	1.953
MSKHRQ	13.274	–	–	TBO8	6.556	0.074	1.974
DBRDY	13.243	–	–	TBO7	6.571	0.058	1.958
EVIEN	13.192	–	–	TBO6	6.561	0.068	1.968
EVOEN	13.328	–	–	TBO5	6.561	0.068	1.968
EVINTRQ	13.324	–	–	TBO4	6.573	0.056	1.956
EVINTLV6	13.028	–	–	TBO3	6.561	0.068	1.968
EVINTLV5	12.762	–	–	TBO2	6.571	0.059	1.959
EVINTLV4	12.936	–	–	TBO1	6.566	0.063	1.963
EVINTLV3	13.012	–	–	TBO0	6.562	0.067	1.967
EVINTLV2	13.183	–	–	TESEN	13.064	–	–
EVINTLV1	13.252	–	–	VPTCLK	13.054	–	–
EVINTLV0	13.006	–	–	PHTDIN1	13.071	–	–
TBO34	6.581	0.048	1.948	PHTDIN0	13.071	–	–
TBO33	6.577	0.052	1.952	VPRESZ	13.304	–	–
TBO32	6.572	0.057	1.957	PHTEST	13.054	–	–
TBO31	6.569	0.060	1.960	TMODE1	12.802	–	–
TBO30	6.581	0.048	1.948	TMODE0	12.737	–	–
TBO29	6.576	0.053	1.953	TBREDZ	13.338	–	–
TBO28	6.578	0.051	1.951				

(3) I/O pins (1/2)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
VPD15	5.926	0.703	2.603	VBA4	5.515	1.161	3.061
VPD14	5.903	0.727	2.627	VBA3	5.472	1.204	3.104
VPD13	5.877	0.752	2.652	VBA2	5.492	1.184	3.084
VPD12	5.841	0.788	2.688	VBA1	5.833	0.842	2.742
VPD11	5.871	0.758	2.658	VBA0	5.772	0.903	2.803
VPD10	5.891	0.738	2.638	VBD31	5.156	1.520	3.420
VPD9	5.892	0.737	2.637	VBD30	5.261	1.414	3.314
VPD8	5.897	0.732	2.632	VBD29	5.218	1.457	3.357
VPD7	5.886	0.744	2.644	VBD28	5.245	1.431	3.331
VPD6	5.846	0.783	2.683	VBD27	4.763	1.913	3.813
VPD5	5.774	0.855	2.755	VBD26	4.889	1.786	3.686
VPD4	5.741	0.888	2.788	VBD25	5.085	1.591	3.491
VPD3	5.768	0.861	2.761	VBD24	5.168	1.508	3.408
VPD2	5.867	0.762	2.662	VBD23	5.204	1.471	3.371
VPD1	5.836	0.793	2.693	VBD22	5.135	1.541	3.441
VPD0	5.860	0.769	2.669	VBD21	4.962	1.714	3.614
VBA27	5.944	0.731	2.631	VBD20	4.982	1.694	3.594
VBA26	5.915	0.760	2.660	VBD19	4.801	1.875	3.775
VBA25	5.986	0.690	2.590	VBD18	4.973	1.703	3.603
VBA24	5.985	0.691	2.591	VBD17	5.199	1.477	3.377
VBA23	5.945	0.731	2.631	VBD16	4.879	1.797	3.697
VBA22	5.920	0.756	2.656	VBD15	3.517	1.607	3.507
VBA21	5.932	0.744	2.644	VBD14	3.581	1.542	3.442
VBA20	5.935	0.741	2.641	VBD13	4.948	1.775	3.675
VBA19	5.915	0.761	2.661	VBD12	5.215	1.507	3.407
VBA18	5.819	0.857	2.757	VBD11	4.863	1.860	3.760
VBA17	5.906	0.770	2.670	VBD10	3.578	1.546	3.446
VBA16	5.910	0.765	2.665	VBD9	3.435	1.688	3.588
VBA15	5.922	0.754	2.654	VBD8	3.500	1.624	3.524
VBA14	5.905	0.771	2.671	VBD7	4.892	1.831	3.731
VBA13	5.656	1.020	2.920	VBD6	3.637	1.487	3.387
VBA12	5.790	0.886	2.786	VBD5	3.535	1.588	3.488
VBA11	5.491	1.185	3.085	VBD4	3.528	1.596	3.496
VBA10	5.531	1.145	3.045	VBD3	4.727	1.996	3.896
VBA9	5.630	1.046	2.946	VBD2	3.492	1.631	3.531
VBA8	5.652	1.024	2.924	VBD1	3.463	1.661	3.561
VBA7	5.415	1.260	3.160	VBD0	4.814	1.909	3.809
VBA6	5.430	1.245	3.145	VBTTYP1	5.956	0.719	2.619
VBA5	5.438	1.238	3.138	VBTTYP0	5.982	0.694	2.594

(3) I/O pins (2/2)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
VBSTZ	5.750	0.925	2.825	IDED20	5.929	0.700	2.600
VBBENZ3	5.984	0.691	2.591	IDED19	5.956	0.673	2.573
VBBENZ2	6.001	0.674	2.574	IDED18	5.987	0.642	2.542
VBBENZ1	5.847	0.829	2.729	IDED17	5.940	0.689	2.589
VBBENZ0	6.006	0.670	2.570	IDED16	5.895	0.734	2.634
VBSIZE1	5.884	0.792	2.692	IDED15	5.884	0.745	2.645
VBSIZE0	5.898	0.778	2.678	IDED14	5.876	0.753	2.653
VBWRITE	5.725	0.950	2.850	IDED13	5.998	0.631	2.531
VBLOCK	5.820	0.856	2.756	IDED12	5.937	0.692	2.592
VBCTYP2	5.904	0.771	2.671	IDED11	5.915	0.714	2.614
VBCTYP1	5.955	0.721	2.621	IDED10	5.923	0.706	2.606
VBCTYP0	5.941	0.735	2.635	IDED9	5.891	0.739	2.639
VBSEQ2	5.952	0.724	2.624	IDED8	5.917	0.713	2.613
VBSEQ1	5.957	0.719	2.619	IDED7	5.985	0.645	2.545
VBSEQ0	5.971	0.704	2.604	IDED6	6.021	0.608	2.508
VBBSTR	5.972	0.704	2.604	IDED5	5.828	0.801	2.701
VBWAIT	4.961	1.715	3.615	IDED4	5.858	0.771	2.671
VBLAST	5.842	0.834	2.734	IDED3	5.901	0.729	2.629
VBAHLD	5.771	0.905	2.805	IDED2	6.034	0.595	2.495
VDCSZ7	6.017	0.659	2.559	IDED1	6.031	0.598	2.498
VDCSZ6	6.044	0.632	2.532	IDED0	5.928	0.701	2.601
VDCSZ5	6.015	0.661	2.561	EVAD15	5.875	0.754	2.654
VDCSZ4	6.020	0.656	2.556	EVAD14	5.905	0.724	2.624
VDCSZ3	6.036	0.640	2.540	EVAD13	5.818	0.811	2.711
VDCSZ2	6.017	0.659	2.559	EVAD12	5.849	0.780	2.680
VDCSZ1	5.983	0.693	2.593	EVAD11	5.830	0.799	2.699
VDCSZ0	6.036	0.640	2.540	EVAD10	5.827	0.802	2.702
VDSELPZ	5.599	1.077	2.977	EVAD9	5.821	0.808	2.708
IDED31	5.888	0.742	2.642	EVAD8	5.783	0.846	2.746
IDED30	5.862	0.767	2.667	EVAD7	5.772	0.857	2.757
IDED29	5.927	0.702	2.602	EVAD6	5.814	0.815	2.715
IDED28	5.964	0.666	2.566	EVAD5	5.849	0.780	2.680
IDED27	5.944	0.685	2.585	EVAD4	5.747	0.882	2.782
IDED26	5.907	0.723	2.623	EVAD3	5.850	0.779	2.679
IDED25	5.896	0.733	2.633	EVAD2	5.845	0.784	2.684
IDED24	5.928	0.701	2.601	EVAD1	5.828	0.801	2.701
IDED23	5.944	0.686	2.586	EVAD0	5.820	0.809	2.709
IDED22	5.898	0.731	2.631	EVLKRT	5.981	0.648	2.548
IDED21	5.973	0.656	2.556				

9. 2 Initialization of Internal Registers

Before executing the test program, be sure to execute an instruction to assign initial values to the internal registers used in test program execution. Failure to do this will result in the propagation of undefined values.

9. 3 Pin Functions

(1/5)

Pin Name		I/O	Function
NPB pins	VPA13 to VPA0	Output	Address output for peripheral macro connected to NPB
	VPD15 to VPD0[Note]	I/O	Data I/O for peripheral macro connected to NPB
	VPWRITE	Output	Write access strobe output of signals VPD15 to VPD0
	VPSTB	Output	Data strobe output of signals VPD15 to VPD0
	VPLOCK	Output	Bus lock output
	VPUBENZ	Output	Upper byte enable output
	VPRETR[Note]	Input	Retry request input from peripheral macro connected to NPB
	VPDACT	Input	Retry function control input
VSB pins	VAREQ	Input	Bus access right request input
	VAACK	Output	Bus access right acknowledge output
	VBA27 to VBA0[Note]	I/O	Address I/O for peripheral macro connected to VSB
	VBD31 to VBD0[Note]	I/O	Data I/O for peripheral macro connected to VSB
	VBTTYP1, VBTTYP0[Note]	I/O	Bus transfer type I/O
	VBSTZ[Note]	I/O	Transfer start I/O
	VBBENZ3 to VBBENZ0[Note]	I/O	Byte enable I/O
	VBSIZE1, VBSIZE0[Note]	I/O	Transfer size I/O
	VBWRITE[Note]	I/O	Read/write status I/O
	VBLOCK[Note]	I/O	Bus lock I/O
	VBCTYP2 to VBCTYP0[Note]	I/O	Bus cycle status I/O
	VBSEQ2 to VBSEQ0[Note]	I/O	Sequential status I/O
	VBBSTR[Note]	I/O	Burst read status I/O
	VBWAIT[Note]	I/O	Wait response I/O
	VBLAST[Note]	I/O	Last response I/O
	VBAHLD[Note]	I/O	Address hold response I/O
	VBDC	Output	Data bus direction control output
	VDCSZ7 to VDCSZ0[Note]	I/O	Chip select I/O
	VDSELPZ[Note]	I/O	Peripheral I/O area access status I/O
System control pins	RESETZ	Input	System reset input
	VBCLK	Input	Internal system clock input
	CLKB1	Output	Internal system clock output
	CGREL	Input	Clock generator release input
	SWSTOPRQ	Output	Software STOP mode request output to clock generator
	HWSTOPRQ	Output	Hardware STOP mode request output to clock generator
	STOPZ	Input	Hardware STOP mode request input
	STPRQ	Output	Hardware/software STOP mode request output to MEMC
	STPAK	Input	Acknowledge input for input of STPRQ of MEMC

Note Connected internally to the bus holder.

(2/5)

Pin Name		I/O	Function
DMAC pins	IDMASTP	Input	DMA transfer terminate input
	DMARQ3 to DMARQ0	Input	DMA transfer request input
	DMTCO3 to DMTCO0	Output	Terminal count (DMA transfer completed) output
	DMACTV3 to DMACTV0	Output	DMA acknowledge output
INTC pins	NMI2 to NMI0	Input	Non-maskable interrupt request (NMI) input
	INT63 to INT0	Input	Maskable interrupt request input
VFB pins	IROMA19 to IROMA2	Output	Address output for ROM
	IROMZ31 to IROMZ0	Input	Data input for ROM
	IROMEN	Output	Access enable output for ROM
	IROMWT	Input	Wait input for ROM
	IROMCS	Output	NEC reserved pin (leave open)
	IROMIA	Output	
	IROMAE	Output	
VDB pins	IRAMA27 to IRAMA2	Output	Address output for RAM
	IRAMZ31 to IRAMZ0	Input	Data input for RAM
	IRAOZ31 to IRAOZ0	Output	Data output for RAM
	IRAMEN	Output	Access enable output for RAM
	IRAMWR3 to IRAMWR0	Output	Write enable output for RAM
	IRAMRWB	Output	Read/write status output for RAM
	IRAMWT	Input	Wait input for RAM
Instruction cache pins	IBDRRQ	Input	Fetch request input from instruction cache
	IBEA25 to IBEA2	Input	Fetch address input from instruction cache
	IBAACK	Output	Address acknowledge output to instruction cache
	IBDRDY	Output	Data ready output to instruction cache
	IBDLE3 to IBDLE0	Output	Data latch enable output to instruction cache
	IBEDI31 to IBEDI0	Output	Data output to instruction cache
	IIDRRQ	Output	Fetch request output to instruction cache
	IIEA25 to IIEA2	Output	Fetch address output to instruction cache
	IIAACK	Input	Address acknowledge input from instruction cache
	IIDLEF	Input	Data latch enable input from instruction cache
	IIEDI31 to IIEDI0	Input	Data input from instruction cache
	IIBTFT	Output	Branch target fetch status output to instruction cache
	IIRCAN	Output	Code cancel status output to instruction cache
	BCUNCH	Output	Uncache status output to instruction cache
	IBBTFT	Input	NEC reserved pin (input a low level)

(3/5)

Pin Name		I/O	Function
Data cache pins	IDDARQ	Output	Read/write access request output to data cache
	IDAACK	Output	Acknowledge output
	IDDRRQ	Input	VSB read operation request input to BCU
	IDDWRQ	Input	VSB write operation request input to BCU
	IDSEQ4	Input	Read/write operation type setting input
	IDSEQ2	Input	Read/write operation type setting input
	IRRSA	Output	VDB hold status output
	IDRETR	Output	Read retry request output
	IDUNCH	Output	Uncache status output
	IDDRDY	Output	Read data ready output
	IDRRDY	Input	Read data ready input from data cache
	IDHUM	Input	Hit under miss-hit read input
	IDEA27 to IDEA0	Input	Address input
	IDED31 to IDED0[Note 1]	I/O	Data I/O
	IDES	Output	NEC reserved pin[Note 2]
External INTC pins	EINTLV6 to EINTLV0	Input	Interrupt type input from external INTC
	EINTRQ	Input	Interrupt request input from external INTC
	EINTAK	Output	Interrupt acknowledge output to external INTC
	ECLRIP	Output	Interrupt servicing end output to external INTC
DCU pins	DCK	Input	Clock input for DCU
	DMS	Input	Debug mode selection input
	DDI	Input	Debug data input
	DDO	Output	Debug data output
	DRSTZ	Input	Reset input for DCU
	TRCCLK	Output	Trace clock output
	TRCDATA3 to TRCDATA0	Output	Trace data output
	TRCEND	Output	Trace processing end output
	IDBR2 to IDBR0	Output	Debug mode output
	EVTTRG	Output	Event trigger output
	DCRESZ	Output	Forcible reset output
	MWAIT	Input	Wait insertion control input
	DCWAIT	Output	Wait insertion control output
	EXHLT	Output	HALT mode status output

Notes 1. Connected internally to the bus holder.

2. When using the data cache, always connect this pin to the IDES pin of the data cache. Leave open when unused.

(4/5)

Pin Name		I/O	Function
DCU pins	DBINT	Input	External debug interrupt input
	ROMTYPE	Input	NEC reserved pin (input a low level)
	DDOOUT	Output	NEC reserved pin (leave open)
	DDOENB	Output	
	TAPSM3 to TAPSM0	Output	
	TRG1, TRG0	Output	
	DBRESZ	Output	
	RESMK	Output	
	MSKSTP	Output	
	MSKNMI2 to MSKNMI0	Output	
	MSKHRQ	Output	
	DBRDY	Output	
Peripheral EVA chip mode pins	EVASTB	Input	Address strobe input
	EVDSTB	Input	Data strobe input
	EVAD15 to EVAD0[Note]	I/O	Address/data I/O
	EVIEN	Output	EVADn input enable output (n = 15 to 0)
	EVOEN	Output	EVADn output enable output (n = 15 to 0)
	EVLKRT[Note]	I/O	Lock/retry I/O
	EVIREL	Input	Standby release input
	EVCLRIP	Input	ISPR clear input
	EVINTAK	Input	Interrupt acknowledge input
	EVINTRQ	Output	Interrupt request output
	EVINTLV6 to EVINTLV0	Output	Interrupt vector output
Operation mode setting pins	IFIROME	Input	ROM mapping enable input
	IFIROB2	Input	Location setting input of ROM area
	IFIRA64	Input	RAM area size selection input
	IFIRA32	Input	RAM area size selection input
	IFIRA16	Input	RAM area size selection input
	IFIMAEN	Input	Misalign access setting input
	IFID256	Input	Data area setting input
	IFINSZ1, IFINSZ0	Input	VSB data bus size selection input
	IFIWRTH	Input	Data cache write-back/write-through mode selection input

Note Connected internally to the bus holder.

(5/5)

Pin Name		I/O	Function
Operation mode setting pins	IFIUNCH1	Input	Data cache setting input
	IFIUNCH0	Input	Instruction cache setting input
	PHEVA	Input	Peripheral EVA chip mode setting input
	IFIEVA	Input	External INTC/internal INTC selection input
	IFIMODE2	Input	NEC reserved pin (input a low level)
	IFIROBE	Input	
	IFIROPR	Input	
	IFIRASE	Input	
	IFIRABE	Input	
	IFIMODE3	Input	
	IFIUSWE	Input	
	FCOMB	Input	
Test mode pins	TBI39 to TBI0	Input	Input test bus
	TBO34 to TBO0	Output	Output test bus
	TEST	Input	Test bus control input
	BUNRI	Input	Normal/test mode selection input
	PHTDO1, PHTDO0[Note]	Input	Peripheral macro test input
	TESEN	Output	Peripheral macro test enable output
	VPTCLK	Output	Clock output for peripheral macro test
	PHTDIN1, PHTDIN0	Output	Peripheral macro test output
	VPRESZ	Output	Peripheral macro reset output
	PHTEST	Output	Peripheral test mode status output
	TMODE1, TMODE0	Output	NEC reserved pin (leave open)
	TBREDZ	Output	

Note Connected internally to the bus holder.

9. 4 Electrical Specifications (Preliminary)

The following specifications are for a single macro. An actual chip consists of two or more macros. Design the system so that all the specifications of the individual macros are satisfied when the chip is used.

9. 4. 1 Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to +4.6	V
Operating ambient temperature	T_A	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

9. 4. 2 Recommended operation range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	−40		+85	°C
★ Clock cycle	t_{CYK}	20.0			ns

9. 4. 3 DC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

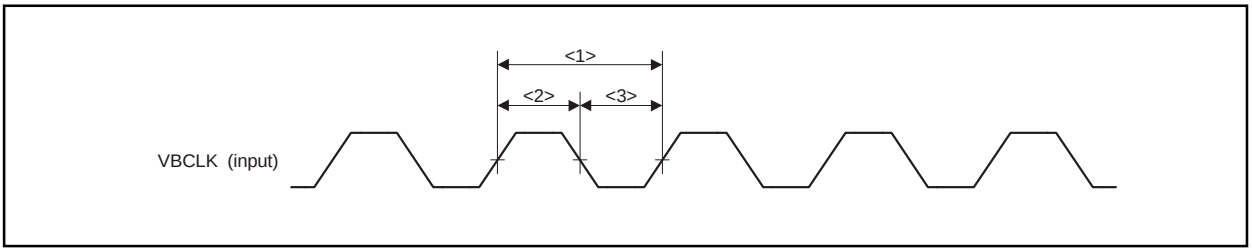
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1}	In normal operation mode		0.5	0.6	mA/MHz
	I_{DD2}	In HALT mode (when DMAC is not operating)		0.17	0.2	mA/MHz
	I_{DD3}	In STOP mode		0	1.0	μA

Remark The TYP. value is a reference value for when T_A = 25°C, V_{DD} = 3.3 V.

9. 4. 4 AC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

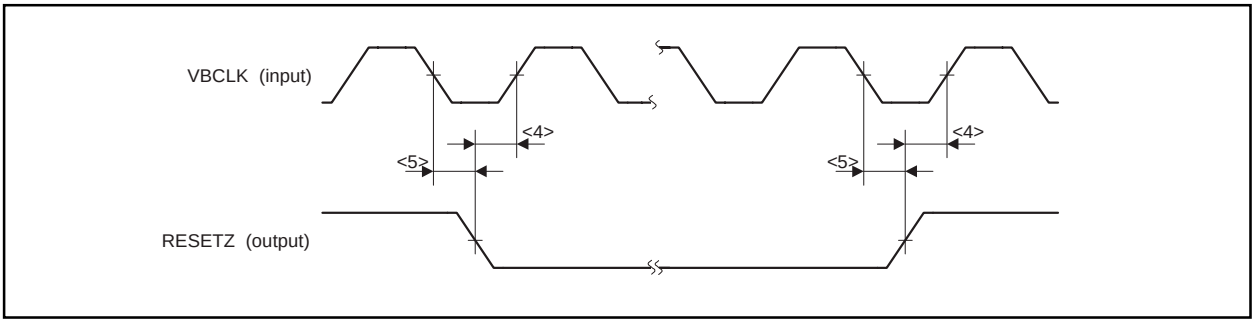
(1) Clock timing

	Parameter	Symbol		Conditions	MIN.	MAX.	Unit
★	VBCLK input cycle	<1>	t_{CYK}		20.0		ns
★	VBCLK input high-level width	<2>	t_{KKH}		10.0		ns
★	VBCLK input low-level width	<3>	t_{KKL}		10.0		ns
	CPU operating frequency	–	ϕ		0	50	MHz



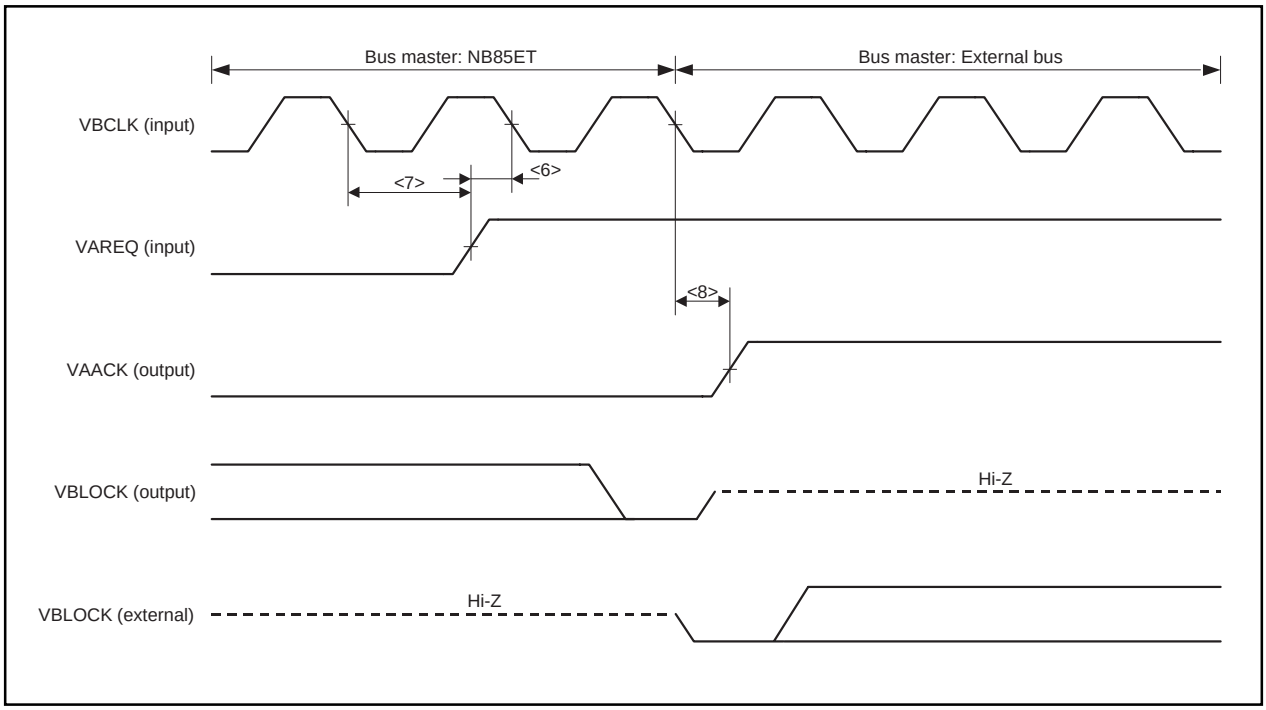
(2) Reset timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
RESETZ setup time (to VBCLK↑)	<4>	t_{SKR}		2.3		ns
RESETZ hold time (from VBCLK↓)	<5>	t_{HKR}		1.9		ns
Delay time from RESETZ to VPRESZ	–	t_{DRPR}		0.9	3.2	ns



(3) VSB arbitration timing

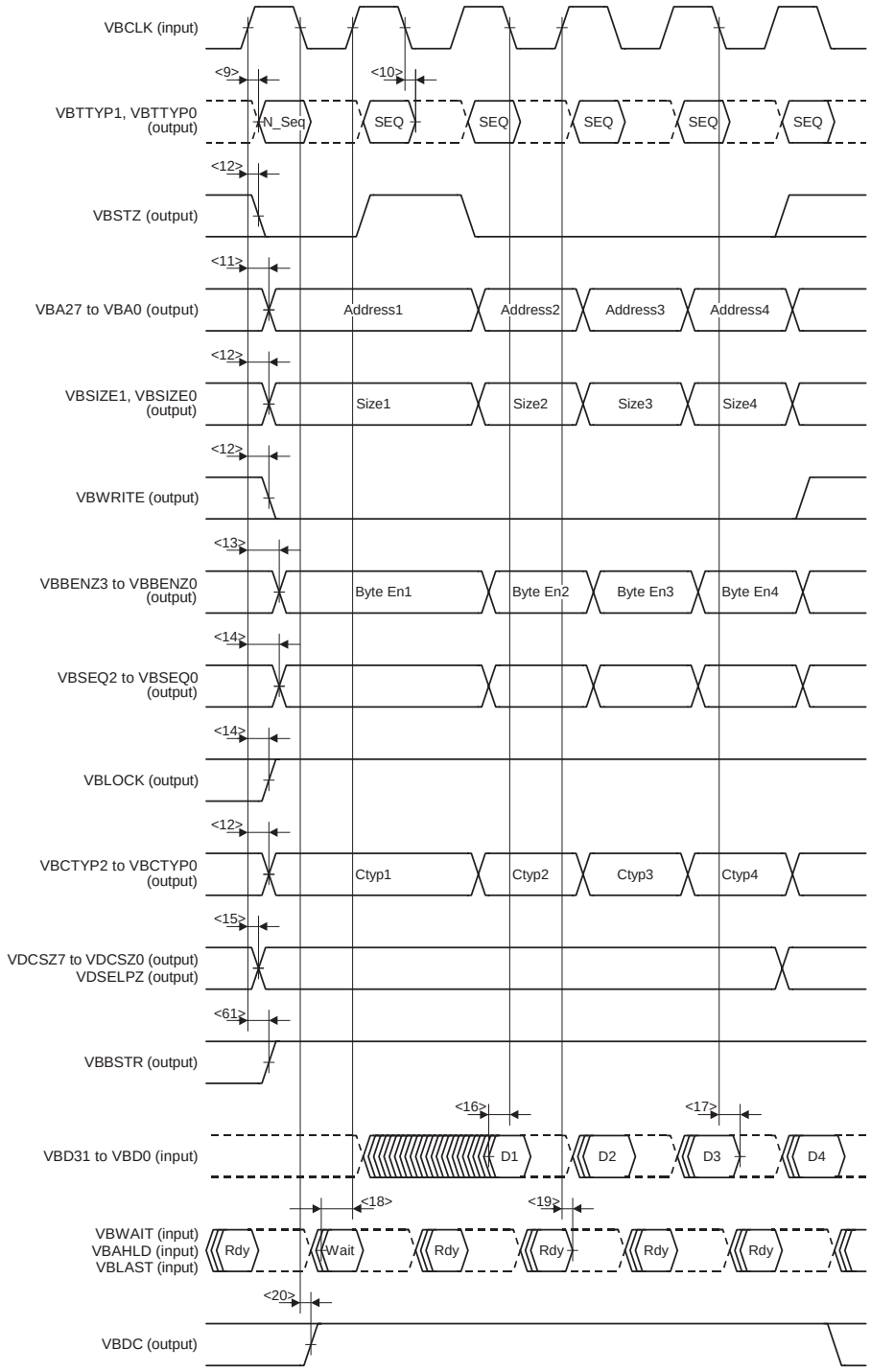
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VAREQ setup time (to VBCLK↓)	<6>	t_{SKQ}		0		ns
VAREQ hold time (from VBCLK↓)	<7>	t_{HKQ}		3.4		ns
Delay time from VBCLK↓ to VAACK	<8>	t_{DKK}		2.0	5.4	ns



(4) VSB master read timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to VBTTYP	<9>	t_{DKT}		1.8	7.0	ns
VBTTYP hold time (from VBCLK↓)	<10>	t_{HKT}		3.2		ns
Delay time from VBCLK↑ to VBA	<11>	t_{DKA}		2.0	7.8	ns
Delay time from VBCLK↑ to VBSTZ, VBSIZE, VBWRITE, VBCTYP	<12>	t_{DKS1}		2.1	7.4	ns
Delay time from VBCLK↑ to VBBENZ	<13>	t_{DKS2}		2.2	8.7	ns
Delay time from VBCLK↑ to VBSEQ, VBLOCK	<14>	t_{DKS3}		2.3	8.2	ns
Delay time from VBCLK↑ to VDCSZ, VDSELPZ	<15>	t_{DKC}		2.3	8.0	ns
Delay time from VBCLK↑ to VBBSTR	<61>	t_{DKBSR}		2.1	6.6	ns
VBD data setup time (to VBCLK↓)	<16>	t_{SKD}		0		ns
VBD data hold time (from VBCLK↓)	<17>	t_{HKD}		2.8		ns
VBWAIT, VBAHLD, VBLAST setup time (to VBCLK↑)	<18>	t_{SKW}		0.6		ns
VBWAIT, VBAHLD, VBLAST hold time (from VBCLK↑)	<19>	t_{HKW}		3.5		ns
Delay time from VBCLK↓ to VBDC	<20>	t_{DKS4}		2.2	6.1	ns

(4) VSB master read timing (2/2)



Remarks 1. The level of the broken line portion indicates the undefined state (weak unknown) in which the bus holder in the NB85ET is driving.

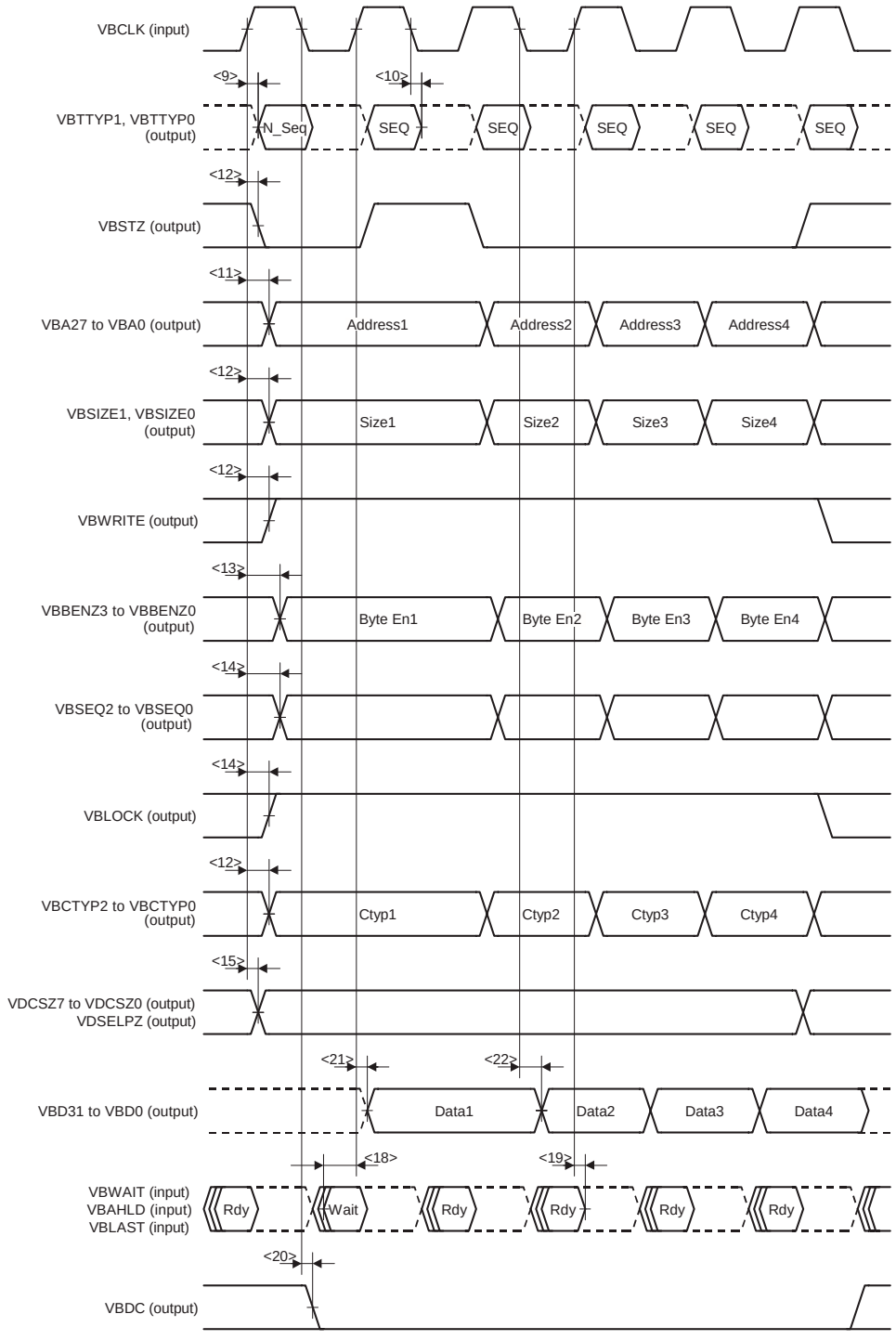
2. Rdy: When the VBWAIT, VBAHLD, and VBLAST signals are all low level

Wait: When the VBWAIT signal is high level, and the VBAHLD and VBLAST signals are low level

(5) VSB master write timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to VBTTYP	<9>	t_{DKT}		1.8	7.0	ns
VBTTYP hold time (from VBCLK↓)	<10>	t_{HKT}		3.2		ns
Delay time from VBCLK↑ to VBA	<11>	t_{DKA}		2.0	8.0	ns
Delay time from VBCLK↑ to VBSTZ, VBSIZE, VBWRITE, VBCTYP	<12>	t_{DKS1}		2.1	7.4	ns
Delay time from VBCLK↑ to VBBENZ	<13>	t_{DKS2}		2.2	8.7	ns
Delay time from VBCLK↑ to VBSEQ, VBLOCK	<14>	t_{DKS3}		2.3	8.2	ns
Delay time from VBCLK↑ to VDCSZ, VDSELPZ	<15>	t_{DKC}		2.3	8.0	ns
VBWAIT, VBAHLD, VBLAST setup time (to VBCLK↑)	<18>	t_{SKW}		0.6		ns
VBWAIT, VBAHLD, VBLAST hold time (from VBCLK↑)	<19>	t_{HKW}		3.5		ns
Delay time from VBCLK↓ to VBDC	<20>	t_{DKS4}		2.2	6.2	ns
Delay time from VBCLK↑ to VBD data	<21>	t_{DKD0}		1.9	6.3	ns
Delay time from VBCLK↓	<22>	t_{DKD1}		2.1	7.1	ns

(5) VSB master write timing (2/2)



Remarks 1. The level of the broken line portion indicates the undefined state (weak unknown) in which the bus holder in the NB85ET is driving.

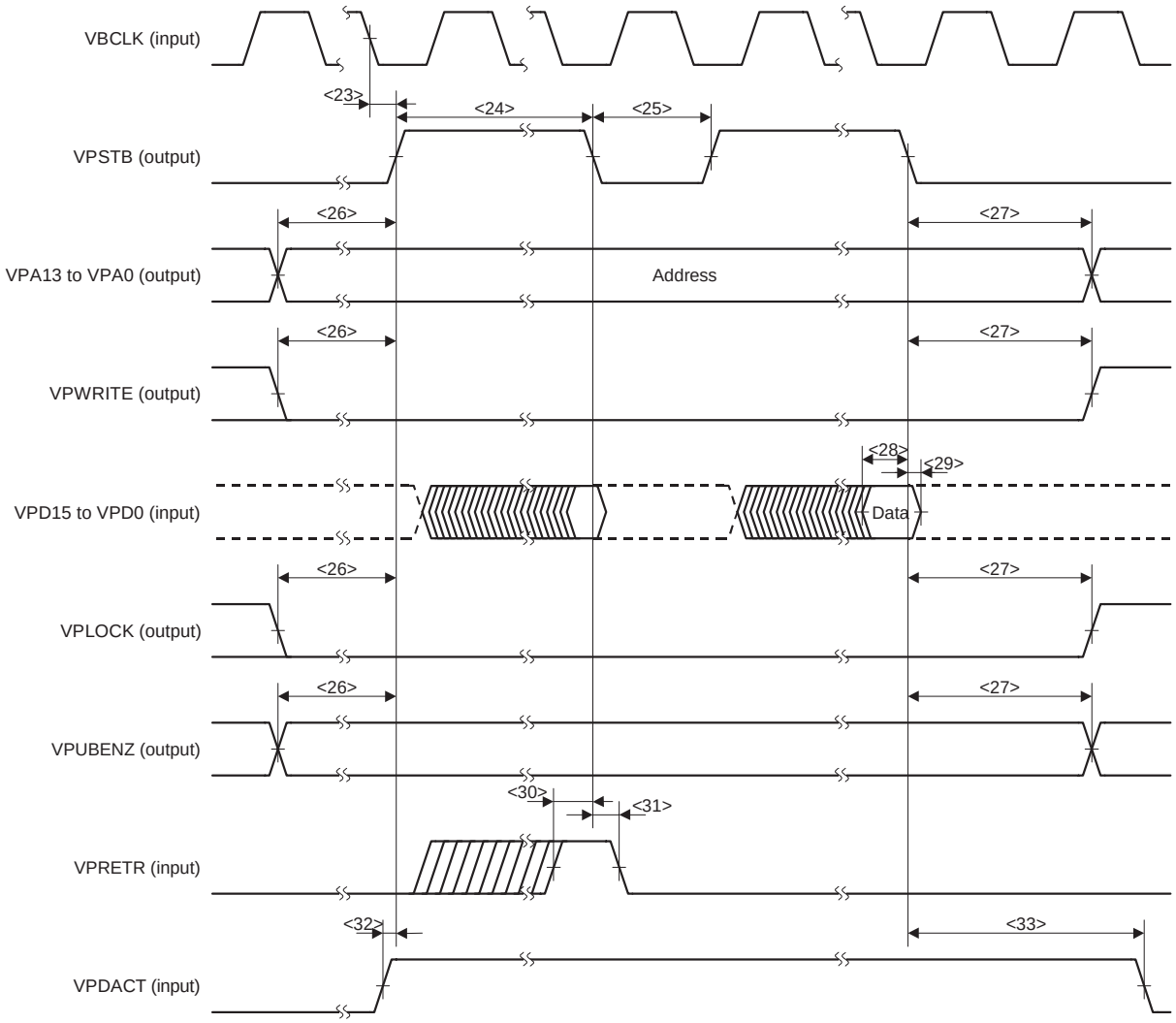
2. Rdy: When the VBWAIT, VBAHLD, and VBLAST signals are all low level

Wait: When the VBWAIT signal is high level, and the VBAHLD and VBLAST signals are low level

(6) NPB read timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↓ to VPSTB	<23>	t_{DKP}		2.4	7.1	ns
VPSTB output high-level width	<24>	t_{SSH}		60		ns
VPSTB output low-level width	<25>	t_{SSL}		20		ns
VPA address, VPWRITE, VPLOCK, VPUBENZ setup time (to VPSTB↑)	<26>	t_{SSA}		20		ns
VPA address, VPWRITE, VPLOCK, VPUBENZ hold time (from VPSTB↓)	<27>	t_{HSA}		20		ns
VPD read data setup time (to VPSTB↓)	<28>	t_{SSD}		20		ns
VPD read data hold time (from VPSTB↓)	<29>	t_{HSD}		0		ns
VPRETR setup time (to VPSTB↓)	<30>	t_{SSR}		20		ns
VPRETR hold time (from VPSTB↓)	<31>	t_{HSR}		0		ns
VPDACT setup time (to VPSTB↑)	<32>	t_{SSC}		20		ns
VPDACT hold time (from VPSTB↓)	<33>	t_{HSC}		20		ns

(6) NPB read timing (2/2)

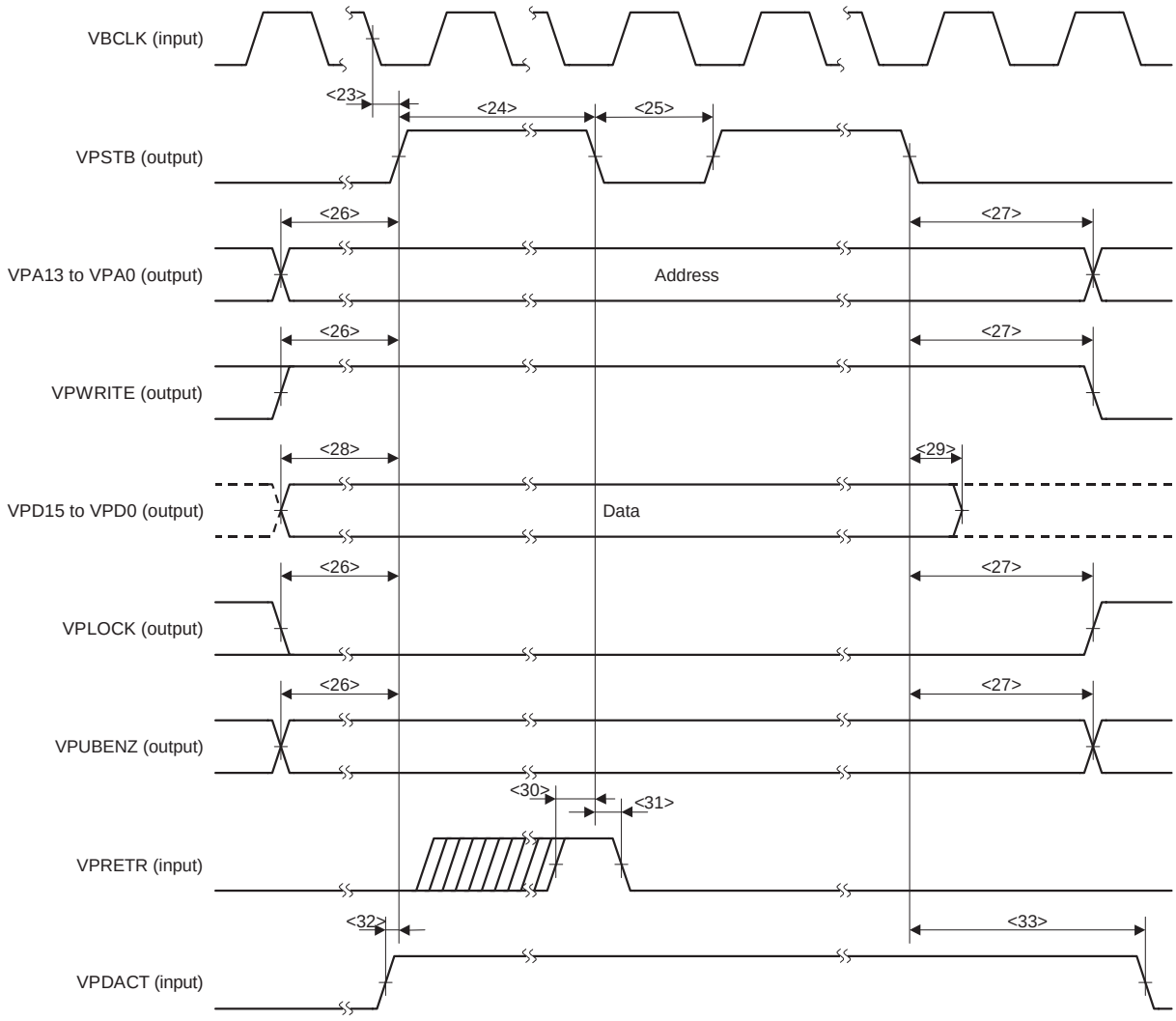


Remark The level of the broken line portion indicates the undefined state (weak unknown) in which the bus holder in the NB85ET is driving.

(7) NPB write timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↓ to VPSTB	<23>	t_{DKP}		2.4	7.1	ns
VPSTB output high-level width	<24>	t_{SSH}		60		ns
VPSTB output low-level width	<25>	t_{SSL}		20		ns
VPA address, VPWRITE, VPLOCK, VPUBENZ setup time (to VPSTB↑)	<26>	t_{SSA}		20		ns
VPA address, VPWRITE, VPLOCK, VPUBENZ hold time (from VPSTB↓)	<27>	t_{HSA}		20		ns
VPD write data setup time (to VPSTB↑)	<28>	t_{SSD}		20		ns
VPD write data hold time (from VPSTB↓)	<29>	t_{HSD}		20		ns
VPRETR setup time (to VPSTB↓)	<30>	t_{SSR}		20		ns
VPRETR hold time (from VPSTB↓)	<31>	t_{HSR}		0		ns
VPDACT setup time (to VPSTB↑)	<32>	t_{SSC}		20		ns
VPDACT hold time (from VPSTB↓)	<33>	t_{HSC}		20		ns

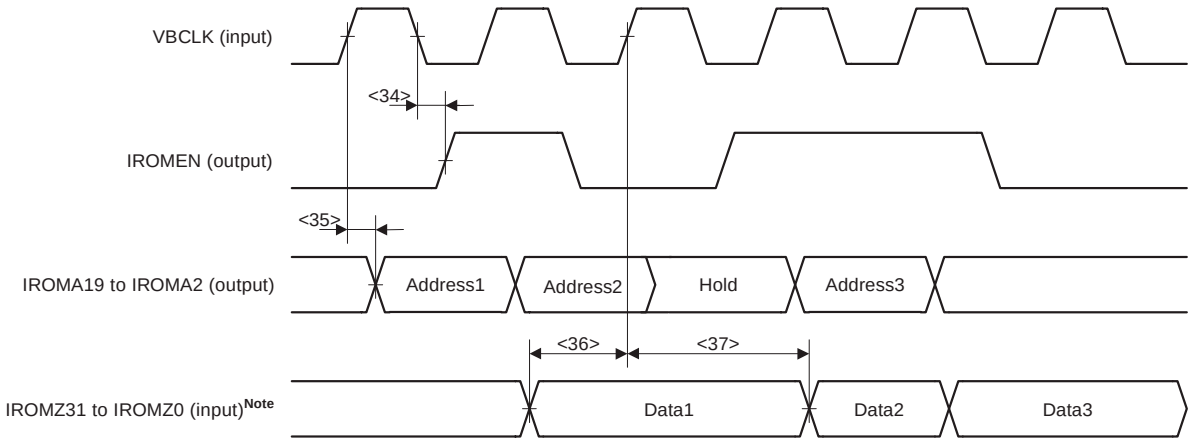
(7) NPB write timing (2/2)



Remark The level of the broken line portion indicates the undefined state (weak unknown) in which the bus holder in the NB85ET is driving.

(8) VFB access timing

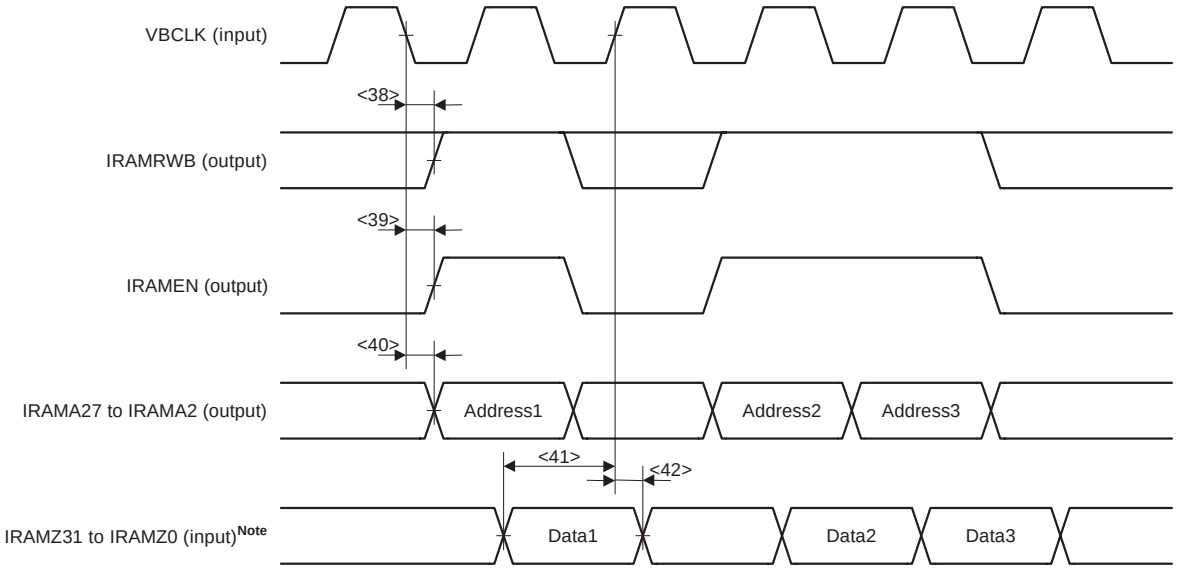
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↓ to IROMEN	<34>	t_{DKROE}		2.5	9.1	ns
Delay time from VBCLK↑ to IROMA	<35>	t_{DKROA}		2.6	13.7	ns
IROMZ setup time (to VBCLK↑)	<36>	t_{SKROZ}		3.3		ns
IROMZ hold time (from VBCLK↑)	<37>	t_{HKROZ}		3.2		ns



★ **Note** Hold data during the IROMEN signal is low level.

(9) VDB read timing

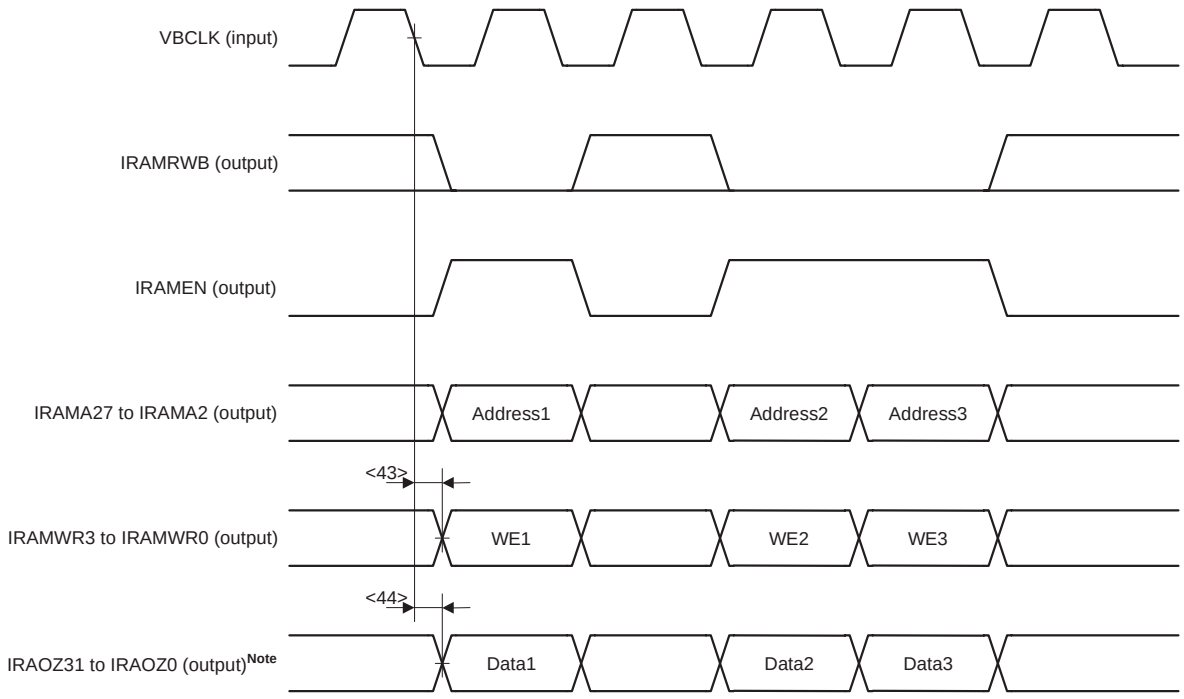
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↓ to IRAMRWB	<38>	t_{DKRAR}		2.5	9.7	ns
Delay time from VBCLK↓ to IRAMEN	<39>	t_{DKRAE}		2.2	10.4	ns
Delay time from VBCLK↓ to IRAMA	<40>	t_{DKRAA}		2.7	10.2	ns
IRAMZ setup time (to VBCLK↑)	<41>	t_{SKRAZ}		4.6		ns
IRAMZ hold time (from VBCLK↑)	<42>	t_{HKRAZ}		3.8		ns



Note Do not make signals IRAMZ31 to IRAMZ0 high impedance.

(10) VDB write timing

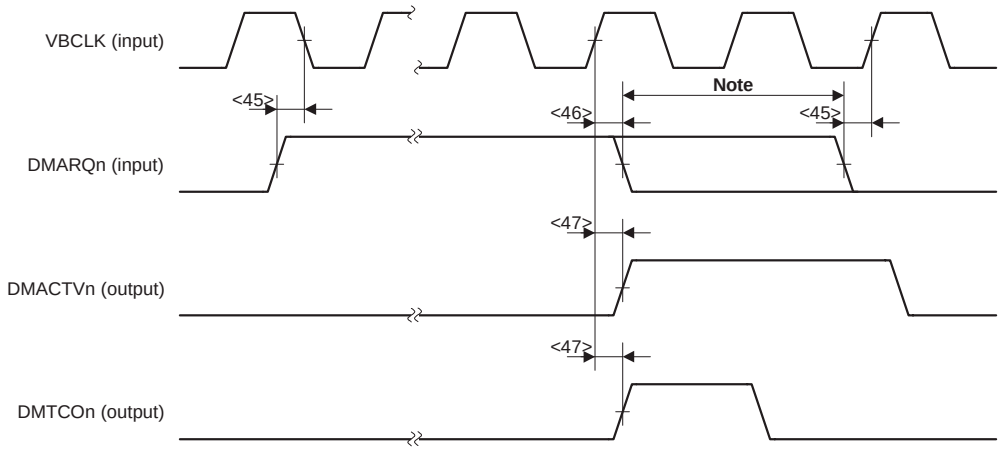
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↓ to IRAMWR	<43>	t_{DKRAW}		2.6	10.2	ns
Delay time from VBCLK↓ to IRAOZ	<44>	t_{DKRAZ}		2.5	10.2	ns



Note Signals IRAOZ31 to IRAOZ0 are always output and do not become high impedance.
Write operations are controlled by the IRAMEN signal and signals IRAMWR3 to IRAMWR0. Data cannot be written when the IRAMEN signal is low level.

(11) DMA transfer request, transfer completion timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
DMARQ setup time (to VBCLK↓)	<45>	t_{SKDQ}		0		ns
DMARQ hold time (from VBCLK↑)	<46>	t_{HKDQ}		2.3		ns
Delay time from VBCLK↑ to DMACTV, DMTCO	<47>	t_{DKDC}		2.1	6.5	ns

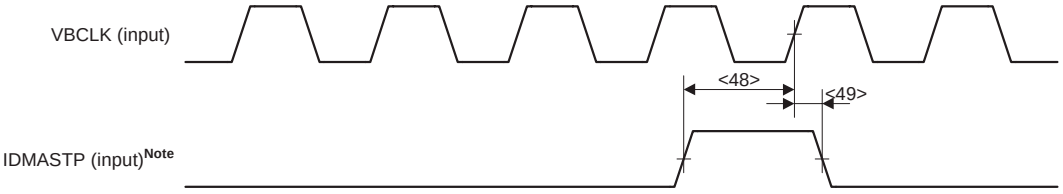


Note In order to avoid the generation of the next cycle, make the DMARQn signal low level in this cycle.

Remark n = 3 to 0

(12) DMA transfer abort timing

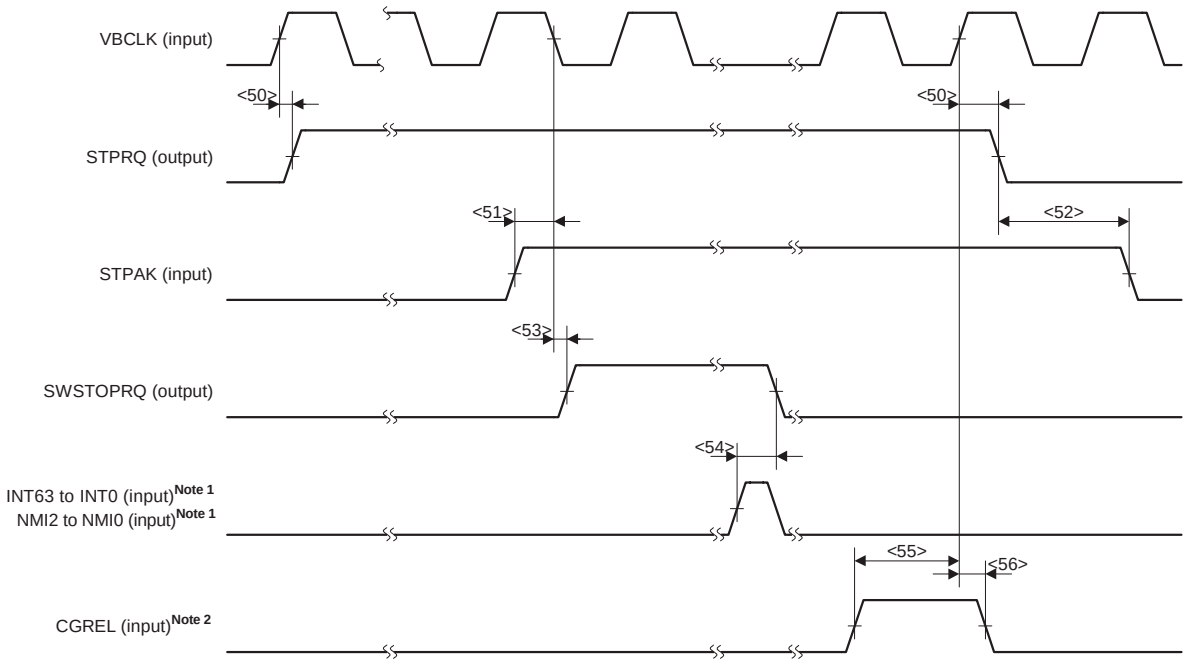
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
IDMASTP setup time (to VBCLK↑)	<48>	t_{SKDS}		3.5		ns
IDMASTP hold time (from VBCLK↑)	<49>	t_{HKDS}		2.9		ns



Note Input an active level (high level) of 1 clock or more.

(13) Software STOP mode timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to STPRQ	<50>	t_{DKSQ}		2.2	6.1	ns
STPAK setup time (to VBCLK↓)	<51>	t_{SKSA}		1.0		ns
STPAK hold time (from STPRQ↓)	<52>	t_{HQSA}		9.6		ns
Delay time from VBCLK↓ to SWSTOPRQ↑	<53>	t_{DKSS}		2.1	5.7	ns
Delay time from INT, NMI to SWSTOPRQ↓	<54>	t_{DRSR}		0	20.8	ns
CGREL setup time (to VBCLK↑)	<55>	t_{SKSG}		0		ns
CGREL hold time (from VBCLK↑)	<56>	t_{HKSG}		3.2		ns

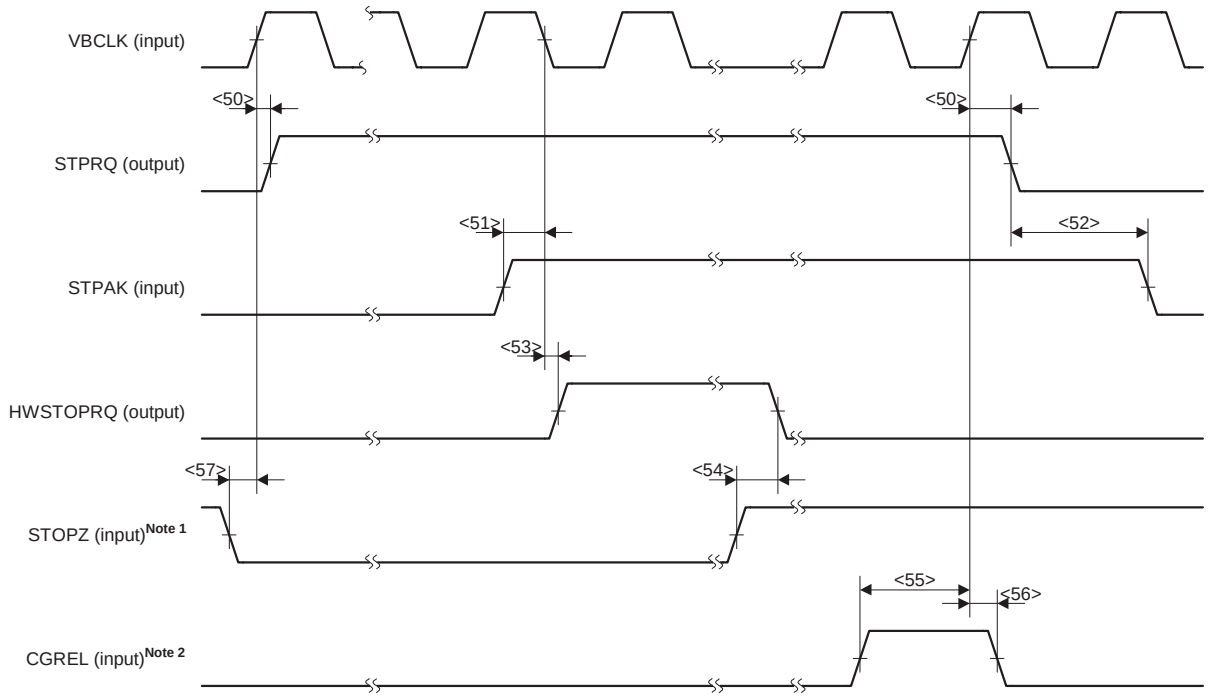


Notes 1. Software STOP mode is released upon detection of the rising edge of these signals.

2. Input an active level (high level) of 1 clock or more.

(14) Hardware STOP mode timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to STPRQ	<50>	t_{DKSQ}		2.2	6.1	ns
STPAK setup time (to VBCLK↓)	<51>	t_{SKSA}		1.0		ns
STPAK hold time (from STPRQ↓)	<52>	t_{HQSA}		9.6		ns
Delay time from VBCLK↓ to HWSTOPRQ↑	<53>	t_{DKSS}		2.2	5.9	ns
Delay time from STOPZ to HWSTOPRQ↓	<54>	t_{DRSR}		0	20.8	ns
CGREL setup time (to VBCLK↑)	<55>	t_{SKSG}		0		ns
CGREL hold time (from VBCLK↑)	<56>	t_{HKSG}		3.2		ns
STOPZ setup time (to VBCLK↑)	<57>	t_{SKST}		0		ns

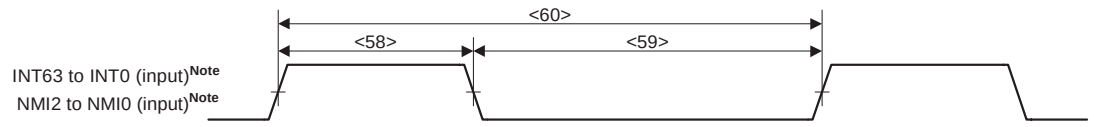


Notes 1. Hardware STOP mode is released upon detection of the rising edge of this signal.

2. Input an active level (high level) of 1 clock or more.

(15) Interrupt timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
INT, NMI high-level width	<58>	t_{WIH}		5.0		ns
INT, NMI low-level width	<59>	t_{WIL}		5.0		ns
INT, NMI interval time	<60>	t_{CYI}		$3 \times t_{CYK}$		ns

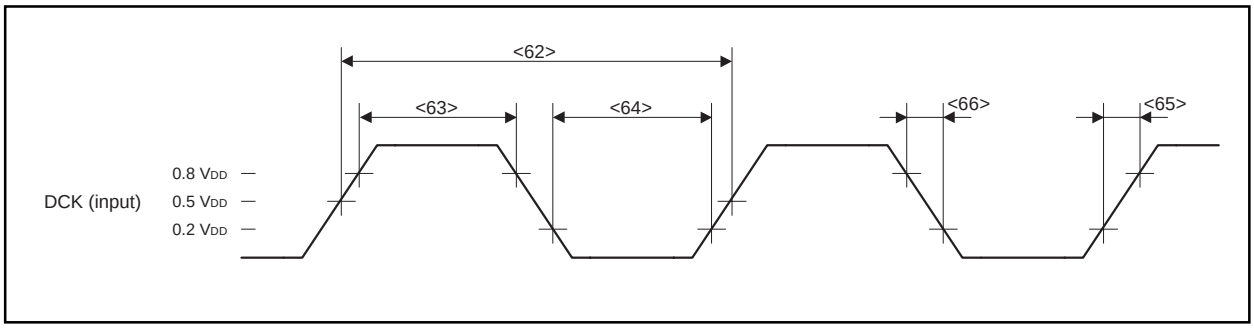


Note An interrupt is generated upon detection of the rising edge of these signals.

(16) DCU timing

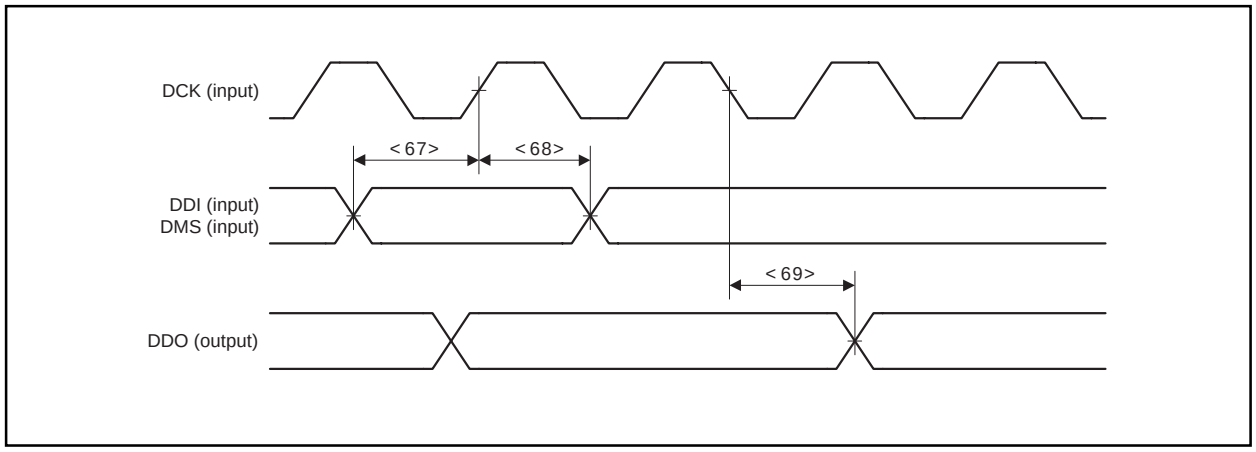
(a) DCK input timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
DCK input cycle	<62>	t_{CYD}		30.0		ns
DCK input high-level width	<63>	t_{DDH}		10.0		ns
DCK input low-level width	<64>	t_{DDL}		10.0		ns
DCK rise time	<65>	t_{DR}			5.0	ns
DCK fall time	<66>	t_{DF}			5.0	ns



(b) DDI, DMS, DDO timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
DDI, DMS setup time (to DCK↑)	<67>	t_{SDTD}		7.0		ns
DDI, DMS hold time (from DCK↑)	<68>	t_{HDDT}		3.0		ns
Delay time from DCK↓ to DDO	<69>	t_{DDDT}		2.0	10.0	ns



CHAPTER 10 NB85E500

(Under Development)

The NB85E500 is used as follows according to the type of external memory that is connected.

Target CPU Core	Types of Connected External Memory	Memory Controller (MEMC)
NB85E, NB85ET	SRAM, ROM, page ROM, flash memory	NB85E500
	SDRAM	NB85E500 + NU85E502

Remark For details of the NU85E502, refer to **CHAPTER 12 NU85E502**.

10. 1 Outline

The NB85E500 is a basic core macro used to control external memory. It features on chip SRAM, and I/O controller, and a page ROM controller.

The NB85E500 can be used to start the external bus cycle when it is connected to the NB85E (or NB85ET) via VSB.

It can also be used to control SDRAM by connecting an SDRAM controller (NU85E502) to the NB85E500.

10. 1. 1 Symbol diagram

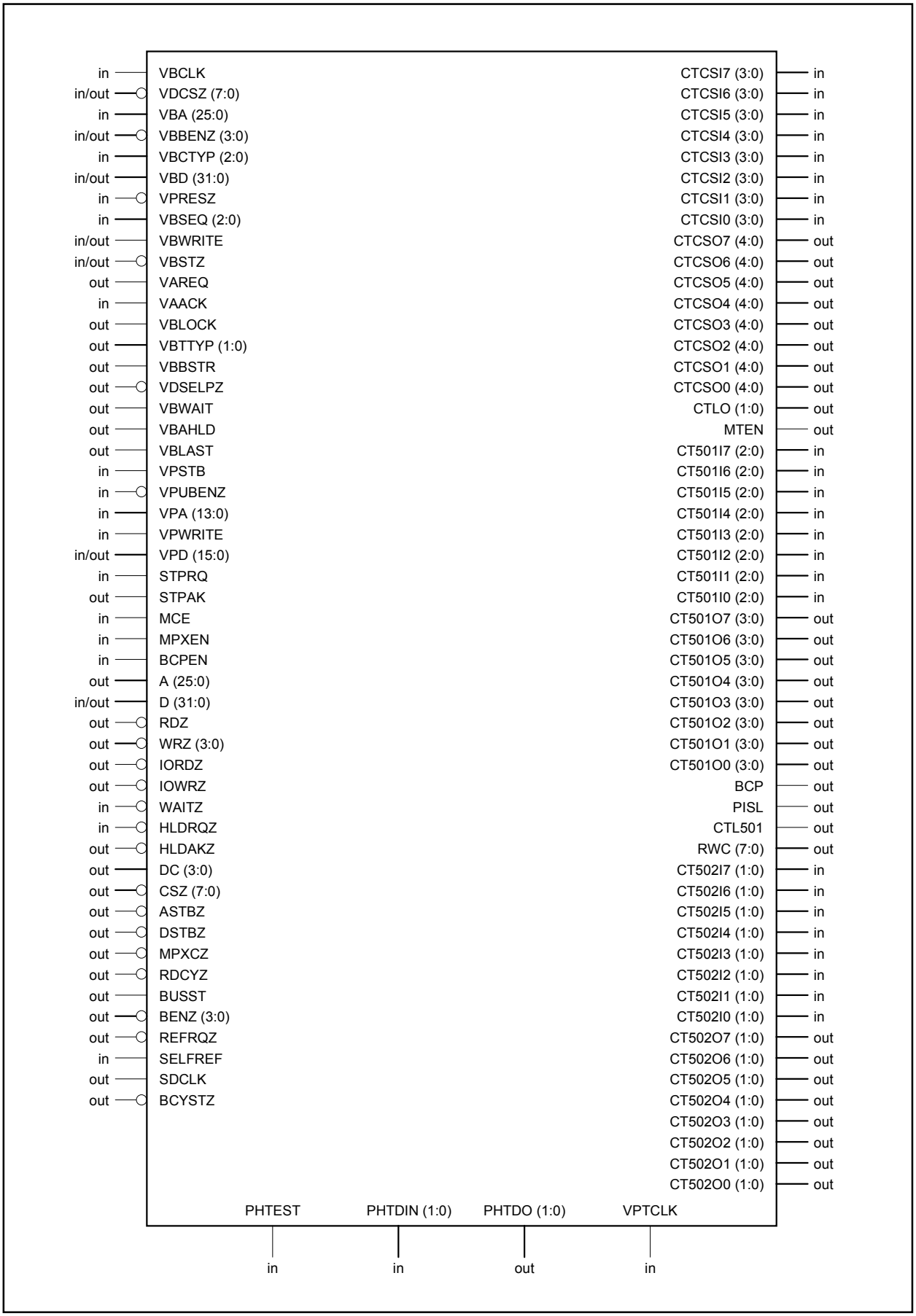
Number of grids

34.0k grids

96.9k grids (including wiring area)

Number of separation simulation patterns

14.3k


in VBCLK
in/out VDCSZ (7:0)
in VBA (25:0)
in/out VBBENZ (3:0)
in VBCTYP (2:0)
in/out VBD (31:0)
in VPRESZ
in VBSEQ (2:0)
in/out VBWRITE
in/out VBSTZ
out VAREQ
in VAACK
out VBLOCK
out VBTTYP (1:0)
out VBBSTR
out VDSELPZ
out VBWAIT
out VBAHLD
out VBLAST
in VPSTB
in VPUBENZ
in VPA (13:0)
in VPWRITE
in/out VPD (15:0)
in STPRQ
out STPAK
in MCE
in MPXEN
in BCPEN
out A (25:0)
in/out D (31:0)
out RDZ
out WRZ (3:0)
out IORDZ
out IOWRZ
in WAITZ
in HLDRQZ
out HLDAKZ
out DC (3:0)
out CSZ (7:0)
out ASTBZ
out DSTBZ
out MPXCZ
out RDCYZ
out BUSST
out BENZ (3:0)
out REFRQZ
in SELFREF
out SDCLK
out BCYSTZ
CTCSI7 (3:0) in
CTCSI6 (3:0) in
CTCSI5 (3:0) in
CTCSI4 (3:0) in
CTCSI3 (3:0) in
CTCSI2 (3:0) in
CTCSI1 (3:0) in
CTCSI0 (3:0) in
CTCSO7 (4:0) out
CTCSO6 (4:0) out
CTCSO5 (4:0) out
CTCSO4 (4:0) out
CTCSO3 (4:0) out
CTCSO2 (4:0) out
CTCSO1 (4:0) out
CTCSO0 (4:0) out
CTLO (1:0) out
MTEN out
CT501I7 (2:0) in
CT501I6 (2:0) in
CT501I5 (2:0) in
CT501I4 (2:0) in
CT501I3 (2:0) in
CT501I2 (2:0) in
CT501I1 (2:0) in
CT501I0 (2:0) in
CT501O7 (3:0) out
CT501O6 (3:0) out
CT501O5 (3:0) out
CT501O4 (3:0) out
CT501O3 (3:0) out
CT501O2 (3:0) out
CT501O1 (3:0) out
CT501O0 (3:0) out
BCP out
PISL out
CTL501 out
RWC (7:0) out
CT502I7 (1:0) in
CT502I6 (1:0) in
CT502I5 (1:0) in
CT502I4 (1:0) in
CT502I3 (1:0) in
CT502I2 (1:0) in
CT502I1 (1:0) in
CT502I0 (1:0) in
CT502O7 (1:0) out
CT502O6 (1:0) out
CT502O5 (1:0) out
CT502O4 (1:0) out
CT502O3 (1:0) out
CT502O2 (1:0) out
CT502O1 (1:0) out
CT502O0 (1:0) out
PHTEST in
PHTDIN (1:0) in
PHTDO (1:0) out
VPTCLK in

10. 1. 2 Pin capacitance

Remark C_{IN}: Capacitance of only input pin

C_{inewl}: Value of C_{IN} with wiring capacitance (estimated wire length capacitance) taken into consideration (l = 10 mm)

(1) Input pins (1/2)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
VBCLK	0.029	1.929	VPSTB	0.009	1.909
VBA25	0.081	1.981	VPUBENZ	0.011	1.911
VBA24	0.064	1.964	VPA13	0.035	1.935
VBA23	0.063	1.963	VPA12	0.036	1.936
VBA22	0.065	1.965	VPA11	0.034	1.934
VBA21	0.071	1.971	VPA10	0.045	1.945
VBA20	0.099	1.999	VPA9	0.035	1.935
VBA19	0.061	1.961	VPA8	0.013	1.913
VBA18	0.155	2.055	VPA7	0.052	1.952
VBA17	0.062	1.962	VPA6	0.043	1.943
VBA16	0.063	1.963	VPA5	0.046	1.946
VBA15	0.102	2.002	VPA4	0.008	1.908
VBA14	0.107	2.007	VPA3	0.008	1.908
VBA13	0.076	1.976	VPA2	0.061	1.961
VBA12	0.087	1.987	VPA1	0.012	1.912
VBA11	0.112	2.012	VPA0	0.075	1.975
VBA10	0.122	2.022	VPWRITE	0.013	1.913
VBA9	0.068	1.968	STPRQ	0.182	2.082
VBA8	0.091	1.991	MCE	0.137	2.037
VBA7	0.069	1.969	BCPEN	0.131	2.031
VBA6	0.096	1.996	WAITZ	0.151	2.051
VBA5	0.075	1.975	HLDRQZ	0.135	2.035
VBA4	0.068	1.968	SELFREF	0.162	2.062
VBA3	0.075	1.975	CTCSI73	0.043	1.943
VBA2	0.070	1.970	CTCSI72	0.041	1.941
VBA1	0.107	2.007	CTCSI71	0.042	1.942
VBA0	0.070	1.970	CTCSI70	0.178	2.078
VBCTYP2	0.025	1.925	CTCSI63	0.149	2.049
VBCTYP1	0.036	1.936	CTCSI62	0.067	1.967
VBCTYP0	0.049	1.949	CTCSI61	0.136	2.036
VPRESZ	0.011	1.911	CTCSI60	0.232	2.132
VBSEQ2	0.100	2.000	CTCSI53	0.110	2.010
VBSEQ1	0.092	1.992	CTCSI52	0.105	2.005
VBSEQ0	0.085	1.985	CTCSI51	0.069	1.969
VAACK	0.146	2.046	CTCSI50	0.126	2.026

(1) Input pins (2/2)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
CTCSI43	0.069	1.969	CT502I10	0.224	2.124
CTCSI42	0.064	1.964	CT502I01	0.079	1.979
CTCSI41	0.150	2.050	CT502I00	0.090	1.990
CTCSI40	0.199	2.099	PHTEST	0.016	1.916
CTCSI33	0.119	2.019	PHTDIN1	0.014	1.914
CTCSI32	0.073	1.973	PHTDIN0	0.028	1.928
CTCSI31	0.156	2.056	VPTCLK	0.176	2.076
CTCSI30	0.081	1.981	MPXEN	0.166	2.066
CTCSI23	0.079	1.979	CT501I72	0.111	2.011
CTCSI22	0.067	1.967	CT501I71	0.025	1.925
CTCSI21	0.132	2.032	CT501I70	0.214	2.114
CTCSI20	0.350	2.250	CT501I62	0.093	1.993
CTCSI13	0.168	2.068	CT501I61	0.171	2.071
CTCSI12	0.054	1.954	CT501I60	0.044	1.944
CTCSI11	0.146	2.046	CT501I52	0.180	2.080
CTCSI10	0.080	1.980	CT501I51	0.058	1.958
CTCSI03	0.134	2.034	CT501I50	0.298	2.198
CTCSI02	0.046	1.946	CT501I42	0.044	1.944
CTCSI01	0.109	2.009	CT501I41	0.140	2.040
CTCSI00	0.045	1.945	CT501I40	0.073	1.973
CT502I71	0.043	1.943	CT501I32	0.051	1.951
CT502I70	0.105	2.005	CT501I31	0.053	1.953
CT502I61	0.216	2.116	CT501I30	0.057	1.957
CT502I60	0.201	2.101	CT501I22	0.208	2.108
CT502I51	0.092	1.992	CT501I21	0.048	1.948
CT502I50	0.125	2.025	CT501I20	0.196	2.096
CT502I41	0.061	1.961	CT501I12	0.074	1.974
CT502I40	0.270	2.170	CT501I11	0.209	2.109
CT502I31	0.242	2.142	CT501I10	0.131	2.031
CT502I30	0.231	2.131	CT501I02	0.286	2.186
CT502I21	0.062	1.962	CT501I01	0.056	1.956
CT502I20	0.070	1.970	CT501I00	0.175	2.075
CT502I11	0.112	2.012			

(2) Output pins (1/3)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
VAREQ	13.311	–	–	WRZ1	13.298	–	–
VBLOCK	6.565	0.063	1.963	WRZ0	13.300	–	–
VBTTYP1	6.580	0.049	1.949	IORDZ	13.314	–	–
VBTTYP0	6.580	0.048	1.948	IOWRZ	13.323	–	–
VBBSTR	6.569	0.059	1.959	HLDAKZ	13.289	–	–
VDSELPZ	6.574	0.055	1.955	DC3	13.043	–	–
VBWAIT	6.526	0.102	2.002	DC2	13.067	–	–
VBAHLD	6.527	0.102	2.002	DC1	13.062	–	–
VBLAST	6.524	0.104	2.004	DC0	13.070	–	–
STPAK	13.276	–	–	CSZ7	13.338	–	–
A25	13.055	–	–	CSZ6	13.326	–	–
A24	13.047	–	–	CSZ5	13.337	–	–
A23	13.001	–	–	CSZ4	13.324	–	–
A22	13.053	–	–	CSZ3	13.333	–	–
A21	13.052	–	–	CSZ2	13.337	–	–
A20	13.068	–	–	CSZ1	13.328	–	–
A19	13.060	–	–	CSZ0	13.335	–	–
A18	13.049	–	–	BENZ3	13.043	–	–
A17	13.051	–	–	BENZ2	13.047	–	–
A16	13.051	–	–	BENZ1	13.048	–	–
A15	13.057	–	–	BENZ0	13.043	–	–
A14	13.049	–	–	BCYSTZ	13.035	–	–
A13	13.024	–	–	REFRQZ	13.296	–	–
A12	13.058	–	–	SDCLK	13.066	–	–
A11	13.047	–	–	CTCSO74	13.067	–	–
A10	13.066	–	–	CTCSO73	13.064	–	–
A9	13.052	–	–	CTCSO72	13.271	–	–
A8	13.063	–	–	CTCSO71	13.067	–	–
A7	13.053	–	–	CTCSO70	13.068	–	–
A6	13.051	–	–	CTCSO64	13.059	–	–
A5	13.034	–	–	CTCSO63	13.063	–	–
A4	13.029	–	–	CTCSO62	13.064	–	–
A3	13.049	–	–	CTCSO61	13.068	–	–
A2	13.044	–	–	CTCSO60	13.061	–	–
A1	13.054	–	–	CTCSO54	13.039	–	–
A0	13.055	–	–	CTCSO53	13.051	–	–
RDZ	13.012	–	–	CTCSO52	13.237	–	–
WRZ3	13.280	–	–	CTCSO51	13.034	–	–
WRZ2	13.326	–	–	CTCSO50	13.037	–	–

(2) Output pins (2/3)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
CTCSO44	13.056	–	–	CT502O11	12.972	–	–
CTCSO43	13.063	–	–	CT502O10	13.061	–	–
CTCSO42	13.314	–	–	CT502O01	13.026	–	–
CTCSO41	13.048	–	–	CT502O00	13.035	–	–
CTCSO40	13.056	–	–	PHTDO1	3.248	–	–
CTCSO34	12.963	–	–	PHTDO0	3.296	–	–
CTCSO33	12.867	–	–	ASTBZ	13.049	–	–
CTCSO32	13.335	–	–	DSTBZ	13.332	–	–
CTCSO31	13.015	–	–	MPXCZ	13.329	–	–
CTCSO30	12.959	–	–	RDCYZ	13.068	–	–
CTCSO24	13.043	–	–	BUSST	13.316	–	–
CTCSO23	13.069	–	–	CT501O73	13.064	–	–
CTCSO22	13.311	–	–	CT501O72	13.330	–	–
CTCSO21	13.063	–	–	CT501O71	12.967	–	–
CTCSO20	13.068	–	–	CT501O70	12.952	–	–
CTCSO14	13.065	–	–	CT501O63	13.039	–	–
CTCSO13	13.063	–	–	CT501O62	13.065	–	–
CTCSO12	13.233	–	–	CT501O61	13.056	–	–
CTCSO11	13.063	–	–	CT501O60	13.058	–	–
CTCSO10	12.910	–	–	CT501O53	13.334	–	–
CTCSO04	13.030	–	–	CT501O52	13.065	–	–
CTCSO03	13.022	–	–	CT501O51	13.061	–	–
CTCSO02	13.300	–	–	CT501O50	12.990	–	–
CTCSO01	13.040	–	–	CT501O43	13.264	–	–
CTCSO00	13.041	–	–	CT501O42	13.140	–	–
CTLO1	13.326	–	–	CT501O41	13.062	–	–
CTLO0	13.062	–	–	CT501O40	13.067	–	–
MTEN	12.950	–	–	CT501O33	13.056	–	–
CT502O71	13.070	–	–	CT501O32	12.893	–	–
CT502O70	13.062	–	–	CT501O31	13.056	–	–
CT502O61	13.067	–	–	CT501O30	13.065	–	–
CT502O60	12.944	–	–	CT501O23	13.028	–	–
CT502O51	13.012	–	–	CT501O22	13.021	–	–
CT502O50	13.065	–	–	CT501O21	12.984	–	–
CT502O41	13.057	–	–	CT501O20	12.970	–	–
CT502O40	12.925	–	–	CT501O13	13.176	–	–
CT502O31	13.046	–	–	CT501O12	13.210	–	–
CT502O30	13.054	–	–	CT501O11	13.061	–	–
CT502O21	12.934	–	–	CT501O10	13.060	–	–
CT502O20	12.999	–	–	CT501O03	13.064	–	–

(2) Output pins (3/3)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
CT501O10	13.060	–	–	RWC7	12.959	–	–
CT501O03	13.064	–	–	RWC6	12.992	–	–
CT501O02	13.319	–	–	RWC5	13.062	–	–
CT501O01	13.038	–	–	RWC4	13.009	–	–
CT501O00	13.029	–	–	RWC3	12.929	–	–
BCP	13.046	–	–	RWC2	13.060	–	–
PISL	13.063	–	–	RWC1	13.062	–	–
CTL501	12.941	–	–	RWC0	13.067	–	–

(3) I/O pins (1/2)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
VDCSZ7	6.313	0.315	2.215	VBD16	6.459	0.170	2.070
VDCSZ6	6.282	0.347	2.247	VBD15	6.509	0.120	2.020
VDCSZ5	6.263	0.365	2.265	VBD14	6.500	0.128	2.028
VDCSZ4	6.226	0.403	2.303	VBD13	6.509	0.120	2.020
VDCSZ3	6.312	0.316	2.216	VBD12	6.473	0.155	2.055
VDCSZ2	6.233	0.395	2.295	VBD11	6.407	0.221	2.121
VDCSZ1	6.207	0.421	2.321	VBD10	6.420	0.209	2.109
VDCSZ0	6.294	0.335	2.235	VBD9	6.509	0.120	2.020
VBBENZ3	6.494	0.135	2.035	VBD8	6.474	0.155	2.055
VBBENZ2	6.496	0.132	2.032	VBD7	6.459	0.170	2.070
VBBENZ1	6.502	0.126	3.026	VBD6	6.488	0.140	2.040
VBBENZ0	6.488	0.141	2.041	VBD5	6.460	0.169	2.069
VBD31	6.509	0.120	2.020	VBD4	6.489	0.140	2.040
VBD30	6.512	0.117	2.017	VBD3	6.487	0.142	2.042
VBD29	6.519	0.110	2.010	VBD2	6.511	0.117	2.017
VBD28	6.469	0.160	2.060	VBD1	6.457	0.171	2.071
VBD27	6.508	0.121	2.021	VBD0	6.452	0.177	2.077
VBD26	6.510	0.119	2.019	VBWRITE	6.455	0.173	2.073
VBD25	6.506	0.123	2.023	VBSTZ	6.389	0.240	2.140
VBD24	6.450	0.179	2.079	VPD15	6.564	0.111	2.011
VBD23	6.490	0.139	2.039	VPD14	6.492	0.183	2.083
VBD22	6.481	0.147	2.047	VPD13	6.487	0.188	2.088
VBD21	6.485	0.144	2.044	VPD12	6.528	0.147	2.047
VBD20	6.486	0.142	2.042	VPD11	6.548	0.127	2.027
VBD19	6.436	0.193	2.093	VPD10	6.555	0.120	2.020
VBD18	6.477	0.151	2.051	VPD9	6.545	0.130	2.030
VBD17	6.465	0.164	2.064	VPD8	6.535	0.140	2.040

(3) I/O pins (2/2)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
VPD7	6.522	0.199	2.099	D19	6.483	0.146	2.046
VPD6	6.552	0.169	2.069	D18	6.455	0.173	2.073
VPD5	6.548	0.173	2.073	D17	6.463	0.166	2.066
VPD4	6.529	0.192	2.092	D16	6.458	0.171	2.071
VPD3	6.509	0.212	2.112	D15	6.423	0.206	2.106
VPD2	6.473	0.248	2.148	D14	6.436	0.193	2.093
VPD1	6.467	0.255	2.155	D13	6.410	0.219	2.119
VPD0	6.479	0.242	2.142	D12	6.454	0.175	2.075
D31	6.433	0.196	2.096	D11	6.505	0.124	2.024
D30	6.393	0.235	2.135	D10	6.474	0.155	2.055
D29	6.414	0.214	2.114	D9	6.423	0.205	2.105
D28	6.452	0.177	2.077	D8	6.440	0.189	2.089
D27	6.427	0.201	2.101	D7	6.449	0.180	2.080
D26	6.421	0.208	2.108	D6	6.417	0.212	2.112
D25	6.435	0.194	2.094	D5	6.463	0.166	2.066
D24	6.437	0.192	2.092	D4	6.431	0.197	2.097
D23	6.436	0.193	2.093	D3	6.393	0.236	2.136
D22	6.450	0.179	2.079	D2	6.361	0.267	2.167
D21	6.439	0.189	2.089	D1	6.472	0.156	2.056
D20	6.443	0.185	2.085	D0	6.472	0.157	2.057

10. 2 Initialization of Internal Registers

Before executing the test program, be sure to execute an instruction to assign initial values to the internal registers used in the test program. Failure to this so will result in the propagation of undefined values.

10. 3 Pin Functions

(1/3)

Pin Name		I/O	Function
NB85E/NB85ET connection pins	VBCLK	Input	Internal system clock input
	VDCSZ7 to VDCSZ0	I/O	Chip select I/O
	VBA25 to VBA0	Input	Address input
	VBBENZ3 to VBBENZ0	I/O	Byte enable I/O
	VBCTYP2 to VBCTYP0	Input	Bus cycle status input
	VBD31 to VBD0	I/O	Data I/O
	VPRESZ	Input	Reset input
	VBSEQ2 to VBSEQ0	Input	Sequential status input
	VBWRITE	I/O	Read/write status I/O
	VBSTZ	I/O	Transfer start I/O
	VAREQ	Output	Bus access right request output
	VAACK	Input	Bus access right acknowledge input
	VBLOCK	Output	Bus lock output
	VBTTYP1, VBTTYP0	Output	Bus transfer type output
	VBBSTR	Output	Burst read status output
	VDSELPZ	Output	Peripheral I/O area access status output
	VBWAIT	Output	Wait response output
	VBAHLD	Output	Address hold response output
	VBLAST	Output	Last response output
	VPSTB	Input	Data strobe input (for NPB)
	VPUBENZ	Input	Upper byte enable input (for NPB)
	VPA13 to VPA0	Input	Address input (for NPB)
	VPWRITE	Input	Write access strobe input (for NPB)
	VPD15 to VPD0	I/O	Data I/O (for NPB)
	STPRQ	Input	STOP mode request input
	STPAK	Output	Acknowledge output for STPRQ input
Initial setting pins	MCE	Input	MEn bit reset value control input for BCT register (n = 0 to 7)
	BCPEN	Input	BCP bit reset value control input for BCP register
External memory connection pins	A25 to A0	Output	External memory address output
	D31 to D0	I/O	External memory data I/O
	RDZ	Output	SRAM/page ROM read strobe output
	WRZ3 to WRZ0	Output	SRAM/page ROM write strobe output
	IORDZ	Output	External I/O read strobe output
	IOWRZ	Output	External I/O write strobe output
	WAITZ	Input	Wait request input
	HLDRQZ	Input	External bus hold request input
	HLDAKZ	Output	External bus hold request acknowledge output

(2/3)

Pin Name		I/O	Function
External memory connection pins	DC3 to DC0	Output	Data bus control output
	CSZ7 to CSZ0	Output	Chip select output
	BENZ3 to BENZ0	Output	Byte enable output
	BCYSTZ	Output	Bus cycle start status output
	REFRQZ	Output	Refresh status output
	SELFREF	Input	Self refresh request input
	SDCLK	Output	SDRAM sync clock output
NU85E502 connection pins	CTCSI73 to CTCSI70	Input	Control input from NU85E502 (for CS7 area)
	CTCSI63 to CTCSI60	Input	Control input from NU85E502 (for CS6 area)
	CTCSI53 to CTCSI50	Input	Control input from NU85E502 (for CS5 area)
	CTCSI43 to CTCSI40	Input	Control input from NU85E502 (for CS4 area)
	CTCSI33 to CTCSI30	Input	Control input from NU85E502 (for CS3 area)
	CTCSI23 to CTCSI20	Input	Control input from NU85E502 (for CS2 area)
	CTCSI13 to CTCSI10	Input	Control input from NU85E502 (for CS1 area)
	CTCSI03 to CTCSI00	Input	Control input from NU85E502 (for CS0 area)
	CTCSO74 to CTCSO70	Output	Control output to NU85E502 (for CS7 area)
	CTCSO64 to CTCSO60	Output	Control output to NU85E502 (for CS6 area)
	CTCSO54 to CTCSO50	Output	Control output to NU85E502 (for CS5 area)
	CTCSO44 to CTCSO40	Output	Control output to NU85E502 (for CS4 area)
	CTCSO34 to CTCSO30	Output	Control output to NU85E502 (for CS3 area)
	CTCSO24 to CTSO20	Output	Control output to NU85E502 (for CS2 area)
	CTCSO14 to CTCSO10	Output	Control output to NU85E502 (for CS1 area)
	CTCSO04 to CTCSO00	Output	Control output to NU85E502 (for CS0 area)
	CTLO1, CTLO0	Output	Control output to NU85E502
	MTEN	Output	Test mode enable output to NU85E502
	CT502I71, CT502I70	Input	Control input from NU85E502 (for CS7 area)
	CT502I61, CT502I60	Input	Control input from NU85E502 (for CS6 area)
	CT502I51, CT502I50	Input	Control input from NU85E502 (for CS5 area)
	CT502I41, CT502I40	Input	Control input from NU85E502 (for CS4 area)
	CT502I31, CT502I30	Input	Control input from NU85E502 (for CS3 area)
	CT502I21, CT502I20	Input	Control input from NU85E502 (for CS2 area)
	CT502I11, CT502I10	Input	Control input from NU85E502 (for CS1 area)
	CT502I01, CT502I00	Input	Control input from NU85E502 (for CS0 area)
	CT502O71, CT502O70	Output	Control output to NU85E502 (for CS7 area)
	CT502O61, CT502O60	Output	Control output to NU85E502 (for CS6 area)
	CT502O51, CT502O50	Output	Control output to NU85E502 (for CS5 area)
	CT502O41, CT502O40	Output	Control output to NU85E502 (for CS4 area)

(3/3)

Pin Name		I/O	Function
NU85E502 connection pins	CT502O31, CT502O30	Output	Control output to NU85E502 (for CS3 area)
	CT502O21, CT502O20	Output	Control output to NU85E502 (for CS2 area)
	CT502O11, CT502O10	Output	Control output to NU85E502 (for CS1 area)
	CT502O01, CT502O00	Output	Control output to NU85E502 (for CS0 area)
Test mode pins	PHTEST	Input	Peripheral test mode status input
	PHTDIN1, PHTDIN0	Input	Peripheral macro test input
	PHTDO1, PHTDO0	Output	Peripheral macro test output
	VPTCLK	Input	Test clock input
NEC reserved pins	MPXEN	Input	NEC reserved pin (input a low level)
	ASTBZ	Output	NEC reserved pin (leave open)
	DSTBZ	Output	NEC reserved pin (leave open)
	MPXCZ	Output	NEC reserved pin (leave open)
	RDCYZ	Output	NEC reserved pin (leave open)
	BUSST	Output	NEC reserved pin (leave open)
	CT501I72 to CT501I70	Input	NEC reserved pin (input a low level)
	CT501I62 to CT501I60	Input	NEC reserved pin (input a low level)
	CT501I52 to CT501I50	Input	NEC reserved pin (input a low level)
	CT501I42 to CT501I40	Input	NEC reserved pin (input a low level)
	CT501I32 to CT501I30	Input	NEC reserved pin (input a low level)
	CT501I22 to CT501I20	Input	NEC reserved pin (input a low level)
	CT501I12 to CT501I10	Input	NEC reserved pin (input a low level)
	CT501I02 to CT501I00	Input	NEC reserved pin (input a low level)
	CT501O73 to CT501O70	Output	NEC reserved pin (leave open)
	CT501O63 to CT501O60	Output	NEC reserved pin (leave open)
	CT501O53 to CT501O50	Output	NEC reserved pin (leave open)
	CT501O43 to CT501O40	Output	NEC reserved pin (leave open)
	CT501O33 to CT501O30	Output	NEC reserved pin (leave open)
	CT501O23 to CT501O20	Output	NEC reserved pin (leave open)
	CT501O13 to CT501O10	Output	NEC reserved pin (leave open)
	CT501O03 to CT501O00	Output	NEC reserved pin (leave open)
	BCP	Output	NEC reserved pin (leave open)
	PISL	Output	NEC reserved pin (leave open)
	CTL501	Output	NEC reserved pin (leave open)
	RWC7 to RWC0	Output	NEC reserved pin (leave open)

10. 4 Electrical Specifications (Preliminary)

The following specifications are for a single macro. An actual chip consists of two or more macros. Design the system so that all the specifications of the individual macros are satisfied when the chip is used.

10. 4. 1 Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to +4.6	V
Operating ambient temperature	T_A	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

10. 4. 2 Recommended operation range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	−40		+85	°C
Clock cycle	t_{CYK}	15.0			ns

10. 4. 3 DC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1}	In normal operation mode		0.18	0.27	mA/MHz
	I_{DD2}	In STOP mode		0	1.0	μA

Remarks 1. The above supply current value is a reference value calculated from the number of grids.

2. The TYP. value is a reference value for when T_A = 25°C, V_{DD} = 3.3 V.

10. 4. 4 AC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

(1) SRAM/page ROM read timing (1/3)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VBCLK input cycle	<1>	t_{CYK}		15.0		ns
Delay time from VBCLK↑ to address	<2>	t_{AD}		t_{DKA} + 0.4[Note]	t_{DKA} + 2.5[Note]	ns
Delay time from VBCLK↑ to CSZ	<3>	t_{CSZD1}		t_{DKC} + 0.5[Note]	t_{DKC} + 2.5[Note]	ns
Delay time from VBCLK↓ to RDZ	<4>	t_{RDZD1}		1.5	5.4	ns
Delay time from VBCLK↑ to RDZ	<5>	t_{RDZD2}		1.5	5.0	ns
Data setup time (to VBCLK↑)	<6>	t_{DS1}		0		ns
Data hold time (from VBCLK↑)	<7>	t_{DH1}		1.0		ns
Delay time from VBCLK↑ to BCYSTZ	<8>	t_{BCYD}		1.6	t_{DKS1} + 1.7[Note]	ns
WAITZ setup time (to VBCLK↑)	<9>	t_{WTS}		0		ns
WAITZ hold time (from VBCLK↑)	<10>	t_{WTH}		0.9		ns
Delay time from VBCLK↓ to VBWAIT, VBAHLD, VBLAST	<11>	t_{VRD1}			5.6	ns
Delay time from VBCLK↑ to VBWAIT, VBAHLD, VBLAST	<12>	t_{VRD2}		1.2		ns
Delay time from VBCLK↑ to VBD	<13>	t_{VBD1}			6.5	ns
Delay time from VBCLK↓ to VBD	<14>	t_{VBD2}		1.7		ns
Delay time from VBCLK↑ to DC	<15>	t_{DCD1}		t_{DKS1} + 0.7[Note]	t_{DKS1} + 3.1[Note]	ns

Note t_{DKA}: Delay time from VBCLK↑ to VBA

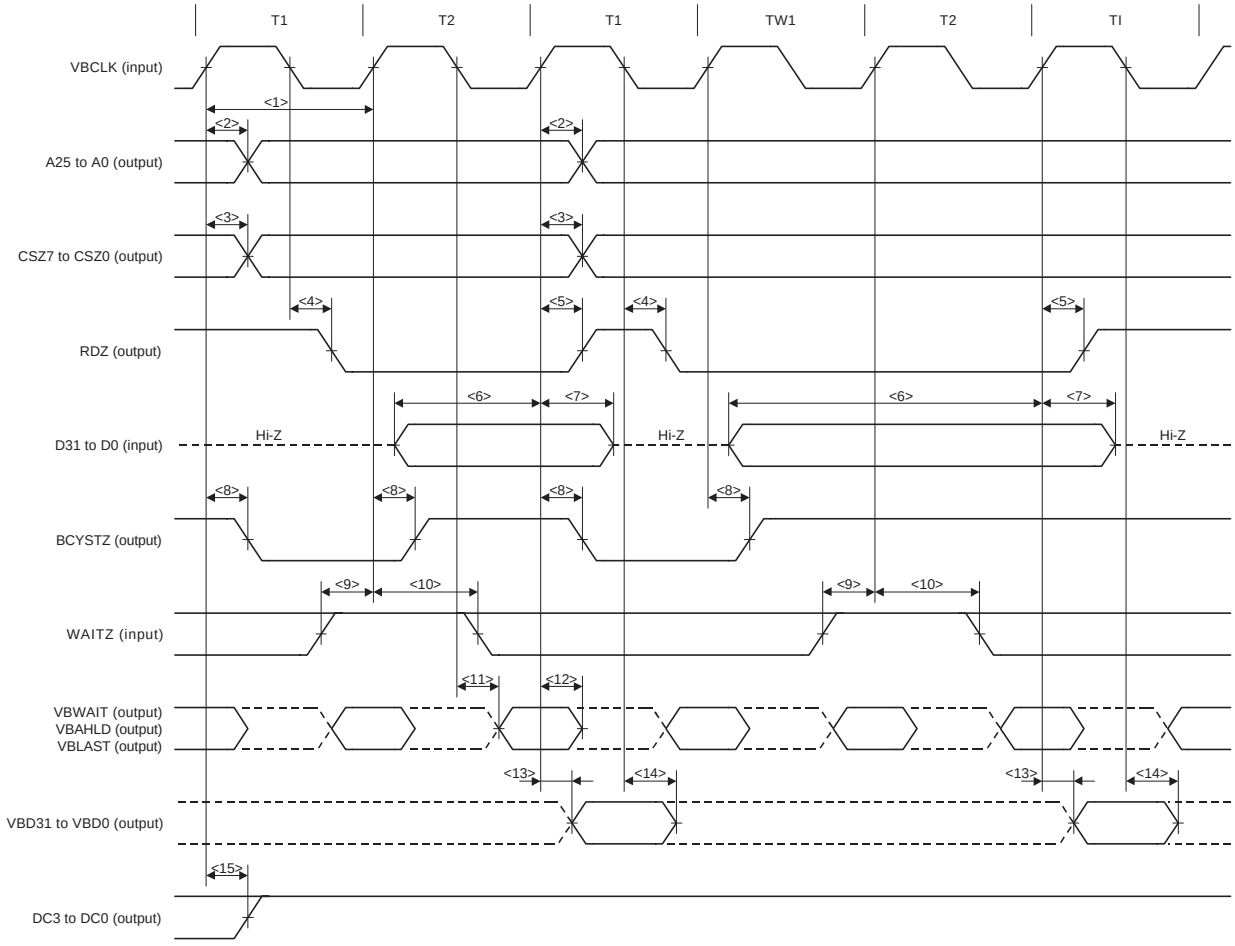
t_{DKC}: Delay time from VBCLK↑ to VDCSZ, VDSELPZ

t_{DKS1}: Delay time from VBCLK↑ to VBSTZ, VBSIZE, VBWRITE, VBCTYP

The above are the electrical specifications of the NB85E (or NB85ET). Refer to section **7. 4. 4 AC characteristics** (or **9. 4. 4 AC characteristics**).

(1) SRAM/page ROM read timing (2/3)

(a) When wait is inserted



Remarks 1. T1, T2: Basic state in which NB85E500 access is performed

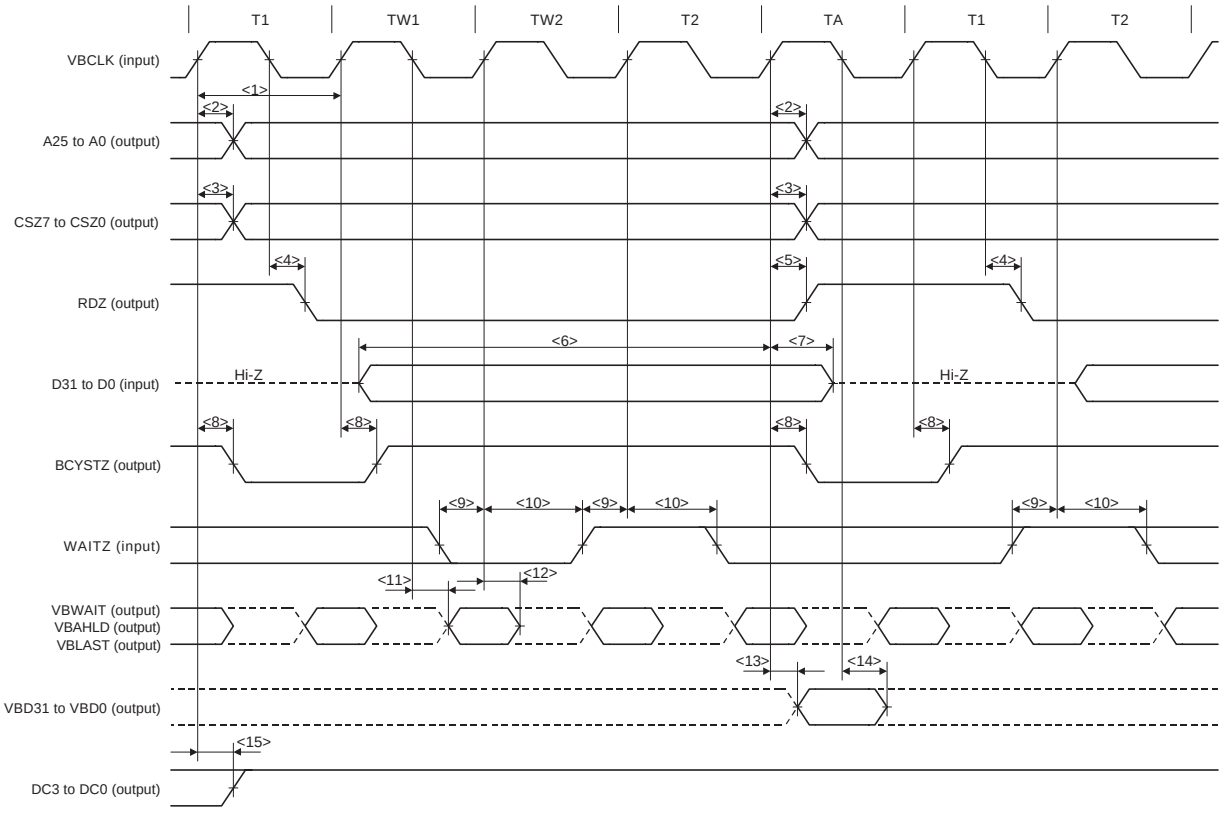
TW1: Wait state inserted by setting data wait control registers 0, 1 (DWC0, DWC1)

TI: Idle state inserted by setting bus cycle control register (BCC)

2. The level of the broken line portion of the VBWAIT, VBAHLD, VBLAST, and VBD31 to VBD0 signals indicates the undefined state (weak unknown) in which the bus holder in the NB85E (or NB85ET) is driving.

(1) SRAM/page ROM read timing (3/3)

(b) When address setting wait is inserted



Remarks 1. T1, T2: Basic state in which NB85E500 access is performed

TW1: Wait state inserted by setting data wait control registers 0, 1 (DWC0, DWC1)

TW2: Wait state through WAITZ pin input

TA: Address setting wait state inserted by setting the address setting wait control register (ASC)

2. The level of the broken line portion of the VBWAIT, VBAHLD, VBLAST, and VBD31 to VBD0 signals indicates the undefined state (weak unknown) in which the bus holder in the NB85E (or NB85ET) is driving.

(2) SRAM write timing (1/3)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VBCLK input cycle	<1>	t_{CYK}		15.0		ns
Delay time from VBCLK↑ to address	<2>	t_{AD}		t_{DKA} + 0.4[Note]	t_{DKA} + 2.5[Note]	ns
Delay time from VBCLK↑ to CSZ	<3>	t_{CSZD1}		t_{DKC} + 0.5[Note]	t_{DKC} + 2.5[Note]	ns
Delay time from VBCLK↑ to BCYSTZ	<8>	t_{BCYD}		1.6	t_{DKS1} + 1.7[Note]	ns
WAITZ setup time (to VBCLK↑)	<9>	t_{WTS}		0		ns
WAITZ hold time (from VBCLK↑)	<10>	t_{WTH}		0.9		ns
Delay time from VBCLK↓ to VBWAIT, VBAHLD, VBLAST	<11>	t_{VRD1}			5.6	ns
Delay time from VBCLK↑ to VBWAIT, VBAHLD, VBLAST	<12>	t_{VRD2}		1.2		ns
Delay time from VBCLK↓ to DC	<16>	t_{DCD2}		1.8	6.0	ns
Delay time from VBCLK↓ to WRZ	<17>	t_{WRZD}		1.6	4.9	ns
Delay time from VBCLK↓ to data	<18>	t_{DD1}		t_{DKD1} + 0.4[Note]	t_{DKD1} + 2.0[Note]	ns
Delay time from VBCLK↑ to data	<19>	t_{DD2}		t_{DKD0} + 0.4[Note]	t_{DKD0} + 2.0[Note]	ns
Delay time from VBBENZ to BENZ	–	t_{BNZD}		0.4	1.8	ns

Note t_{DKA}: Delay time from VBCLK↑ to VBA

t_{DKC}: Delay time from VBCLK↑ to VDCSZ, VDSELPZ

t_{DKS1}: Delay time from VBCLK↑ to VBSTZ, VBSIZE, VBWRITE, VBCTYP

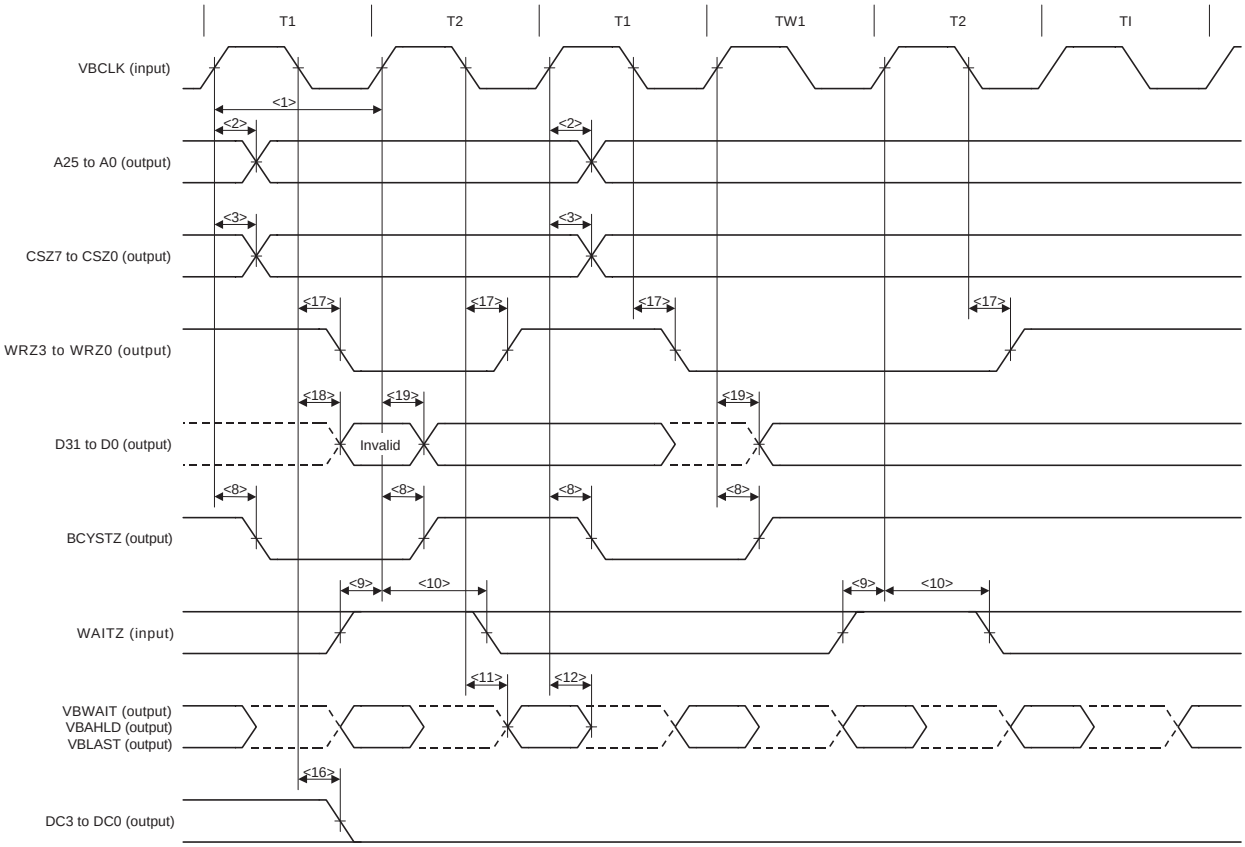
t_{DKD1}: Delay time from VBCLK↓ to VBD data

t_{DKD0}: Delay time from VBCLK↑ to VBD data

The above are the electrical specifications of the NB85E (or NB85ET). Refer to section **7. 4. 4 AC characteristics** (or **9. 4. 4 AC characteristics**).

(2) SRAM write timing (2/3)

(a) When wait is inserted



Remarks 1. T1, T2: Basic state in which NB85E500 access is performed

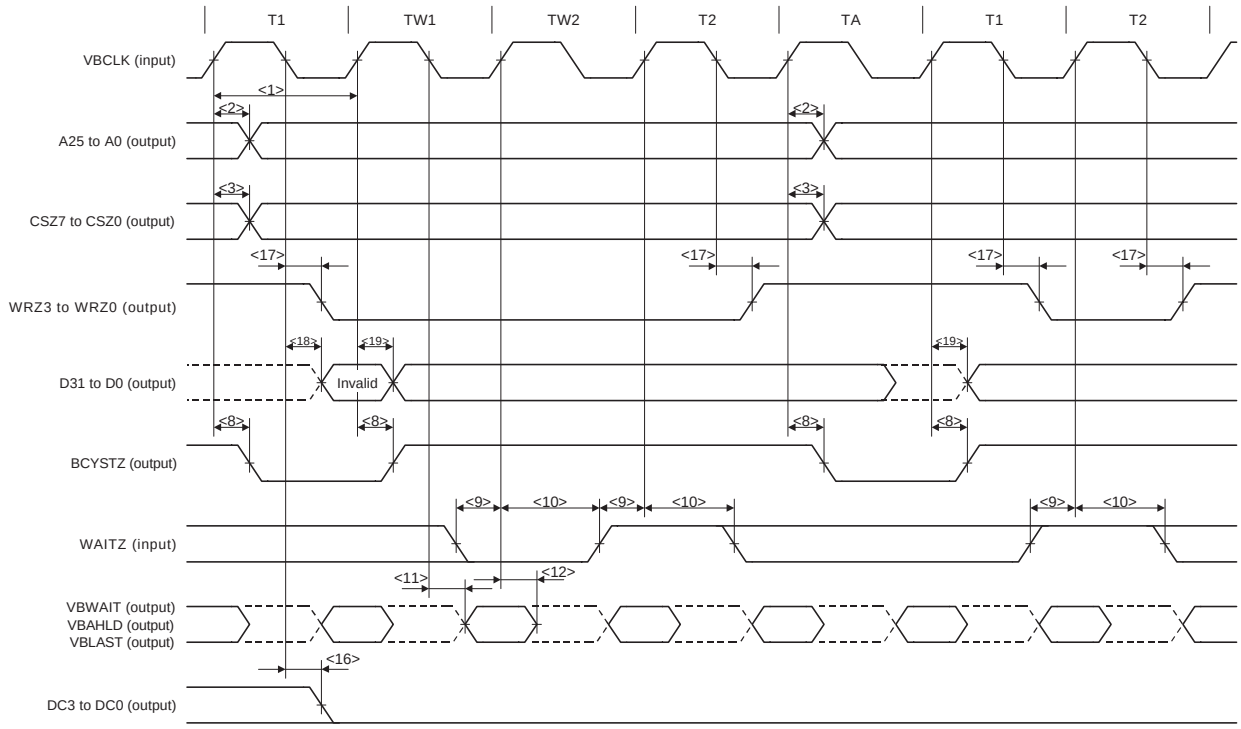
TW1: Wait state inserted by setting data wait control registers 0, 1 (DWC0, DWC1)

TI: Idle state inserted by setting bus cycle control register (BCC)

2. The level of the broken line portion of the D31 to D0 signals is undefined. The level of the broken line portion of the VBWAIT, VBAHLD, and VBLAST signals indicates undefined state (weak unknown) in which the bus holder in the NB85E (or NB85ET) is driving.

(2) SRAM write timing (3/3)

(b) When address setting wait is inserted



Remarks 1. T1, T2: Basic state in which NB85E500 access is performed

TW1: Wait state inserted by setting data wait control registers 0, 1 (DWC0, DWC1)

TW2: Wait state through WAITZ pin input

TA: Address setting wait state inserted by setting the address setting wait control register (ASC)

2. The level of the broken line portion of the D31 to D0 signals is undefined. The level of the broken line portion of the VBWAIT, VBAHLD, and VBLAST signals indicates undefined state (weak unknown) in which the bus holder in the NB85E (or NB85ET) is driving.

(3) SRAM read/write timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VBCLK input cycle	<1>	t_{CYK}		15.0		ns
Delay time from VBCLK↑ to address	<2>	t_{AD}		t_{DKA} + 0.4[Note]	t_{DKA} + 2.5[Note]	ns
Delay time from VBCLK↑ to CSZ	<3>	t_{CSZD1}		t_{DKC} + 0.5[Note]	t_{DKC} + 2.5[Note]	ns
Delay time from VBCLK↓ to RDZ	<4>	t_{RDZD1}		1.5	5.4	ns
Delay time from VBCLK↑ to RDZ	<5>	t_{RDZD2}		1.5	5.0	ns
Data setup time (to VBCLK↑)	<6>	t_{DS1}		0		ns
Data hold time (from VBCLK↑)	<7>	t_{DH1}		1.0		ns
Delay time from VBCLK↑ to BCYSTZ	<8>	t_{BCYD}		1.6	t_{DKS1} + 1.7[Note]	ns
WAITZ setup time (to VBCLK↑)	<9>	t_{WTS}		0		ns
WAITZ hold time (from VBCLK↑)	<10>	t_{WTH}		0.9		ns
Delay time from VBCLK↓ to VBWAIT, VBAHLD, VBLAST	<11>	t_{VRD1}			5.6	ns
Delay time from VBCLK↑ to VBWAIT, VBAHLD, VBLAST	<12>	t_{VRD2}		1.2		ns
Delay time from VBCLK↑ to VBD	<13>	t_{VBD1}			6.5	ns
Delay time from VBCLK↓ to VBD	<14>	t_{VBD2}		1.7		ns
Delay time from VBCLK↑ to DC	<15>	t_{DCD1}		t_{DKS1} + 0.7[Note]	t_{DKS1} + 3.1[Note]	ns
Delay time from VBCLK↓ to DC	<16>	t_{DCD2}		1.8	6.0	ns
Delay time from VBCLK↓ to WRZ	<17>	t_{WRZD}		1.6	4.9	ns
Delay time from VBCLK↓ to data	<18>	t_{DD1}		t_{DKD1} + 0.4[Note]	t_{DKD1} + 2.0[Note]	ns
Delay time from VBCLK↑ to data	<19>	t_{DD2}		t_{DKD0} + 0.4[Note]	t_{DKD0} + 2.0[Note]	ns

Note t_{DKA}: Delay time from VBCLK↑ to VBA

t_{DKC}: Delay time from VBCLK↑ to VDCSZ, VDSELPZ

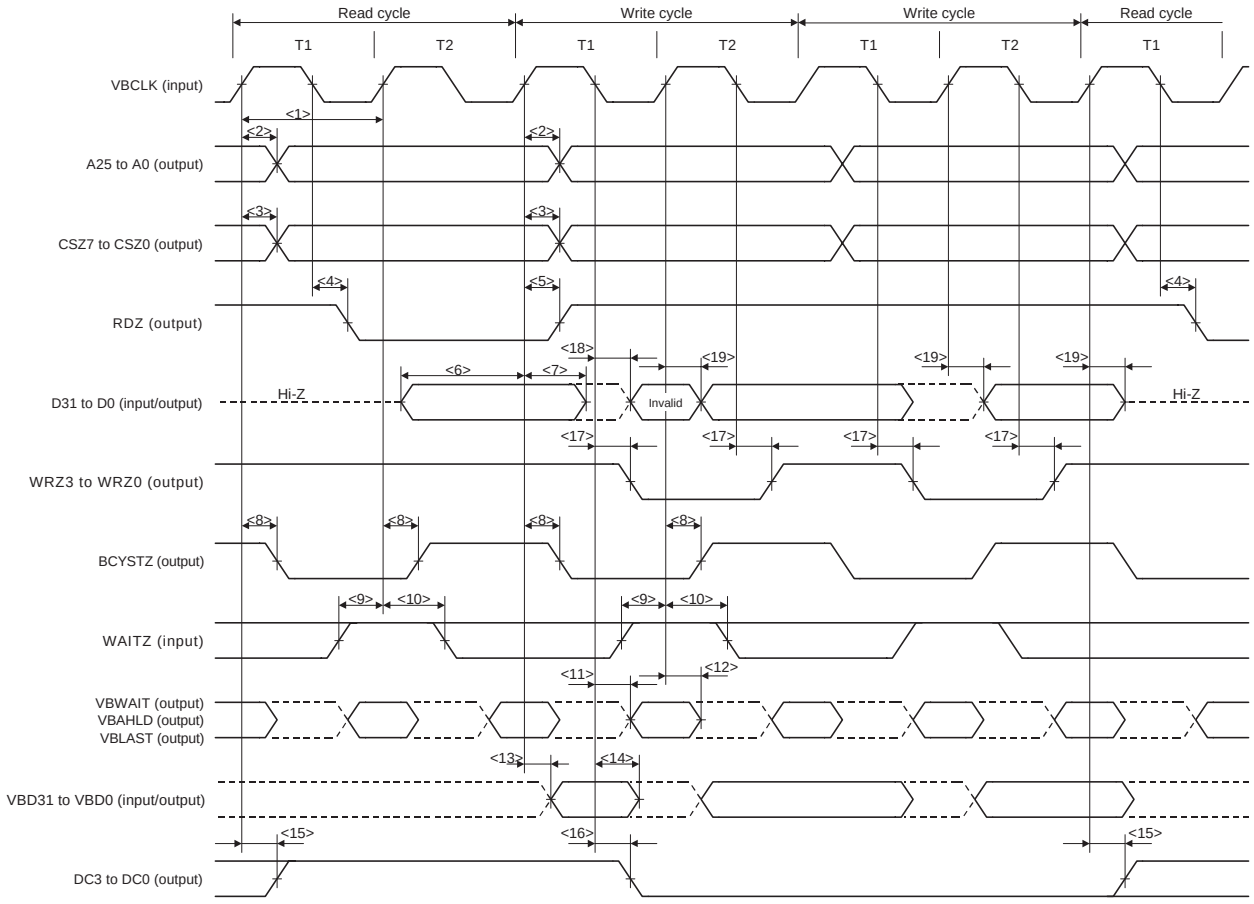
t_{DKS1}: Delay time from VBCLK↑ to VBSTZ, VBSIZE, VBWRITE, VBCTYP

t_{DKD1}: Delay time from VBCLK↓ to VBD data

t_{DKD0}: Delay time from VBCLK↑ to VBD data

The above are the electrical specifications of the NB85E (or NB85ET). Refer to section **7. 4. 4 AC characteristics** (or **9. 4. 4 AC characteristics**).

(3) SRAM read/write timing (2/2)



Remarks 1. T1, T2: Basic state in which NB85E500 access is performed

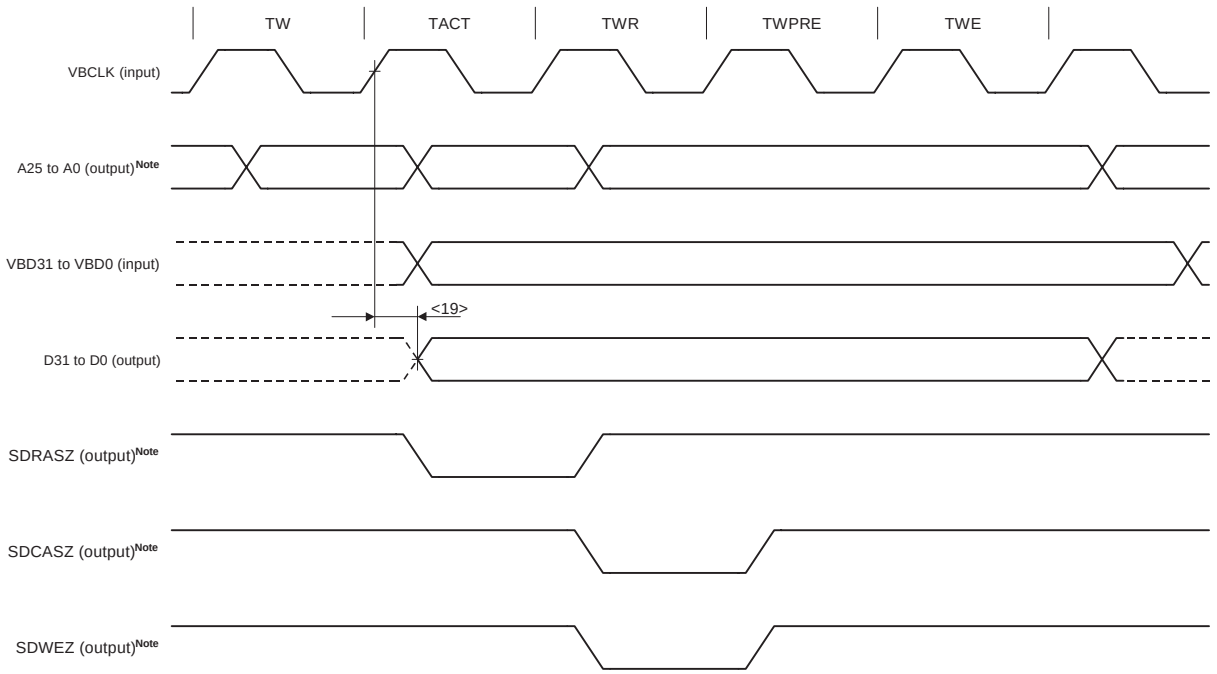
2. The level of the broken line portion of the D31 to D0 signals is undefined. The level of the broken line portion of the VBWAIT, VBAHLD, VBLAST, and VBD31 to VBD0 signals indicates undefined state (weak unknown) in which the bus holder in the NB85E (or NB85ET) is driving.

(4) SDRAM write timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to data	<19>	t_{DD2}		t_{DKD0} + 0.4[Note]	t_{DKD0} + 2.0[Note]	ns

Note t_{DKD0}: Delay time from VBCLK↑ to VBD data

The above is the electrical specifications of the NB85E (or NB85ET). Refer to section **7. 4. 4 AC characteristics** (or **9. 4. 4 AC characteristics**).



Note Signal of the NU85E502

Remarks 1. TW: Wait state
TACT: Bank active command state
TWR: Write command state
TWPRE: State indicating a precharge
TWE: State indicating the end of a write cycle

2. The level of the broken line portion of the VBD31 to VBD0 signals indicates undefined state (weak unknown) in which the bus holder in the NB85E (or NB85ET) is driving.
The level of the broken line portion of the D31 to D0 signals is undefined.

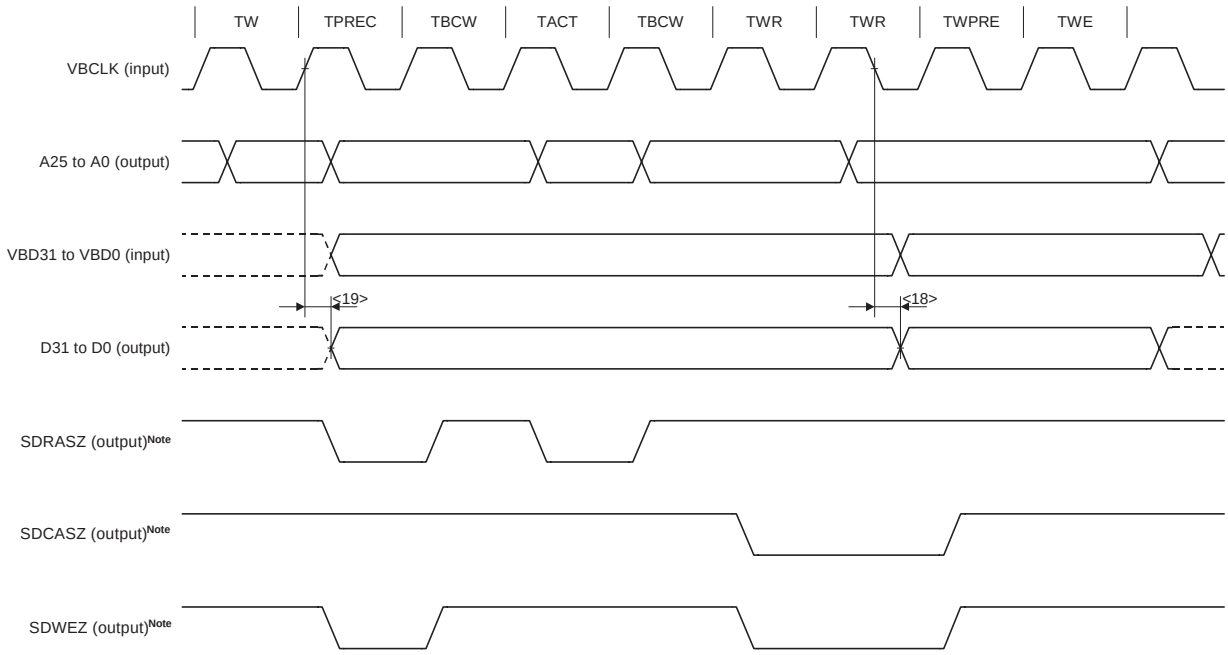
(5) SDRAM sequential write timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↓ to data	<18>	t_{DD1}		t_{DKD1} + 0.4[Note]	t_{DKD1} + 2.0[Note]	ns
Delay time from VBCLK↑ to data	<19>	t_{DD2}		t_{DKD0} + 0.4[Note]	t_{DKD0} + 2.0[Note]	ns

Note t_{DKD1}: Delay time from VBCLK↓ to VBD data

t_{DKD0}: Delay time from VBCLK↑ to VBD data

The above are the electrical specifications of the NB85E (or NB85ET). Refer to section **7. 4. 4 AC characteristics** (or **9. 4. 4 AC characteristics**).



Note Signal of the NU85E502

Remarks 1. TW: Wait state

TPREC: Bank precharge command state

TBCW: Wait state inserted by setting the BCW1 and BCW0 bits of the SDRAM configuration register n (SCRn) (n = 0 to 7)

TACT: Bank active command state

TWR: Write command state

TWPRE: State indicating a precharge

TWE: State indicating the end of a write cycle

2. The level of the broken line portion of the VBD31 to VBD0 signals indicates undefined state (weak unknown) in which the bus holder in the NB85E (or NB85ET) is driving. The level of the broken line portion of the D31 to D0 signals is undefined.

(6) SDRAM refresh timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to REFRQZ	–	t_{RFRQD}		1.5	4.9	ns
SELFREF setup time (to VBCLK↑)	–	t_{SRFS}		0.8		ns
SELFREF hold time (from VBCLK↑)	–	t_{SRFH}		1.0		ns
Delay time from CT502In1 to CSZ	–	t_{CSZD2}		t_{C2I1D} + 0.4[Note]	t_{C2I1D} + 2.3[Note]	ns

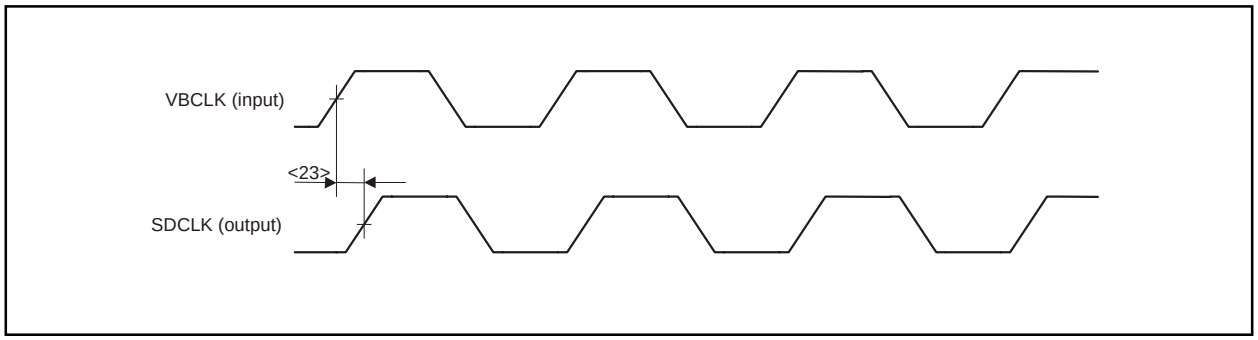
Note t_{C2I1D}: Delay time from VBCLK↑ to CT502I1

The above is the electrical specifications of the NU85E502. Refer to section **12. 4. 4 (3) NU85E500/NB85E500 connection signal timing**.

Remark n = 7 to 0

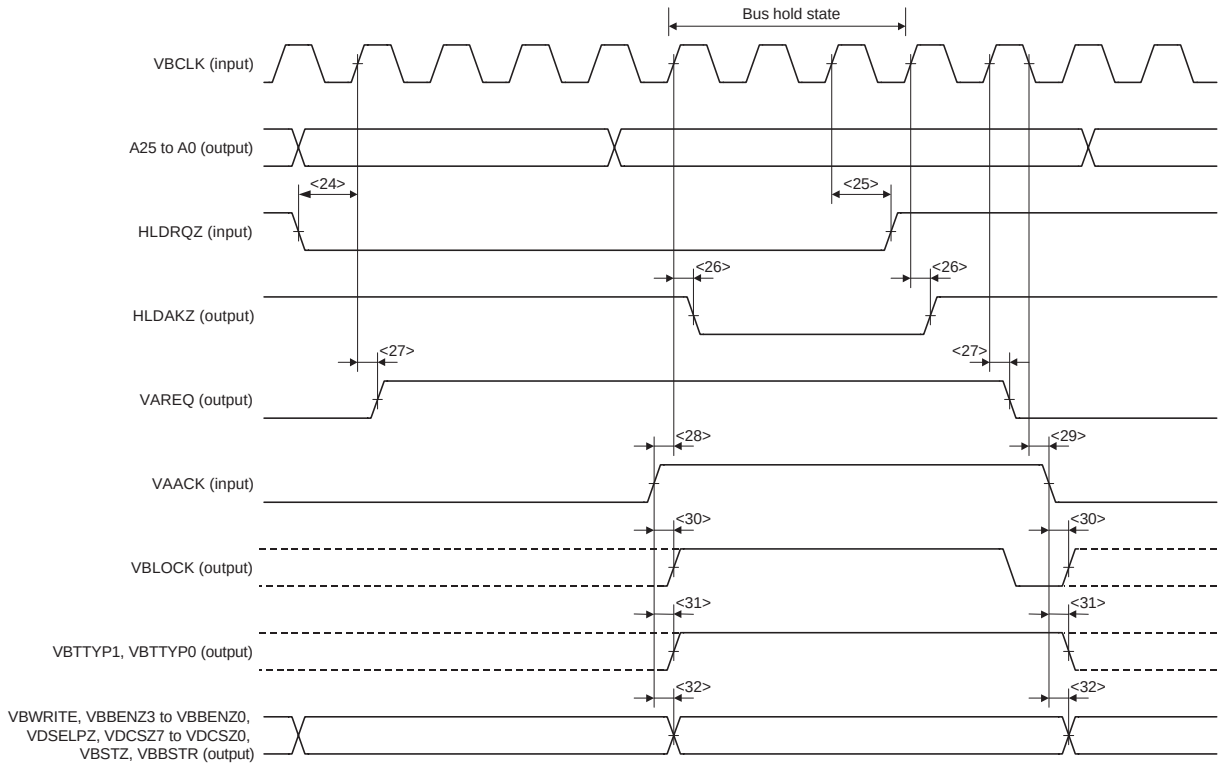
(7) SDCLK output timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to SDCLK↑	<23>	t_{SDCKD}		1.1	3.7	ns



(8) Bus hold timing

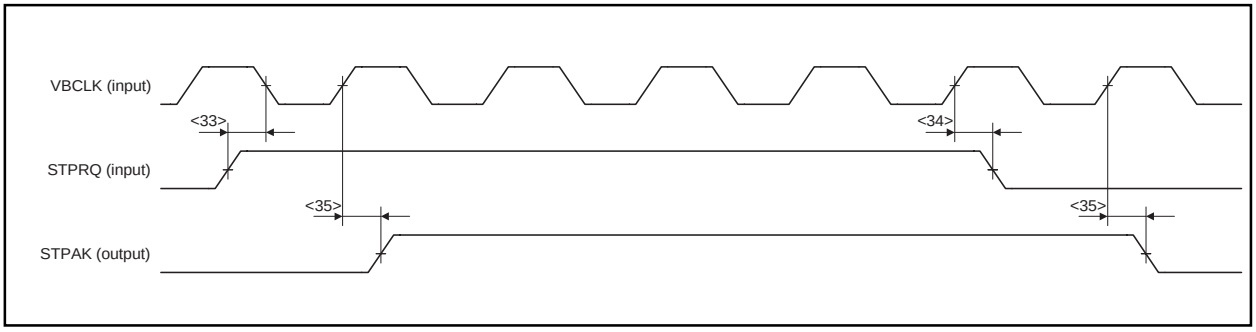
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
HLDRQZ setup time (to VBCLK↑)	<24>	t_{HRQS}		0		ns
HLDRQZ hold time (from VBCLK↑)	<25>	t_{HRQH}		0.6		ns
Delay time from VBCLK↑ to HLDAKZ	<26>	t_{HAKD}		1.5	4.6	ns
Delay time from VBCLK↑ to VAREQ	<27>	t_{VAQD}		1.6	4.6	ns
VAACK setup time (to VBCLK↑)	<28>	t_{VAKS}		0.5		ns
VAACK hold time (from VBCLK↓)	<29>	t_{VAKH}		0.8		ns
Delay time from VAACK↑ to VBLOCK	<30>	t_{VLKD}		1.7	5.6	ns
Delay time from VAACK↑ to VBTTYP	<31>	t_{VTTPD}		1.8	6.0	ns
Delay time from VAACK↑ to VBWRITE, VBBENZ, VDSELPZ, VDCSZ, VBSTZ, VBBSTR	<32>	t_{VSBD}		1.7	6.1	ns



Remark The level of the broken line portion of the VBLOCK, VBTTYP1, and VBTTYP0 signals indicates undefined state (weak unknown) in which the bus holder in the NB85E (or NB85ET) is driving.

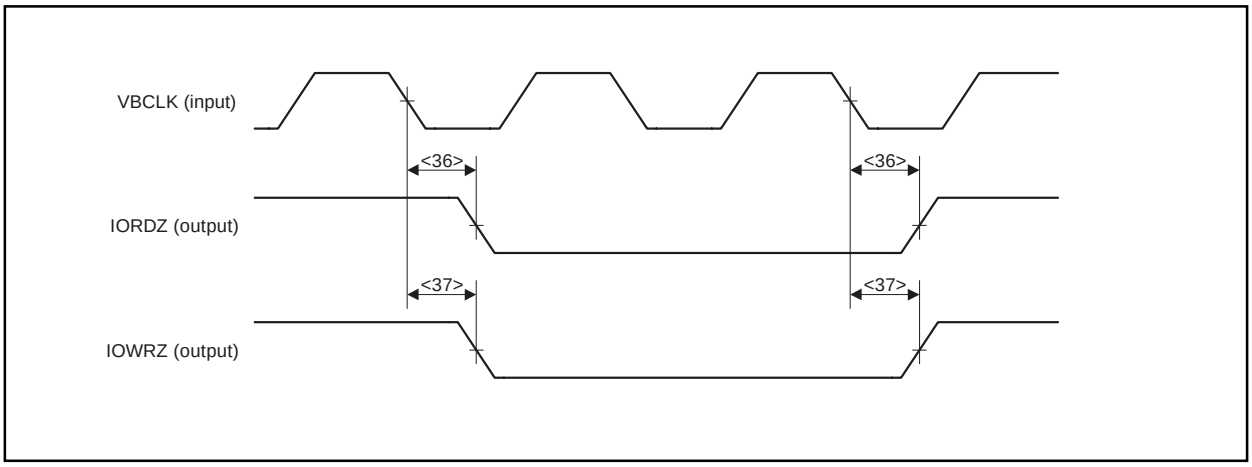
(9) STOP mode timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
STPRQ setup time (to VBCLK↓)	<33>	t_{SPQS}		0		ns
STPRQ hold time (from VBCLK↑)	<34>	t_{SPQH}		0.7		ns
Delay time from VBCLK↑ to STPAK	<35>	t_{SPAKD}		1.5	4.7	ns



(10) I/O control signal timing

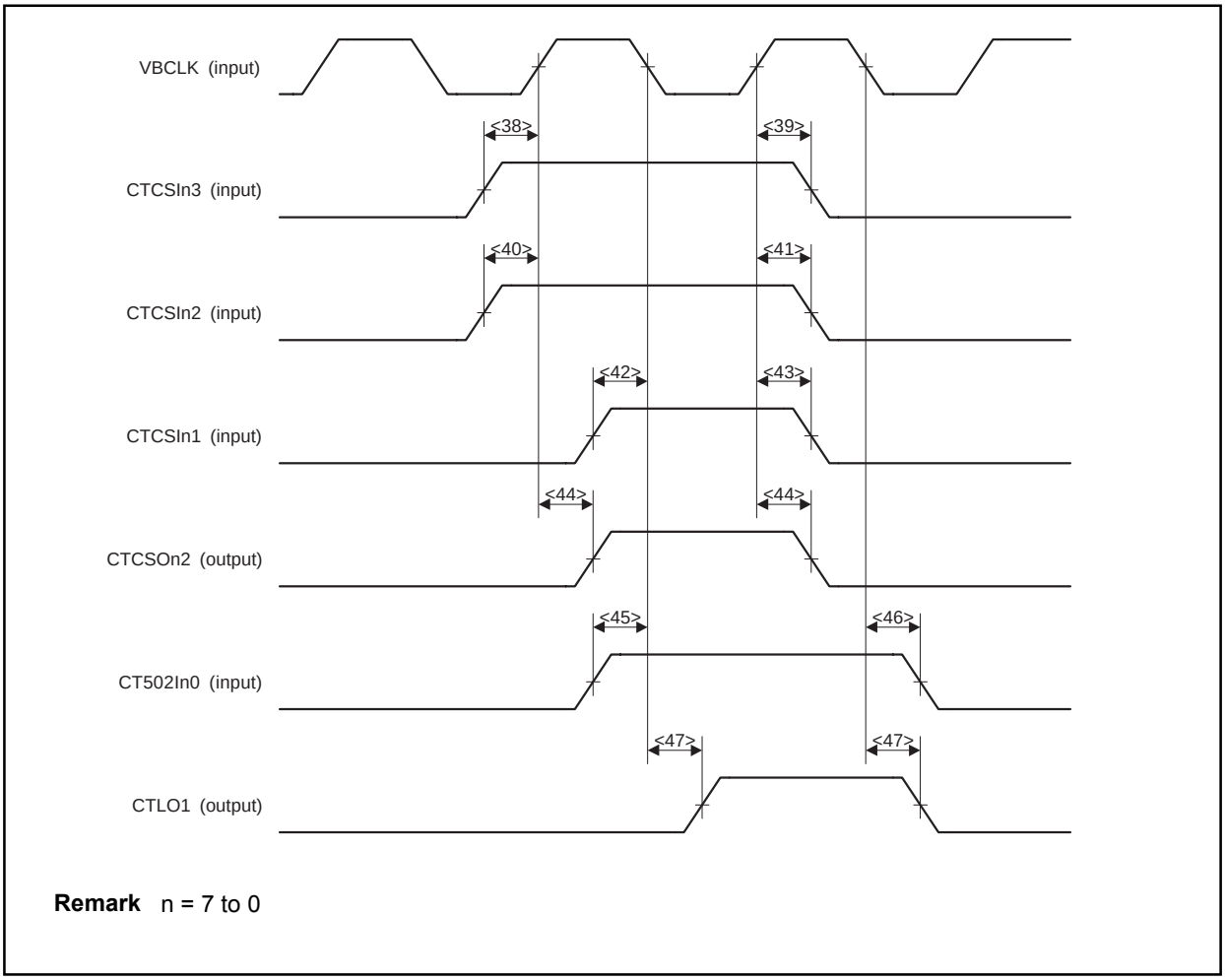
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↓ to IORDZ	<36>	t_{IORD}	During DMA flyby transfer	1.6	5.1	ns
Delay time from VBCLK↓ to IOWRZ	<37>	t_{IOWD}	During DMA flyby transfer	1.6	5.1	ns



(11) NU85E502 connection signal timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
CTCSIn3 setup time (to VBCLK↑)	<38>	t_{CSI3S}		0.5		ns
CTCSIn3 hold time (from VBCLK↑)	<39>	t_{CSI3H}		0.6		ns
CTCSIn2 setup time (to VBCLK↑)	<40>	t_{CSI2S}		0.9		ns
CTCSIn2 hold time (from VBCLK↑)	<41>	t_{CSI2H}		0.5		ns
CTCSIn1 setup time (to VBCLK↓)	<42>	t_{CSI1S}		0		ns
CTCSIn1 hold time (from VBCLK↑)	<43>	t_{CSI1H}		0.9		ns
Delay time from VBCLK↑ to CTCSOn2	<44>	t_{CSO2D}		1.5	5.0	ns
CT502In0 setup time (to VBCLK↓)	<45>	t_{C2I0S}		0		ns
CT502In0 hold time (from VBCLK↓)	<46>	t_{C2I0H}		0.5		ns
Delay time from VBCLK↓ to CTLO1	<47>	t_{CTL1D}		1.6	5.2	ns

Remark n = 7 to 0



Remark n = 7 to 0

(12) VSB timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VBA setup time (to VBCLK↑)	–	t_{VBAS1}	When using page ROM	0		ns
VBA hold time (from VBCLK↑)	–	t_{VBAH1}	When using page ROM	1.0		ns
VDCSZ setup time (to VBCLK↓)	–	t_{CSZS1}		2.0		ns
VDCSZ hold time (from VBCLK↑)	–	t_{CSZH1}		0.6		ns
VBWRITE setup time (to VBCLK↓)	–	t_{VBWRS1}		0		ns
VBWRITE hold time (from VBCLK↓)	–	t_{VBWRH1}		1.3		ns
VBBENZ setup time (to VBCLK↓)	–	t_{BENZS1}		0		ns
VBBENZ hold time (from VBCLK↓)	–	t_{BENZH1}		1.3		ns
VBCTYP setup time (to VBCLK↓)	–	t_{CTYPS1}		0.8		ns
VBCTYP hold time (from VBCLK↓)	–	t_{CTYPH1}		0.7		ns
VBSEQ setup time (to VBCLK↓)	–	t_{SEQS1}		0.9		ns
VBSEQ hold time (from VBCLK↑)	–	t_{SEQH1}		1.1		ns
VBSTZ setup time (to VBCLK↓)	–	t_{STZS1}		0		ns
VBSTZ hold time (from VBCLK↑)	–	t_{STZH1}		1.2		ns

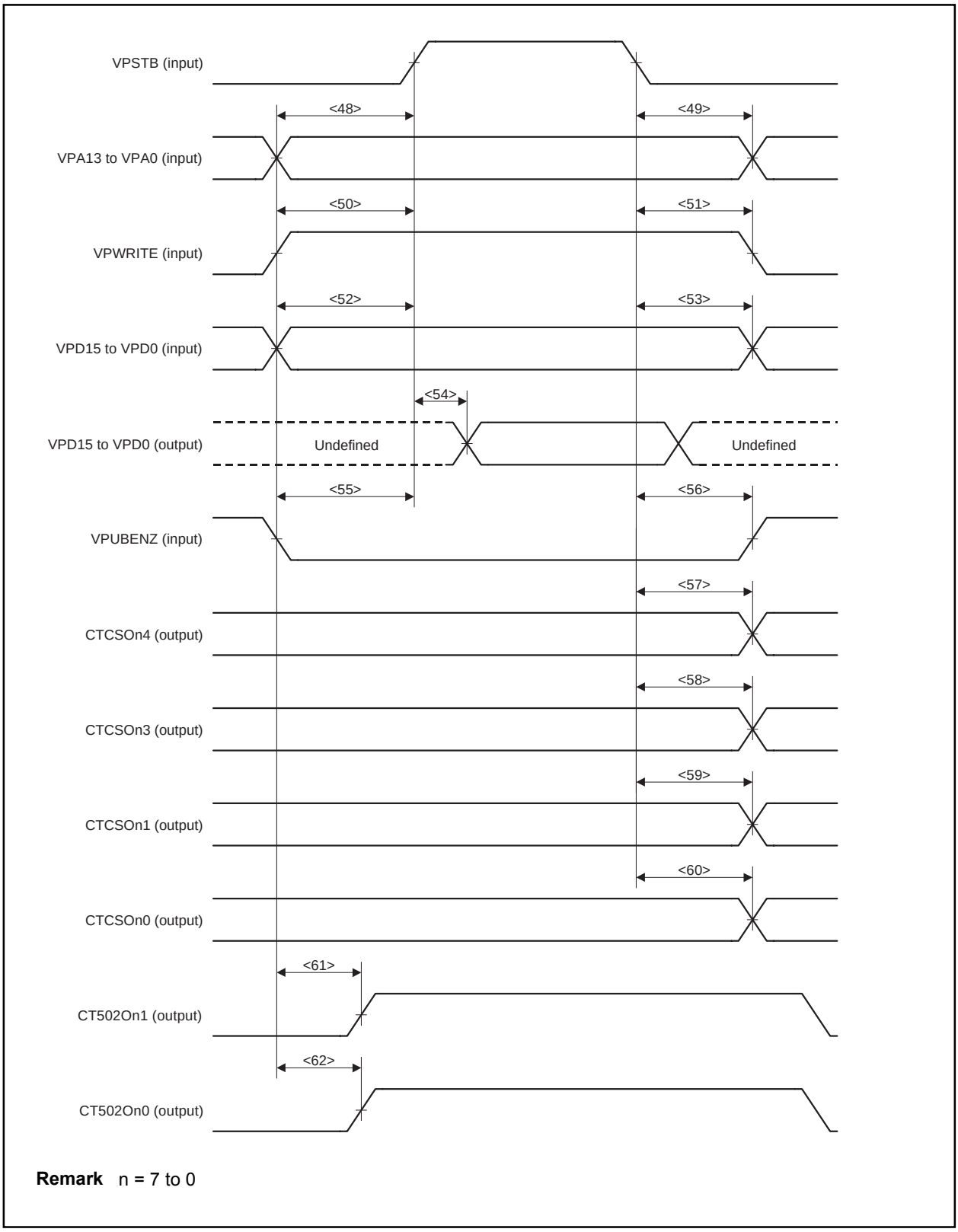
[MEMO]

(13) NPB timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VPA address setup time (to VPSTB↑)	<48>	t_{VPAS}		20		ns
VPA address hold time (from VPSTB↓)	<49>	t_{VPAH}		20		ns
VPWRITE setup time (to VPSTB↑)	<50>	t_{VPWRS}		20		ns
VPWRITE hold time (from VPSTB↓)	<51>	t_{VPWRH}		20		ns
VPD data setup time (to VPSTB↑)	<52>	t_{VPDS}		20		ns
VPD data hold time (from VPSTB↓)	<53>	t_{VPDH}		20		ns
Delay time from VPSTB↑ to VPD data	<54>	t_{VPDD}		1.1	9.5	ns
VPUBENZ setup time (to VPSTB↑)	<55>	t_{VPUBS}		20		ns
VPUBENZ hold time (from VPSTB↓)	<56>	t_{VPUBH}		20		ns
Delay time from VPSTB↓ to CTCSOn4	<57>	t_{CSO4D}			5	ns
Delay time from VPSTB↓ to CTCSOn3	<58>	t_{CSO3D}			5	ns
Delay time from VPSTB↓ to CTCSOn1	<59>	t_{CSO1D}			5	ns
Delay time from VPSTB↓ to CTCSOn0	<60>	t_{CSO0D}			5	ns
Delay time from VPA address to CT502On1	<61>	t_{C2O1D}			5	ns
Delay time from VPA address to CT502On0	<62>	t_{C2O0D}			5	ns

Remark n = 7 to 0

(13) NPB timing (2/2)



Remark n = 7 to 0

CHAPTER 11 NU85E500

(Under Development)

The NU85E500 is used as follows according to the type of external memory that is connected.

Target CPU Core	Types of Connected External Memory	Memory Controller (MEMC)
NB85E	SRAM, ROM, page ROM, flash memory	NU85E500
	SDRAM	NU85E500 + NU85E502

Remark For details of the NU85E502, refer to **CHAPTER 12 NU85E502**.

11. 1 Outline

The NU85E500 is a basic core macro used to control external memory. It features on chip SRAM, and I/O controller, and a page ROM controller.

The NU85E500 can be used to start the external bus cycle when it is connected to the NB85E via VSB.

It can also be used to control SDRAM by connecting an SDRAM controller (NU85E502) to the NU85E500.

11. 1. 1 Symbol diagram

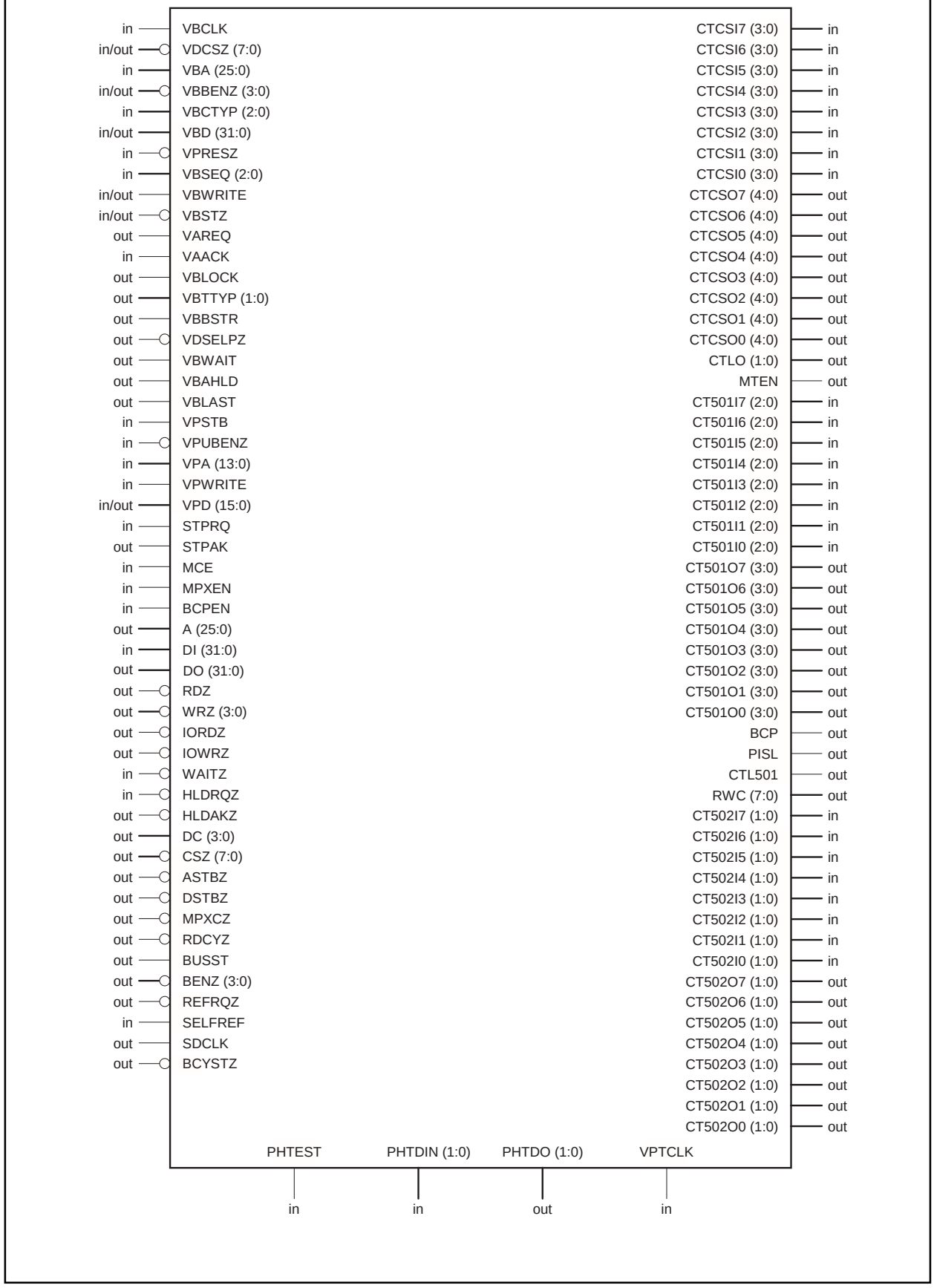
Number of grids

35.6k grids

106.0k grids (including wiring area)

Number of separation simulation patterns

14.3k


in VBCLK
in/out VDCSZ (7:0)
in VBA (25:0)
in/out VBBENZ (3:0)
in VBCTYP (2:0)
in/out VBD (31:0)
in VPRESZ
in VBSEQ (2:0)
in/out VBWRITE
in/out VBSTZ
out VAREQ
in VAACK
out VBLOCK
out VBTTYP (1:0)
out VBBSTR
out VDSELPZ
out VBWAIT
out VBAHLD
out VBLAST
in VPSTB
in VPUBENZ
in VPA (13:0)
in VPWRITE
in/out VPD (15:0)
in STPRQ
out STPAK
in MCE
in MPXEN
in BCPEN
out A (25:0)
in DI (31:0)
out DO (31:0)
out RDZ
out WRZ (3:0)
out IORDZ
out IOWRZ
in WAITZ
in HLDRQZ
out HLDAKZ
out DC (3:0)
out CSZ (7:0)
out ASTBZ
out DSTBZ
out MPXCZ
out RDCYZ
out BUSST
out BENZ (3:0)
out REFRQZ
in SELFREF
out SDCLK
out BCYSTZ
CTCSI7 (3:0) in
CTCSI6 (3:0) in
CTCSI5 (3:0) in
CTCSI4 (3:0) in
CTCSI3 (3:0) in
CTCSI2 (3:0) in
CTCSI1 (3:0) in
CTCSI0 (3:0) in
CTCSO7 (4:0) out
CTCSO6 (4:0) out
CTCSO5 (4:0) out
CTCSO4 (4:0) out
CTCSO3 (4:0) out
CTCSO2 (4:0) out
CTCSO1 (4:0) out
CTCSO0 (4:0) out
CTLO (1:0) out
MTEN out
CT501I7 (2:0) in
CT501I6 (2:0) in
CT501I5 (2:0) in
CT501I4 (2:0) in
CT501I3 (2:0) in
CT501I2 (2:0) in
CT501I1 (2:0) in
CT501I0 (2:0) in
CT501O7 (3:0) out
CT501O6 (3:0) out
CT501O5 (3:0) out
CT501O4 (3:0) out
CT501O3 (3:0) out
CT501O2 (3:0) out
CT501O1 (3:0) out
CT501O0 (3:0) out
BCP out
PISL out
CTL501 out
RWC (7:0) out
CT502I7 (1:0) in
CT502I6 (1:0) in
CT502I5 (1:0) in
CT502I4 (1:0) in
CT502I3 (1:0) in
CT502I2 (1:0) in
CT502I1 (1:0) in
CT502I0 (1:0) in
CT502O7 (1:0) out
CT502O6 (1:0) out
CT502O5 (1:0) out
CT502O4 (1:0) out
CT502O3 (1:0) out
CT502O2 (1:0) out
CT502O1 (1:0) out
CT502O0 (1:0) out
PHTEST in
PHTDIN (1:0) in
PHTDO (1:0) out
VPTCLK in

11. 1. 2 Pin capacitance

Remark C_{IN}: Capacitance of only input pin

C_{inewl}: Value of C_{IN} with wiring capacitance (estimated wire length capacitance) taken into consideration (l = 10 mm)

(1) Input pins (1/3)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
VBCLK	0.135	2.035	VAACK	0.157	2.057
VBA25	0.051	1.951	VPSTB	0.017	1.917
VBA24	0.120	2.020	VPUBENZ	0.036	1.936
VBA23	0.140	2.040	VPA13	0.013	1.913
VBA22	0.166	2.066	VPA12	0.016	1.916
VBA21	0.133	2.033	VPA11	0.014	1.914
VBA20	0.101	2.001	VPA10	0.016	1.916
VBA19	0.166	2.066	VPA9	0.013	1.913
VBA18	0.014	1.914	VPA8	0.020	1.920
VBA17	0.106	2.006	VPA7	0.015	1.915
VBA16	0.494	2.394	VPA6	0.037	1.937
VBA15	0.097	1.997	VPA5	0.015	1.915
VBA14	0.091	1.991	VPA4	0.014	1.914
VBA13	0.108	2.008	VPA3	0.013	1.913
VBA12	0.110	2.010	VPA2	0.021	1.921
VBA11	0.056	1.956	VPA1	0.013	1.913
VBA10	0.129	2.029	VPA0	0.016	1.916
VBA9	0.100	2.000	VPWRITE	0.012	1.912
VBA8	0.163	2.063	STPRQ	0.161	2.061
VBA7	0.143	2.043	MCE	0.110	2.010
VBA6	0.021	1.921	BCPEN	0.113	2.013
VBA5	0.189	2.089	DI31	0.027	1.927
VBA4	0.054	1.954	DI30	0.018	1.918
VBA3	0.119	2.019	DI29	0.025	1.925
VBA2	0.025	1.925	DI28	0.019	1.919
VBA1	0.131	2.031	DI27	0.018	1.918
VBA0	0.161	2.061	DI26	0.024	1.924
VBCTYP2	0.017	1.917	DI25	0.018	1.918
VBCTYP1	0.022	1.922	DI24	0.022	1.922
VBCTYP0	0.018	1.918	DI23	0.022	1.922
VPRESZ	0.013	1.913	DI22	0.026	1.926
VBSEQ2	0.016	1.916	DI21	0.032	1.932
VBSEQ1	0.023	1.923	DI20	0.024	1.924
VBSEQ0	0.022	1.922	DI19	0.029	1.929

(1) Input pins (2/3)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
DI18	0.020	1.920	CTCSI32	0.026	1.926
DI17	0.016	1.916	CTCSI31	0.039	1.939
DI16	0.014	1.914	CTCSI30	0.237	2.137
DI15	0.026	1.926	CTCSI23	0.063	1.963
DI14	0.024	1.924	CTCSI22	0.126	2.026
DI13	0.040	1.940	CTCSI21	0.287	2.187
DI12	0.034	1.934	CTCSI20	0.212	2.112
DI11	0.018	1.918	CTCSI13	0.143	2.043
DI10	0.023	1.923	CTCSI12	0.031	1.931
DI9	0.055	1.955	CTCSI11	0.037	1.937
DI8	0.030	1.930	CTCSI10	0.196	2.096
DI7	0.020	1.920	CTCSI03	0.243	2.143
DI6	0.020	1.920	CTCSI02	0.171	2.071
DI5	0.024	1.924	CTCSI01	0.165	2.065
DI4	0.017	1.917	CTCSI00	0.151	2.051
DI3	0.023	1.923	CT502I71	0.017	1.917
DI2	0.025	1.925	CT502I70	0.234	2.134
DI1	0.028	1.928	CT502I61	0.097	1.997
DI0	0.014	1.914	CT502I60	0.094	1.994
WAITZ	0.063	1.963	CT502I51	0.029	1.929
HLDRQZ	0.051	1.951	CT502I50	0.201	2.101
SELFREF	0.184	2.084	CT502I41	0.055	1.955
CTCSI73	0.491	2.391	CT502I40	0.070	1.970
CTCSI72	0.167	2.067	CT502I31	0.227	2.127
CTCSI71	0.130	2.030	CT502I30	0.098	1.998
CTCSI70	0.151	2.051	CT502I21	0.020	1.920
CTCSI63	0.068	1.968	CT502I20	0.181	2.081
CTCSI62	0.018	1.918	CT502I11	0.022	1.922
CTCSI61	0.018	1.918	CT502I10	0.118	2.018
CTCSI60	0.157	2.057	CT502I01	0.015	1.915
CTCSI53	0.198	2.098	CT502I00	0.211	2.111
CTCSI52	0.023	1.923	PHTEST	0.076	1.976
CTCSI51	0.102	2.002	PHTDIN1	0.034	1.934
CTCSI50	0.124	2.024	PHTDIN0	0.054	1.954
CTCSI43	0.089	1.989	VPTCLK	0.064	1.964
CTCSI42	0.076	1.976	MPXEN	0.117	2.017
CTCSI41	0.017	1.917	CT501I72	0.066	1.966
CTCSI40	0.267	2.167	CT501I71	0.096	1.996
CTCSI33	0.069	1.969	CT501I70	0.293	2.193

(1) Input pins (3/3)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
CT501I62	0.044	1.944	CT501I30	0.273	2.173
CT501I61	0.044	1.944	CT501I22	0.318	2.218
CT501I60	0.042	1.942	CT501I21	0.094	1.994
CT501I52	0.360	2.260	CT501I20	0.043	1.943
CT501I51	0.121	2.021	CT501I12	0.066	1.966
CT501I50	0.064	1.964	CT501I11	0.123	2.023
CT501I42	0.358	2.258	CT501I10	0.078	1.978
CT501I41	0.077	1.977	CT501I02	0.262	2.162
CT501I40	0.016	1.916	CT501I01	0.193	2.093
CT501I32	0.055	1.955	CT501I00	0.331	2.231
CT501I31	0.062	1.962			

(2) Output pins (1/3)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
VAREQ	12.885	–	–	A11	13.065	–	–
VBLOCK	6.549	0.084	1.984	A10	13.065	–	–
VBTTYP1	6.581	0.048	1.948	A9	13.068	–	–
VBTTYP0	6.581	0.048	1.948	A8	13.064	–	–
VBBSTR	6.575	0.053	1.953	A7	13.066	–	–
VDSELPZ	6.579	0.050	1.950	A6	13.305	–	–
VBWAIT	6.577	0.051	1.951	A5	13.041	–	–
VBAHLD	6.574	0.054	1.954	A4	13.320	–	–
VBLAST	6.571	0.057	1.957	A3	13.067	–	–
STPAK	12.914	–	–	A2	13.071	–	–
A25	13.066	–	–	A1	13.071	–	–
A24	13.054	–	–	A0	13.058	–	–
A23	13.064	–	–	DO31	13.071	–	–
A22	13.063	–	–	DO30	13.066	–	–
A21	13.069	–	–	DO29	13.071	–	–
A20	13.071	–	–	DO28	13.067	–	–
A19	13.071	–	–	DO27	13.068	–	–
A18	13.063	–	–	DO26	13.069	–	–
A17	13.060	–	–	DO25	13.069	–	–
A16	13.044	–	–	DO24	13.071	–	–
A15	13.069	–	–	DO23	13.061	–	–
A14	13.037	–	–	DO22	13.063	–	–
A13	13.071	–	–	DO21	13.070	–	–
A12	13.045	–	–	DO20	13.062	–	–

(2) Output pins (2/3)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
DO19	13.070	–	–	CSZ0	13.054	–	–
DO18	13.064	–	–	BENZ3	12.962	–	–
DO17	13.071	–	–	BENZ2	12.968	–	–
DO16	13.059	–	–	BENZ1	13.307	–	–
DO15	13.071	–	–	BENZ0	13.328	–	–
DO14	13.062	–	–	BCYSTZ	13.203	–	–
DO13	13.071	–	–	REFRQZ	13.054	–	–
DO12	13.070	–	–	SDCLK	13.071	–	–
DO11	13.071	–	–	CTCSO74	13.335	–	–
DO10	13.070	–	–	CTCSO73	13.332	–	–
DO9	13.071	–	–	CTCSO72	13.118	–	–
DO8	13.070	–	–	CTCSO71	13.338	–	–
DO7	13.071	–	–	CTCSO70	13.335	–	–
DO6	13.068	–	–	CTCSO64	13.338	–	–
DO5	13.062	–	–	CTCSO63	13.334	–	–
DO4	13.071	–	–	CTCSO62	13.039	–	–
DO3	13.068	–	–	CTCSO61	13.274	–	–
DO2	13.062	–	–	CTCSO60	13.335	–	–
DO1	7.907	–	–	CTCSO54	13.329	–	–
DO0	7.904	–	–	CTCSO53	13.337	–	–
RDZ	12.905	–	–	CTCSO52	13.202	–	–
WRZ3	13.175	–	–	CTCSO51	13.332	–	–
WRZ2	13.177	–	–	CTCSO50	13.334	–	–
WRZ1	13.141	–	–	CTCSO44	13.325	–	–
WRZ0	13.187	–	–	CTCSO43	13.291	–	–
IORDZ	13.014	–	–	CTCSO42	13.041	–	–
IOWRZ	12.873	–	–	CTCSO41	13.267	–	–
HLDAKZ	13.338	–	–	CTCSO40	13.336	–	–
DC3	13.320	–	–	CTCSO34	13.311	–	–
DC2	13.035	–	–	CTCSO33	13.311	–	–
DC1	13.048	–	–	CTCSO32	13.279	–	–
DC0	13.071	–	–	CTCSO31	13.331	–	–
CSZ7	13.037	–	–	CTCSO30	13.309	–	–
CSZ6	13.311	–	–	CTCSO24	13.336	–	–
CSZ5	13.035	–	–	CTCSO23	13.311	–	–
CSZ4	12.999	–	–	CTCSO22	12.939	–	–
CSZ3	13.002	–	–	CTCSO21	13.331	–	–
CSZ2	13.071	–	–	CTCSO20	13.330	–	–
CSZ1	13.025	–	–	CTCSO14	13.277	–	–

(2) Output pins (3/3)

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
CTCSO13	13.251	–	–	CT501O63	13.334	–	–
CTCSO12	13.039	–	–	CT501O62	13.256	–	–
CTCSO11	13.324	–	–	CT501O61	13.334	–	–
CTCSO10	13.323	–	–	CT501O60	13.323	–	–
CTCSO04	13.278	–	–	CT501O53	13.336	–	–
CTCSO03	13.255	–	–	CT501O52	13.031	–	–
CTCSO02	12.931	–	–	CT501O51	13.338	–	–
CTCSO01	13.326	–	–	CT501O50	13.108	–	–
CTCSO00	13.324	–	–	CT501O43	13.283	–	–
CTLO1	13.210	–	–	CT501O42	13.248	–	–
CTLO0	13.261	–	–	CT501O41	13.283	–	–
MTEN	13.314	–	–	CT501O40	13.338	–	–
CT502O71	13.224	–	–	CT501O33	13.325	–	–
CT502O70	13.328	–	–	CT501O32	13.333	–	–
CT502O61	13.335	–	–	CT501O31	13.338	–	–
CT502O60	13.338	–	–	CT501O30	13.333	–	–
CT502O51	13.140	–	–	CT501O23	13.334	–	–
CT502O50	13.219	–	–	CT501O22	13.322	–	–
CT502O41	13.334	–	–	CT501O21	13.338	–	–
CT502O40	13.330	–	–	CT501O20	13.328	–	–
CT502O31	13.332	–	–	CT501O13	13.170	–	–
CT502O30	13.324	–	–	CT501O12	13.324	–	–
CT502O21	13.130	–	–	CT501O11	13.319	–	–
CT502O20	13.338	–	–	CT501O10	13.318	–	–
CT502O11	13.332	–	–	CT501O03	13.324	–	–
CT502O10	13.335	–	–	CT501O02	13.228	–	–
CT502O01	13.320	–	–	CT501O01	13.107	–	–
CT502O00	13.325	–	–	CT501O00	13.313	–	–
PHTDO1	13.223	–	–	BCP	13.286	–	–
PHTDO0	13.309	–	–	PISL	13.338	–	–
ASTBZ	13.172	–	–	CTL501	13.308	–	–
DSTBZ	13.161	–	–	RWC7	13.296	–	–
MPXCZ	12.961	–	–	RWC6	13.334	–	–
RDCYZ	13.039	–	–	RWC5	13.323	–	–
BUSST	12.955	–	–	RWC4	13.282	–	–
CT501O73	13.331	–	–	RWC3	13.315	–	–
CT501O72	12.986	–	–	RWC2	13.242	–	–
CT501O71	13.148	–	–	RWC1	13.303	–	–
CT501O70	13.063	–	–	RWC0	13.325	–	–

(3) I/O pins

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
VDCSZ7	6.446	0.183	2.083	VBD12	6.338	0.290	2.190
VDCSZ6	6.374	0.254	2.154	VBD11	6.345	0.284	2.184
VDCSZ5	6.320	0.308	2.208	VBD10	6.344	0.285	2.185
VDCSZ4	6.298	0.331	2.231	VBD9	6.329	0.299	2.199
VDCSZ3	6.211	0.418	2.318	VBD8	6.315	0.314	2.214
VDCSZ2	6.355	0.273	2.173	VBD7	6.329	0.300	2.200
VDCSZ1	6.313	0.316	2.216	VBD6	6.344	0.285	2.185
VDCSZ0	6.477	0.152	2.052	VBD5	6.314	0.315	2.215
VBBENZ3	6.428	0.200	2.100	VBD4	6.318	0.311	2.211
VBBENZ2	6.462	0.166	2.066	VBD3	6.359	0.270	2.170
VBBENZ1	6.489	0.140	2.040	VBD2	6.333	0.296	2.196
VBBENZ0	6.484	0.145	2.045	VBD1	6.366	0.263	2.163
VBD31	6.385	0.244	2.144	VBD0	6.394	0.235	2.135
VBD30	6.375	0.254	2.154	VBWRITE	6.492	0.137	2.037
VBD29	6.383	0.246	2.146	VBSTZ	6.394	0.234	2.134
VBD28	6.366	0.263	2.163	VPD15	6.493	0.188	2.088
VBD27	6.364	0.265	2.165	VPD14	6.555	0.120	2.020
VBD26	6.393	0.236	2.136	VPD13	6.525	0.150	2.050
VBD25	6.390	0.239	2.139	VPD12	6.530	0.145	2.045
VBD24	6.399	0.230	2.130	VPD11	6.504	0.176	2.076
VBD23	6.373	0.256	2.156	VPD10	6.519	0.161	2.061
VBD22	6.394	0.235	2.135	VPD9	6.519	0.161	2.061
VBD21	6.378	0.251	2.151	VPD8	6.537	0.143	2.043
VBD20	6.373	0.256	2.156	VPD7	6.503	0.218	2.118
VBD19	6.373	0.256	2.156	VPD6	6.514	0.207	2.107
VBD18	6.384	0.244	2.144	VPD5	6.508	0.213	2.113
VBD17	6.346	0.282	2.182	VPD4	6.534	0.188	2.088
VBD16	6.366	0.262	2.162	VPD3	6.475	0.246	2.146
VBD15	6.364	0.264	2.164	VPD2	6.478	0.244	2.144
VBD14	6.362	0.266	2.166	VPD1	6.493	0.228	2.128
VBD13	6.348	0.281	2.181	VPD0	6.489	0.233	2.133

11. 2 Initialization of Internal Registers

Before executing the test program, be sure to execute an instruction to assign initial values to the internal registers used in the test program. Failure to this so will result in the propagation of undefined values.

11. 3 Pin Functions

(1/3)

Pin Name		I/O	Function
NB85E connection pins	VBCLK	Input	Internal system clock input
	VDCSZ7 to VDCSZ0	I/O	Chip select I/O
	VBA25 to VBA0	Input	Address input
	VBBENZ3 to VBBENZ0	I/O	Byte enable I/O
	VBCTYP2 to VBCTYP0	Input	Bus cycle status input
	VBD31 to VBD0	I/O	Data I/O
	VPRESZ	Input	Reset input
	VBSEQ2 to VBSEQ0	Input	Sequential status input
	VBWRITE	I/O	Read/write status I/O
	VBSTZ	I/O	Transfer start I/O
	VAREQ	Output	Bus access right request output
	VAACK	Input	Bus access right acknowledge input
	VBLOCK	Output	Bus lock output
	VBTTYP1, VBTTYP0	Output	Bus transfer type output
	VBBSTR	Output	Burst read status output
	VDSELPZ	Output	Peripheral I/O area access status output
	VBWAIT	Output	Wait response output
	VBAHLD	Output	Address hold response output
	VBLAST	Output	Last response output
	VPSTB	Input	Data strobe input (for NPB)
	VPUBENZ	Input	Upper byte enable input (for NPB)
	VPA13 to VPA0	Input	Address input (for NPB)
	VPWRITE	Input	Write access strobe input (for NPB)
	VPD15 to VPD0	I/O	Data I/O (for NPB)
	STPRQ	Input	STOP mode request input
	STPAK	Output	Acknowledge output for STPRQ input
Initial setting pins	MCE	Input	MEn bit reset value control input for BCT register (n = 7 to 0)
	BCPEN	Input	BCP bit reset value control input for BCP register
External memory connection pins	A25 to A0	Output	External memory address output
	DI31 to DI0	Input	External memory data input
	DO31 to DO0	Output	External memory data output
	RDZ	Output	SRAM/page ROM read strobe output
	WRZ3 to WRZ0	Output	SRAM/page ROM write strobe output
	IORDZ	Output	External I/O read strobe output
	IOWRZ	Output	External I/O write strobe output
	WAITZ	Input	Wait request input

(2/3)

Pin Name		I/O	Function
External memory connection pins	HLDRQZ	Input	External bus hold request input
	HLDAKZ	Output	External bus hold request acknowledge output
	DC3 to DC0	Output	Data bus control output
	CSZ7 to CSZ0	Output	Chip select output
	BENZ3 to BENZ0	Output	Byte enable output
	BCYSTZ	Output	Bus cycle start status output
	REFRQZ	Output	Refresh status output
	SELFREF	Input	Self refresh request input
	SDCLK	Output	SDRAM sync clock output
NU85E502 connection pins	CTCSI73 to CTCSI70	Input	Control input from NU85E502 (for CS7 area)
	CTCSI63 to CTCSI60	Input	Control input from NU85E502 (for CS6 area)
	CTCSI53 to CTCSI50	Input	Control input from NU85E502 (for CS5 area)
	CTCSI43 to CTCSI40	Input	Control input from NU85E502 (for CS4 area)
	CTCSI33 to CTCSI30	Input	Control input from NU85E502 (for CS3 area)
	CTCSI23 to CTCSI20	Input	Control input from NU85E502 (for CS2 area)
	CTCSI13 to CTCSI10	Input	Control input from NU85E502 (for CS1 area)
	CTCSI03 to CTCSI00	Input	Control input from NU85E502 (for CS0 area)
	CTCSO74 to CTCSO70	Output	Control output to NU85E502 (for CS7 area)
	CTCSO64 to CTCSO60	Output	Control output to NU85E502 (for CS6 area)
	CTCSO54 to CTCSO50	Output	Control output to NU85E502 (for CS5 area)
	CTCSO44 to CTCSO40	Output	Control output to NU85E502 (for CS4 area)
	CTCSO34 to CTCSO30	Output	Control output to NU85E502 (for CS3 area)
	CTCSO24 to CTSO20	Output	Control output to NU85E502 (for CS2 area)
	CTCSO14 to CTCSO10	Output	Control output to NU85E502 (for CS1 area)
	CTCSO04 to CTCSO00	Output	Control output to NU85E502 (for CS0 area)
	CTLO1, CTLO0	Output	Control output to NU85E502
	MTEN	Output	Test mode enable output to NU85E502
	CT502I71, CT502I70	Input	Control input from NU85E502 (for CS7 area)
	CT502I61, CT502I60	Input	Control input from NU85E502 (for CS6 area)
	CT502I51, CT502I50	Input	Control input from NU85E502 (for CS5 area)
	CT502I41, CT502I40	Input	Control input from NU85E502 (for CS4 area)
	CT502I31, CT502I30	Input	Control input from NU85E502 (for CS3 area)
	CT502I21, CT502I20	Input	Control input from NU85E502 (for CS2 area)
	CT502I11, CT502I10	Input	Control input from NU85E502 (for CS1 area)
	CT502I01, CT502I00	Input	Control input from NU85E502 (for CS0 area)

(3/3)

Pin Name		I/O	Function
NU85E502 connection pins	CT502O71, CT502O70	Output	Control output to NU85E502 (for CS7 area)
	CT502O61, CT502O60	Output	Control output to NU85E502 (for CS6 area)
	CT502O51, CT502O50	Output	Control output to NU85E502 (for CS5 area)
	CT502O41, CT502O40	Output	Control output to NU85E502 (for CS4 area)
	CT502O31, CT502O30	Output	Control output to NU85E502 (for CS3 area)
	CT502O21, CT502O20	Output	Control output to NU85E502 (for CS2 area)
	CT502O11, CT502O10	Output	Control output to NU85E502 (for CS1 area)
	CT502O01, CT502O00	Output	Control output to NU85E502 (for CS0 area)
Test mode pins	PHTEST	Input	Peripheral test mode status input
	PHTDIN1, PHTDIN0	Input	Peripheral macro test input
	PHTDO1, PHTDO0	Output	Peripheral macro test output
	VPTCLK	Input	Test clock input
NEC reserved pins	MPXEN	Input	NEC reserved pin (input a low level)
	ASTBZ	Output	NEC reserved pin (leave open)
	DSTBZ	Output	NEC reserved pin (leave open)
	MPXCZ	Output	NEC reserved pin (leave open)
	RDCYZ	Output	NEC reserved pin (leave open)
	BUSST	Output	NEC reserved pin (leave open)
	CT501I72 to CT501I70	Input	NEC reserved pin (input a low level)
	CT501I62 to CT501I60	Input	NEC reserved pin (input a low level)
	CT501I52 to CT501I50	Input	NEC reserved pin (input a low level)
	CT501I42 to CT501I40	Input	NEC reserved pin (input a low level)
	CT501I32 to CT501I30	Input	NEC reserved pin (input a low level)
	CT501I22 to CT501I20	Input	NEC reserved pin (input a low level)
	CT501I12 to CT501I10	Input	NEC reserved pin (input a low level)
	CT501I02 to CT501I00	Input	NEC reserved pin (input a low level)
	CT501O73 to CT501O70	Output	NEC reserved pin (leave open)
	CT501O63 to CT501O60	Output	NEC reserved pin (leave open)
	CT501O53 to CT501O50	Output	NEC reserved pin (leave open)
	CT501O43 to CT501O40	Output	NEC reserved pin (leave open)
	CT501O33 to CT501O30	Output	NEC reserved pin (leave open)
	CT501O23 to CT501O20	Output	NEC reserved pin (leave open)
	CT501O13 to CT501O10	Output	NEC reserved pin (leave open)
	CT501O03 to CT501O00	Output	NEC reserved pin (leave open)
	BCP	Output	NEC reserved pin (leave open)
	PISL	Output	NEC reserved pin (leave open)
	CTL501	Output	NEC reserved pin (leave open)
	RWC7 to RWC0	Output	NEC reserved pin (leave open)

11. 4 Electrical Specifications (Preliminary)

The following specifications are for a single macro. An actual chip consists of two or more macros. Design the system so that all the specifications of the individual macros are satisfied when the chip is used.

11. 4. 1 Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to +4.6	V
Operating ambient temperature	T_A	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

11. 4. 2 Recommended operation range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	−40		+85	°C
Clock cycle	t_{CYK}	15.0			ns

11. 4. 3 DC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1}	In normal operation mode		0.18	0.27	mA/MHz
	I_{DD2}	In STOP mode		0	1.0	μA

Remarks 1. The above supply current value is a reference value calculated from the number of grids.

2. The TYP. value is a reference value for when T_A = 25°C, V_{DD} = 3.3 V.

11. 4. 4 AC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

(1) SRAM/page ROM read timing (1/3)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VBCLK input cycle	<1>	t_{CYK}		15.0		ns
Delay time from VBCLK↑ to address	<2>	t_{AD}		t_{DKA} + 0.7[Note]	t_{DKA} + 3.4[Note]	ns
Delay time from VBCLK↑ to CSZ	<3>	t_{CSZD1}		t_{DKC} + 0.8[Note]	t_{DKC} + 3.4[Note]	ns
Delay time from VBCLK↓ to RDZ	<4>	t_{RDZD1}		2.1	6.2	ns
Delay time from VBCLK↑ to RDZ	<5>	t_{RDZD2}		1.9	5.3	ns
Data setup time (to VBCLK↑)	<6>	t_{DIS}		0		ns
Data hold time (from VBCLK↑)	<7>	t_{DIH}		1.5		ns
Delay time from VBCLK↑ to BCYSTZ	<8>	t_{BCYD}		1.7	t_{DKS1} + 1.8[Note]	ns
WAITZ setup time (to VBCLK↑)	<9>	t_{WTS}		0		ns
WAITZ hold time (from VBCLK↑)	<10>	t_{WTH}		1.3		ns
Delay time from VBCLK↓ to VBWAIT, VBAHLD, VBLAST	<11>	t_{VRD1}			5.9	ns
Delay time from VBCLK↑ to VBWAIT, VBAHLD, VBLAST	<12>	t_{VRD2}		1.6		ns
Delay time from VBCLK↑ to VBD	<13>	t_{VBD1}			6.5	ns
Delay time from VBCLK↓ to VBD	<14>	t_{VBD2}		1.7		ns
Delay time from VBCLK↑ to DC	<15>	t_{DCD1}		t_{DKS1} + 0.8[Note]	t_{DKS1} + 2.9[Note]	ns

Note t_{DKA}: Delay time from VBCLK↑ to VBA

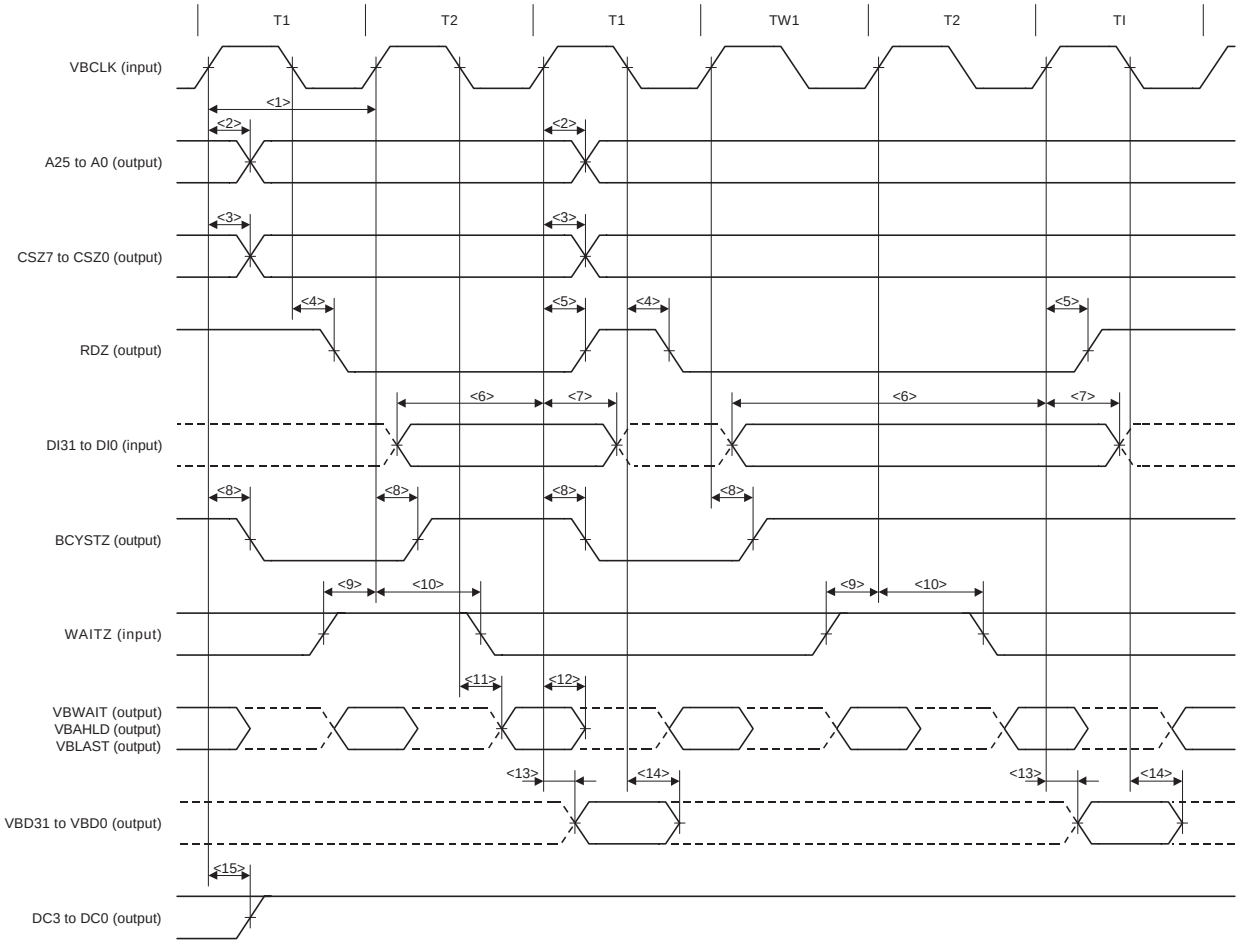
t_{DKC}: Delay time from VBCLK↑ to VDCSZ, VDSELPZ

t_{DKS1}: Delay time from VBCLK↑ to VBSTZ, VBSIZE, VBWRITE, VBCTYP

The above are the electrical specifications of the NB85E. Refer to section **7. 4. 4 AC characteristics**.

(1) SRAM/page ROM read timing (2/3)

(a) When wait is inserted



Remarks 1. T1, T2: Basic state in which NU85E500 access is performed

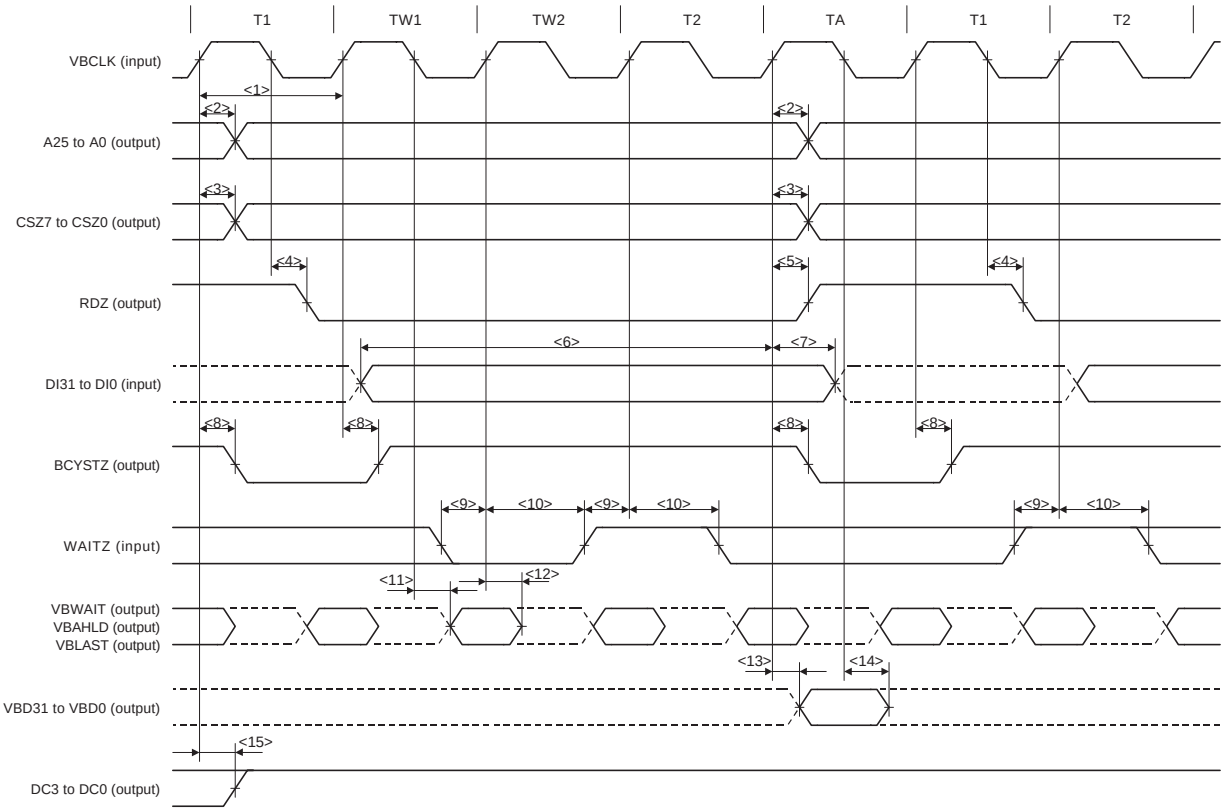
TW1: Wait state inserted by setting data wait control registers 0, 1 (DWC0, DWC1)

TI: Idle state inserted by setting bus cycle control register (BCC)

2. The level of the broken line portion of the DI31 to DI0 signals is undefined. The level of the broken line portion of the VBWAIT, VBAHLD, VBLAST, and VBD31 to VBD0 signals indicates the undefined state (weak unknown) in which the bus holder in the NB85E is driving.

(1) SRAM/page ROM read timing (3/3)

(b) When address setting wait is inserted



Remarks 1. T1, T2: Basic state in which NU85E500 access is performed

TW1: Wait state inserted by setting data wait control registers 0, 1 (DWC0, DWC1)

TW2: Wait state through WAITZ pin input

TA: Address setting wait state inserted by setting the address setting wait control register (ASC)

2. The level of the broken line portion of the DI31 to DI0 signals is undefined. The level of the broken line portion of the VBWAIT, VBAHLD, VBLAST, and VBD31 to VBD0 signals indicates the undefined state (weak unknown) in which the bus holder in the NB85E is driving.

(2) SRAM write timing (1/3)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VBCLK input cycle	<1>	t_{CYK}		15.0		ns
Delay time from VBCLK↑ to address	<2>	t_{AD}		t_{DKA} + 0.7[Note]	t_{DKA} + 3.4[Note]	ns
Delay time from VBCLK↑ to CSZ	<3>	t_{CSZD1}		t_{DKC} + 0.8[Note]	t_{DKC} + 3.4[Note]	ns
Delay time from VBCLK↑ to BCYSTZ	<8>	t_{BCYD}		1.7	t_{DKS1} + 1.8[Note]	ns
WAITZ setup time (to VBCLK↑)	<9>	t_{WTS}		0		ns
WAITZ hold time (from VBCLK↑)	<10>	t_{WTH}		1.3		ns
Delay time from VBCLK↓ to VBWAIT, VBAHLD, VBLAST	<11>	t_{VRD1}			5.9	ns
Delay time from VBCLK↑ to VBWAIT, VBAHLD, VBLAST	<12>	t_{VRD2}		1.6		ns
Delay time from VBCLK↓ to DC	<16>	t_{DCD2}		1.9	5.9	ns
Delay time from VBCLK↓ to WRZ	<17>	t_{WRZD}		2.0	5.6	ns
Delay time from VBCLK↓ to data	<18>	t_{DOD1}		t_{DKD1} + 0.3[Note]	t_{DKD1} + 1.7[Note]	ns
Delay time from VBCLK↑ to data	<19>	t_{DOD2}		t_{DKD0} + 0.3[Note]	t_{DKD0} + 1.7[Note]	ns
Delay time from VBBENZ to BENZ	–	t_{BNZD}		0.5	2.2	ns

Note t_{DKA}: Delay time from VBCLK↑ to VBA

t_{DKC}: Delay time from VBCLK↑ to VDCSZ, VDSELPZ

t_{DKS1}: Delay time from VBCLK↑ to VBSTZ, VBSIZE, VBWRITE, VBCTYP

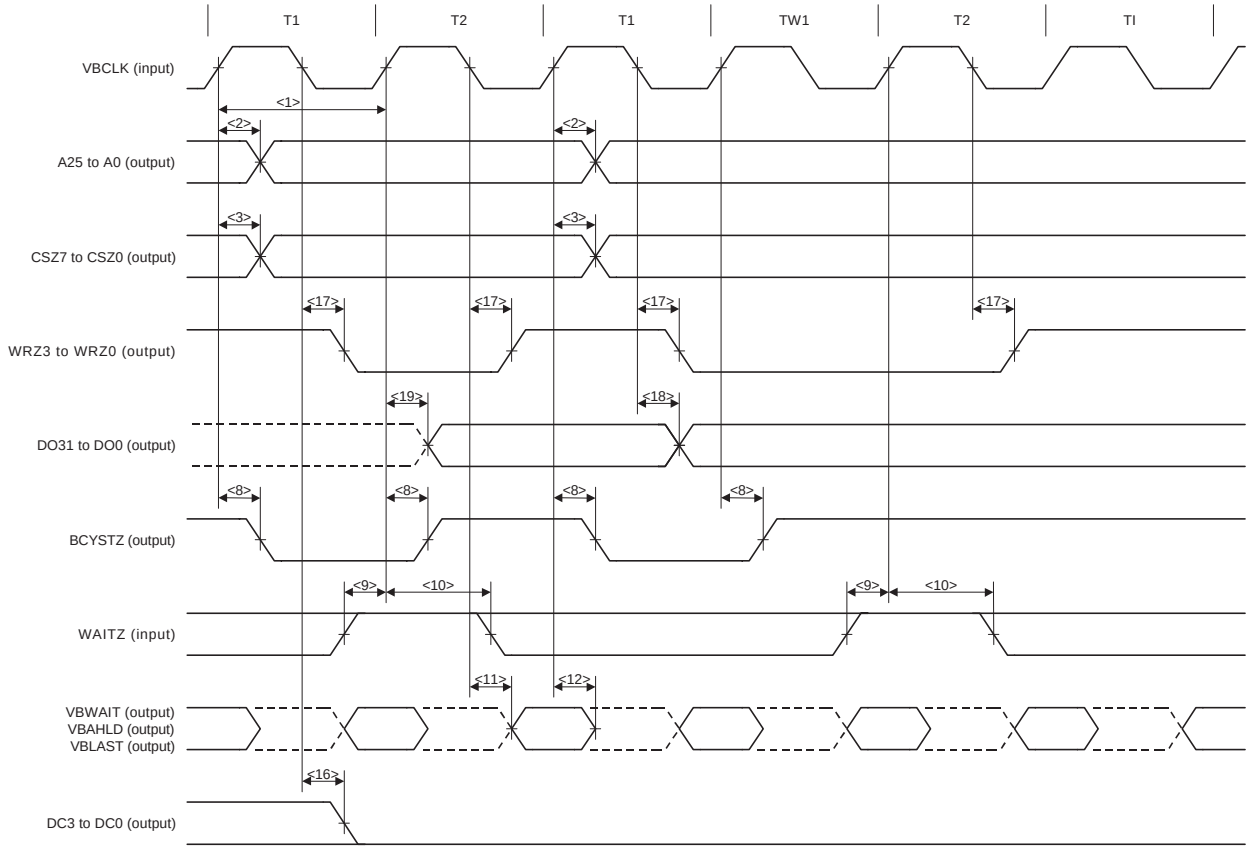
t_{DKD1}: Delay time from VBCLK↓ to VBD data

t_{DKD0}: Delay time from VBCLK↑ to VBD data

The above are the electrical specifications of the NB85E. Refer to section **7. 4. 4 AC characteristics**.

(2) SRAM write timing (2/3)

(a) When wait is inserted



Remarks 1. T1, T2: Basic state in which NU85E500 access is performed

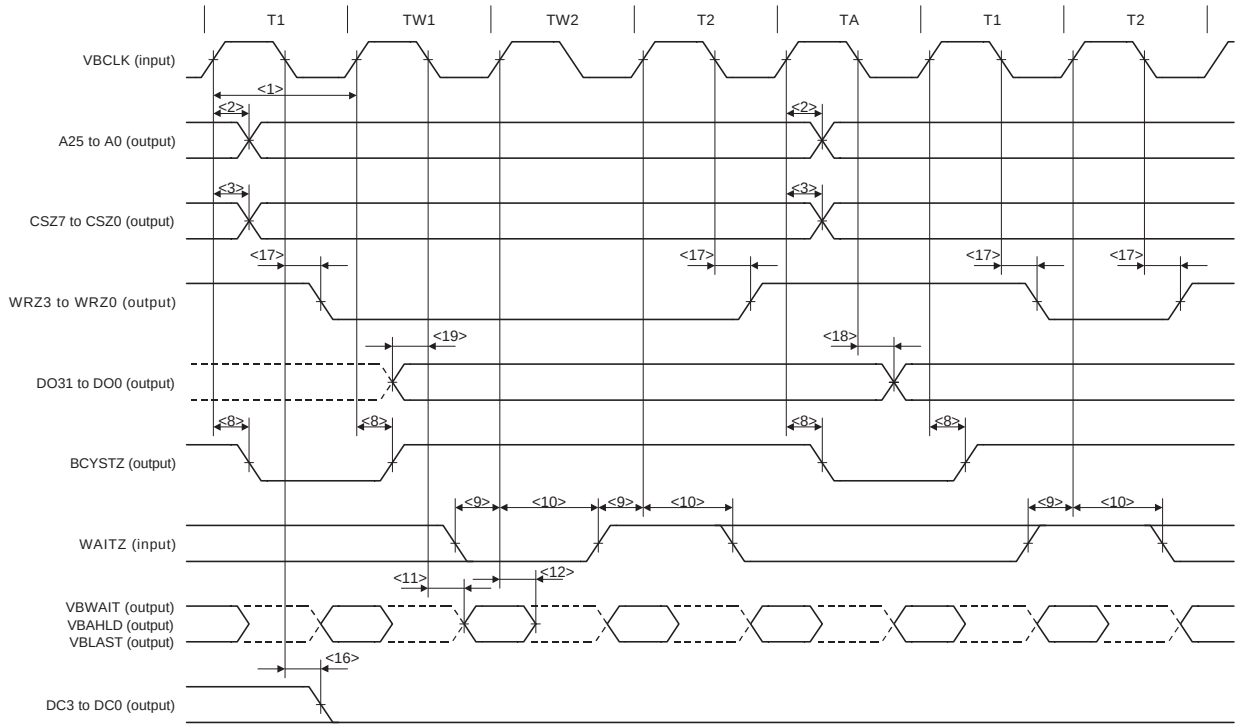
TW1: Wait state inserted by setting data wait control registers 0, 1 (DWC0, DWC1)

TI: Idle state inserted by setting bus cycle control register (BCC)

2. The level of the broken line portion of the DO31 to DO0 signals is undefined. The level of the broken line portion of the VBWAIT, VBAHLD, and VBLAST signals indicates undefined state (weak unknown) in which the bus holder in the NB85E is driving.

(2) SRAM write timing (3/3)

(b) When address setting wait is inserted



Remarks 1. T1, T2: Basic state in which NU85E500 access is performed

TW1: Wait state inserted by setting data wait control registers 0, 1 (DWC0, DWC1)

TW2: Wait state through WAITZ pin input

TA: Address setting wait state inserted by setting the address setting wait control register (ASC)

2. The level of the broken line portion of the DO31 to DO0 signals is undefined. The level of the broken line portion of the VBWAIT, VBAHLD, and VBLAST signals indicates undefined state (weak unknown) in which the bus holder in the NB85E is driving.

(3) SRAM read/write timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VBCLK input cycle	<1>	t_{CYK}		15.0		ns
Delay time from VBCLK↑ to address	<2>	t_{AD}		t_{DKA} + 0.7[Note]	t_{DKA} + 3.4[Note]	ns
Delay time from VBCLK↑ to CSZ	<3>	t_{CSZD1}		t_{DKC} + 0.8[Note]	t_{DKC} + 3.4[Note]	ns
Delay time from VBCLK↓ to RDZ	<4>	t_{RDZD1}		2.1	6.2	ns
Delay time from VBCLK↑ to RDZ	<5>	t_{RDZD2}		1.9	5.3	ns
Data setup time (to VBCLK↑)	<6>	t_{DIS}		0		ns
Data hold time (from VBCLK↑)	<7>	t_{DIH}		1.5		ns
Delay time from VBCLK↑ to BCYSTZ	<8>	t_{BCYD}		1.7	t_{DKS1} + 1.8[Note]	ns
WAITZ setup time (to VBCLK↑)	<9>	t_{WTS}		0		ns
WAITZ hold time (from VBCLK↑)	<10>	t_{WTH}		1.3		ns
Delay time from VBCLK↓ to VBWAIT, VBAHLD, VBLAST	<11>	t_{VRD1}			5.9	ns
Delay time from VBCLK↑ to VBWAIT, VBAHLD, VBLAST	<12>	t_{VRD2}		1.6		ns
Delay time from VBCLK↑ to VBD	<13>	t_{VBD1}			6.5	ns
Delay time from VBCLK↓ to VBD	<14>	t_{VBD2}		1.7		ns
Delay time from VBCLK↑ to DC	<15>	t_{DCD1}		t_{DKS1} + 0.8[Note]	t_{DKS1} + 2.9[Note]	ns
Delay time from VBCLK↓ to DC	<16>	t_{DCD2}		1.9	5.9	ns
Delay time from VBCLK↓ to WRZ	<17>	t_{WRZD}		2.0	5.6	ns
Delay time from VBCLK↓ to data	<18>	t_{DOD1}		t_{DKD1} + 0.3[Note]	t_{DKD1} + 1.7[Note]	ns
Delay time from VBCLK↑ to data	<19>	t_{DOD2}		t_{DKD0} + 0.3[Note]	t_{DKD0} + 1.7[Note]	ns

Note t_{DKA}: Delay time from VBCLK↑ to VBA

t_{DKC}: Delay time from VBCLK↑ to VDCSZ, VDSELPZ

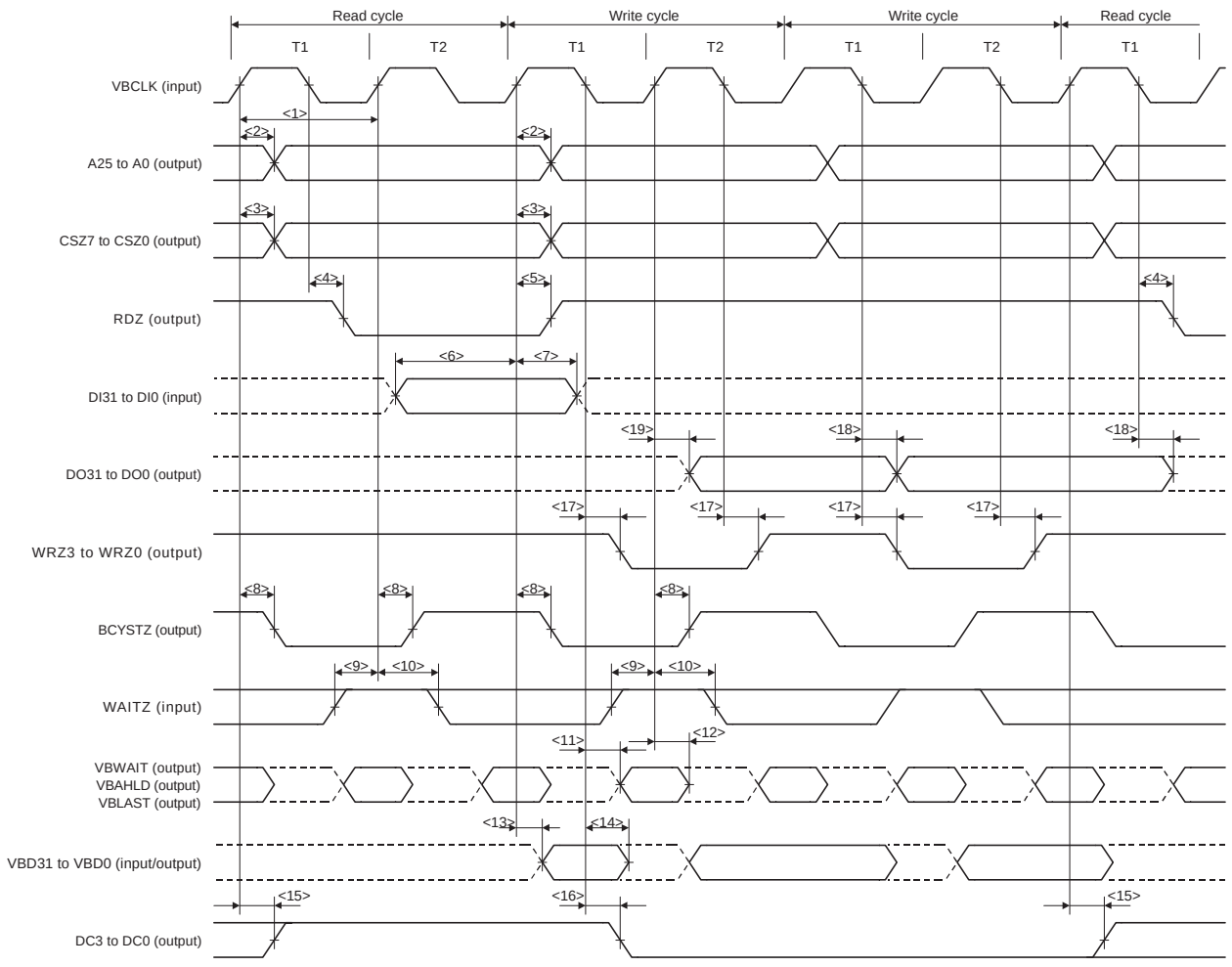
t_{DKS1}: Delay time from VBCLK↑ to VBSTZ, VBSIZE, VBWRITE, VBCTYP

t_{DKD1}: Delay time from VBCLK↓ to VBD data

t_{DKD0}: Delay time from VBCLK↑ to VBD data

The above are the electrical specifications of the NB85E. Refer to section **7. 4. 4 AC characteristics**.

(3) SRAM read/write timing (2/2)



Remarks 1. T1, T2: Basic state in which NU85E500 access is performed

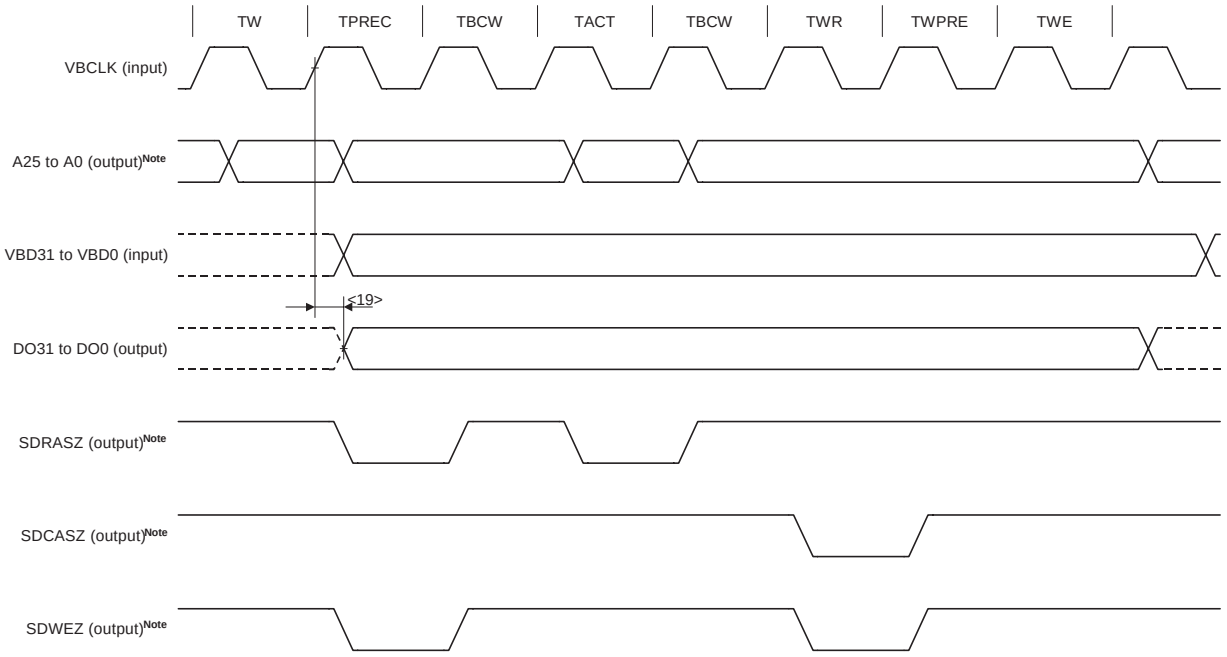
2. The level of the broken line portion of the DI31 to DI0 and DO31 to DO0 signals is undefined. The level of the broken line portion of the VBWAIT, VBAHLD, VBLAST, and VBD31 to VBD0 signals indicates undefined state (weak unknown) in which the bus holder in the NB85E is driving.

(4) SDRAM write timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to data	<19>	t_{DOD2}		t_{DKD0} + 0.3[Note]	t_{DKD0} + 1.7[Note]	ns

Note t_{DKD0}: Delay time from VBCLK↑ to VBD data

The above is the electrical specifications of the NB85E. Refer to section **7. 4. 4 AC characteristics**.



Note Signal of the NU85E502

Remarks 1. TW: Wait state

TPREC: Bank precharge command state

TBCW: Wait state inserted by setting the BCW1 and BCW0 bits of the SDRAM configuration register n (SCRn) (n = 7 to 0)

TACT: Bank active command state

TWR: Write command state

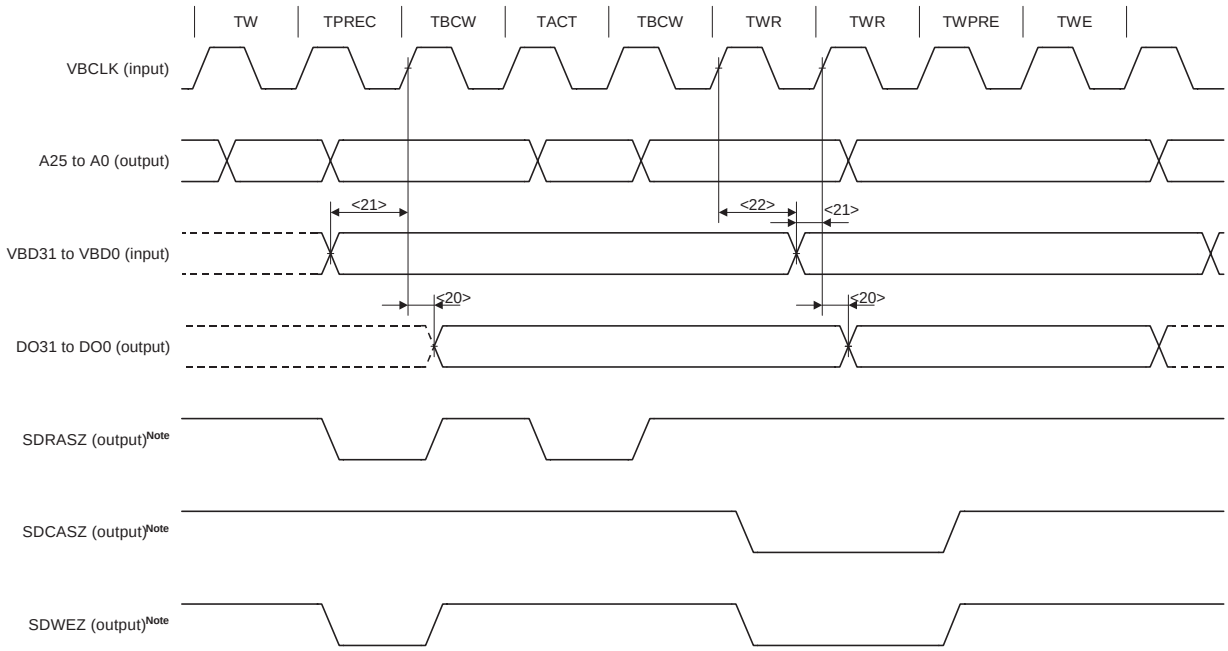
TWPRE: State indicating a precharge

TWE: State indicating the end of a write cycle

2. The level of the broken line portion of the VBD31 to VBD0 signals indicates undefined state (weak unknown) in which the bus holder in the NB85E is driving. The level of the broken line portion of the DO31 to DO0 signals is undefined.

(5) SDRAM sequential write timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to data (SDRAM sequential write)	<20>	t_{DOD3}		1.9	5.7	ns
VBD data setup time (to VBCLK↑)	<21>	t_{VBDS}		0		ns
VBD data hold time (from VBCLK↑)	<22>	t_{VBDH}		1.8		ns



Note Signal of the NU85E502

Remarks 1. TW: Wait state

TPREC: Bank precharge command state

TBCW: Wait state inserted by setting the BCW1 and BCW0 bits of the SDRAM configuration register n (SCRn) (n = 0 to 7)

TACT: Bank active command state

TWR: Write command state

TWPRE: State indicating a precharge

TWE: State indicating the end of a write cycle

2. The level of the broken line portion of the VBD31 to VBD0 signals indicates undefined state (weak unknown) in which the bus holder in the NB85E is driving. The level of the broken line portion of the DO31 to DO0 signals is undefined.

(6) SDRAM refresh timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to REFRQZ	–	t_{RFRQD}		2.0	5.7	ns
SELFREF setup time (to VBCLK↑)	–	t_{SRFS}		0		ns
SELFREF hold time (from VBCLK↑)	–	t_{SRFH}		1.4		ns
Delay time from CT502In1 to CSZ	–	t_{CSZD2}		t_{C2I1D} + 0.5[Note]	t_{C2I1D} + 2.4[Note]	ns

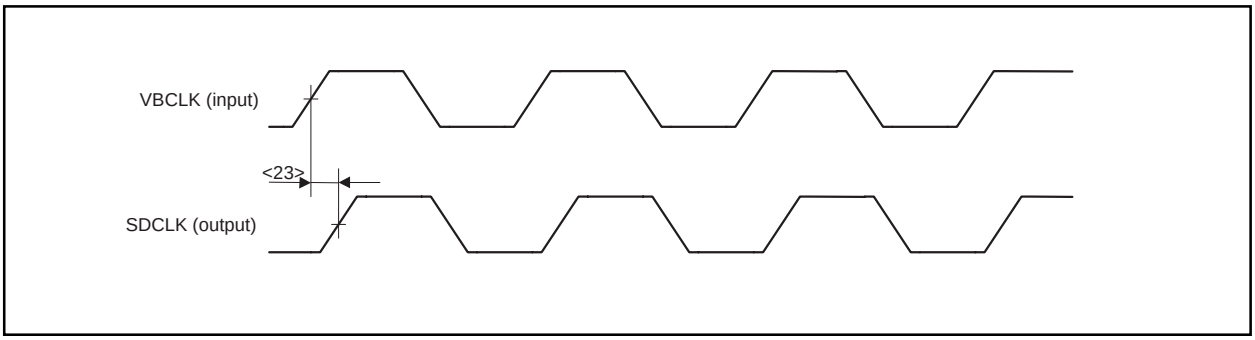
Note t_{C2I1D}: Delay time from VBCLK↑ to CT502I1

The above is the electrical specifications of the NU85E502. Refer to section **12. 4. 4 (3) NU85E500/NB85E500 connection signal timing**.

Remark n = 7 to 0

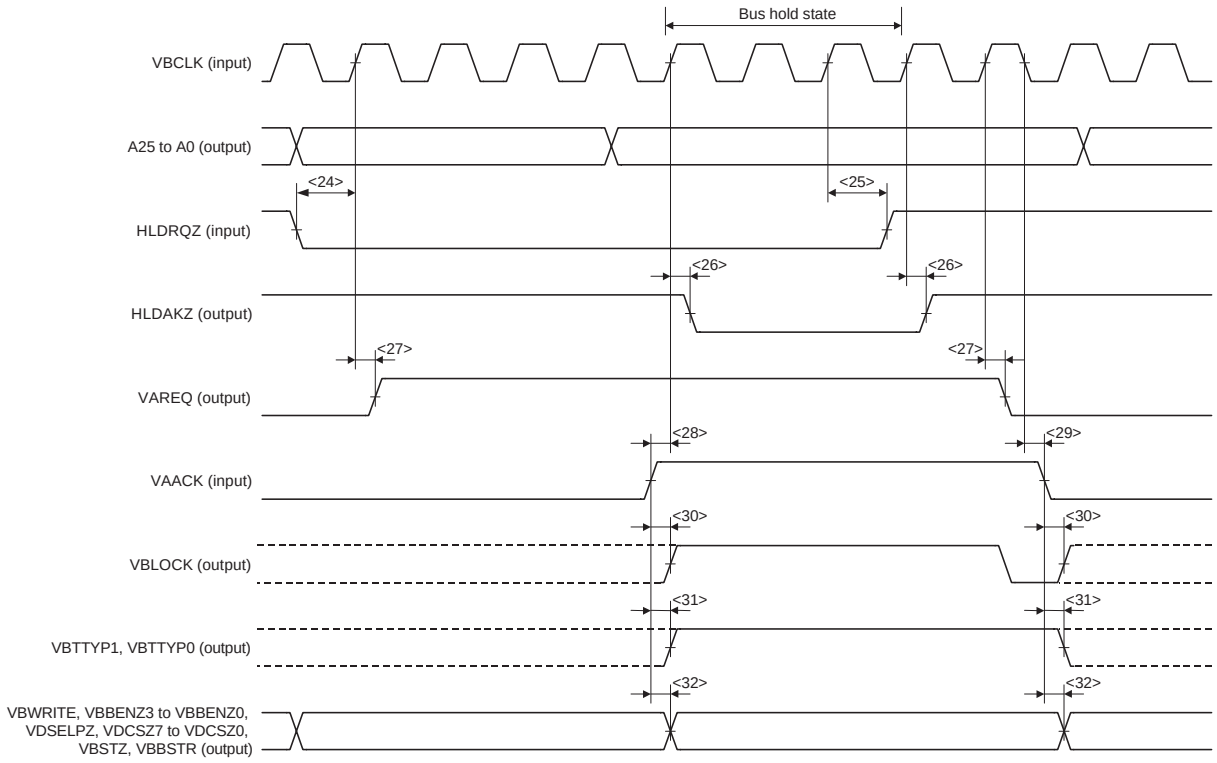
(7) SDCLK output timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to SDCLK↑	<23>	t_{SDCKD}		1.6	4.5	ns



(8) Bus hold timing

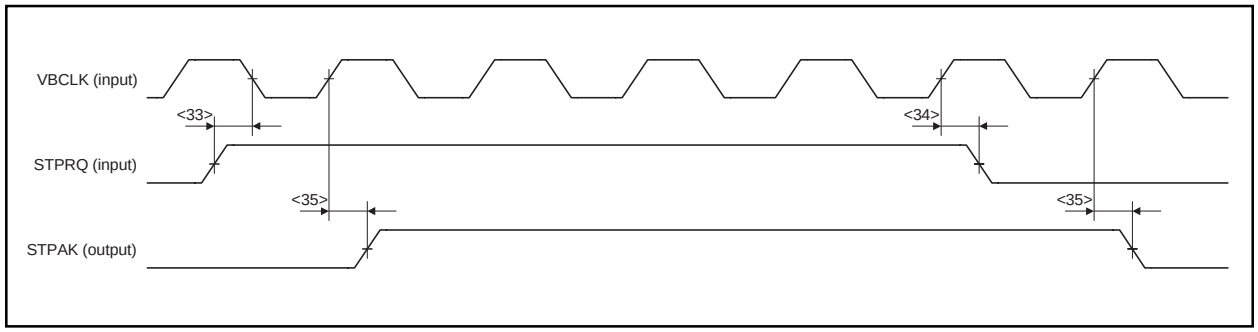
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
HLDRQZ setup time (to VBCLK↑)	<24>	t_{HRQS}		0		ns
HLDRQZ hold time (from VBCLK↑)	<25>	t_{HRQH}		1.2		ns
Delay time from VBCLK↑ to HLDAKZ	<26>	t_{HAKD}		2.0	5.6	ns
Delay time from VBCLK↑ to VAREQ	<27>	t_{VAQD}		1.9	5.3	ns
VAACK setup time (to VBCLK↑)	<28>	t_{VAKS}		0		ns
VAACK hold time (from VBCLK↓)	<29>	t_{VAKH}		1.6		ns
Delay time from VAACK↑ to VBLOCK	<30>	t_{VLKD}		0.6	2.4	ns
Delay time from VAACK↑ to VBTTYP	<31>	t_{VTTPD}		0.4	1.9	ns
Delay time from VAACK↑ to VBWRITE, VBBENZ, VDSELPZ, VDCSZ, VBSTR	<32>	t_{VSBD}		0.5	2.5	ns



Remark The level of the broken line portion of the VBLOCK, VBTTYP1, and VBTTYP0 signals indicates undefined state (weak unknown) in which the bus holder in the NB85E is driving.

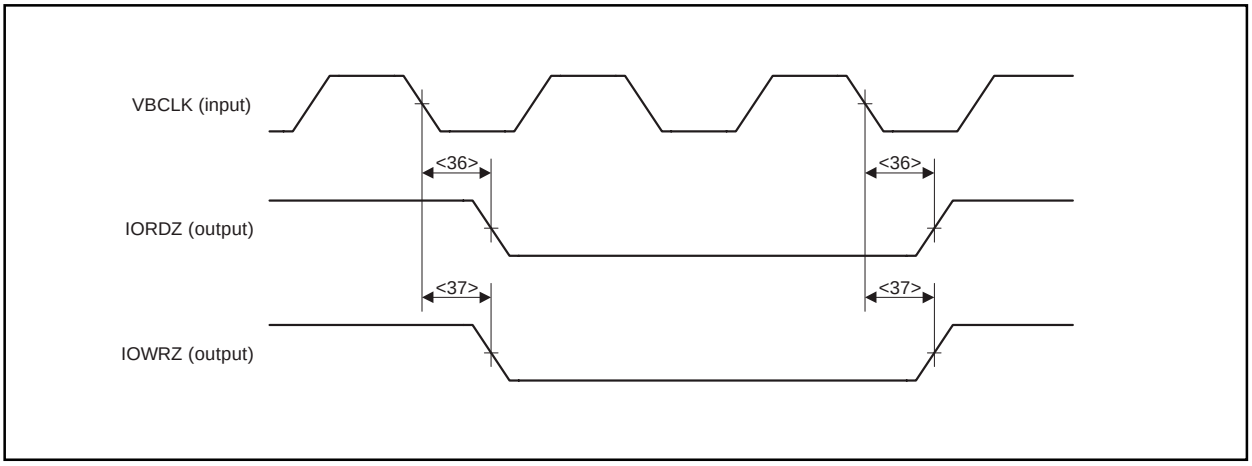
(9) STOP mode timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
STPRQ setup time (to VBCLK↓)	<33>	t_{SPQS}		0		ns
STPRQ hold time (from VBCLK↑)	<34>	t_{SPQH}		1.2		ns
Delay time from VBCLK↑ to STPAK	<35>	t_{SPAKD}		1.9	5.2	ns



(10) I/O control signal timing

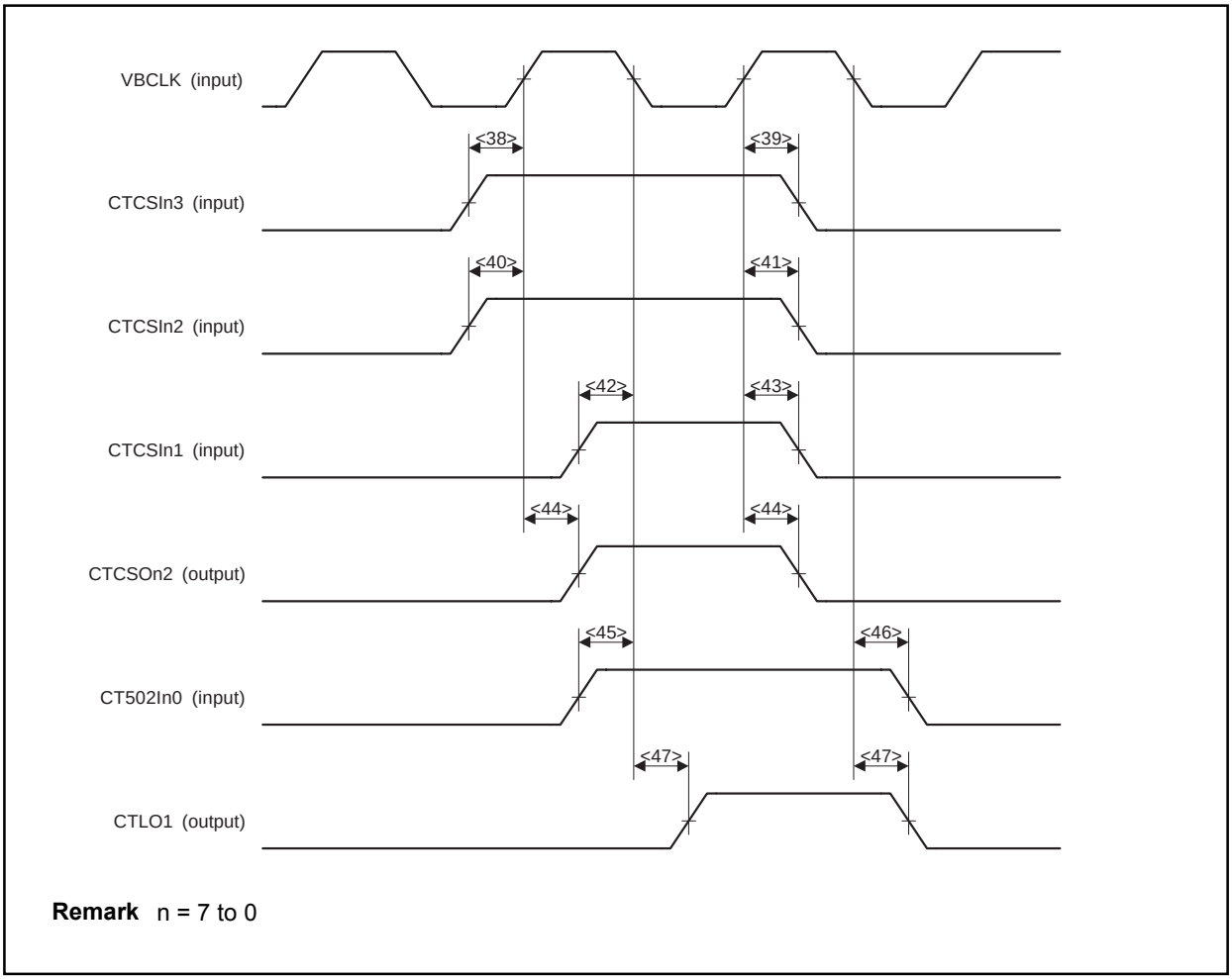
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↓ to IORDZ	<36>	t_{IORD}	During DMA flyby transfer	2.1	5.9	ns
Delay time from VBCLK↓ to IOWRZ	<37>	t_{IOWD}	During DMA flyby transfer	1.9	5.6	ns



(11) NU85E502 connection signal timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
CTCSIn3 setup time (to VBCLK↑)	<38>	t_{CSI3S}		0		ns
CTCSIn3 hold time (from VBCLK↑)	<39>	t_{CSI3H}		0.8		ns
CTCSIn2 setup time (to VBCLK↑)	<40>	t_{CSI2S}		0		ns
CTCSIn2 hold time (from VBCLK↑)	<41>	t_{CSI2H}		1.4		ns
CTCSIn1 setup time (to VBCLK↓)	<42>	t_{CSI1S}		0		ns
CTCSIn1 hold time (from VBCLK↑)	<43>	t_{CSI1H}		1.3		ns
Delay time from VBCLK↑ to CTCSOn2	<44>	t_{CSO2D}		1.9	5.7	ns
CT502In0 setup time (to VBCLK↓)	<45>	t_{C2I0S}		0		ns
CT502In0 hold time (from VBCLK↓)	<46>	t_{C2I0H}		0.5		ns
Delay time from VBCLK↓ to CTLO1	<47>	t_{CTL1D}		1.9	5.5	ns

Remark n = 7 to 0



Remark n = 7 to 0

(12) VSB timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VBA setup time (to VBCLK↑)	–	t_{VBAS1}	When using page ROM	1.5		ns
VBA hold time (from VBCLK↑)	–	t_{VBAH1}	When using page ROM	1.2		ns
VDCSZ setup time (to VBCLK↓)	–	t_{CSZS1}		1.4		ns
VDCSZ hold time (from VBCLK↑)	–	t_{CSZH1}		1.0		ns
VBWRITE setup time (to VBCLK↓)	–	t_{VBWRS1}		0		ns
VBWRITE hold time (from VBCLK↓)	–	t_{VBWRH1}		1.7		ns
VBBENZ setup time (to VBCLK↓)	–	t_{BENZS1}		0		ns
VBBENZ hold time (from VBCLK↓)	–	t_{BENZH1}		2.0		ns
VBCTYP setup time (to VBCLK↓)	–	t_{CTYPS1}		0		ns
VBCTYP hold time (from VBCLK↓)	–	t_{CTYPH1}		1.3		ns
VBSEQ setup time (to VBCLK↓)	–	t_{SEQS1}		0		ns
VBSEQ hold time (from VBCLK↑)	–	t_{SEQH1}		1.3		ns
VBSTZ setup time (to VBCLK↓)	–	t_{STZS1}		0		ns
VBSTZ hold time (from VBCLK↑)	–	t_{STZH1}		1.5		ns

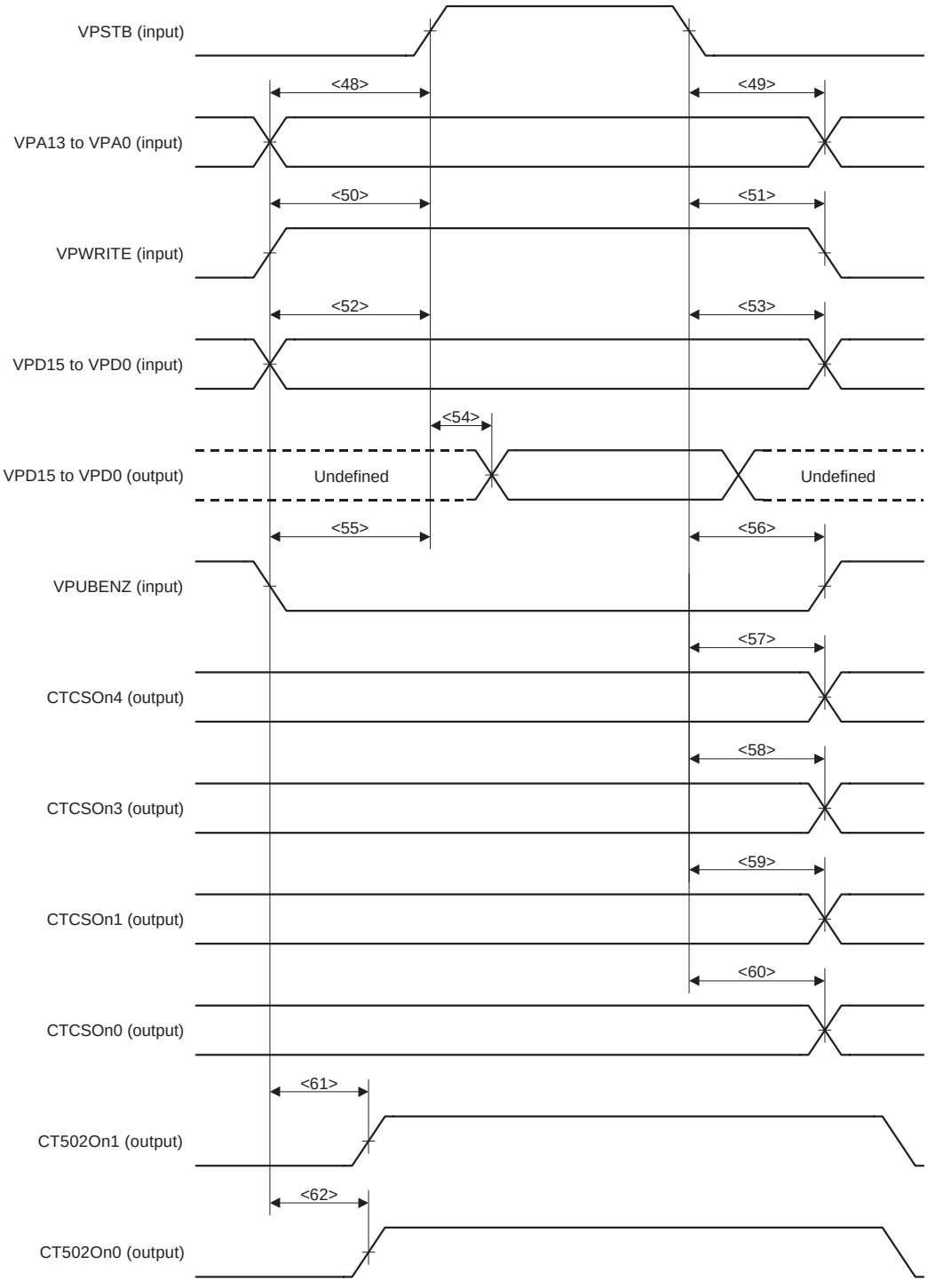
[MEMO]

(13) NPB timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VPA address setup time (to VPSTB↑)	<48>	t_{VPAS}		20		ns
VPA address hold time (from VPSTB↓)	<49>	t_{VPAH}		20		ns
VPWRITE setup time (to VPSTB↑)	<50>	t_{VPWRS}		20		ns
VPWRITE hold time (from VPSTB↓)	<51>	t_{VPWRH}		20		ns
VPD data setup time (to VPSTB↑)	<52>	t_{VPDS}		20		ns
VPD data hold time (from VPSTB↓)	<53>	t_{VPDH}		20		ns
Delay time from VPSTB↑ to VPD data	<54>	t_{VPDD}		0.7	8.0	ns
VPUBENZ setup time (to VPSTB↑)	<55>	t_{VPUBS}		20		ns
VPUBENZ hold time (from VPSTB↓)	<56>	t_{VPUBH}		20		ns
Delay time from VPSTB↓ to CTCSOn4	<57>	t_{CSO4D}			5	ns
Delay time from VPSTB↓ to CTCSOn3	<58>	t_{CSO3D}			5	ns
Delay time from VPSTB↓ to CTCSOn1	<59>	t_{CSO1D}			5	ns
Delay time from VPSTB↓ to CTCSOn0	<60>	t_{CSO0D}			5	ns
Delay time from VPA address to CT502On1	<61>	t_{C2O1D}			5	ns
Delay time from VPA address to CT502On0	<62>	t_{C2O0D}			5	ns

Remark n = 7 to 0

(13) NPB timing (2/2)



Remark n = 7 to 0

CHAPTER 12 NU85E502

(Under Development)

The NU85E502 is an SDRAM controller for the NB85E and NB85ET.

The NU85E502 is used by connecting to the NU85E500 or NB85E500 according to the target CPU core.

Target CPU Core	Type of Connected External Memory	Memory Controller (MEMC)
NB85E	SDRAM	NU85E500 + NU85E502
NB85E, NB85ET		NB85E500 + NU85E502

Remark For details of the NB85E500 and NU85E500, refer to **CHAPTER 10 NB85E500** and **CHAPTER 11 NU85E500**, respectively.

12. 1 Outline

The NU85E502 is a macro for controlling synchronous DRAM (SDRAM).

The NU85E502 can be used to start the external SDRAM bus cycle when it is connected to the NU85E500 (or NB85E500), and to the NB85E (or NB85ET) via the VSB.

The NU85E502 is used connected to the NU85E500 (or NB85E500).

Up to eight NU85E502 can be connected.

12. 1. 1 Symbol diagram

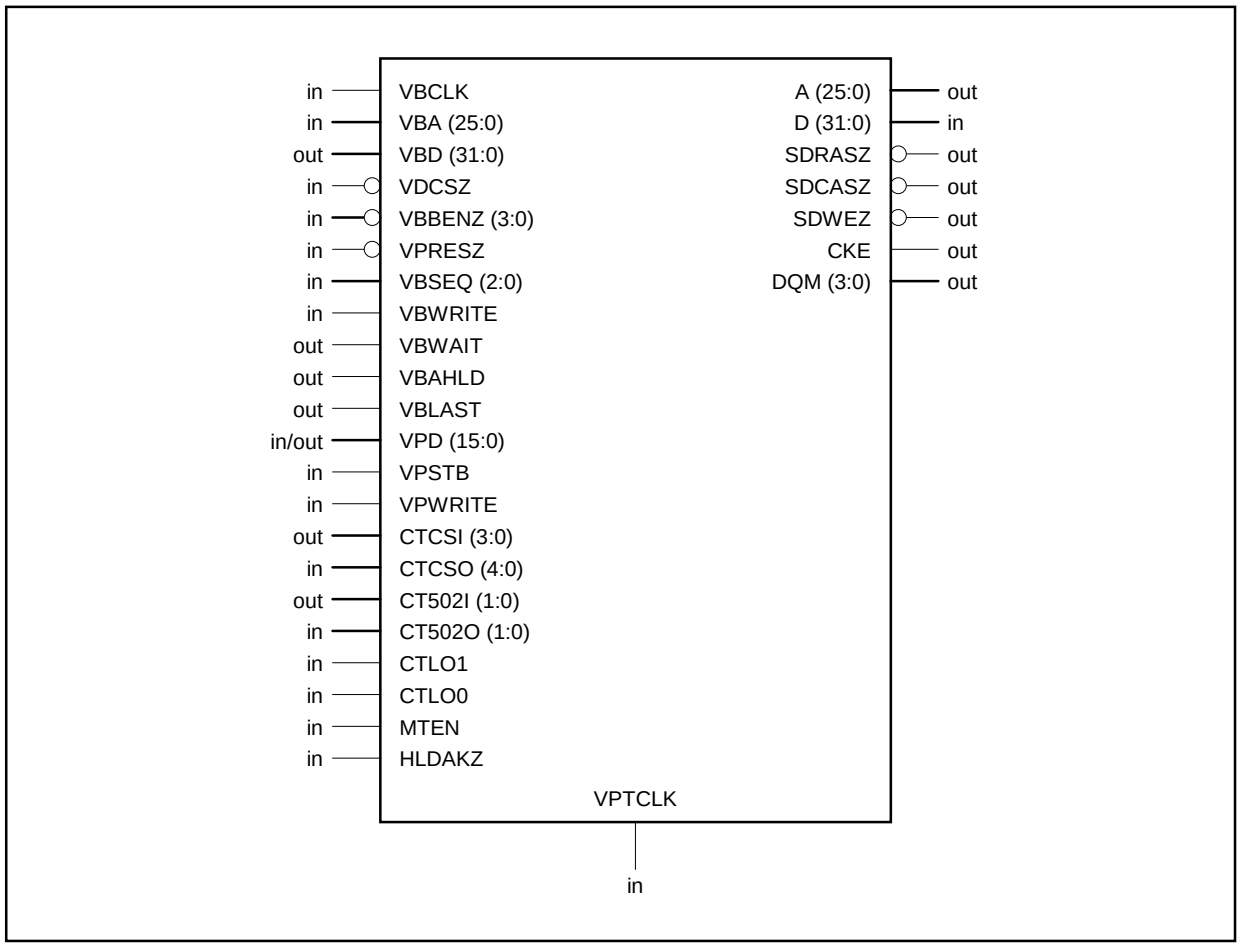
Number of grids

22.3k grids

41.6k grids (including wiring area)

Number of separation simulation patterns

20.3k



12. 1. 2 Pin capacitance

Remark C_{IN}: Capacitance of only input pin

C_{inewl}: Value of C_{IN} with wiring capacitance (estimated wire length capacitance) taken into consideration (l = 10 mm)

(1) Input pins (1/2)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
VBCLK	0.021	1.921	VBSEQ0	0.013	1.913
VBA25	0.060	1.960	VBWRITE	0.057	1.957
VBA24	0.064	1.964	VPSTB	0.012	1.912
VBA23	0.095	1.995	VPWRITE	0.015	1.915
VBA22	0.061	1.961	CTCSO4	0.049	1.949
VBA21	0.062	1.962	CTCSO3	0.051	1.951
VBA20	0.060	1.960	CTCSO2	0.013	1.913
VBA19	0.061	1.961	CTCSO1	0.021	1.921
VBA18	0.101	2.001	CTCSO0	0.008	1.908
VBA17	0.100	2.000	CT502O1	0.019	1.919
VBA16	0.068	1.968	CT502O0	0.030	1.930
VBA15	0.092	1.992	CTLO1	0.066	1.966
VBA14	0.114	2.014	CTLO0	0.019	1.919
VBA13	0.080	1.980	MTEN	0.082	1.982
VBA12	0.092	1.992	HLDAKZ	0.097	1.997
VBA11	0.093	1.993	D31	0.057	1.957
VBA10	0.094	1.994	D30	0.076	1.976
VBA9	0.061	1.961	D29	0.085	1.985
VBA8	0.062	1.962	D28	0.089	1.989
VBA7	0.068	1.968	D27	0.114	2.014
VBA6	0.061	1.961	D26	0.109	2.009
VBA5	0.061	1.961	D25	0.090	1.990
VBA4	0.099	1.999	D24	0.068	1.968
VBA3	0.094	1.994	D23	0.066	1.966
VBA2	0.092	1.992	D22	0.095	1.995
VBA1	0.061	1.961	D21	0.089	1.989
VBA0	0.093	1.993	D20	0.066	1.966
VDCSZ	0.024	1.924	D19	0.060	1.960
VBBENZ3	0.008	1.908	D18	0.093	1.993
VBBENZ2	0.008	1.908	D17	0.062	1.962
VBBENZ1	0.008	1.908	D16	0.062	1.962
VBBENZ0	0.036	1.936	D15	0.064	1.964
VPRESZ	0.011	1.911	D14	0.068	1.968
VBSEQ2	0.008	1.908	D13	0.061	1.961
VBSEQ1	0.013	1.913	D12	0.087	1.987

(1) Input pins (2/2)

Pin Name	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{IN} (pF)	C_{inewl} (pF)
D11	0.028	1.928	D4	0.056	1.956
D10	0.073	1.973	D3	0.102	2.002
D9	0.033	1.933	D2	0.058	1.958
D8	0.060	1.960	D1	0.056	1.956
D7	0.067	1.967	D0	0.078	1.978
D6	0.048	1.948	VPTCLK	0.061	1.961
D5	0.060	1.960			

(2) Output pins

Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)	Pin Name	C_{MAX} (pF)
VBD31	6.566	VBD6	6.558	A16	12.976
VBD30	6.579	VBD5	6.575	A15	13.069
VBD29	6.572	VBD4	6.578	A14	13.067
VBD28	6.562	VBD3	6.576	A13	13.001
VBD27	6.579	VBD2	6.570	A12	13.276
VBD26	6.563	VBD1	6.569	A11	13.245
VBD25	6.576	VBD0	6.578	A10	13.016
VBD24	6.575	VBWAIT	6.560	A9	13.006
VBD23	6.580	VBAHLD	6.493	A8	13.026
VBD22	6.571	VBLAST	6.580	A7	12.980
VBD21	6.579	CTCSI3	13.057	A6	13.245
VBD20	6.575	CTCSI2	13.336	A5	12.954
VBD19	6.578	CTCSI1	13.338	A4	13.265
VBD18	6.564	CTCSI0	13.236	A3	13.031
VBD17	6.575	CT502I1	13.336	A2	13.040
VBD16	6.576	CT502I0	13.338	A1	13.002
VBD15	6.571	A25	13.057	A0	13.040
VBD14	6.574	A24	12.993	SDRASZ	13.058
VBD13	6.573	A23	12.989	SDCASZ	13.056
VBD12	6.579	A22	12.977	SDWEZ	13.054
VBD11	6.571	A21	12.981	CKE	13.064
VBD10	6.579	A20	12.990	DQM3	13.065
VBD9	6.574	A19	12.972	DQM2	13.070
VBD8	6.573	A18	13.070	DQM1	13.055
VBD7	6.562	A17	12.892	DQM0	13.062

(3) I/O pins

Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)	Pin Name	C_{MAX} (pF)	C_{IN} (pF)	C_{inewl} (pF)
VPD15	6.565	0.069	1.969	VPD7	6.575	0.059	1.959
VPD14	6.560	0.073	1.973	VPD6	6.556	0.077	1.977
VPD13	6.573	0.061	1.961	VPD5	6.561	0.072	1.972
VPD12	6.554	0.079	1.979	VPD4	6.575	0.058	1.958
VPD11	6.585	0.049	1.949	VPD3	6.577	0.057	1.957
VPD10	6.578	0.056	1.956	VPD2	6.571	0.063	1.963
VPD9	6.560	0.073	1.973	VPD1	6.573	0.061	1.961
VPD8	6.573	0.061	1.961	VPD0	6.567	0.067	1.967

12. 2 Initialization of Internal Registers

Before executing the test program, be sure to execute an instruction to assign initial values to the internal registers used in the test program execution. Failure to do this will result in the propagation of undefined values.

12. 3 Pin Functions

Pin Name		I/O	Function
NB85E/NB85ET connection pins	VBCLK	Input	Internal system clock input
	VBA25 to VBA0	Input	Address input
	VBD31 to VBD0	Output	Data output
	VDCSZ	Input	Chip select input
	VBBENZ3 to VBBENZ0	Input	Byte enable input
	VPRESZ	Input	Reset input
	VBSEQ2 to VBSEQ0	Input	Sequential status input
	VBWRITE	Input	Read/write status input
	VBWAIT	Output	Wait response output
	VBAHLD	Output	Address hold response output
	VBLAST	Output	Last response output
	VPD15 to VPD0	I/O	Data I/O (for NPB)
	VPSTB	Input	Data strobe input (for NPB)
	VPWRITE	Input	Write access strobe input (for NPB)
NU85E500/NB85E500 connection pins	CTCSI3 to CTCSI0	Output	Control output to NU85E500/NB85E500
	CTCSO4 to CTCSO0	Input	Control input from NU85E500/NB85E500
	CT502I1, CT502I0	Output	Control output to NU85E500/NB85E500
	CT502O1, CT502O0	Input	Control input from NU85E500/NB85E500
	CTLO1, CTLO0	Input	Control input from NU85E500/NB85E500
	MTEN	Input	Test mode enable input from NU85E500/NB85E500
	HLDAKZ	Input	Bus hold status input from NU85E500/NB85E500
External memory connection pins	A25 to A0	Output	External memory address output
	D31 to D0	Input	External memory data input
	SDRASZ	Output	SDRAM row address strobe output
	SDCASZ	Output	SDRAM column address strobe output
	SDWEZ	Output	SDRAM data write enable output
	CKE	Output	Clock enable output
	DQM3 to DQM0	Output	Data mask output
Test mode pins	VPTCLK	Input	Test clock input

12. 4 Electrical Specifications (Preliminary)

The following specifications are for a single macro. An actual chip consists of two or more macros. Design the system so that all the specifications of the individual macros are satisfied when the chip is used.

12. 4. 1 Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to +4.6	V
Operating ambient temperature	T_A	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

12. 4. 2 Recommended operation range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Operating ambient temperature	T_A	−40		+85	°C
Clock cycle	t_{CYK}	15.0			ns

12. 4. 3 DC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1}	In normal operation mode		0.11	0.17	mA/MHz
	I_{DD2}	In STOP mode		0	1.0	μA

Remarks 1. The above supply current value is a reference value calculated from the number of grids.

2. The TYP. value is a reference value for when T_A = 25°C, V_{DD} = 3.3 V.

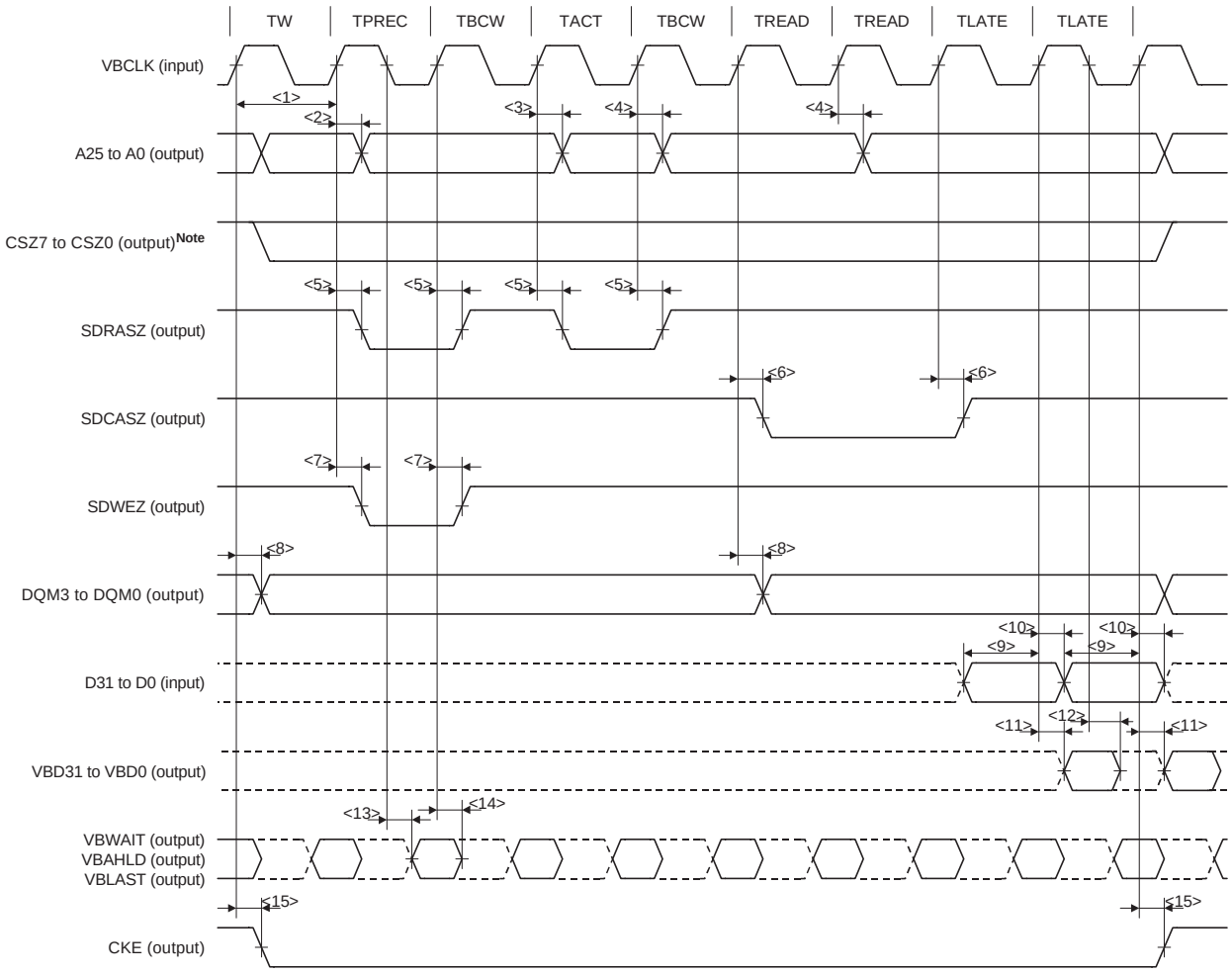
[MEMO]

12. 4. 4 AC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)

(1) SDRAM read timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VBCLK input cycle	<1>	t_{CYK}		15.0		ns
Delay time 1 from VBCLK↑ to row address	<2>	t_{SDRAD1}	During bank precharge command	2.7	9.5	ns
Delay time 2 from VBCLK↑ to row address	<3>	t_{SDRAD2}	During bank active command	2.7	9.5	ns
★ Delay time from VBCLK↑ to column address	<4>	t_{SDCAD}		2.2	8.6	ns
Delay time from VBCLK↑ to SDRASZ	<5>	t_{SRD}		2.3	6.9	ns
Delay time from VBCLK↑ to SDCASZ	<6>	t_{SCD}		2.4	7.1	ns
Delay time from VBCLK↑ to SDWEZ	<7>	t_{SWD}		2.3	6.9	ns
Delay time from VBCLK↑ to DQM	<8>	t_{DQD}		2.3	7.1	ns
Data setup time (to VBCLK↑)	<9>	t_{DS2}		0		ns
Data hold time (from VBCLK↑)	<10>	t_{DH2}		0.8		ns
Delay time from VBCLK↑ to VBD	<11>	t_{VBD3}			5.5	ns
Delay time from VBCLK↓ to VBD	<12>	t_{VBD4}		1.5		ns
Delay time from VBCLK↓ to VBWAIT, VBAHLD, VBLAST	<13>	t_{VRD3}			5.0	ns
Delay time from VBCLK↑ to VBWAIT, VBAHLD, VBLAST	<14>	t_{VRD4}		1.4		ns
Delay time from VBCLK↑ to CKE	<15>	t_{CKED}		2.2	6.6	ns

(1) SDRAM read timing (2/2)



Note Signal of the NU85E500 (or NB85E500)

Remarks 1. TW: Wait state

TPREC: Bank precharge command state

TBCW: Wait state inserted by setting the BCW1 and BCW0 bits of the SDRAM configuration register n (SCRn) (n = 7 to 0)

TACT: Bank active command state

TREAD: Read command state

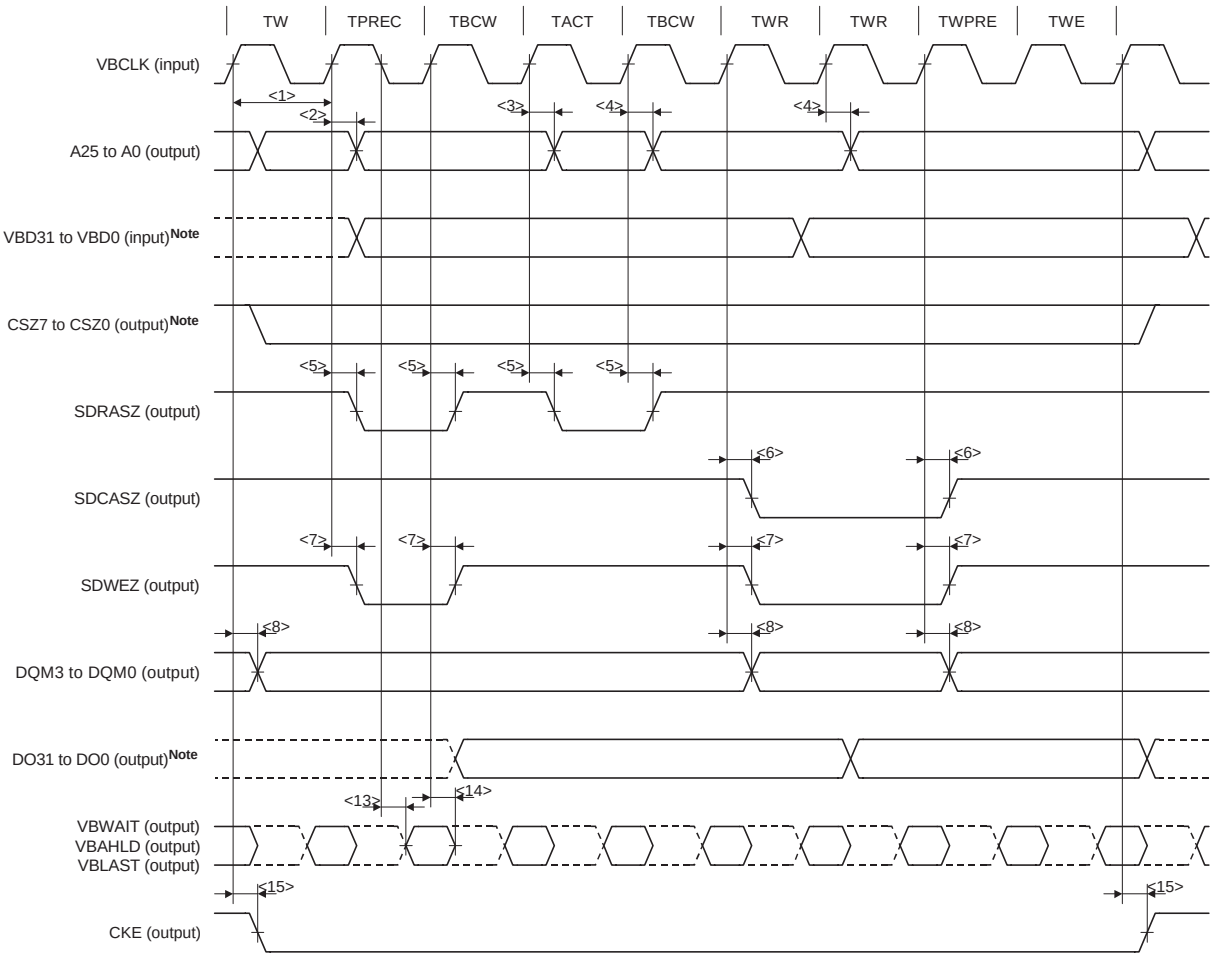
TLATE: Wait state of latency portion

2. The level of the broken line portion of the D31 to D0 signals is undefined. The level of the broken line portion of the VBD31 to VBD0, VBWAIT, VBAHLD, and VBLAST signals indicates undefined state (weak unknown) in which the bus holder in the NB85E (or NB85ET) is driving.

(2) SDRAM write timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
VBCLK input cycle	<1>	t_{CYK}		15.0		ns
Delay time 1 from VBCLK↑ to row address	<2>	t_{SDRAD1}	During bank precharge command	2.7	9.5	ns
Delay time 2 from VBCLK↑ to row address	<3>	t_{SDRAD2}	During bank active command	2.7	9.5	ns
★ Delay time from VBCLK↑ to column address	<4>	t_{SDCAD}		2.2	8.6	ns
Delay time from VBCLK↑ to SDRASZ	<5>	t_{SRD}		2.3	6.9	ns
Delay time from VBCLK↑ to SDCASZ	<6>	t_{SCD}		2.4	7.1	ns
Delay time from VBCLK↑ to SDWEZ	<7>	t_{SWD}		2.3	6.9	ns
Delay time from VBCLK↑ to DQM	<8>	t_{DQD}		2.3	7.1	ns
Delay time from VBCLK↓ to VBWAIT, VBAHLD, VBLAST	<13>	t_{VRD3}			5.0	ns
Delay time from VBCLK↑ to VBWAIT, VBAHLD, VBLAST	<14>	t_{VRD4}		1.4		ns
Delay time from VBCLK↑ to CKE	<15>	t_{CKED}		2.2	6.6	ns

(2) SDRAM write timing (2/2)



Note Signal of the NU85E500

Remarks 1. TW: Wait state

TPREC: Bank precharge command state

TBCW: Wait state inserted by setting the BCW1 and BCW0 bits of the SDRAM configuration register n (SCRn) (n = 7 to 0)

TACT: Bank active command state

TWR: Write command state

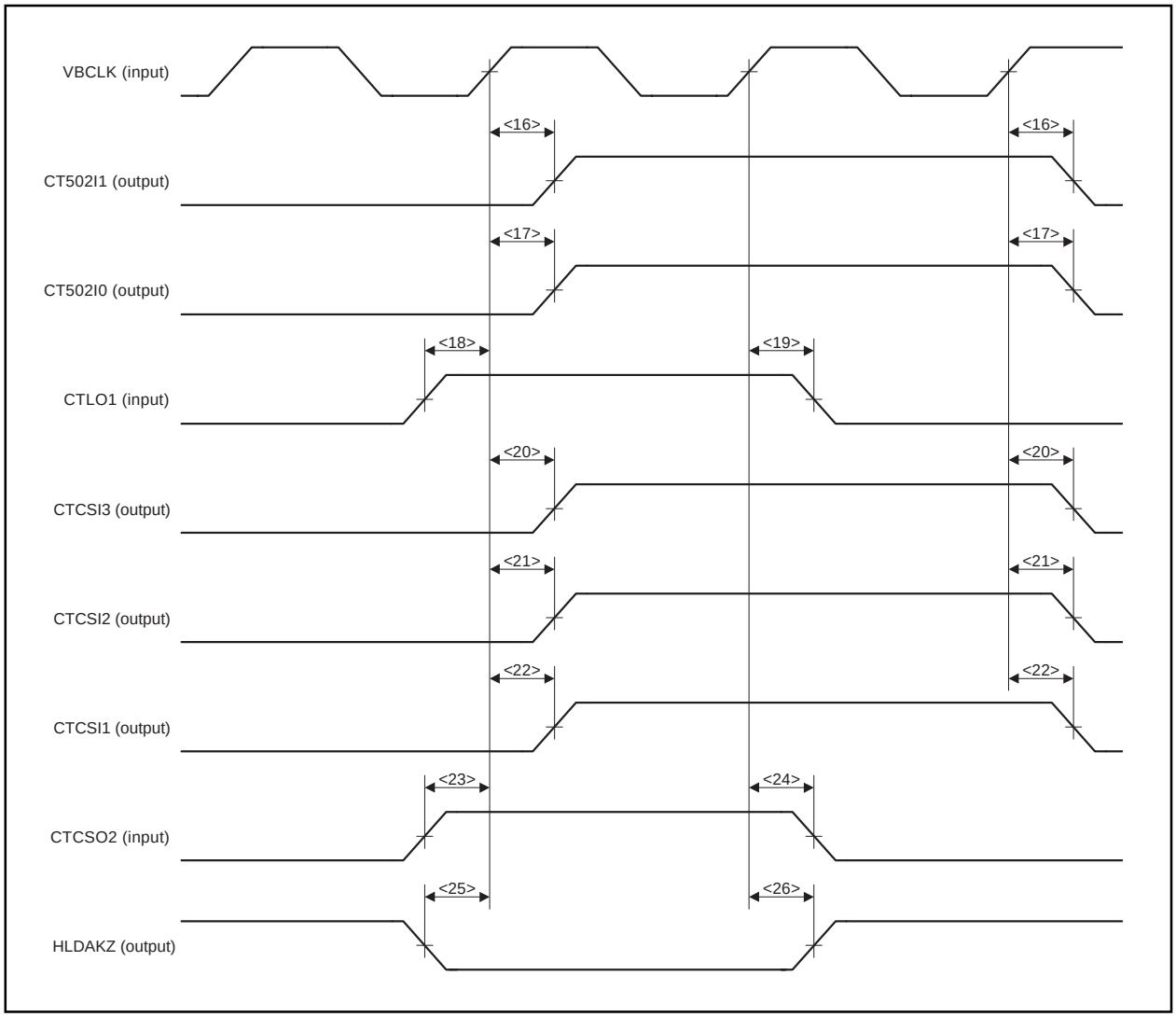
TWPRE: State indicating a precharge

TWE: State indicating the end of a write cycle

2. The level of the broken line portion of the VBD31 to VBD0, VBWAIT, VBAHLD, and VBLAST signals indicates undefined state (weak unknown) in which the bus holder in the NB85E is driving. The level of the broken line portion of the DO31 to DO0 signals is undefined.

(3) NU85E500/NB85E500 connection signal timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from VBCLK↑ to CT502I1	<16>	t_{C2I1D}		1.4	4.0	ns
Delay time from VBCLK↑ to CT502I0	<17>	t_{C2I0D}		1.8	5.5	ns
CTLO1 setup time (to VBCLK↑)	<18>	t_{CTL1S}		1.3		ns
CTLO1 hold time (from VBCLK↑)	<19>	t_{CTL1H}		1.0		ns
Delay time from VBCLK↑ to CTCSI3	<20>	t_{CSI3D}		1.8	5.2	ns
Delay time from VBCLK↑ to CTCSI2	<21>	t_{CSI2D}		1.8	5.3	ns
Delay time from VBCLK↑ to CTCSI1	<22>	t_{CSI1D}		1.5	4.2	ns
CTCSO2 setup time (to VBCLK↑)	<23>	t_{CSO2S}		1.9		ns
CTCSO2 hold time (from VBCLK↑)	<24>	t_{CSO2H}		0.5		ns
HLDAKZ setup time (to VBCLK↑)	<25>	t_{HAKS}		0		ns
HLDAKZ hold time (from VBCLK↑)	<26>	t_{HAKH}		0.8		ns



(4) VSB timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
★ VBA setup time (to VBCLK↑)	–	t_{VBAS2}		7.9		ns
VBA hold time (from VBCLK↑)	–	t_{VBAH2}		0.3		ns
VDCSZ setup time (to VBCLK↑)	–	t_{CSZS2}		3.7		ns
VDCSZ hold time (from VBCLK↑)	–	t_{CSZH2}		0.1		ns
VBWRITE setup time (to VBCLK↓)	–	t_{VBWRS2}		0		ns
VBWRITE hold time (from VBCLK↓)	–	t_{VBWRH2}		1.6		ns
VBBENZ setup time (to VBCLK↑)	–	t_{BENZS2}		0		ns
VBBENZ hold time (from VBCLK↑)	–	t_{BENZH2}		1.0		ns
VBSEQ setup time (to VBCLK↑)	–	t_{SEQS2}		5.2		ns
VBSEQ hold time (from VBCLK↑)	–	t_{SEQH2}		0.5		ns

★

APPENDIX REVISION HISTORY

Revisions up to the previous edition are shown below. The “Pages” column indicates pages in the older documents.

(1) 1st edition → 2nd edition

Pages	Description
p.16	Modification of the explanation in **1. 2. 4 Initialize**
pp.18 to 20	Modification of the number of grids in **2. 1. 1 Symbol diagram**
pp.21 to 23	Modification of **2. 1. 2 Pin capacitance**
p.26	Modification of **2. 3. 3 DC characteristics**
p.26	Addition of CPU operating frequency in **2. 3. 4 AC characteristics**
p.31	Addition of **Caution** in **2. 3. 4 (6) (e) I^2C bus mode**
p.32	Addition of **Figure 2-1. Example of Circuit Construction of Serial Interface (IIC0) Input/Output Pin**
p.35	Modification of **2. 4 (6) Write timing 1**
p.35	Modification of **2. 4 (7) Write timing 2**
p.38	Modification of **2. 4 (12) External wait input write timing 1**
p.38	Modification of **2. 4 (13) External wait input write timing 2**
p.40	Modification of **2. 4 (17) (a) 3-wire serial I/O mode**
p.43	Modification of **3. 1 Outline**
p.44	Modification of the number of separation simulation patterns in **3. 1. 1 Symbol diagram**
pp.46, 47	Modification of **3. 1. 2 Pin capacitance**
p.48	Modification of **3. 2 RESETB Signal**
pp.51 to 62	Modification of **3. 5 Electrical Specifications**
p.63	Modification of **4. 1 Outline**
p.64	Modification of the number of separation simulation patterns in **4. 1. 1 Symbol diagram**
pp.66 to 68	Modification of **4. 1. 2 Pin capacitance**
p.69	Modification of **4. 2 RESETB Signal**
pp.72 to 87	Modification of **4. 5 Electrical Specifications**
pp.89 to 107	Addition of **CHAPTER 5 V30MX**
pp.109 to 119	Addition of **CHAPTER 6 V30MZ**

(2) 2nd edition → 3rd edition

Pages	Description
p.17	Change of “Under development” for the 78K/0 Core to “Developed” in **CHAPTER 2 78K/0 CORE.** Deletion of flash memory versions (NAK0HF4 and NAK0HF8)
p.25	Deletion of description “Preliminary” from **2.3 Electrical Specifications**
p.41	Deletion of a flash memory version (NA851Fxx)
p.42	Modification of the number of grids (including wiring area) in **3.1.1 Symbol diagram**
p.50	Deletion of description “External capacitance load of internal RAM data output pin” from **(1) How to calculate the current consumption value of the V851 core in 3.5.3 DC characteristics**
p.61	Deletion of a flash memory version (NA853Fxx)
p.62	Modification of the number of grids in **4.1.1 Symbol diagram**
p.71	Deletion of description “External capacitance load of internal RAM data output pin” from **(1) How to calculate the current consumption value of the V853 core in 4.5.3 DC characteristics**
pp.119 through 154	Addition of **CHAPTER 7 NB85E**
pp.155 through 204	Addition of **CHAPTER 8 NB85E50x**
pp. 139, 140, 142, 148, 149, 151, 152, 153	Modification of the hold time in **7.4.4 AC characteristics**
pp.155 through 204	Change of name of SDRAM controller from “NB85E502” to “NU85E502”
pp. 194, 195, 198, 204	Addition of description regarding HLDAKZ pin

(3) 3rd edition → 4th edition

Pages	Description
Throughout	• Deletion of description regarding DRAM controller (NB85E501) • Modification of name of SDRAM controller from “NB85E502” to “NU85E502”
pp.20, 21	Correction of the number of grids of NAK0HM0, NAK0HM4, and NAK0HM8
p.44	Correction of the number of grids of V851 core
p.64	Correction of the number of grids of V853 core
p.90	Correction of the number of grids of V30MX
p.93	Correction of **5. 3. 2 RESET signal**
p.108	Correction of the number of grids of V30MZ
p.110	Correction of **6. 3. 1 RESET signal**
p.120	Correction of the number of grids and the number of separation simulation patterns of NB85E
pp.135, 136	Correction of **7. 3 Pin Functions**
pp.138 to 142, 144 to 149, 151 to 153	Correction of **7. 4. 4 AC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)**
pp.155 to 159	Addition of **CHAPTER 8 NB85E901**
pp.161 to 199	Addition of **CHAPTER 9 NB85ET**
p.201	Correction of the number of grids and the number of separation simulation patterns of NB85E500
p.211	Correction of **10. 3 Pin Functions**
p.212	Correction of **10. 4. 3 DC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)**
pp.214 to 233	Correction of **10. 4. 4 AC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)**
pp.235 to 267	Addition of **CHAPTER 11 NU85E500**
p.270	Correction of the number of grids and the number of separation simulation patterns of NU85E502
pp.270, 271, 274	Addition of description regarding HLDAKZ pin
pp.276 to 281	Correction of **12. 4. 4 AC characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V)**

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