Optimizing the Performance of High-Speed Converter Designs

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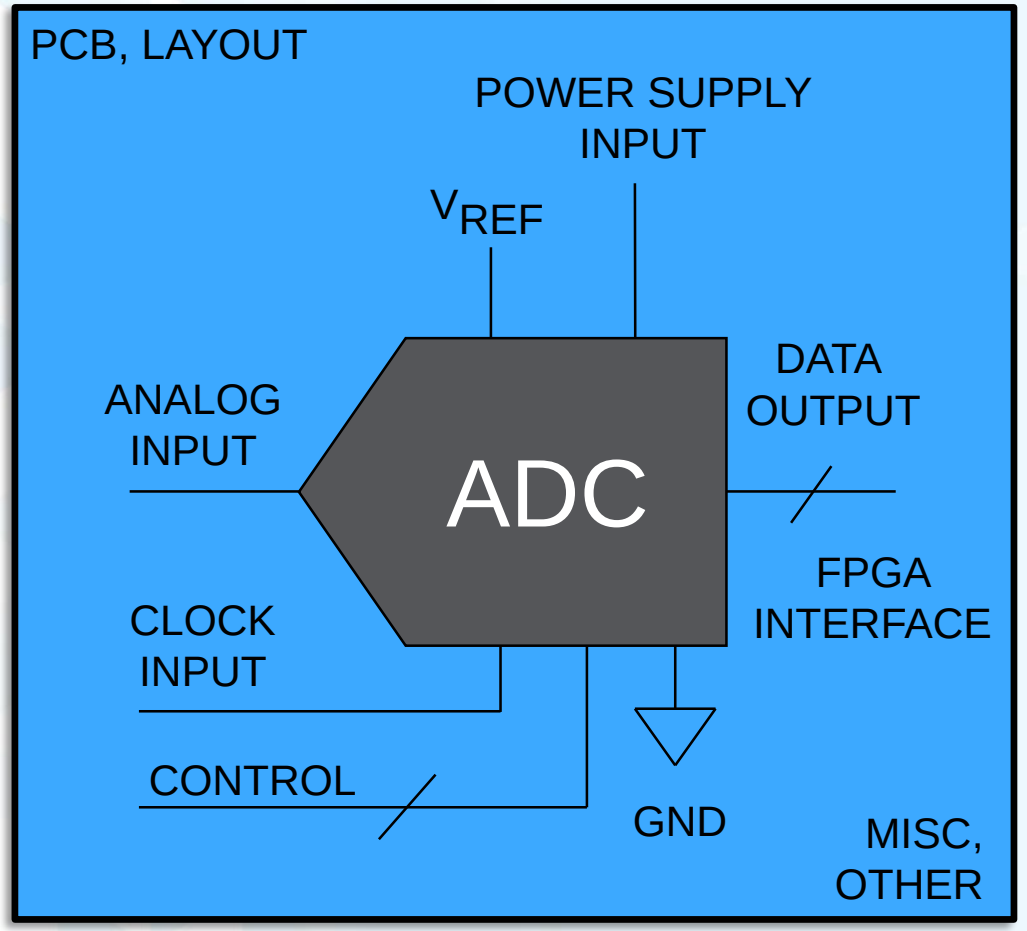
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

Agenda

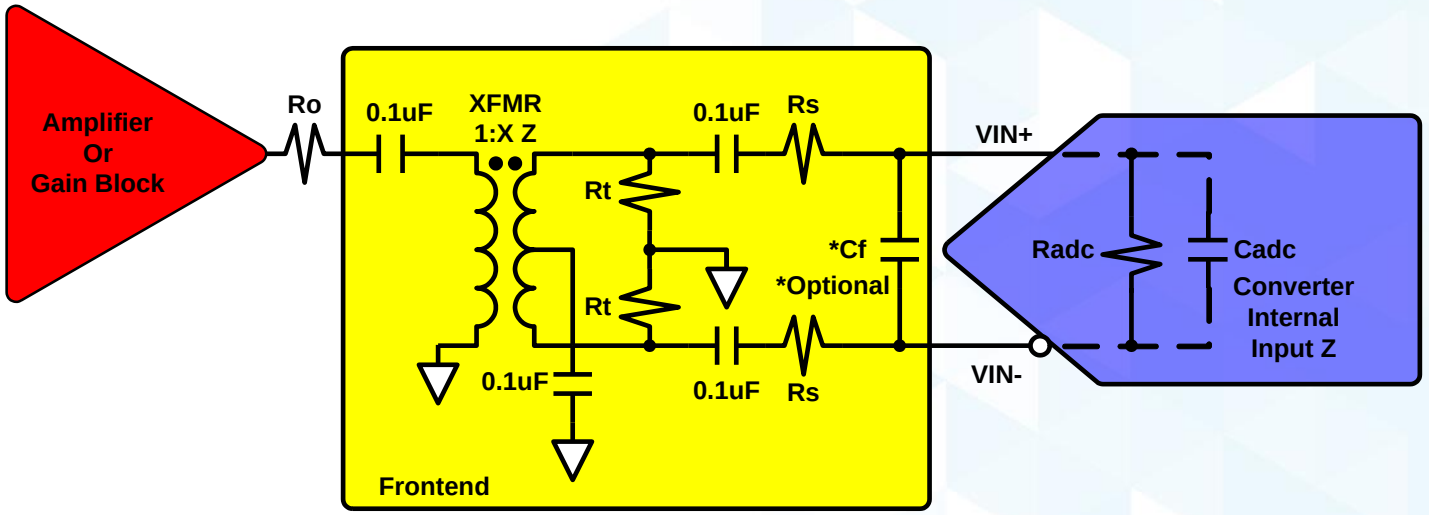
- Every High-Speed Converter Application should pay attention to the following:
  - Analog Input
  - Converter Specifications
  - Sampling Clock
  - Layout & Decoupling
  - Power Supply

This Webinar concentrates on ADCs; however, the same interface concepts apply equally to DACs.



Analog Inputs

Analog Inputs



- "front-end" generally implies a network or coupling circuit that connects between the last stage of the signal chain (usually an amplifier, gain block or tuner) and the converter's analog inputs.
- In order to achieve Datasheet performance the designer must understand the frontend goals
- Two types of front-ends
  - Active
  - Passive
- It must also be very linear, well balanced and properly laid out on the printed circuit board (pcb) in order to preserve the signal content properly.

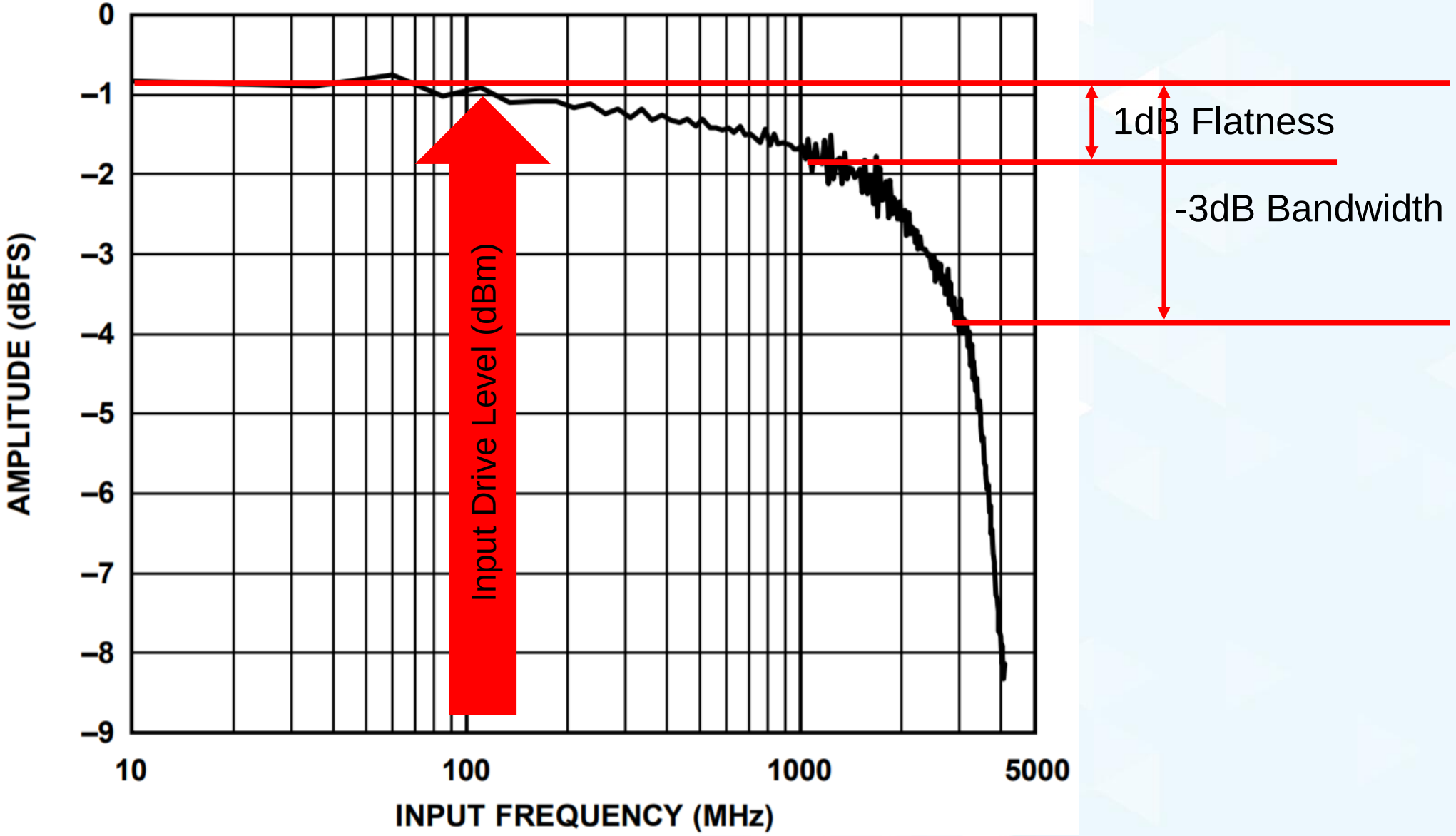
Analog Inputs: Goals

- Designing a good analog input network is important because the converter performance is going to be limited by it.

- When designing the network there are 5 parameters to keep in mind:
  - **Input Impedance**, which is a parameter that shows how much input power is being reflected to the source or transmitted to the load over the bandwidth of interest. Input impedance of the network for high-speed signal and RF is usually 50Ω.
  - **Passband Flatness** is usually defined as the amount of fluctuation/ripple that can be tolerated within the specified bandwidth.
  - **Bandwidth** is the -3dB measurement of the frequency range required by the system.
  - **SNR** (signal-to-noise ratio) / **SFDR** (spurious free dynamic range)
  - **Input Drive Level** is a function of the bandwidth and input impedance specifications. This sets the gain/amplitude required for a full-scale input signal at the converter. It is highly dependent on the frontend components chosen, i.e. – transformer, amplifier, Anti-Aliasing Filter and can be one of the most difficult parameters to achieve.

Gain Flatness/Bandwidth/Drive Level

AD9625

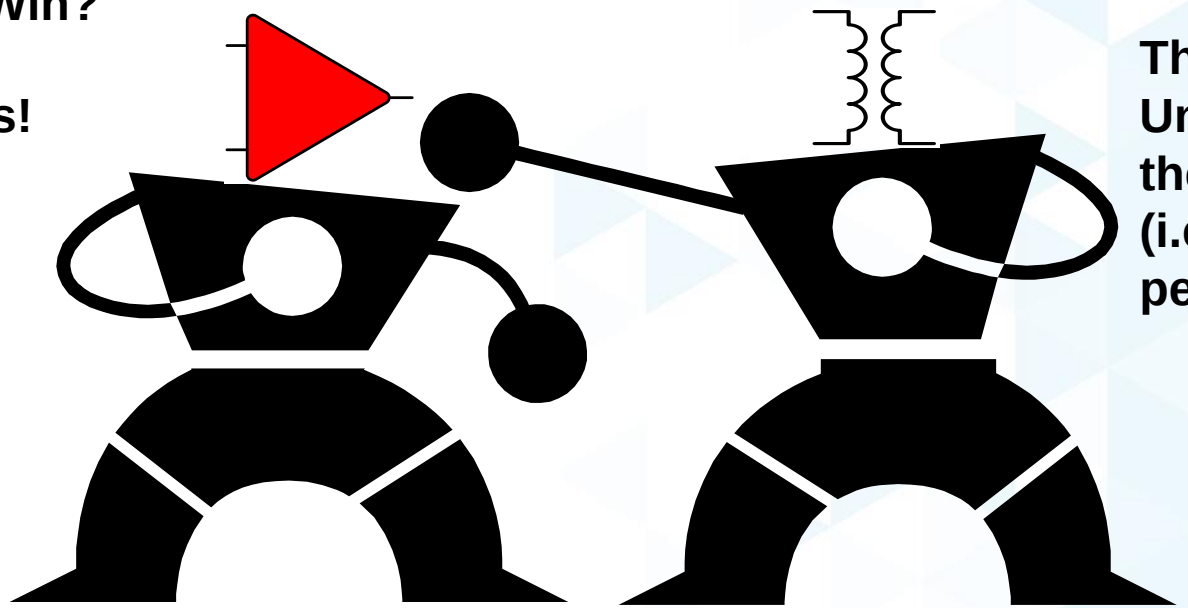


Amplifier vs. Transformer

- An amplifier is an active device
- A transformer is a passive device
- Amplifiers consume power
- Both have dynamic effects that need to be dealt with

Q: Who will Win?

A: It Depends!



The Key is Understanding the Tradeoffs (i.e. – Goals) per Application

Amplifier vs. Transformer Cont.

- Why use an amplifier?
  - Amplifiers can preserve the DC content of the signal (in some cases)
  - Amplifiers preserve isolation between the previous stage and the ADC… on the scale of ~40-60dB.
  - Amplifiers are easier to work with in terms of gain and are not bandwidth dependent.
  - Amplifiers are less likely to ripple through the passband.
  - Can be used to convert Single-Ended Signals to Differential (in some cases)

Amplifier vs. Transformer cont.

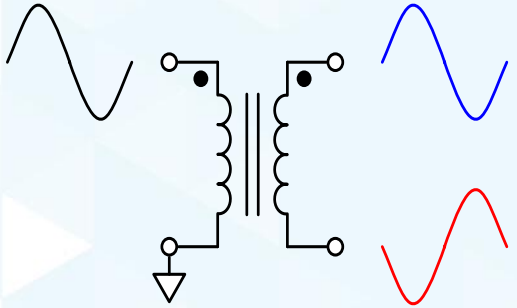
- Why use a Transformer?
  - Transformers have the advantage of coupling higher IF frequencies without significant loss (>200MHz).
  - For this same reason transformers usually have more bandwidth.
  - Transformers don’t require a power supply and thus add no power increment to the overall signal chain.
  - Transformers don’t add noise to the system, they only gain the signal noise, if using a transformer with gain.
  - Transformers provide an inherent AC coupled circuit. Baluns do not.
  - Can be used to convert Single-Ended Signals to Differential (in all cases)

Amplifier vs. Transformer

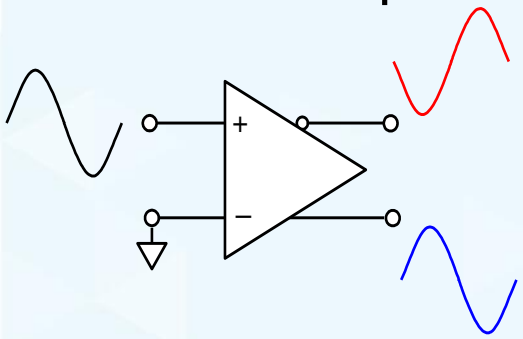
List of critical system parameters and which performs best….

Parameter	Usual preference
Bandwidth	Transformer
Gain	Amplifier
Passband flatness	Amplifier
Low Power	Transformer
Low Noise	Transformer
DC vs. AC coupling	Amplifier (dc level preservation) Transformer (dc isolation)

Transformer



Differential Amplifier

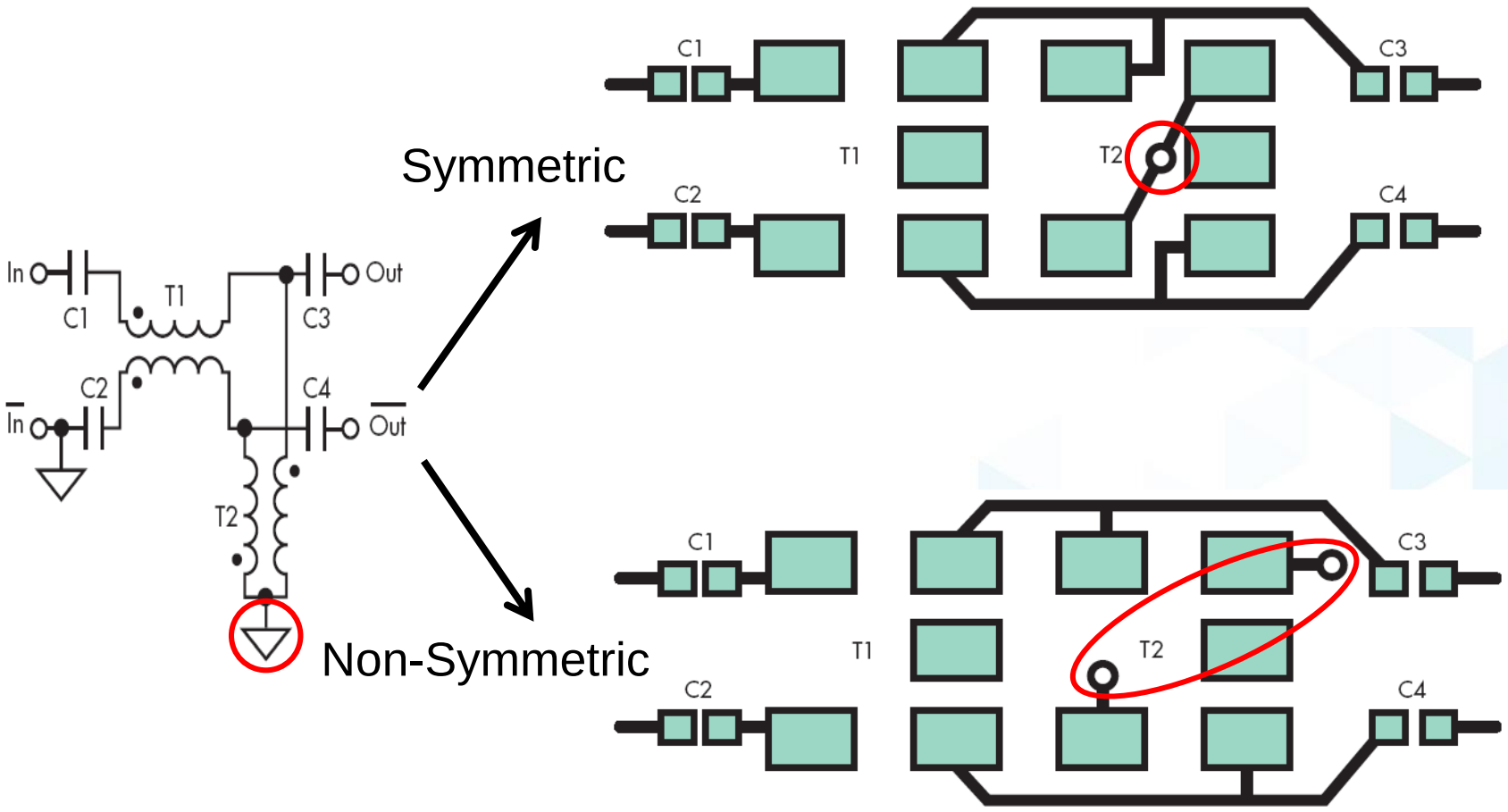


Input Balancing

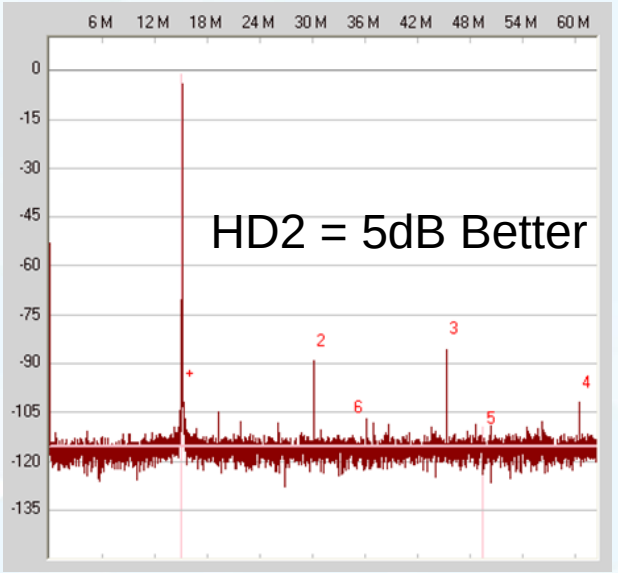
- Layout is another variable that can wreak havoc on any frontend design.
- Improper layout can literally mess up the frontend design causing unexpected performance. Take the time to keep the layout sound and symmetrical.
- Keeping the frontend network symmetrical, forces return currents or ground references to be common.
- On the following slide, the AD9268, 16bit, 125MSPS dual channel A/D converter is shown.
- An FFT performance plot was captured, using the symmetrical layout, this yielded a 2nd harmonic of 85dB with a 140MHz IF applied at -1dBFS.
- The second plot shows the performance under these same conditions however, a non-symmetrical layout was used. This consistently yields a 2nd harmonic of 79.5dB, more than 5dB loss in performance!

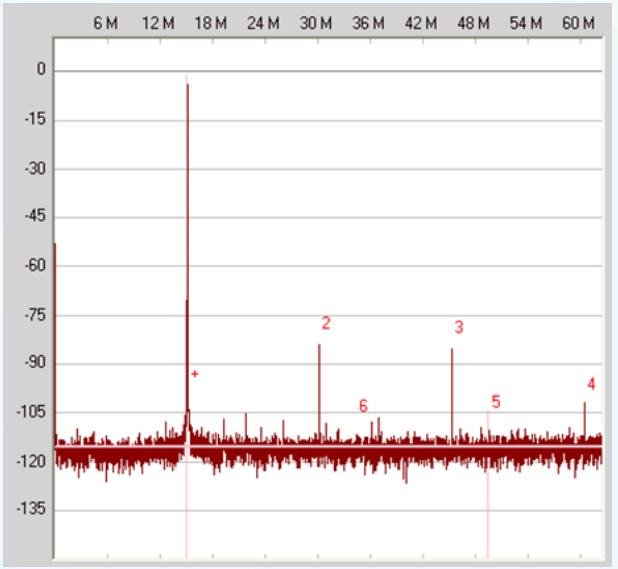
Input Balancing: Layout Consideration

Analog Frontend Balun example:



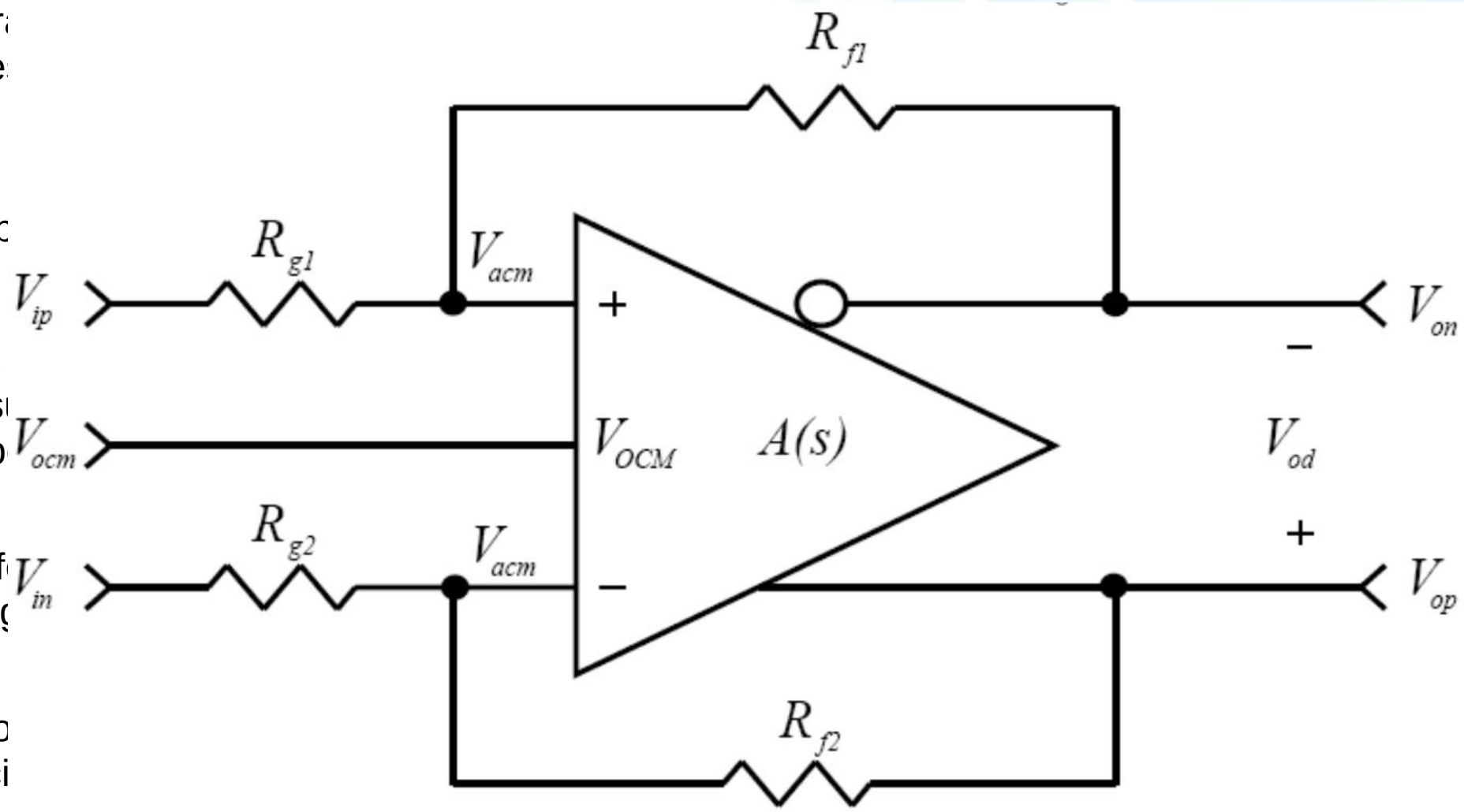
Performance Results





Amplifiers Have Imbalance Issues Too…

- Toler… …mming node… …nverters.
- Next … …mismatch can b…
- Beta … …will cause the s… …lf, the temp…
- A diff… …s, giving…
- To co… …, speci… …ces.



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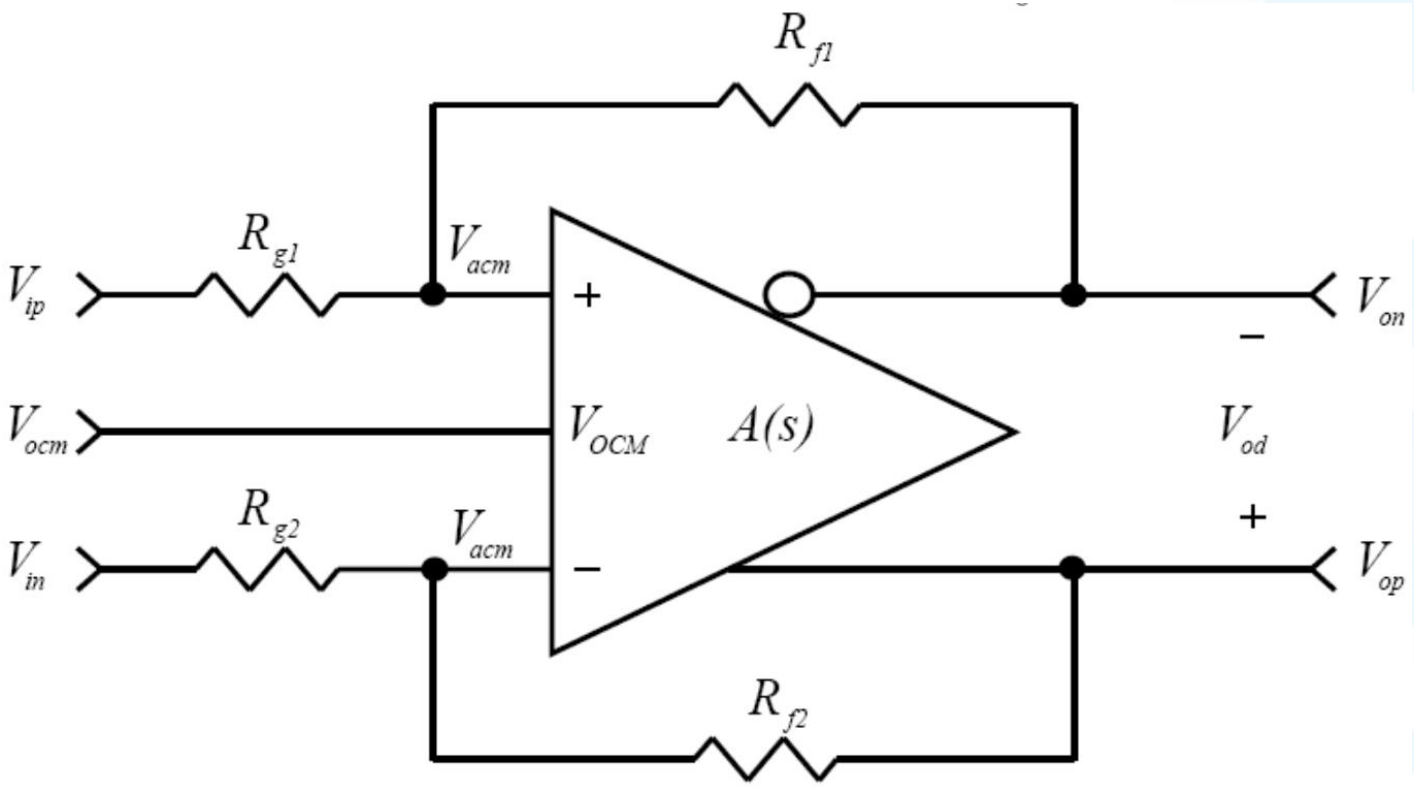


$$\beta_1 \equiv \frac{R_{g1}}{R_{f1} + R_{g1}}$$

$$\beta_2 \equiv \frac{R_{g2}}{R_{f2} + R_{g2}}$$

$$A(s) \rightarrow \infty$$

$$V_{acm} = \frac{2\beta_1\beta_2 V_{ocm} + V_{ip}\beta_2(1-\beta_1) + V_{in}\beta_1(1-\beta_2)}{\beta_1 + \beta_2}$$

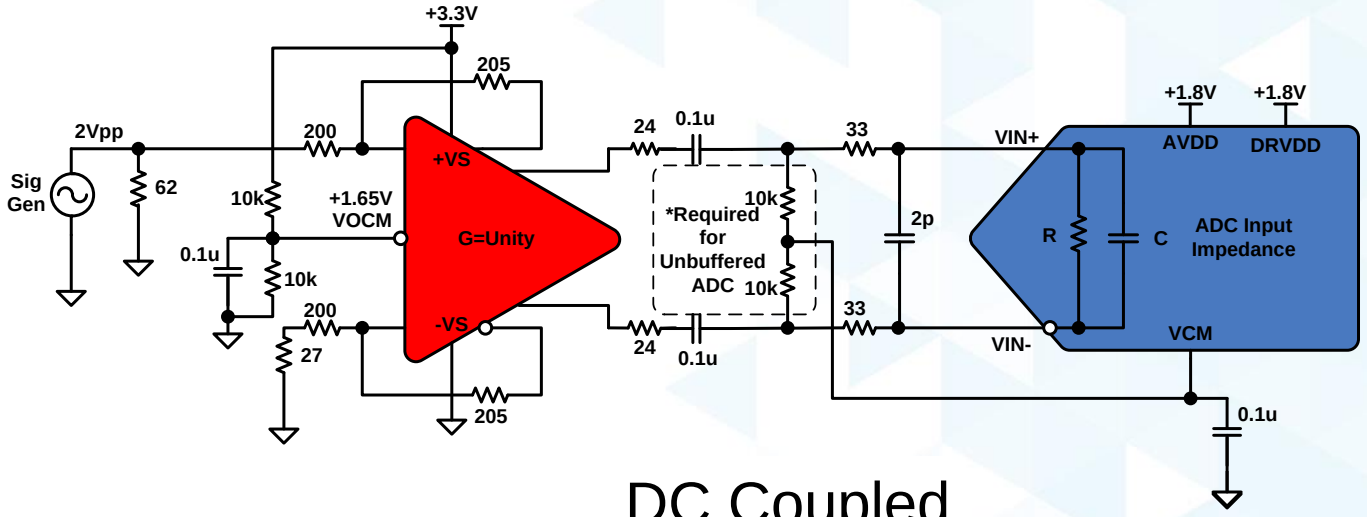
$$\beta_1 = \beta_2 \equiv \beta$$

$$V_{acm} = V_{icm} + \beta\left(V_{ocm} - V_{icm}\right)$$

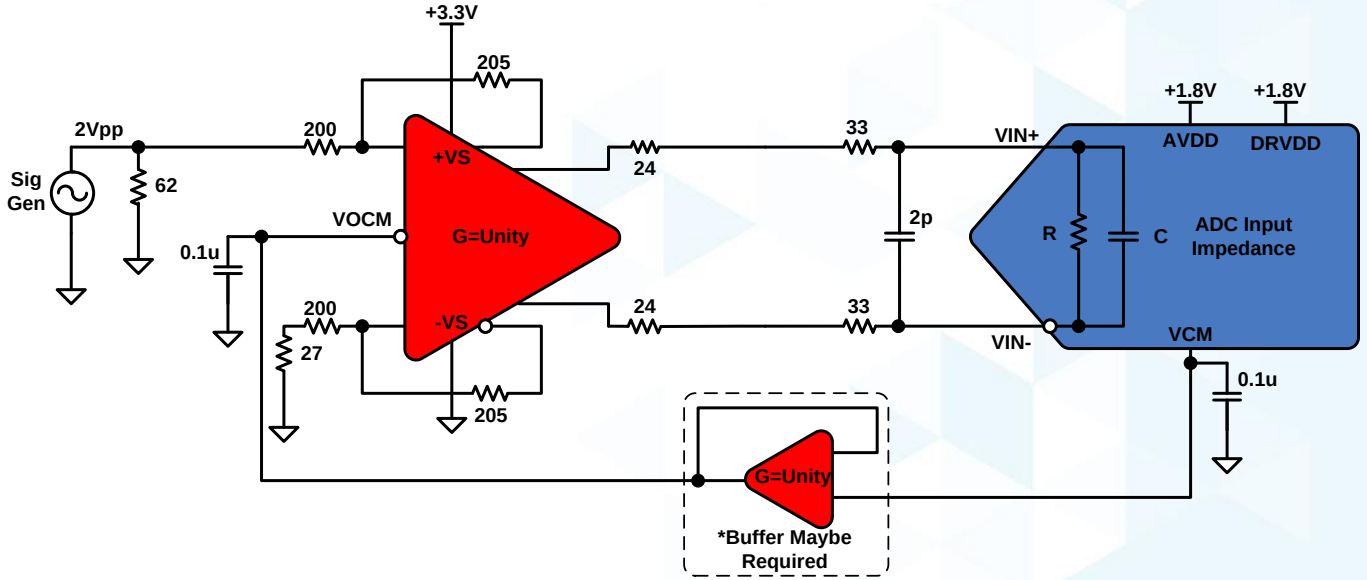
$$V_{icm} \equiv \frac{V_{ip} + V_{in}}{2}$$

Amplifier and ADC Interface Examples

AC Coupled



DC Coupled

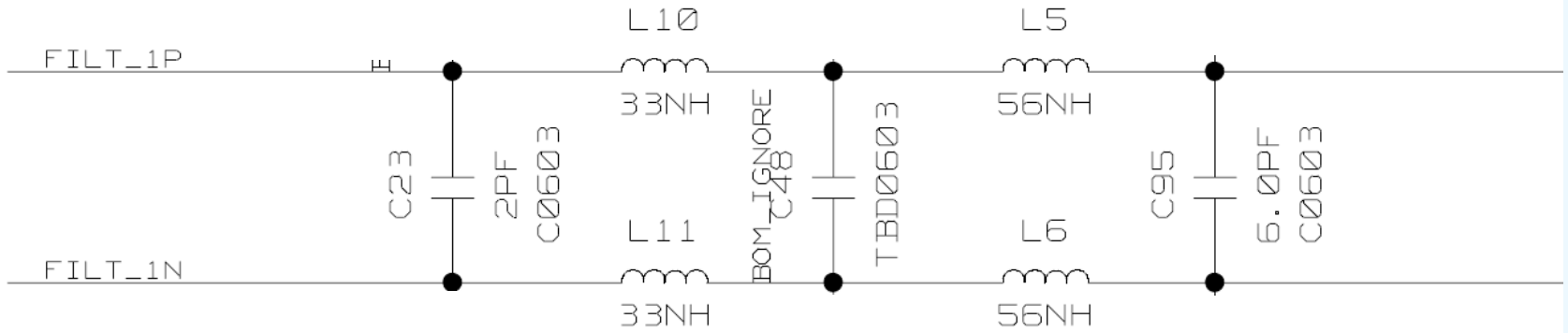


A/D Converter Common Mode Issues

Caution: Don’t use converter’s voltage reference pin (VREF) directly, usually half the converter’s full-scale, it may not be able to provide enough CM bias with good accuracy, use a buffer in between.

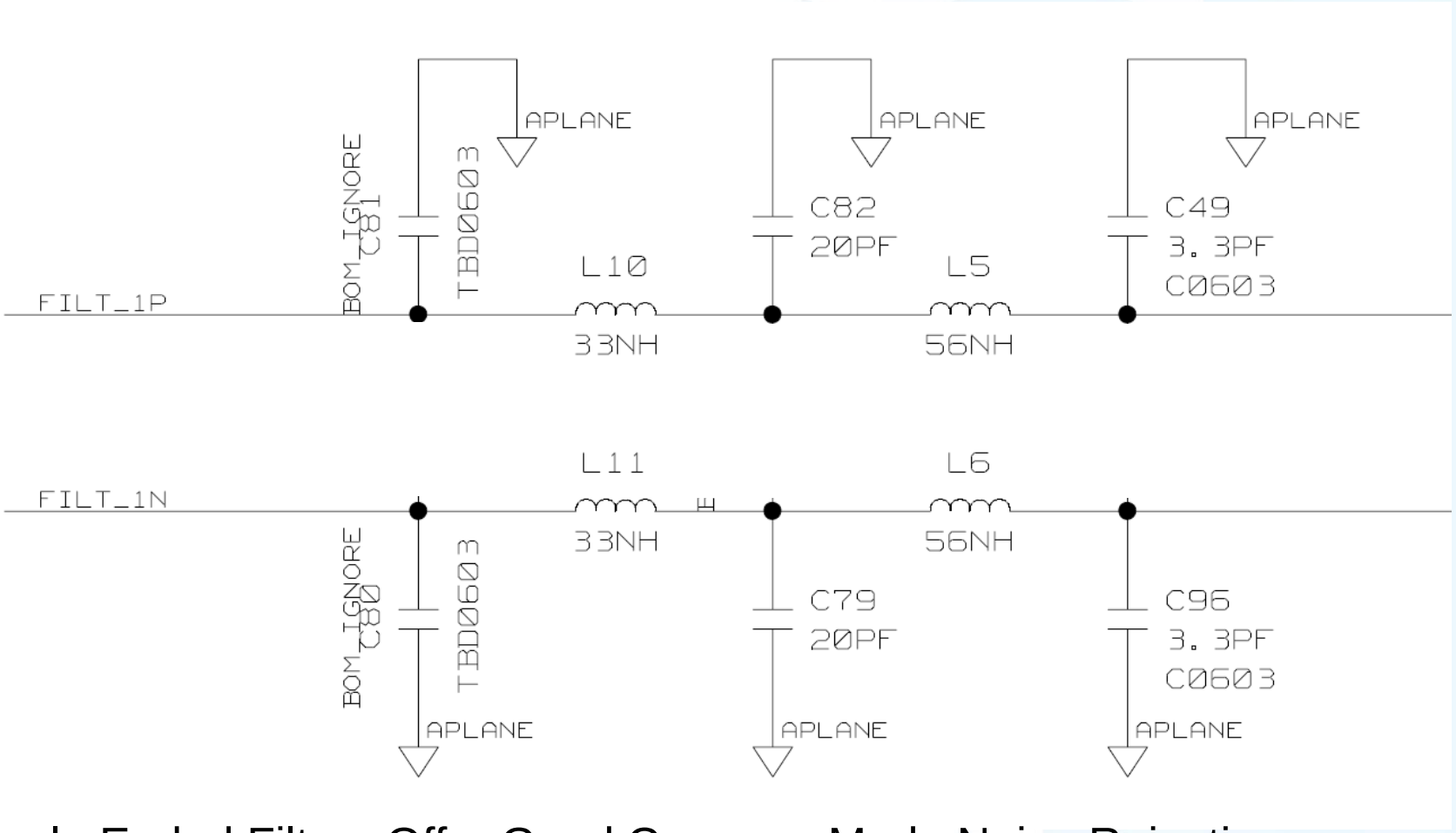
- The ADC needs an established CM bias on the analog inputs to reference signals above ground
- Unbuffered converters (aka: switched-capacitor type) requires an external CM bias on the analog inputs
- Buffered converters have self-biased analog inputs and are typically set by the converter’s internal buffer
- Buffered converters CM = half of the supply plus a diode drop above (AVDD/2+0.7V)
- Unbuffered converters don’t have an internal buffer, CM = AVDD/2 or half the analog supply
- Therefore, unbuffered converters must have this CM bias provided externally

What AFE Filter Topology is Best?



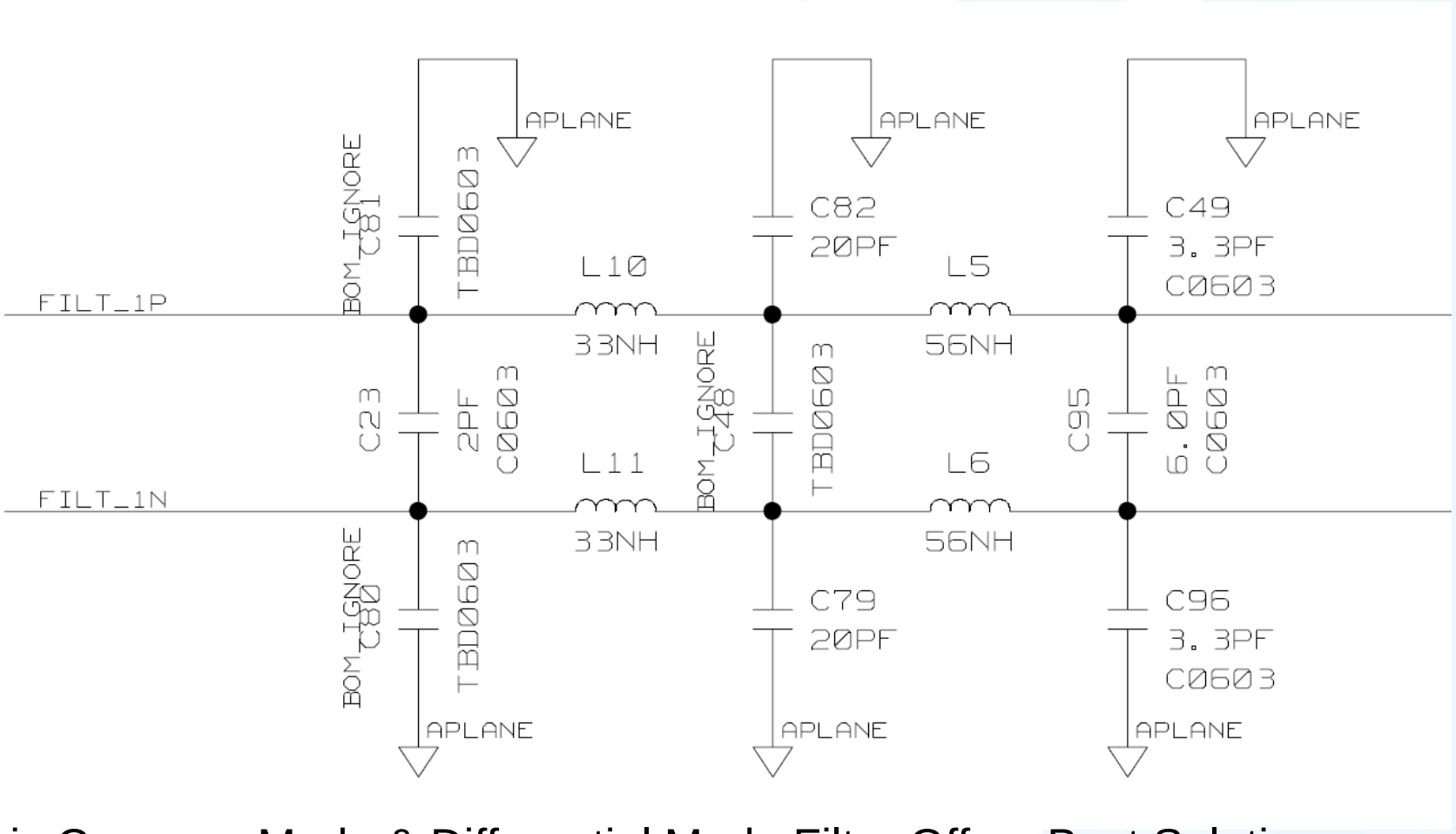
Fully Differential Filter Offers Best Differential Mode noise reduction
… But 0dB of Common Mode Filtering

What about Single-Ended Filtering?



Single Ended Filters Offer Good Common Mode Noise Rejection
…But no Differential Mode Filtering

What if we combine both?



This Common Mode & Differential Mode Filter Offers Best Solution
All three filters need a tight symmetric layout and good component matching.

Converter Specifications

ADC Terminology & Definitions

Test Conditions: How do we obtain the specifications in the datasheet

- Nominal power supply
- Analog input amplitude at -1dBFS
- Other conditions such as Internal reference, clock amplitude, and sampling rate are specified in the datasheet

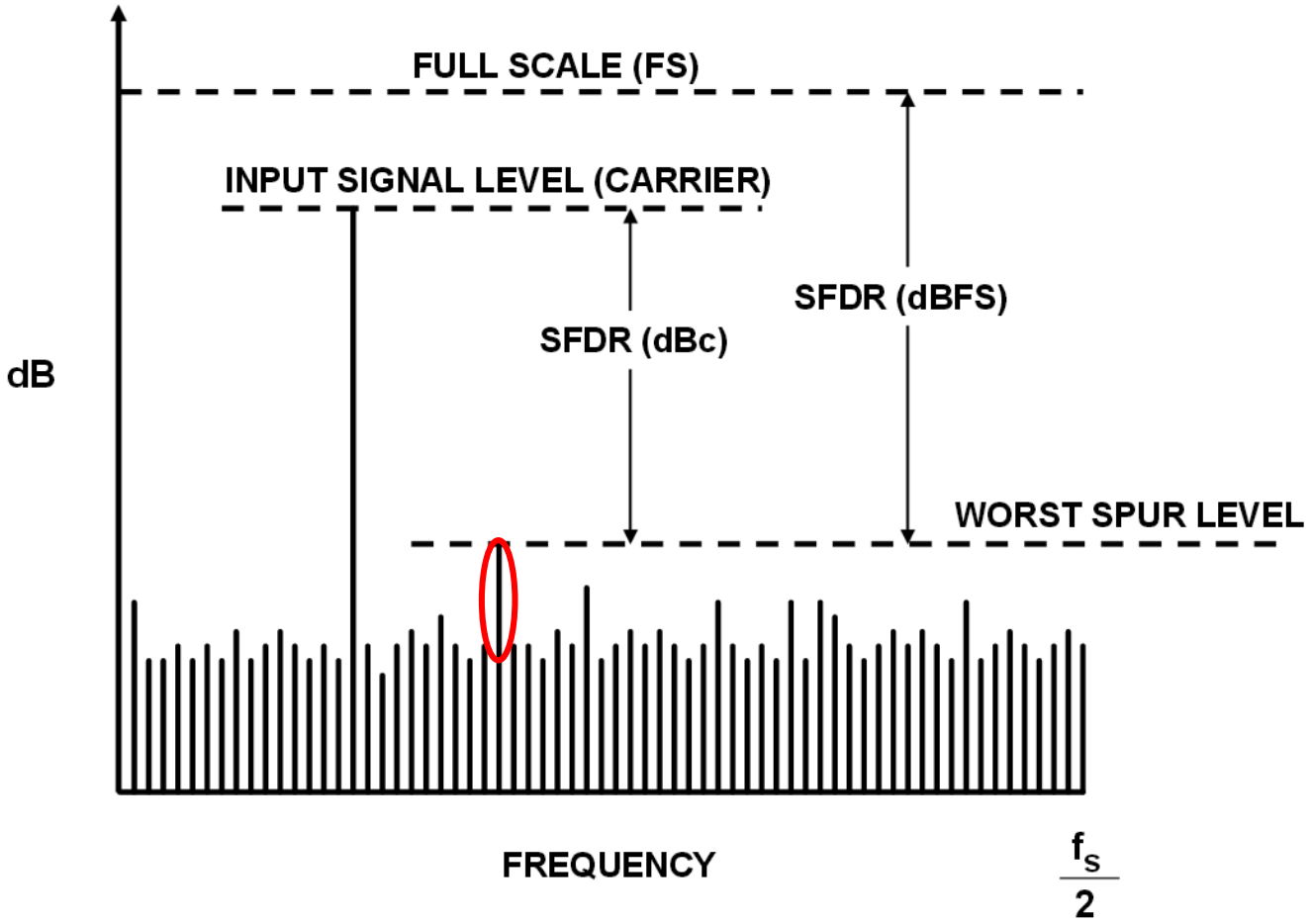
Why –1dB?

AC SPECIFICATIONS

AVDD1 = DVDD1 = DRVDD1 = 1.3 V, AVDD2 = DVDD2 = DRVDD2 = 2.5 V, specified maximum sampling, 1.2 V internal reference, AIN = –1.0 dBFS, sample clock input = 1.65 V p-p differential, default SPI settings, unless otherwise noted.

ADC Terminology & Definitions: SFDR

- A closer look at Spurious-Free Dynamic Range (SFDR)



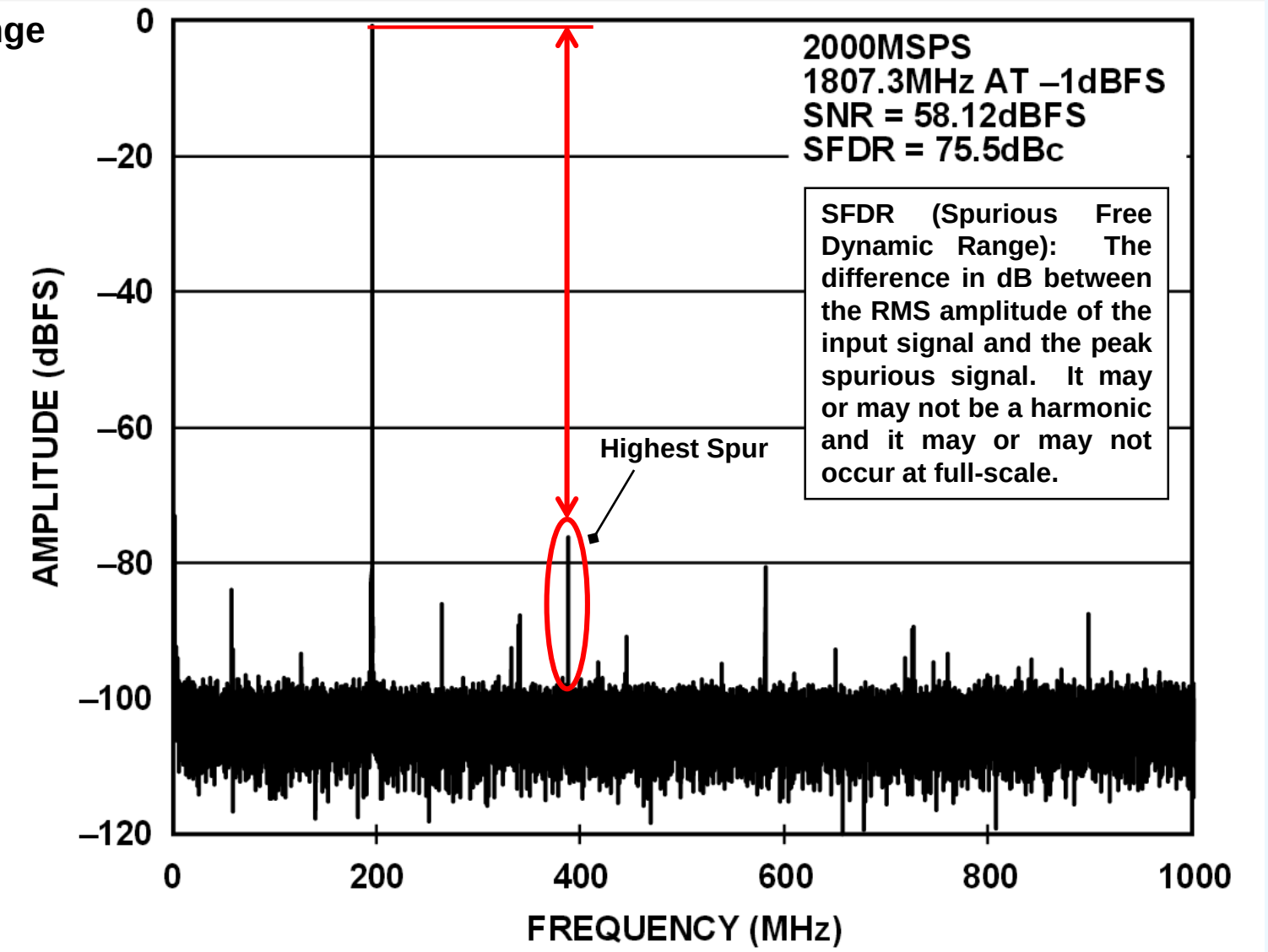
Why is SFDR Important?

SFDR is an important specification in communications systems because it represents the smallest value of signal that can be distinguished from a large interfering signal (blocker).

ADC Terminology & Definitions: SFDR

Spurious-Free Dynamic Range (SFDR, dBc or dBFS)

AD9625



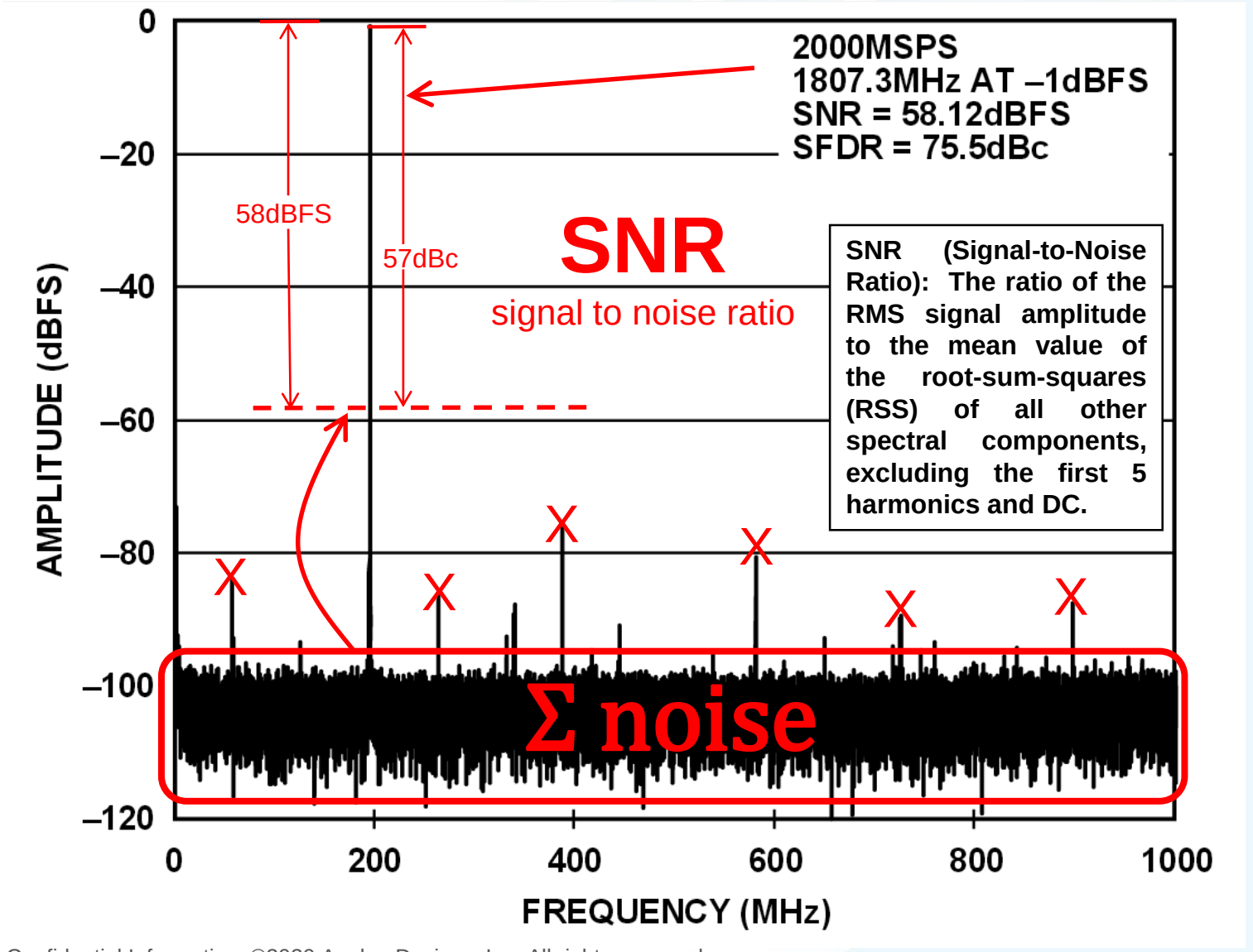
ADC Terminology & Definitions: SNR

Signal to Noise Ratio (SNR, dBc or dBFS)

Or some might use:

Noise Spectral Density (NSD, dBc/Hz)

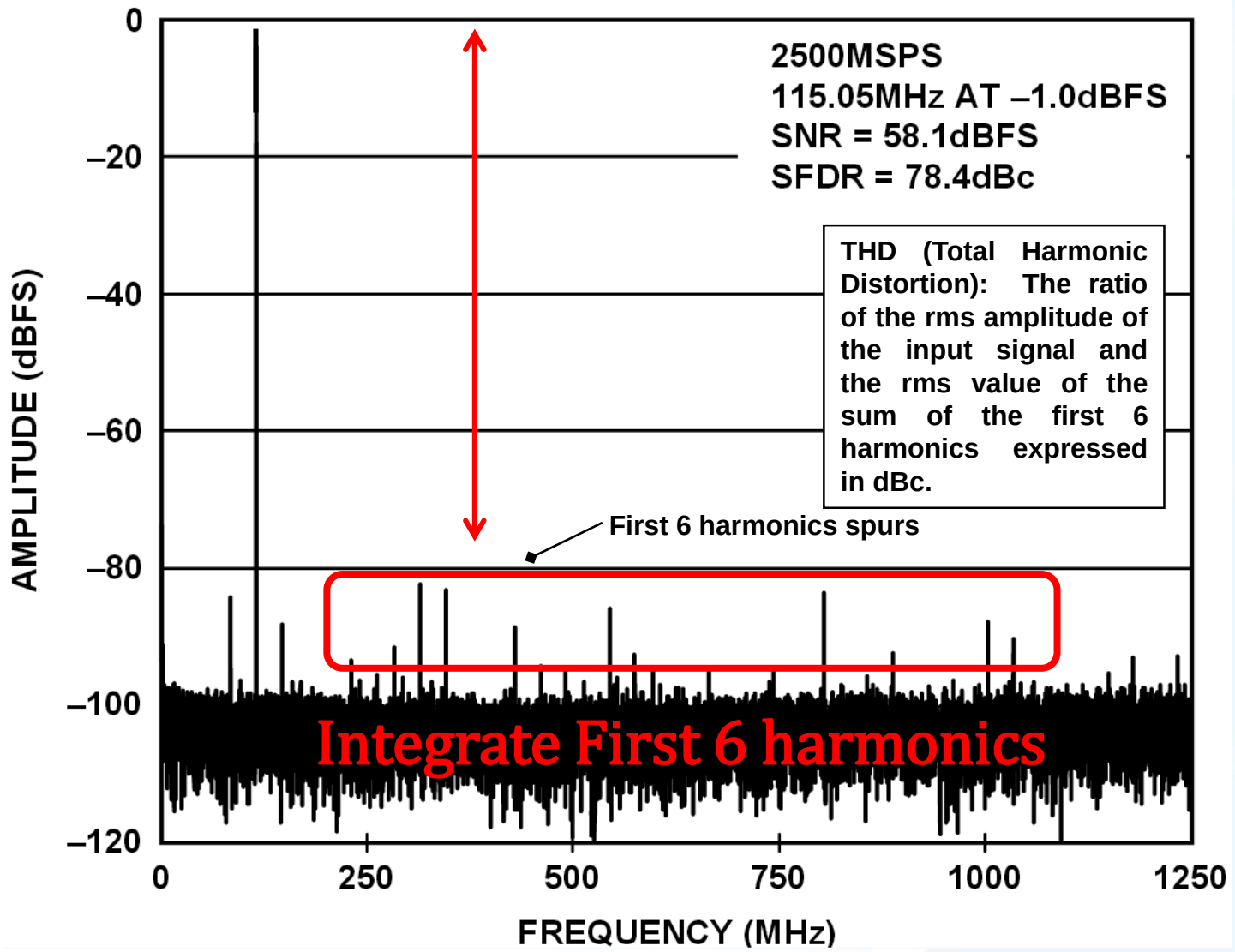
AD9625



ADC Terminology & Definitions: THD

Total Harmonic Distortion (THD, dBc or dBFS)

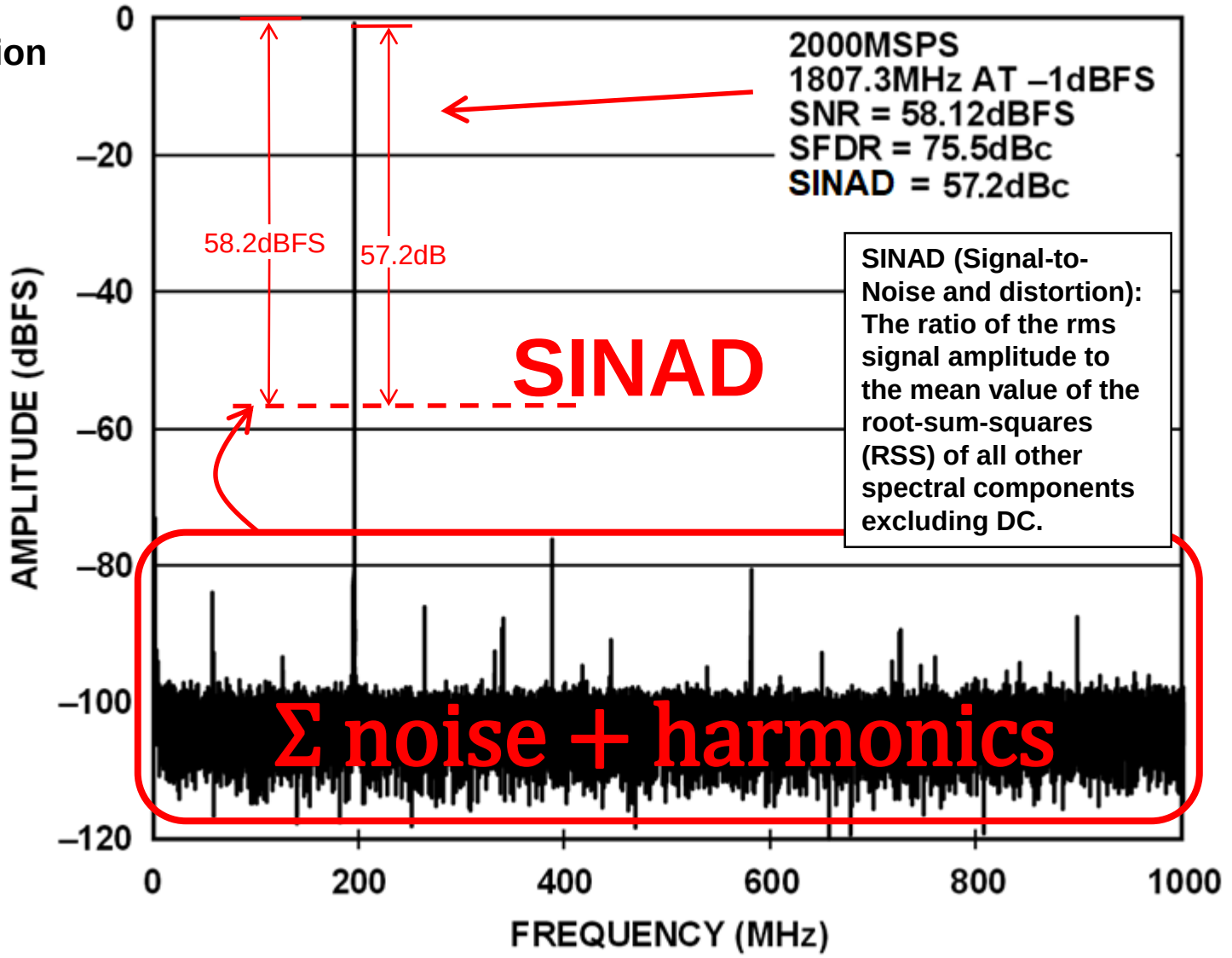
AD9625



ADC Terminology & Definitions: SINAD

Signal-to-Noise-and-Distortion (SINAD, dBc or dBFS)

AD9625



ADC Terminology & Definitions: ENOB

Effective Number of Bits (ENOB)

- SINAD is often converted to effective-number-of-bits (ENOB) using the relationship for the theoretical SNR of an ideal N-bit ADC

$$ENOB = \frac{SINAD(dBFS) - 1.76dB}{6.02}$$

The SINAD table shows that the AC performance of the ADC degrades due to high-frequency distortion. SINAD parameters such as these are very useful in evaluating the dynamic performance of ADCs.

EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 100 MHz		25°C	9.4	9.2	Bits
f_{IN} = 500 MHz		25°C	9.4	9.2	Bits
f_{IN} = 1000 MHz		25°C	9.3	9.1	Bits
f_{IN} = 1800 MHz		25°C	9.2	9.0	Bits

SIGNAL-TO-NOISE AND DISTORTION (SINAD)							
f_{IN} = 100 MHz		25°C		58.4		57.2	
f_{IN} = 500 MHz		25°C		58.4		57.0	
f_{IN} = 1000 MHz		25°C		58.0		56.5	
f_{IN} = 1800 MHz		Full	54.1	57.2	53.1	55.9	

ADC Terminology & Definitions: Resolution vs. ENOB

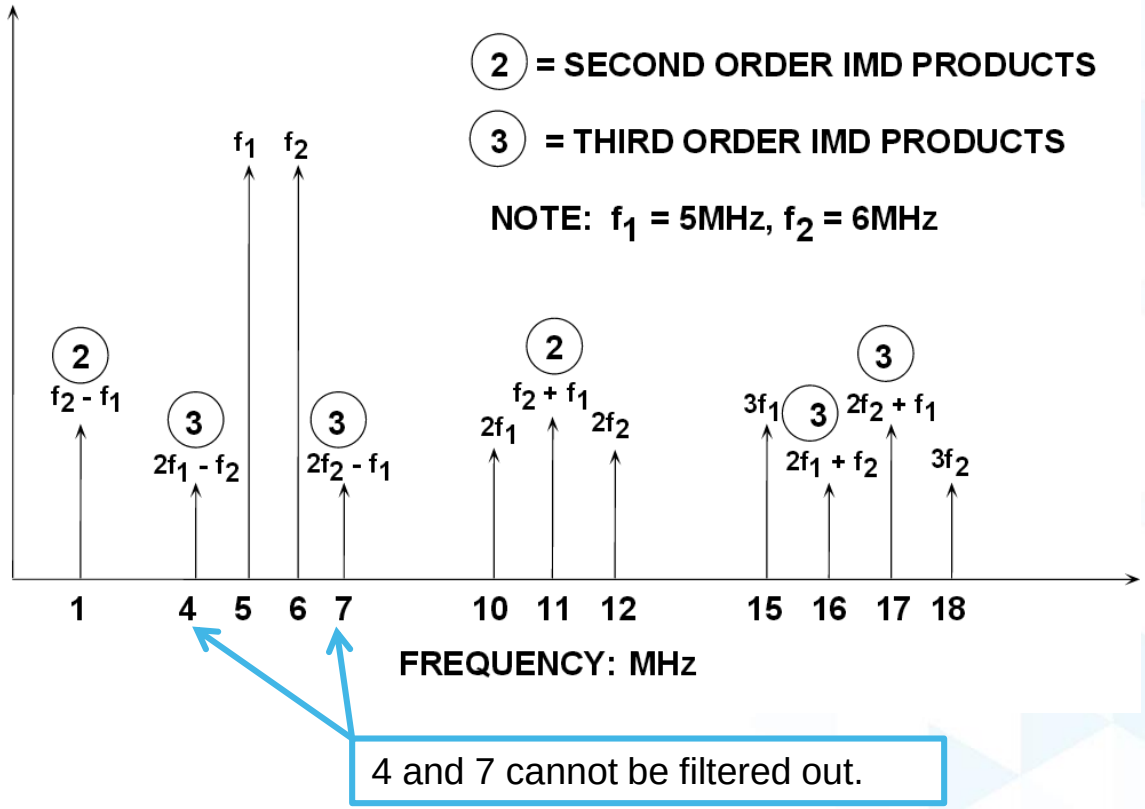
Part #	Max Sample Rate (MSPS)	#bits	Analog Input Full Scale (Vpp)	Low Frequency SINAD (dBFS)	ENOB
ADI Part #1	125	**14**	2	75.1	**12.2**
ADI Part #2	250	**16**	2.5	76.3	**12.4**
ADI Part #3	500	**12**	1.5	65.9	**10.7**

- ENOB is ALWAYS less than the number of bits.
- This gap generally gets wider with higher sample rate.
- More bits still is better!
  - If -1 < DNL < +1 there are no missing codes, therefore the number of codes = $2^{\#bits}$

ADC Terminology & Definitions: IMD

Two-Tone Intermodulation Distortion (IMD)

- When multiple tones are passed through a converter with nonlinearities, intermodulation distortion products (IMD) result.

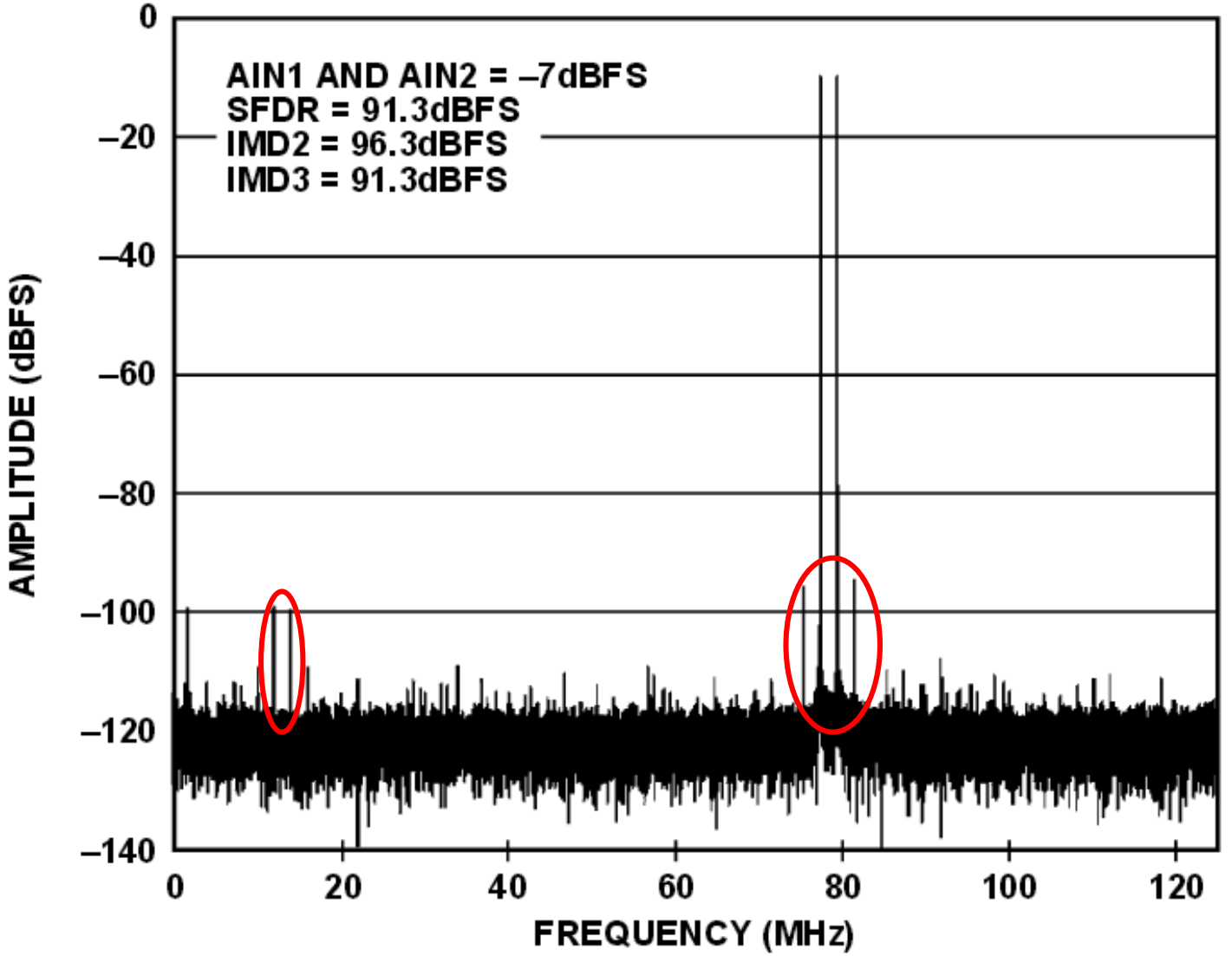


Third-order IMD products are especially troublesome in multi-channel communications systems where the channel separation is constant across the frequency band. Third-order IMD products can mask out small signals in the presence of larger ones.

ADC Terminology & Definitions: IMD

Two-Tone Intermodulation Distortion (IMD)

AD9467



ADC Terminology & Definitions: θ_{JX}

Thermal Specifications

AD9695 1.3GSPS ADC (28nm process)

Junction Temperature Range (T_J)	–40°C to +125°C
Storage Temperature Range, Ambient (T_A)	–65°C to +150°C

ORDERING GUIDE

Model[1]	Temperature Range
AD9695BCPZ-625	–40°C to +85°C
AD9695BCPZRL7-625	–40°C to +85°C
AD9695-625EBZ	
AD9695BCPZ-1300	–40°C to +85°C
AD9695BCPZRL7-1300	–40°C to +85°C
AD9695-1300EBZ	

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC_BOT}[1,3]	θ_{JC_TOP}[1,3]	θ_{JB}[1,4]	θ_{JT}[1,2]	Unit
CP-64-17	0	22.5	1.7	7.6	4.3	0.2	°C/W
	1.0	17.9					°C/W
	2.5	16.8					°C/W

AD9625 2.6GSPS ADC (65nm process)

Storage Temperature Range	–60°C to +150°C
Operating Case Temperature Range	–40°C to +85°C (measured at case)
Maximum Junction Temperature	110°C

PCB	T_A (°C)	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	Ψ_{JB} (°C/W)	θ_{JC} (°C/W)
4-Layer	85.0	18.7	0.61	6.1	1.4
10-Layer	85.0	11.5	0.61	4.1	N/A[1]

ADC Terminology & Definitions: θ_{JX}

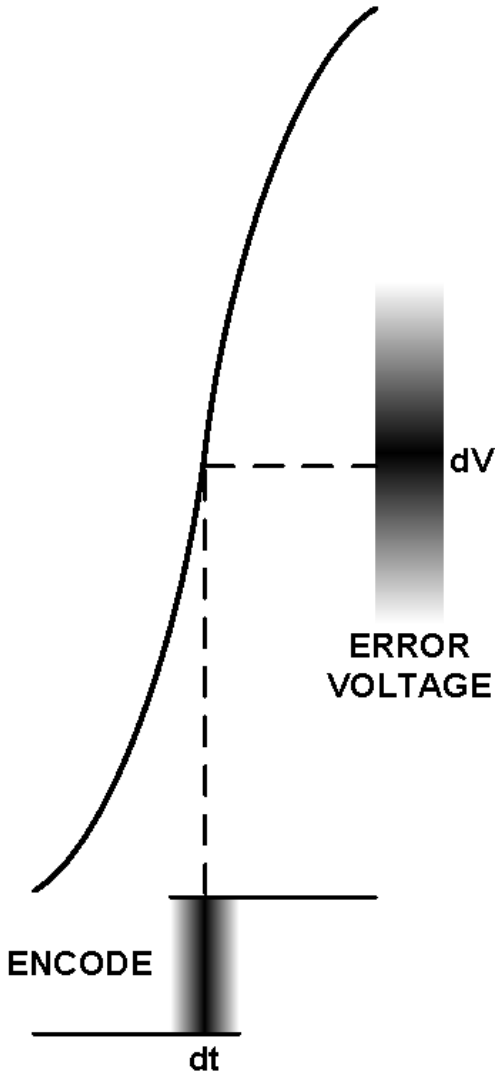
THERMAL CHARACTERISTICS

Typical θ_{JA}, θ_{JB}, and θ_{JC} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation effectively reducing θ_{JA} and θ_{JB}. In addition, metal in direct contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes, reduces θ_{JA}. Thermal performance for actual applications requires careful inspection of the conditions in an application. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 6.

THE MAXIMUM JUNCTION TEMPERTURE SHOULD NEVER BE EXCEEDED

Sampling Clock

Time Jitter is a common noise source



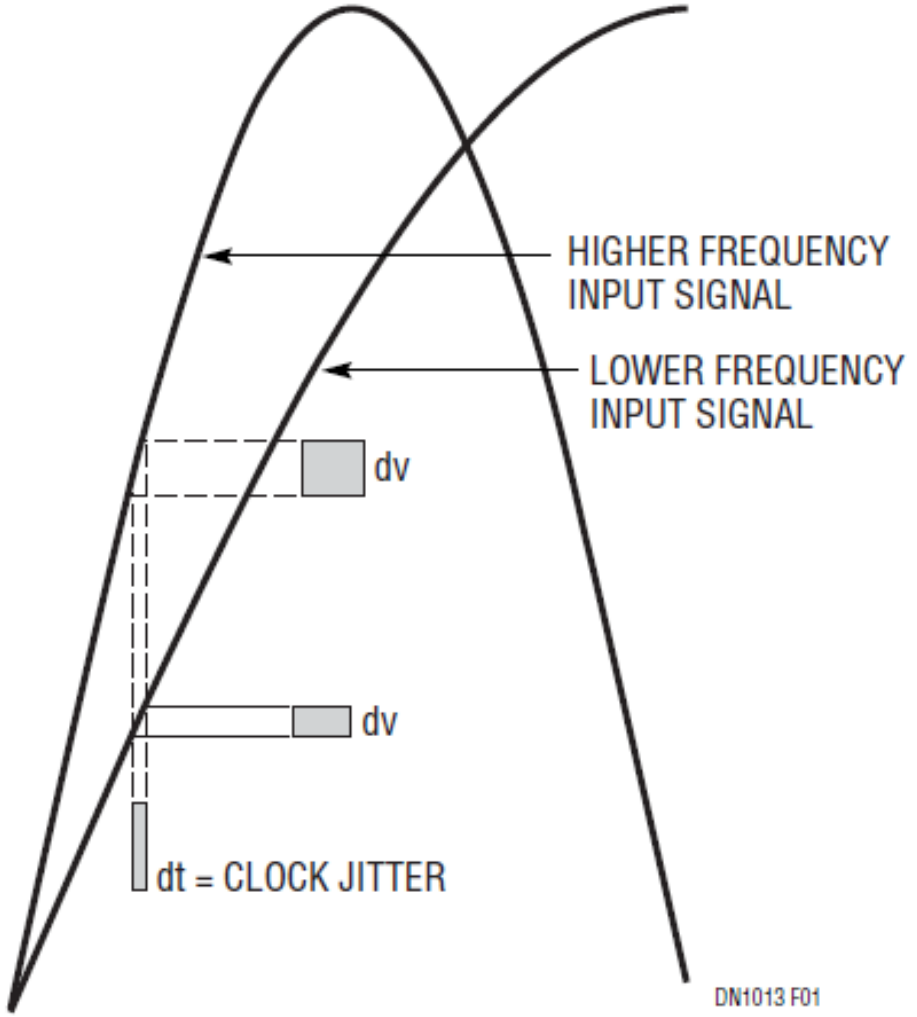
- Clock jitter is the sample-to-sample variation in the encode clock (both the external jitter as well as the internal jitter).
- Jitter (in time domain) is analogous to Phase Noise (in Frequency Domain)
- Phase noise is more common spec for RF converters
- See updated AN-501 and new AN-756

  SHA = Sample & Hold Amplifier

  SNR = Signal to Noise Ratio

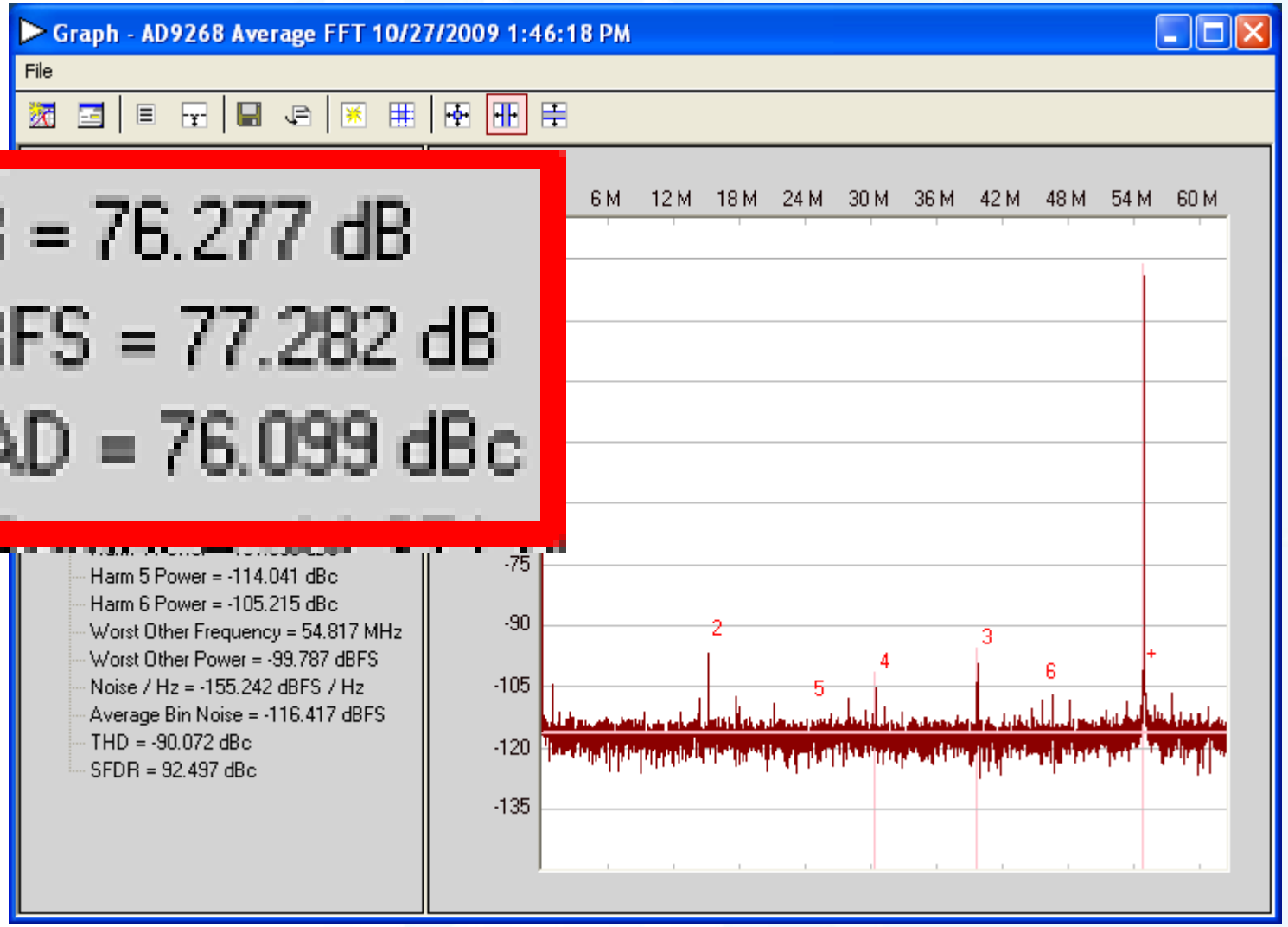
Slew Rate Worsen Effects of clock jitter

$$SNR_{jitter} = 20\log\left(\frac{S_{rms}}{N_{rms}}\right) = 20\log\left(\frac{1}{2\pi f t_{jitter}}\right)$$



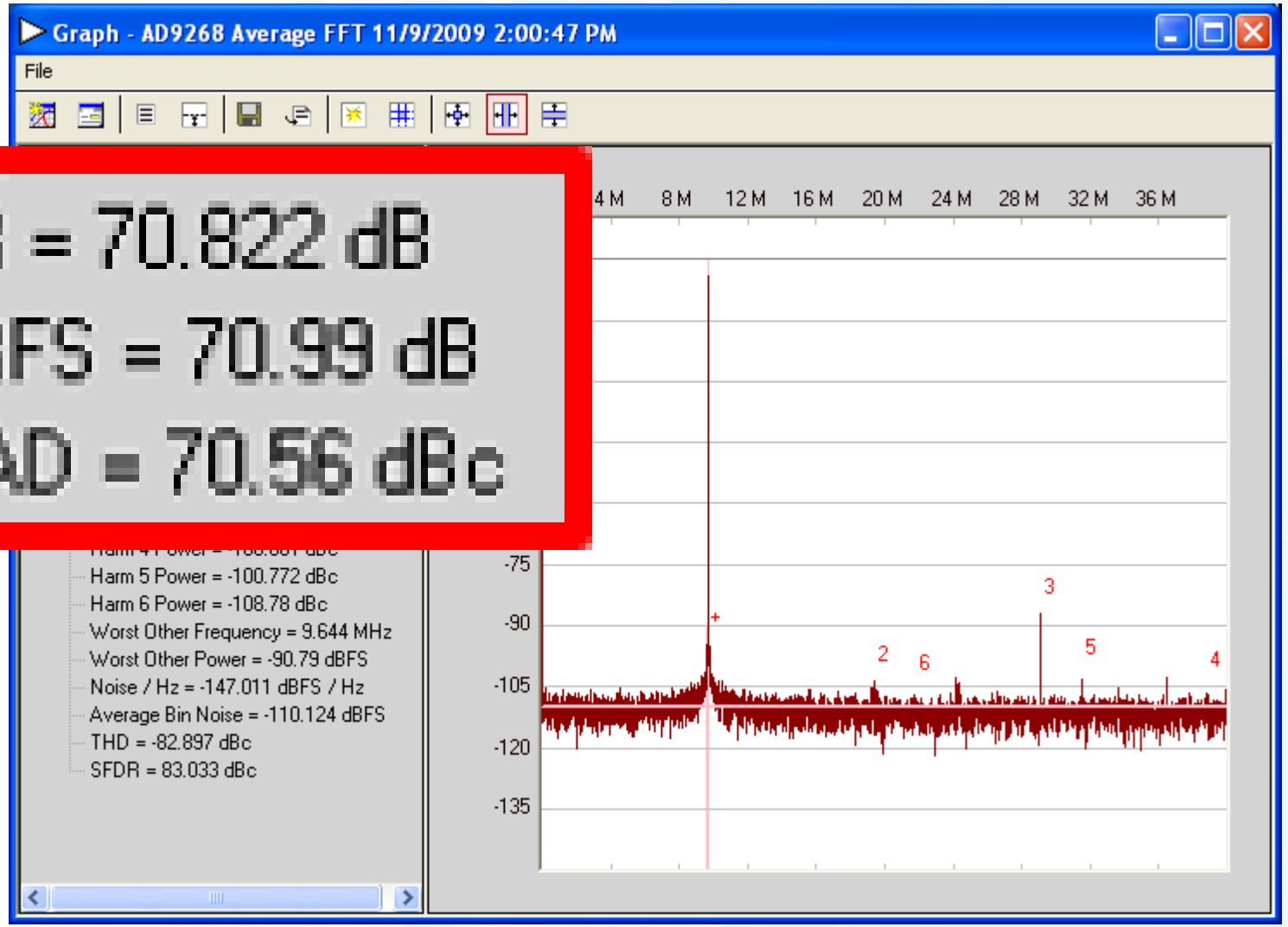
ADC Performance for Various Clock Reference

AD9268, 16bit,
125MSPS FFT Plot
High Performance (l
jitter) Clock Applied



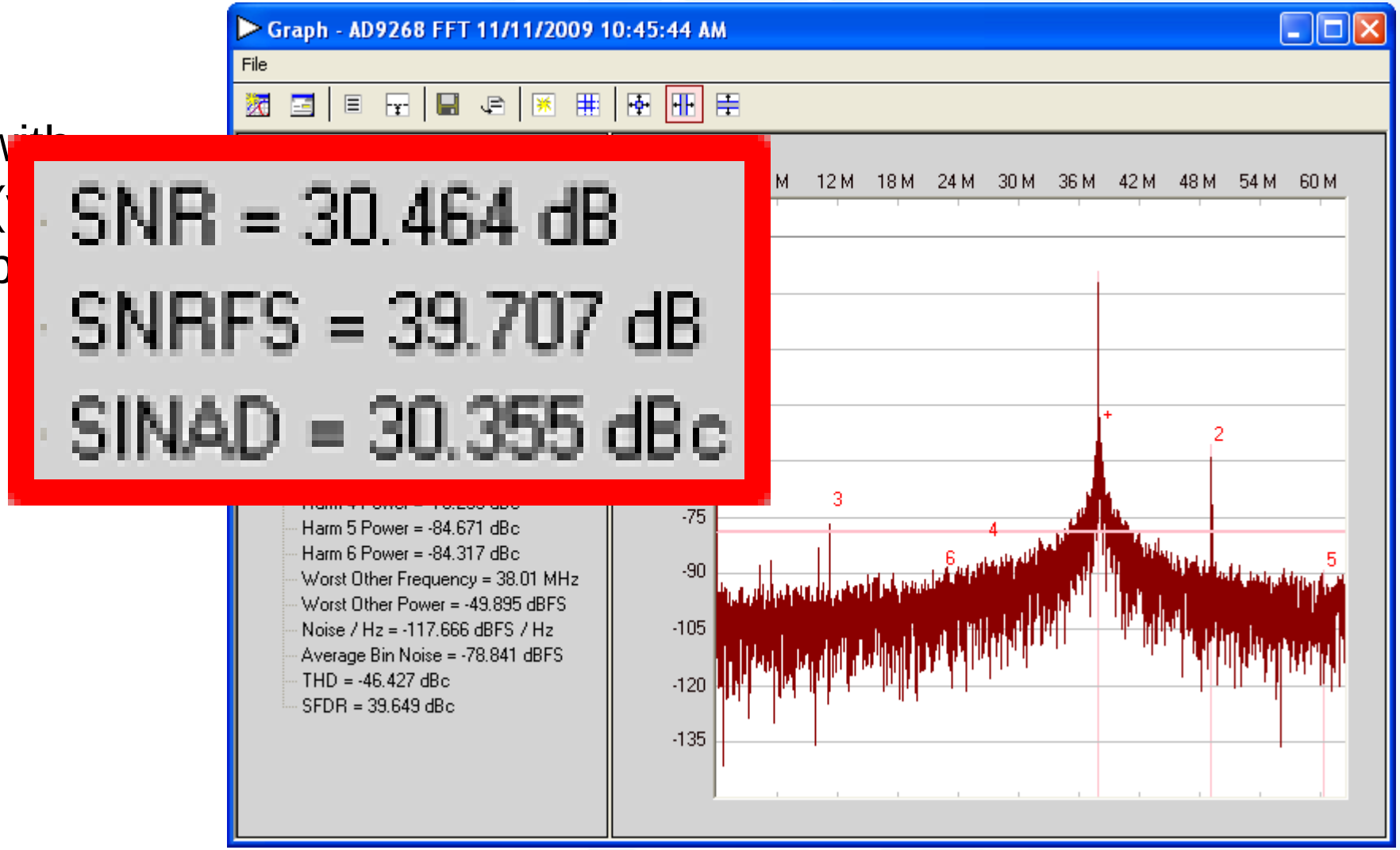
ADC Performance for Various Clock Reference

AD9268 FFT Plot w
Low Performance (
jitter) Clock Applied



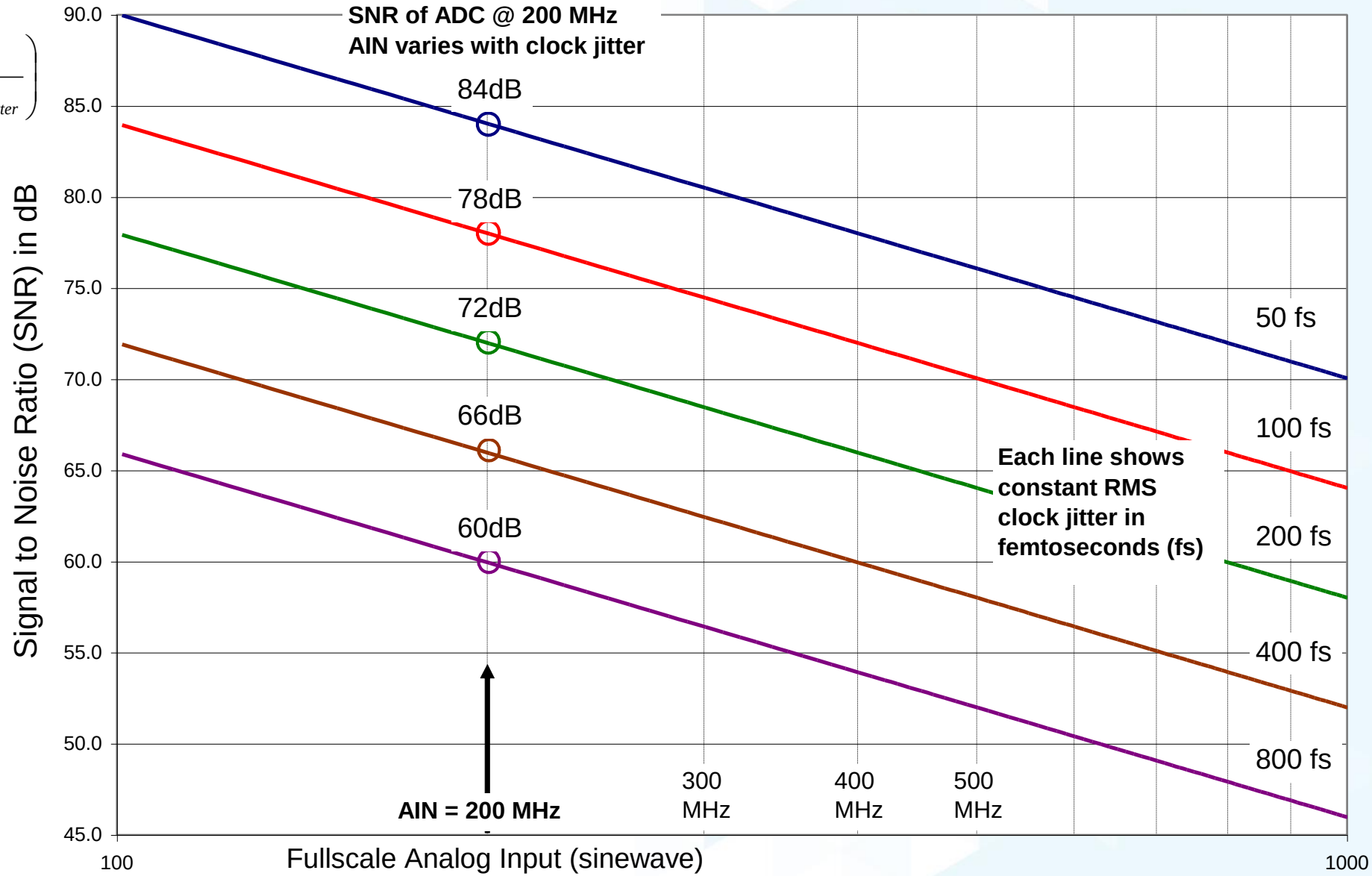
ADC Performance for Various Clock Reference

AD9268 FFT Plot w
Low Performance (
high jitter) Clock Ap



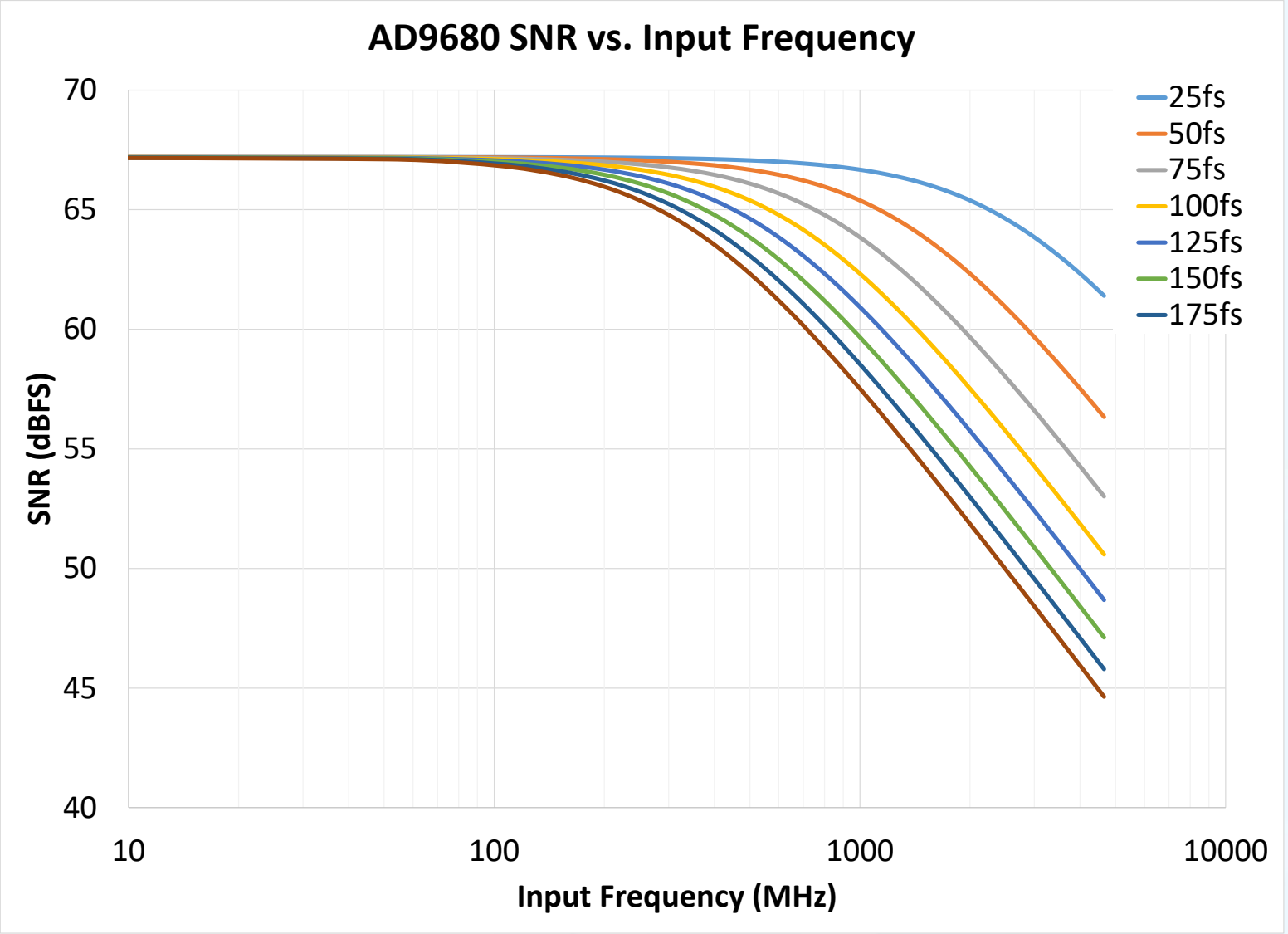
As analog signal increases, jitter hurts SNR

$$SNR_{jit} = 20\log\left(\frac{1}{2\pi f t_{jitter}}\right)$$



Jitter Causes SNR Degradation

HMC7043 has 15fs rms Of additive jitter at 2.4GHz



Clock Summary

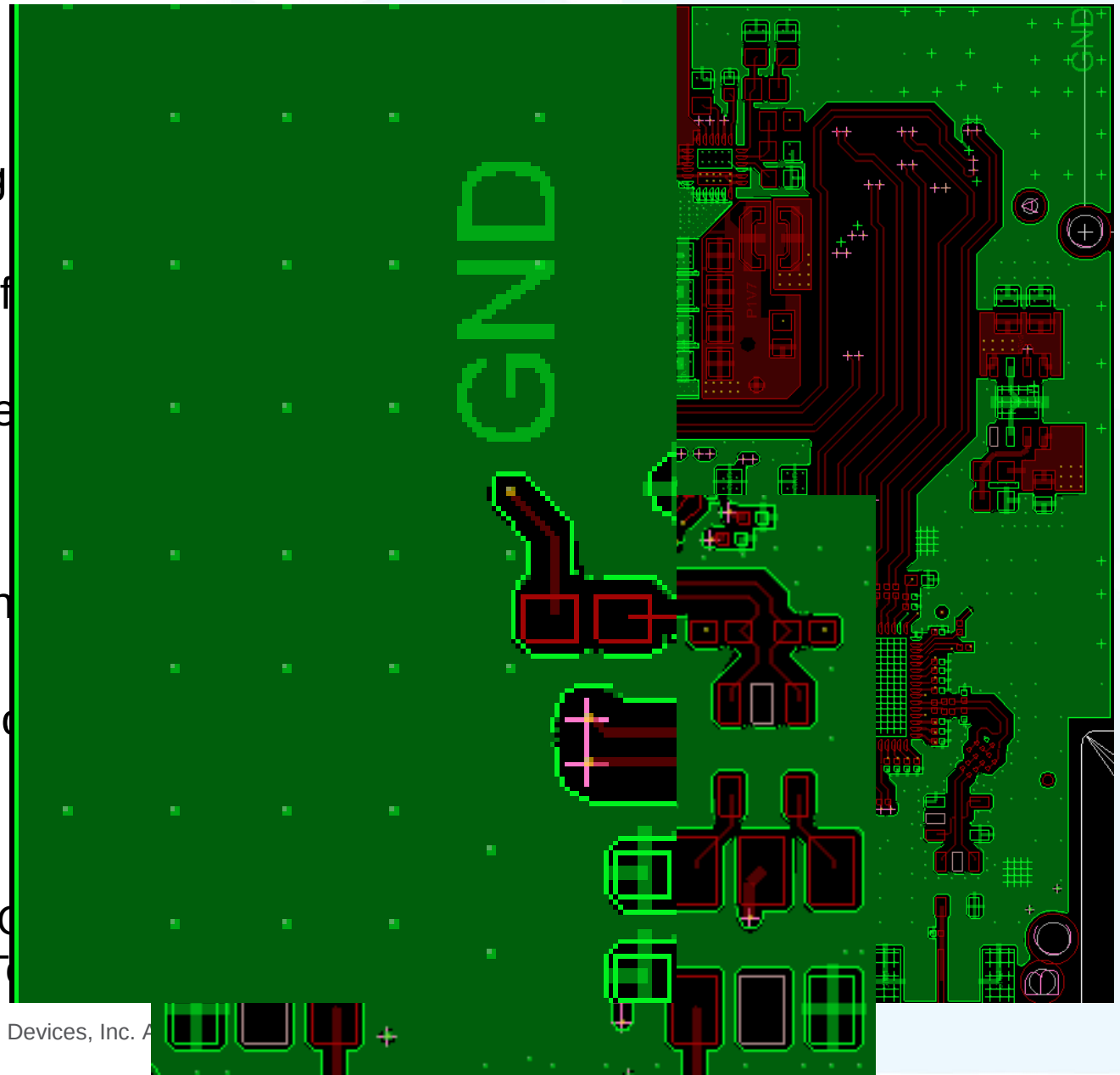
- Gate Driven Input
  - Watch for jitter ratings on logic gates
  - When using multiple gates in series the total RSS jitter is presented to the ADC input clock
  - PECL type gates provide some of the best performance, but burn more power
  - Easily connect multiple gates for fan out distribution
  - Easily provide single-ended to differential conversion

- Transformer Driven Input
  - Free noise gain coupling source
  - Could be used to do some low-level filtering to reduce the noise presented at the clock inputs
  - Jitter free coupling source
  - Limited signal “drive” distance capability
  - More difficult to connect multiple clock drives together
  - Easily provide single-ended to differential conversion

Layout & Decoupling

PCB Layout Recommendation for HS Converters

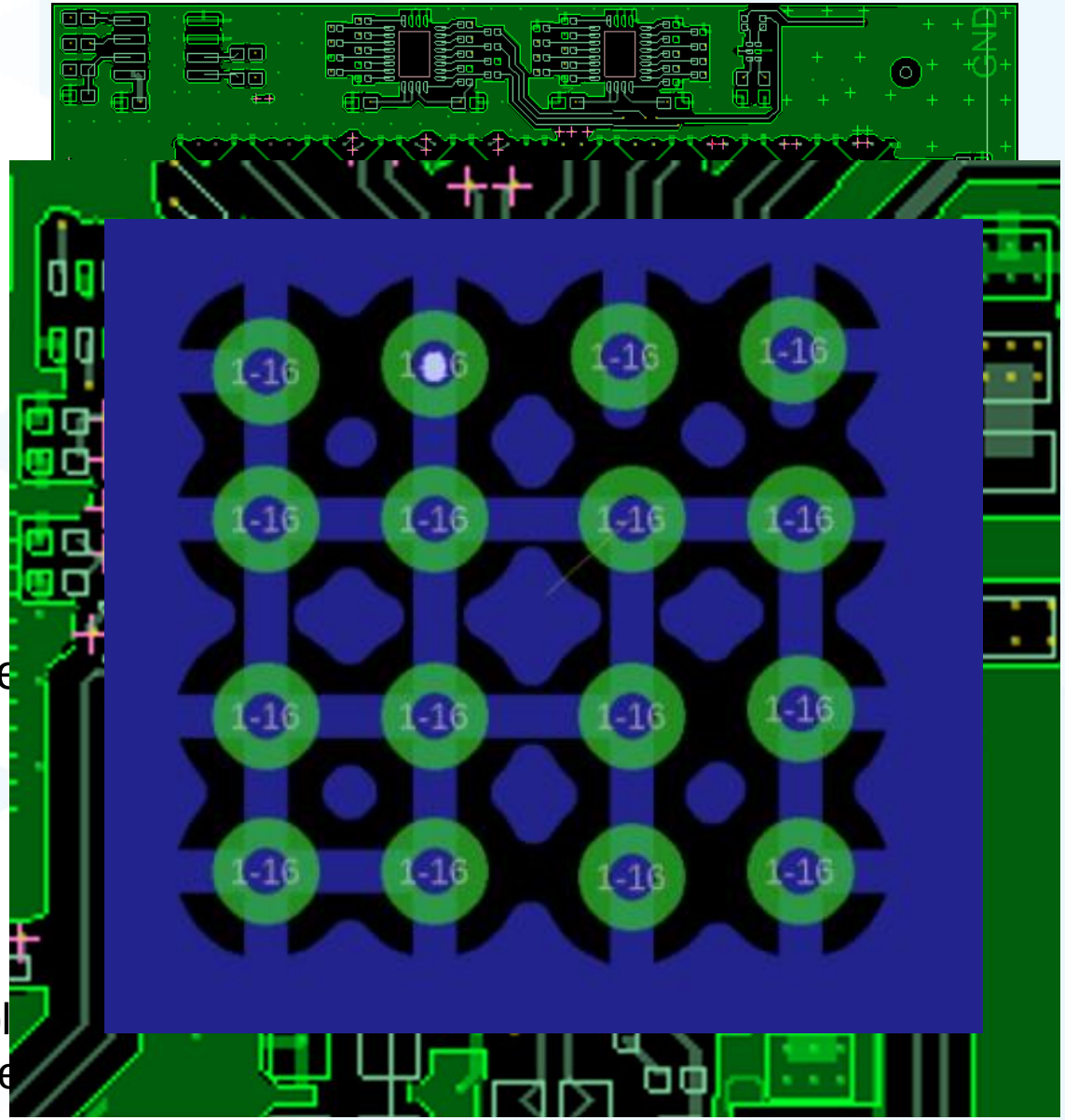
- Keep it compact.
- No splits in the ground plane across a sig
- Use vias every 50 mils to ground copper f
- Don't flood too close to signal lines or one differential pair, especially analog input!
- Don't put any impedance discontinuities n
- Don't create a coupling path where you d them. (Close traces running in parallel)



FMCDAC
Layout T

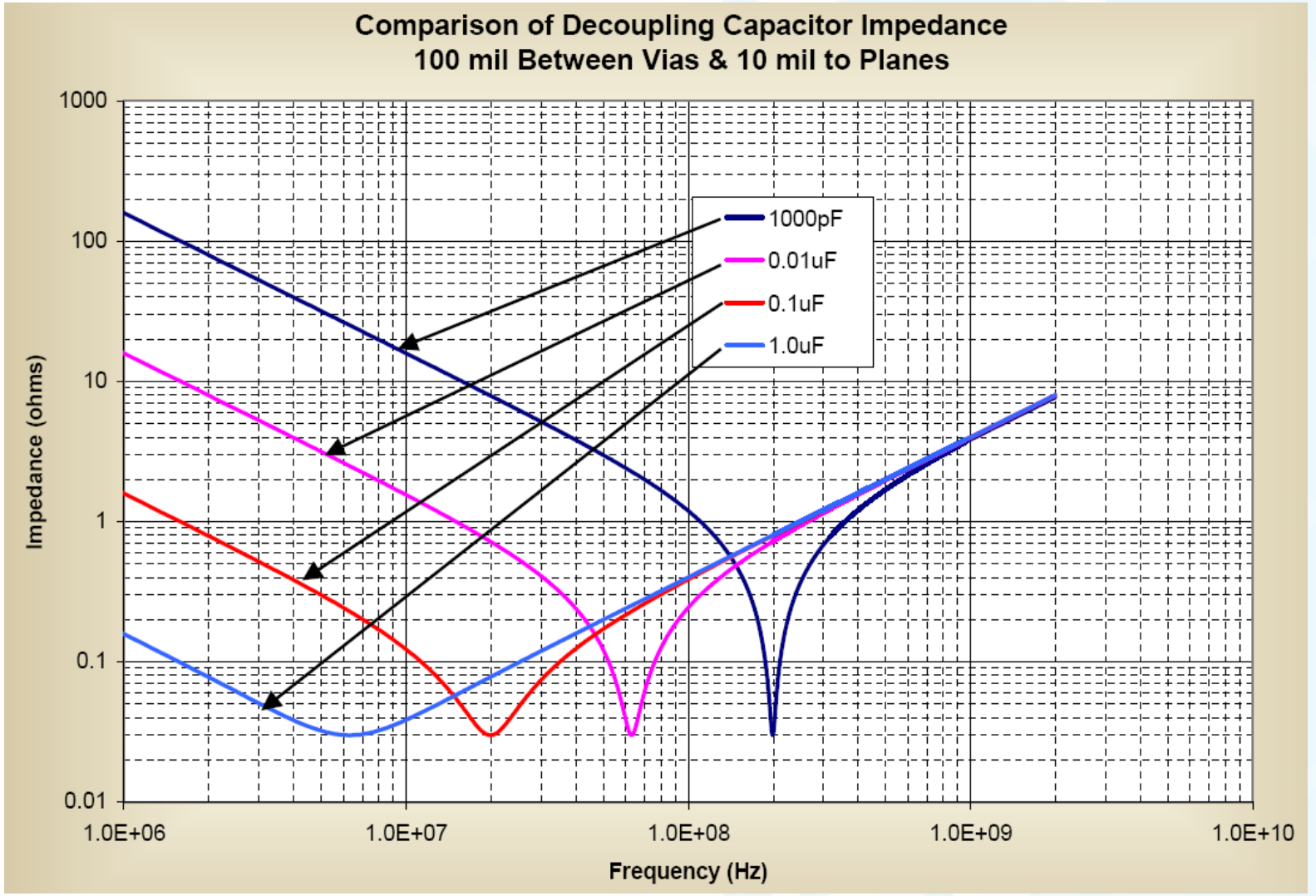
PCB Layout Recommendation for HS Converters

- Keep noise sensitive things, including the ADC, away from edges.
- Be careful with overlapping power planes.
- Ground bypass capacitors to the same plane as that under the ADC.
- The bypass capacitors of an output stage should be grounded towards the load. (might apply to DACs)
- Don't use thermal relief vias for Grounding.

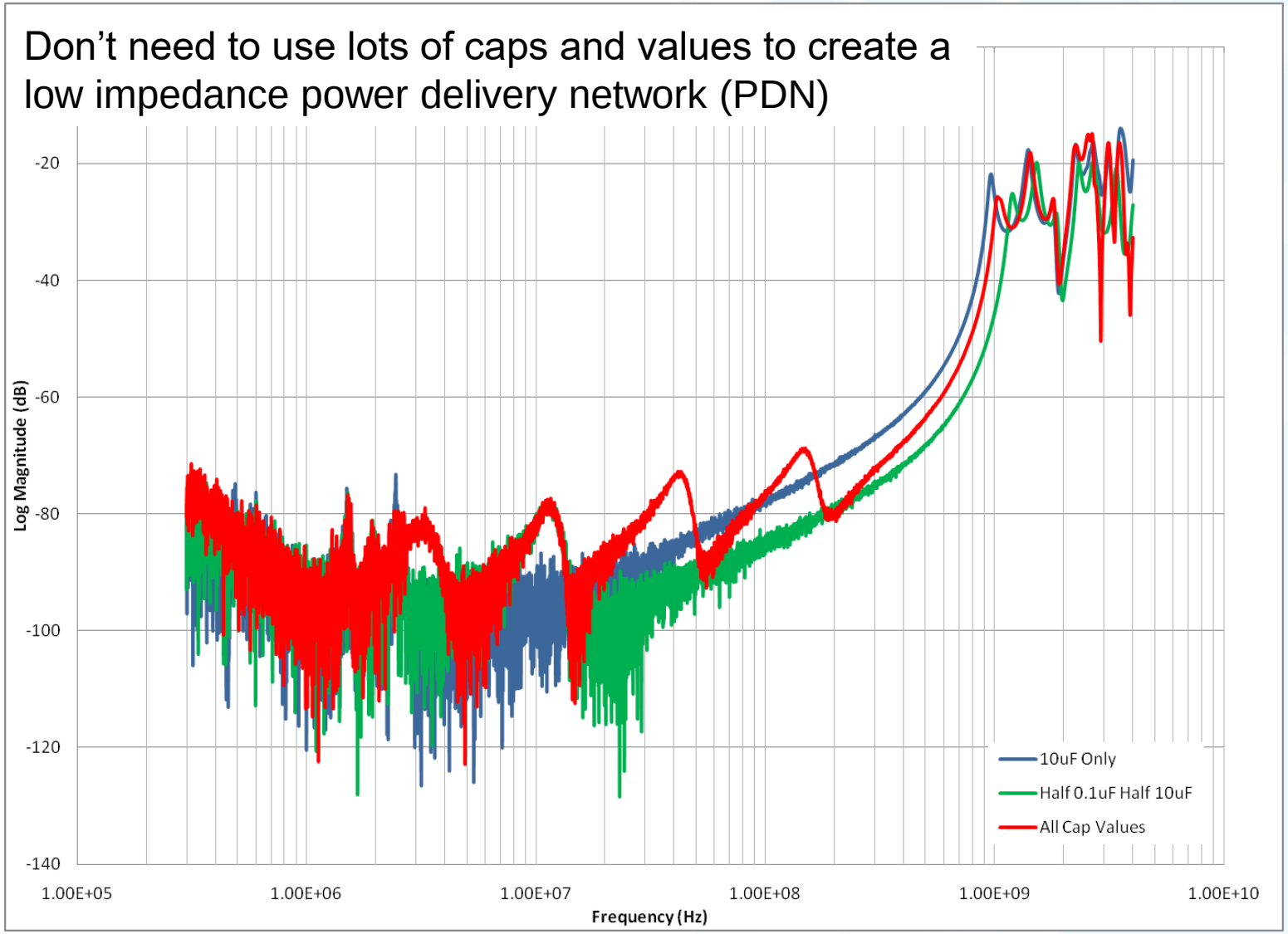


FMCDAQ3 Exampl
Layout Bottom Side

Decoupling – Goal of Multiple Caps in Parallel

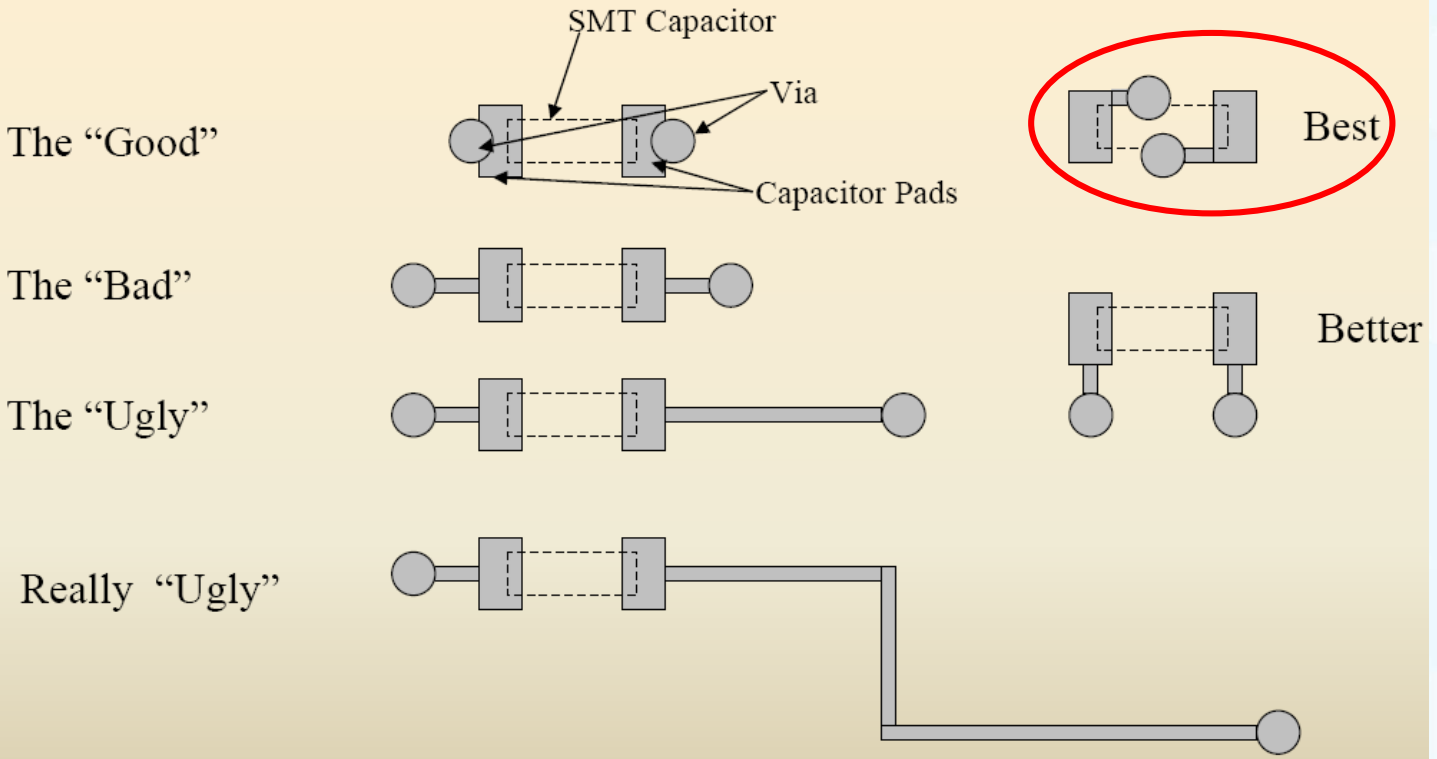


Decoupling Cont. – Reduced Caps



Decoupling Layout Strategies

Via Configuration Can Change Inductance



Power Supply

Power Solution for HS Converter Application

- High Speed Converter has many supply rails
  - Optimizing the overall power is tricky (especially for SWaP)
- SNR/SFDR requirements might not be too rigid
  - LDO not always needed
- LDO dropout can be optimized to minimize power loss
- Select the Switching regulator architecture that better suite your design
  - Controller for higher voltage and currents requirements
  - Monolithic for good power and cost balance, and flexibility
  - uModule for ease of design, smaller pcb footprint and better TTM
- For more details, check out this Power webinar series

Power Design Webinar Series

Topic	Dates	Speaker	Key Element	
Designing your System Power Solution using LTpowerCAD	Thursday, May 28, 2020	Mike Baker | Analog Devices Staff Applications Engineer	Power Supply Designs	REGISTER NOW
Simulating Power Solution Designs using LTspice	Tuesday, June 2, 2020	Mike Lowrie | Field Applications Engineer, Arrow Electronics Paul Perrault | Senior Field Applications Engineer, Analog Devices	Power & Analog Signal Chain Simulations	REGISTER NOW
Designing Power Solutions for RF Signal Chain Applications	Wednesday, June 10, 2020	Piyu Dhaker | Applications Engineer, Analog Devices	RF Power	REGISTER NOW
Designing Power Solutions for Battery Powered/Portable Applications	Friday, June 12, 2020	Tim Watkins | Applications Engineer, Analog Devices	Battery Portable Power	REGISTER NOW
Designing Power Solutions for Precision Signal Chain Applications	Wednesday, June 17, 2020	Piyu Dhaker | Applications Engineer, Analog Devices	Precision Signal Chain	REGISTER NOW
Designing Power Solutions for High Speed Converter Applications	Tuesday, June 23, 2020	Charly El-Khoury | Staff Applications Engineer, Analog Devices	HSC Power with µModule Regulators	REGISTER NOW
Designing Power Solutions for FPGA Applications	Thursday, June 25, 2020	Charly El-Khoury | Staff Applications Engineer, Analog Devices	FPGA Power	REGISTER NOW

https://www.arrow.com/en/research-and-events/events/analog-devices-arrow-2020-power-series-webinars

Conclusion:

- Having the right Analog Front End is crucial when designing a HS Converter application
  - Amplifiers are good for DC coupling, Gain and Bandpass Flatness
  - Transformers are better for Higher Frequencies, Lower Noise & Lower Power.
- Understand your requirements and how they translate to Converter specs is key
- Layout and decoupling are also very important.
  - If not implemented correctly HS Converter will not meet datasheet specs.
- For higher resolutions converters, Clock reference can make or break performance
  - Jitter destroys SNR
- For technical support, please reach out to ADI Central Apps team or Arrow support team

Thank you for attending this webinar, for more info please visit us at www.analog.com
Questions?

Charly El-Khoury
Staff Application Engineer
NA Central Application

AHEAD OF WHAT'S POSSIBLE™

Roadmap & Portfolio Review

HSX Selection Guide: ADC

Part Number	Sample Rate (Max) (GSPS)	Resolution (Bits)	Interface	No. Input Channels	Analog Input BW (GHz)	NSD (typ) (dBFS)	SFDR (typ) (dBFS)	SNR (typ) (dBFS)	Power Per Channel (typ) (W)
AD9083	2.0	12	JESD204B	16	0.125	-147	78	57.0	0.0625
AD9213*	10.25, 6.0	12	JESD204B	1	6.5	-154	70	57.0	5.1
AD9217* (Low Latency)	10.25,6.0	12	HS Parallel	1	6.5	-154	70	57.0	5.1
AD9207	6.0	12	JESD204B/C	2	7.0	-153	75	58.2	2.0
AD9209	4.0	12	JESD204B/C	4	7.0	-150	75	57.0	1.0
16nm Process	20.0	12	JESD204B/C	8	18.0	TBD	TBD	TBD	TBD

* AD9083, AD9217 samples and evaluation boards available – full production release February 2020 (AD9217) and July 2020 (AD9083)

Availability

Released **Development** **Concept**

Indicates platform with same ADC core

HSX Selection Guide: ADC

Part Number	Sample Rate (Max) (GSPS)	Resolution (Bits)	Interface	No. Input Channels	Analog Input BW (GHz)	NSD (typ) (dBFS)	SFDR (typ) (dBFS)	SNR (typ) (dBFS)	Power Per Channel (typ) (W)
AD9208	3.0	14	JESD204B	2	9.0	-152	78	59.5	1.65
AD9689	2.6, 2.0	14	JESD204B	2	9.0	-155.3	73	62.7	1.55
AD9697	1.3	14	JESD204B	1	2.0	-155.6	78	65.6	1.0
AD9695	1.3, 0.625	14	JESD204B	2	2.0	-155.6	78	65.6	1.6
AD9694	0.5	14	JESD204B	4	1.4	-151.5	82	66.8	0.83
AD9625	2.6, 2.5, 2.0	12	JESD204B	1	3.2	-150	79	57	4.0
AD9680	1.25, 1.0, 0.82, 0.5	14	JESD204B	2	2.0	-154	85	65.3	1.65
AD9234	1.0, 0.5	12	JESD204B	2	2.0	-151	85	65.6	1.5
AD9684	0.5	14	LVDS	2	2.0	-153	85	68.6	1.1
AD6676	Sigma Delta	16	JESD204B	1	0.16	-159	90	65	1.2

Availability

Released

Development

Concept

Indicates platform with same ADC core

HSX Selection Guide: DAC

Part Number	Sample/ Update Rate (Max) (GSPS)	Resolution (Bits)	Notes	DAC Channels	Instantaneous BW (GHz)	NSD (typ) (dBFS)	SFDR (typ) (dBFS)	Power Consumption (typ) (W)
AD9176	12.6	16	BW at 2x Int.	2	3.2	-160	80	1,27
AD9174	12.6	16	DDS Engine	2	3.2	-160	80	1.27
AD9173	12.6	16	Exportable	2	2.25	-160	80	1.275
AD9172	12.6	16	BW at 1x int.	2	3.2	-160	80	1.275
AD9171	6.2	16	Exportable	2	0.40	-160	80	1.275
AD9164	12.8	16	JESD204B	1	2.5	-168	82	1.325
AD9163	12.8	16	Exportable	1	1.0	-168	82	1.325
AD9162	12.8	16	JESD204B	1	2.5	-157	82	1.31
AD9161	12.8	11	JESD204B	1	2.25	-157	82	1.31
AD9166*	12.8	16	JESD204B	1	2.5	-147	82	1.325
16nm Process	28.0	12	JESD204B/C	8	8.0	TBD	TBD	TBD

Availability

Released

Development

Concept

Indicates platform with same DAC core

* AD9166 samples available – full production release March 2020

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