PCB Layer Stack-up

Technical Workshop
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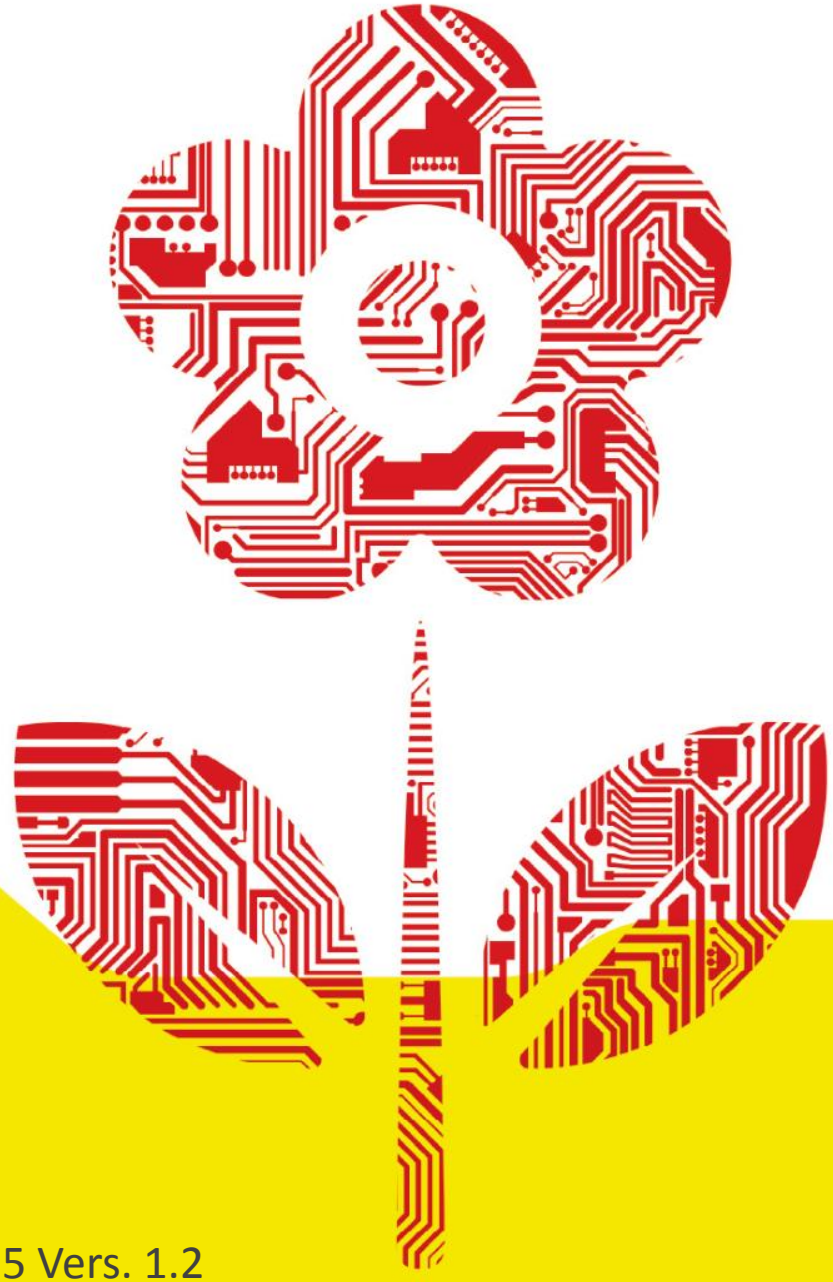

FINELINE
EXCELLENCE IN PCB

Albert Schweitzer
Fine Line Gesellschaft für
Leiterplattentechnik mbH
Itterpark 4, D-40724 Hilden

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Introduction

This presentation has been written mainly for hardware layouter and designer.

The presentation can not replace or substitute studying electrical engineering.

I do not speak today about materials and particularly controlled impedance.

Table of content

Content

1 What is a stack-up design

What is stack-up design?

Stack-up design is the arranging of the signal and power layers of a PCB to meet the electrical and mechanical performance needs of a specific design.

Introduction

The planning of PCB stack-up configuration is one of the most important aspects in achieving the best possible performance of an product.

Introduction

A good stack-up can be very effective in reducing radiation from the loops on the PCB (differential-Mode emission), as well as the cables attached to the board (common-mode emission).

On the other hand, a poor stack-up can increase from both of these mechanisms considerably.

Introduction

PCB stack-up is an important factor:

- in determining the EMC performance of a product,
- to balance Signal Integrity (SI) against manufacturability and reliability of a PCB design
- and it is the basic to avoid emission, and crosstalk and all other kind of disturbances of high-speed applications.

Difference between two-layer and multi-layer PCBs

There is a significant difference between PCBs:

- Single and two- layer PCBs
- Multi-layer PCBs

It is obvious, it make no sense to talk about a layer stack-up in case of single and two layer PCBs.

Difference between two-layer and multi-layer PCBs

It is important to know the technical difference between single and two-layer and multi-layer PCBs.

Two-layer PCBs are useable in a frequency Range until 25MHz.

It makes sense to use multi-layer PCBs are above 10MHz, and it is important to know, they produce 15dB less radiation as two-layer PCBs. The reason for this we will learn later.

Requirements for a high performance PCB

Requirements for a high performance PCB

- Provide enough signal layers to allow successful routing of all signals to signal integrity rules.
- Provide enough power and ground layers to meet needs of the PDS (Power Delivery System).
- Trace widths, spacing and dielectric thickness that meet both impedance and cross talk goals.
- Spacing between power and ground planes that results in adequate plane capacitance while complying with breakdown voltage rules.
- Use of materials that are readily available and comply with assembly requirements.

Deficits with traditional design approach

- Impedance calculation is an electrical engineering issue.
- The strengths of PCB fabricators are:
  – Plating, Lamination, Etching, Drilling etc.
  – In summery: excellence in manufacturing of PCBs,
- <u>but, electrical engineering is not part of that skill set.</u>

Deficits with traditional design approach

- Even so, many fabricators have learned to calculate impedance. (The skill level at each fabricator varies widely.)
- Times have changed and impedance is only one of the electrical requirements that are important in a stack-up.
- Crosstalk and interplane capacitance are two other parameters that have been added to the stack-up requirements.

Four important Factors

Four factors are important with respect to PCB stack-up considerations:

- The count of layers
- The spacing between the layers
- The sequence of the layers
- The number and types of planes used (power and/or ground)

Only “count of layer” is considered as important factor

Usually not much consideration is given except as to the count of layers.

In many cases the other three factors as

- spacing between layers,
- sequence of layers and
- type of planes

are of equal importance. The Issue spacing between layers is sometimes not even known by the PCB designer.

The count of layers

In deciding on the number of layers, the following should be considered:

- The count of signals to be routed and cost
- Frequency, speed of signals
- Class A or Class B emission requirements
- PCB in a shielded or unshielded housing
- EMC engineering expertise of design team

Only “count of signals and cost” is considered as important factor

Often only the first item:

“The count of signals to be routed and the cost”

is considered.

But very important is as well the frequency, the kind of emission requirements, and the kind of housing, used for final application.

15dB less radiation with multi-layers

Multi-layer boards using ground and / or power planes provide significant reduction in radiated emission over two layer PCBs.

A rule of thumb:

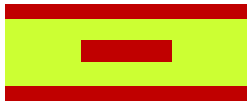
> “A four-layer board will produce 15dB less radiation than a two-layer PCB”.

15dB less radiation with multi-layers

The reason why ML will produce less radiation:

1) ML allow signals to be routed in a microstrip or stripline configuration.

Microstrip Transmission Line

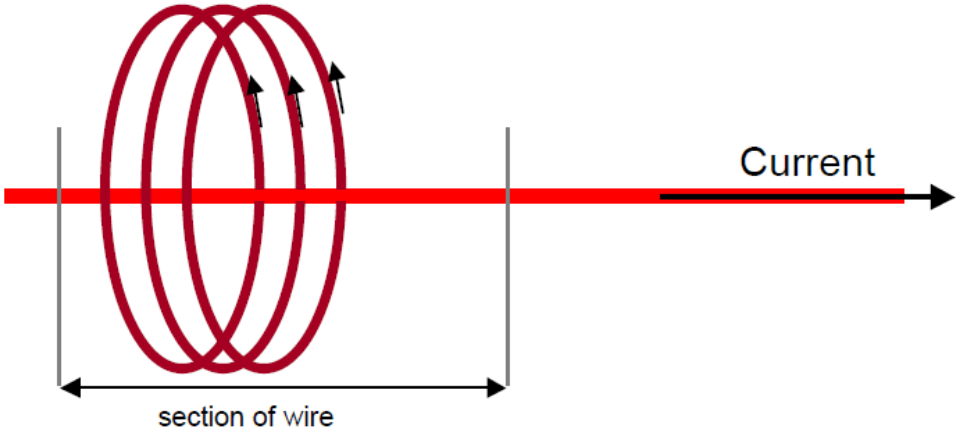


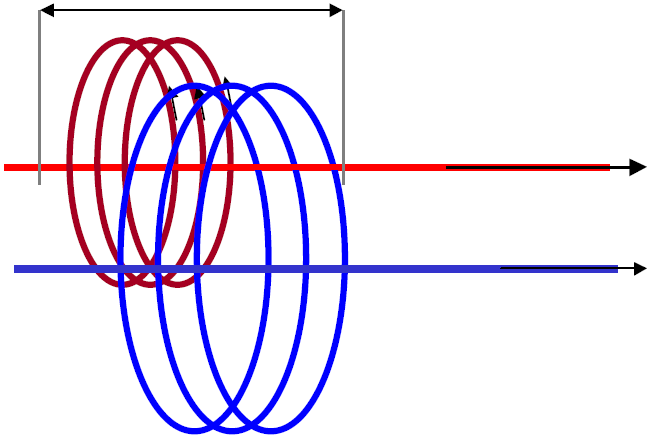
Stripline Transmission Line

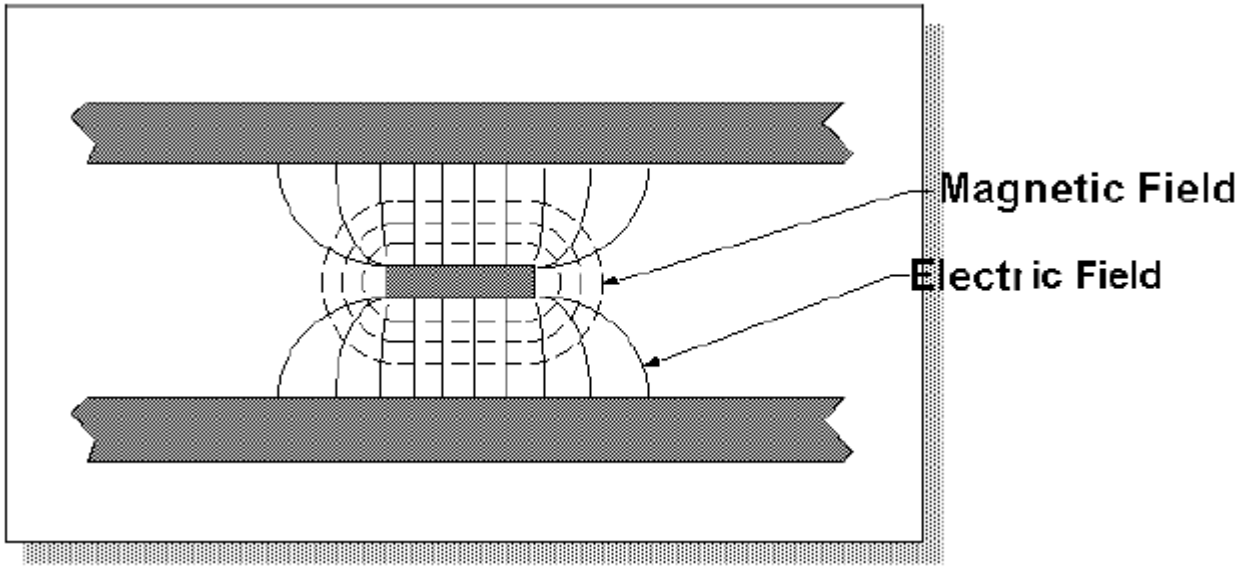
2) The ground plane decreases the ground impedance and therefore the ground noise significantly.

3 Some basics

Magnetic and Electric Fields







Source: Speeding Edge

What is EMC, what is EMI?

EMC = Electro Magnetic Compatibility

The electro magnetic compatibility is the ability of an electrical device to function sufficiently well in its electromagnetic environment without generating unintentional interference to the other equipment in the system.

EMI = Electro Magnetic Interference

Electromagnetic energy emanating from one device which degrades or obstructs the effective performance of another device.

High speed Design

If we talk about “High-speed Design” we have to consider the rise time and fall time of the signal, travelling on the signal path, and NOT the frequency of the signal.

For example, we can have a 0.5ns rise time for a square wave at 10kHz as well as 10MHz. It is the rise and fall time that matter and not the frequency of the signal.

Signal return path

One of the keys in determining the optimum printed circuit board layout is to understand how and where the signal return currents actually flow.

"There is no black hole for signals"

Most designers only think about where the signal current flows (obviously on the signal trace), and ignore the path taken by the return current. Of course, the fact that many designers think this way, helps to keep some EMC engineers employed ☺

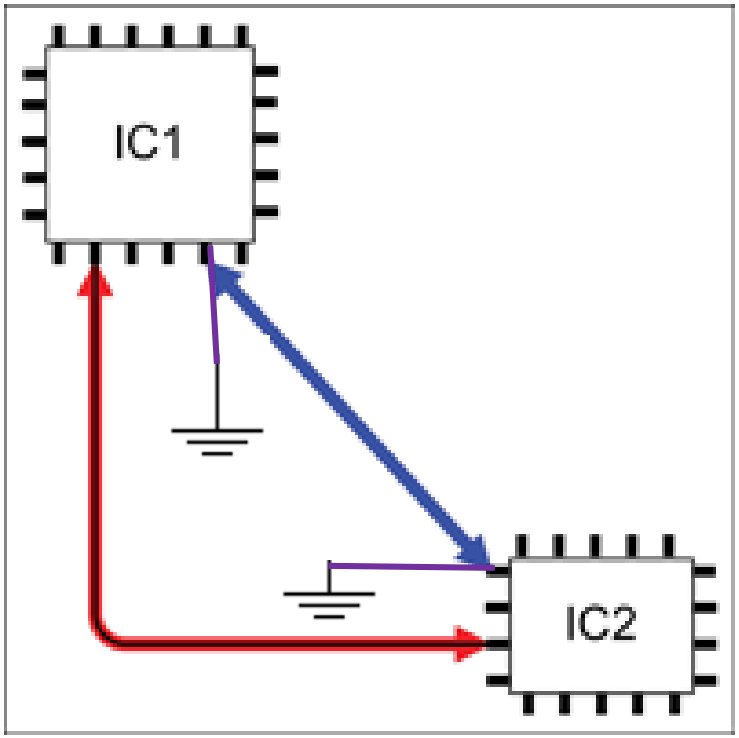
Signal return path

The high speed signal do not use as return path the path of least resistance but use the path of lowest impedance, usually in a plane directly underneath the signal trace.

Signal return path = path of lowest impedance!!

Signal return path

To address the above concern we must understand how high-frequency currents flow in conductors.

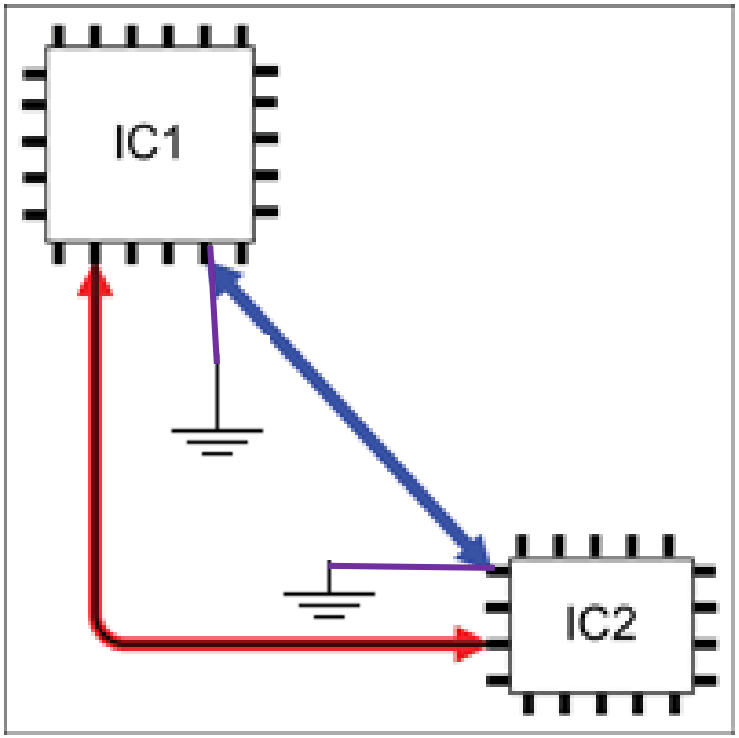


In our example we have a solid ground plane, the **path of least resistance,** and thus the path of DC current and low frequency signals, will be a straight line. (Blue colored)

Source: Maxim

Signal return path

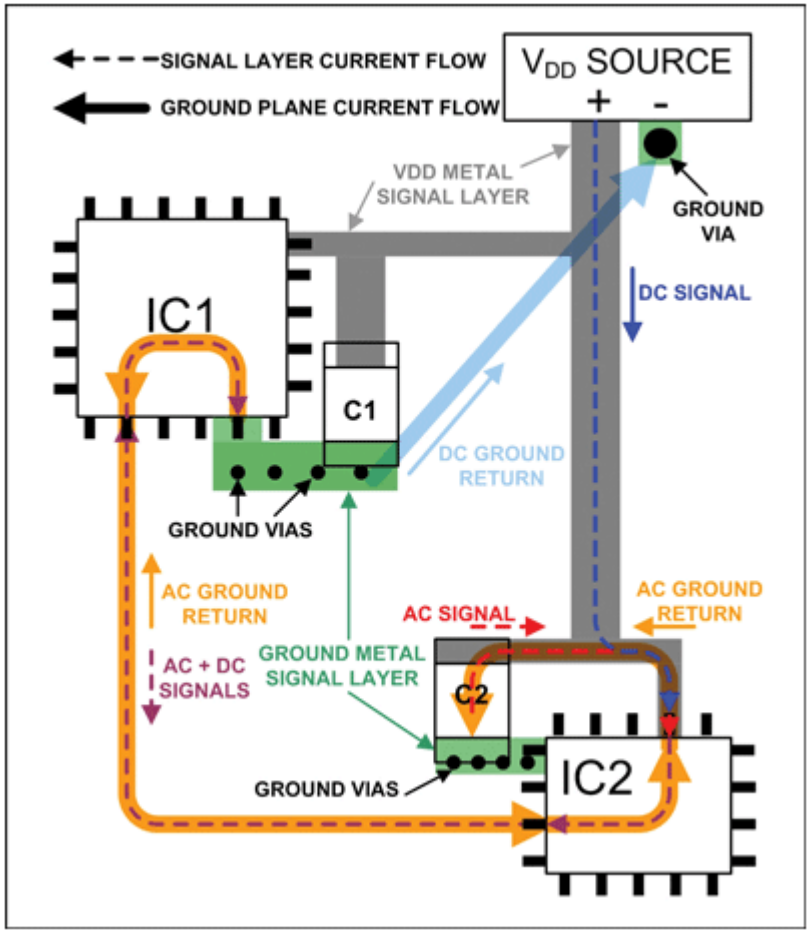
The lowest impedance return path is in a plane directly underneath the signal trace (Red colored)



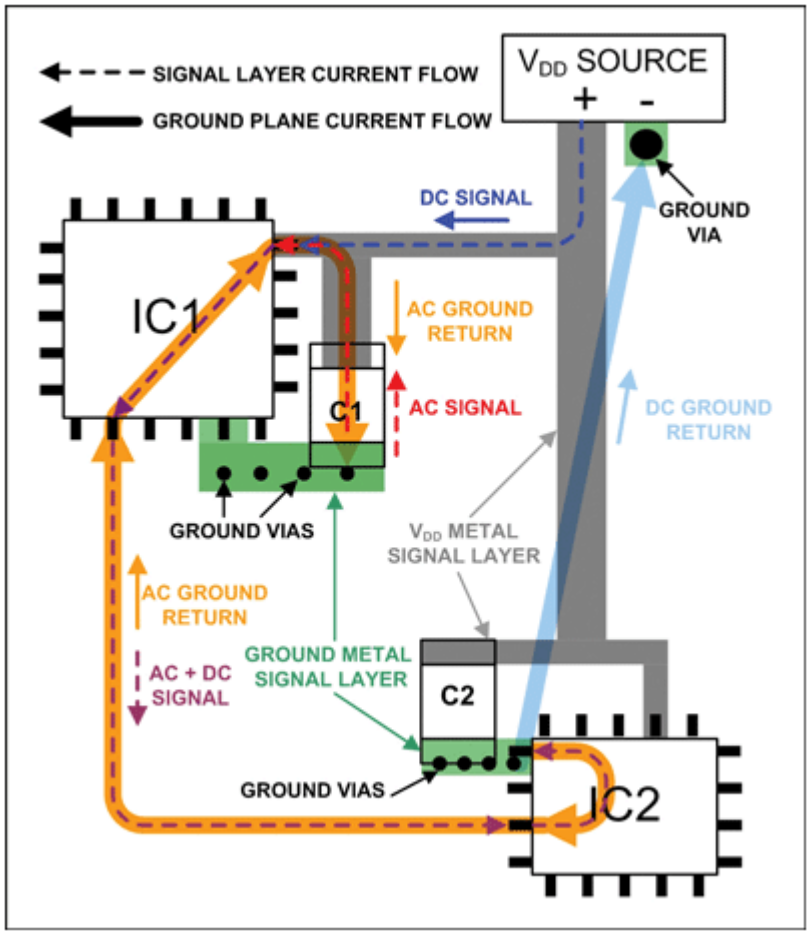
It's irrelevant whether this is a power or ground plane, since this provides the lowest inductance path. This also produces the smallest current loop area possible.

Source: Maxim

Signal return path



Complete current paths, IC1 is sourcing



Complete current paths, IC2 is sourcing

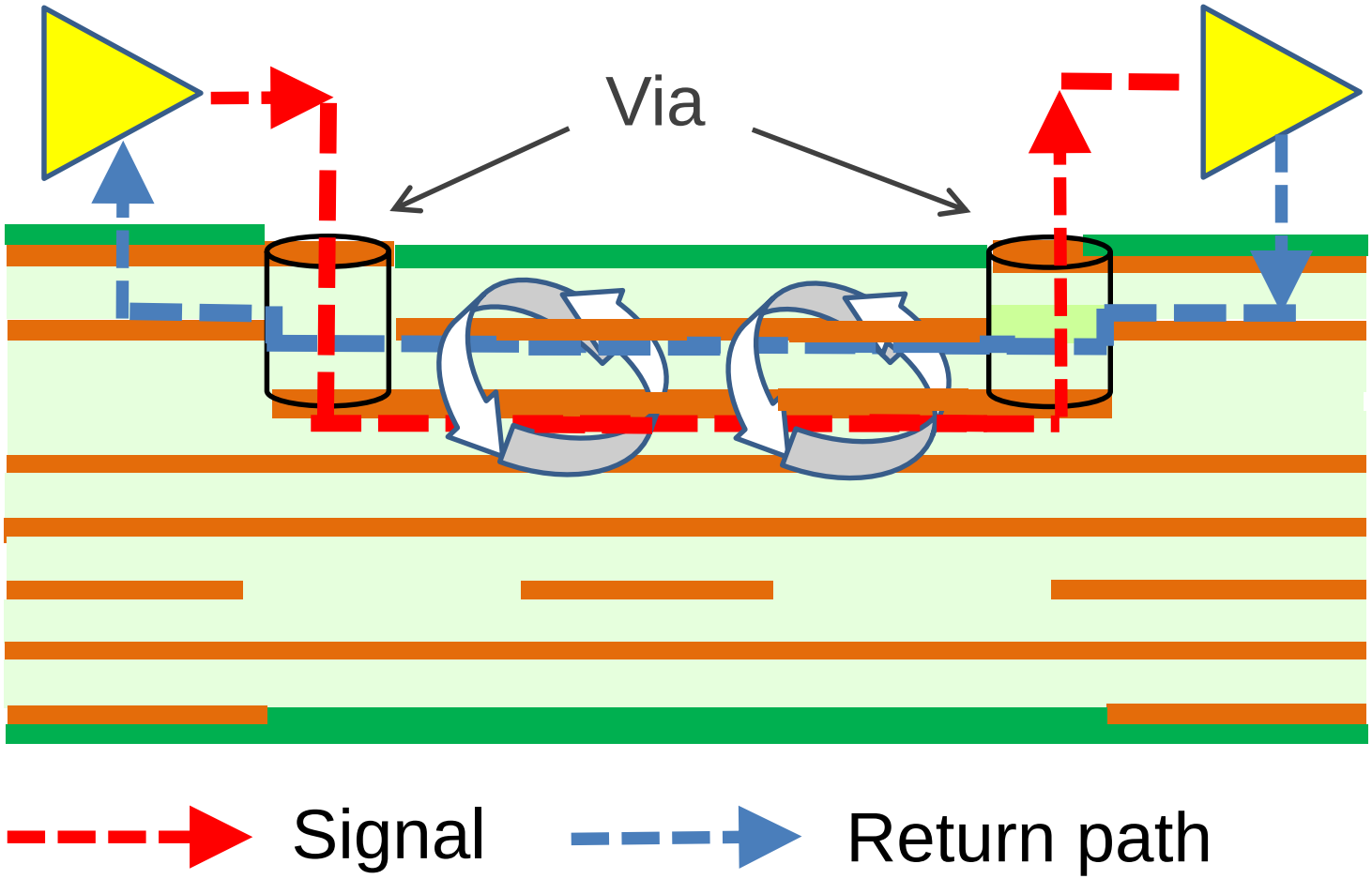
Source: Maxim

Signal return path

A major EMC problem occurs always when there are discontinuities in the current return path. These discontinuities cause the return current to flow in larger loops, which increases the radiation from the board as well as increases the crosstalk between adjacent traces and causes waveform distortion.

In addition in constant impedance PCBs the return path discontinuity will change the characteristic impedance of the trace.

Signal return path



Source: Fineline

What is Impedance?

Impedance is the resistance to the flow of energy in a transmission line.

Relative Permittivity also called Dielectric Constant „ε_r“

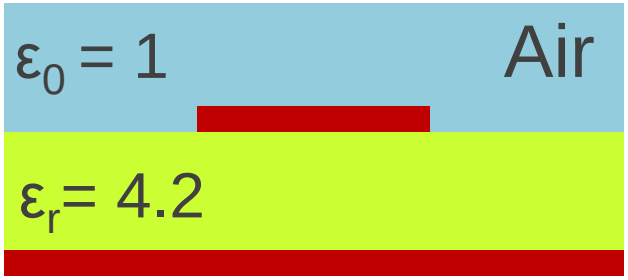
The dielectric constant is the ratio of the permittivity of a substance to the permittivity of free space (air).

$$\varepsilon_r = \frac{\varepsilon}{\varepsilon_0}$$

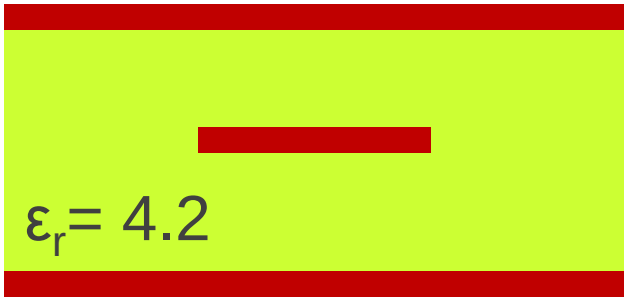
The dielectric constant of PCB material is important in determining the trace width required to produce a characteristic impedance of 50 ohms for example.

Calculation of „ε_{eff}“ for a Microstrip Transmission Line

Microstrip

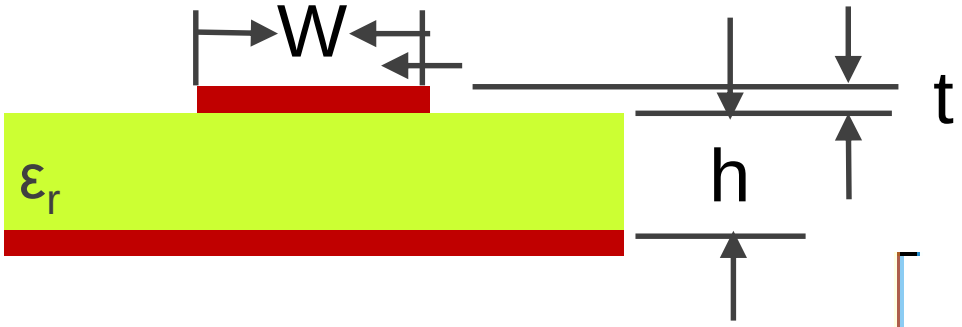


Stripline



It is important to understand that we have to incorporate the dielectric constant of air, in case of Microstrip transmission lines.

Calculation of „ε_{eff}“ for a Microstrip Transmission Line

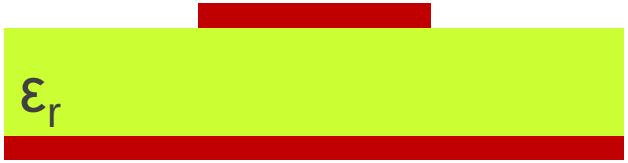


$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + \frac{12h}{w}}} + 0.04\left(1 - \frac{w}{h}\right)^2\right] \quad \underline{\text{if}} \quad \frac{w}{h} < 1$$

$$\underline{\text{otherwise}}$$

$$\varepsilon_{eff} = \left[\frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + \frac{12h}{w}}}\right]\right]$$

One Example to calculate „ε_{eff}“



ε_r of used FR4 material:	4.2
Width of track:	1.5mm
Thickness of dielectric:	793µm
Thickness of copper:	35µm

$$\frac{W}{h} = \frac{1.5}{0.793} = > 1 \quad \left[\frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + \frac{12h}{w}}}\right]\right] \qquad \varepsilon_{eff} = 3.19$$

Download calculation tools for Impedance and dielectric constant

Find good tools to calculate impedance and dielectric constant:

http://www.rogerscorporation.com

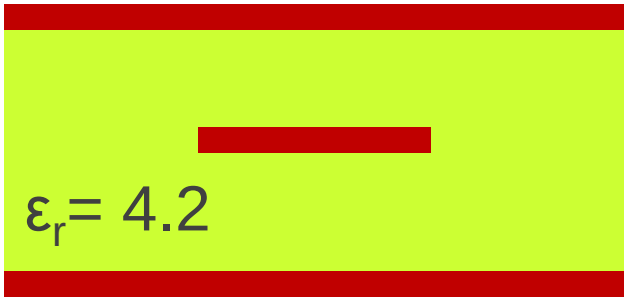
http://www.chemandy.com

Signal Propagation Delay

Microstrip

$$v_{ms} = \frac{c}{\sqrt{\varepsilon_{eff}}}$$

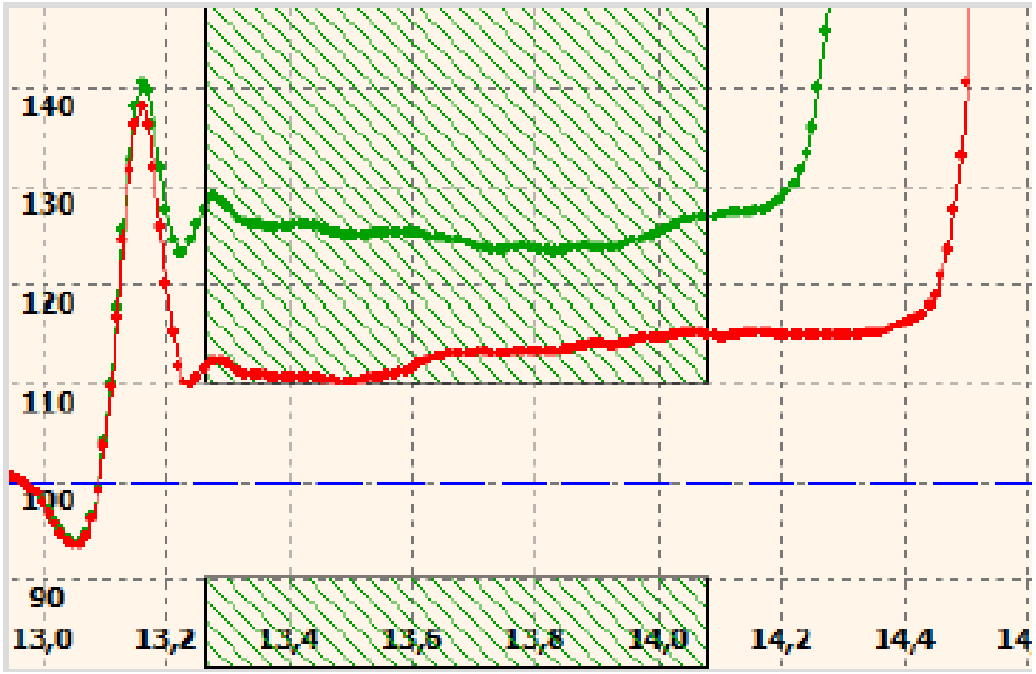
Stripline



$$v_{sl} = \frac{c}{\sqrt{\varepsilon_r}}$$

$$\varepsilon_{eff} < \varepsilon_r \Rightarrow v_{ms} > v_{sl}$$

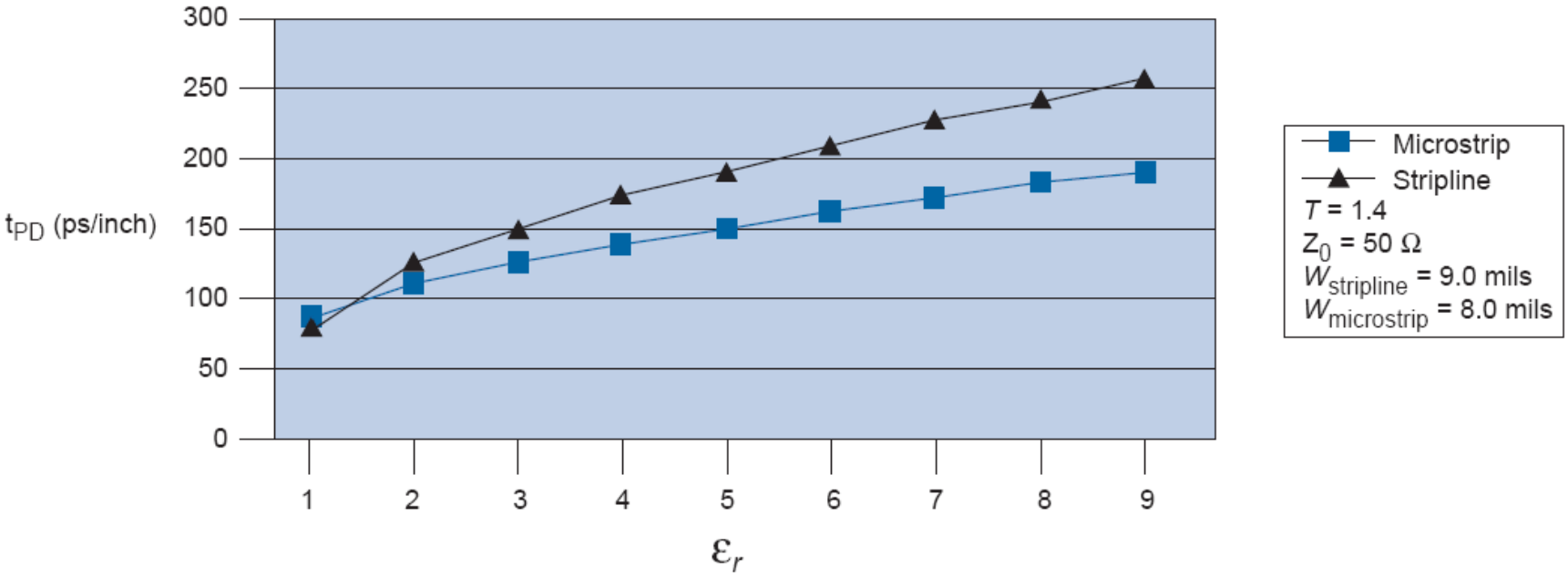
Signal Propagation delay



Picture show a line with length of 100mm
Different signal propagation delay: Outer / Inner layer
Different impedance: 125 / 112 Ohm

Source: Sequid

Signal Propagation delay



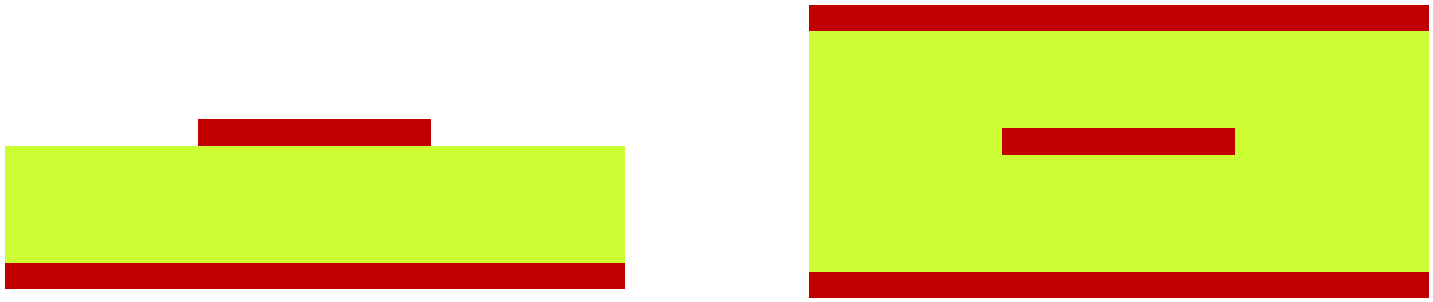
The above figure shows the propagation delay vs. the dielectric constant for Microstrip and Stripline traces. As ε_r increases, the propagation delay (t_{PD}) also increases.

Source: Altium

Important to know about "ε_r" dielectric constant

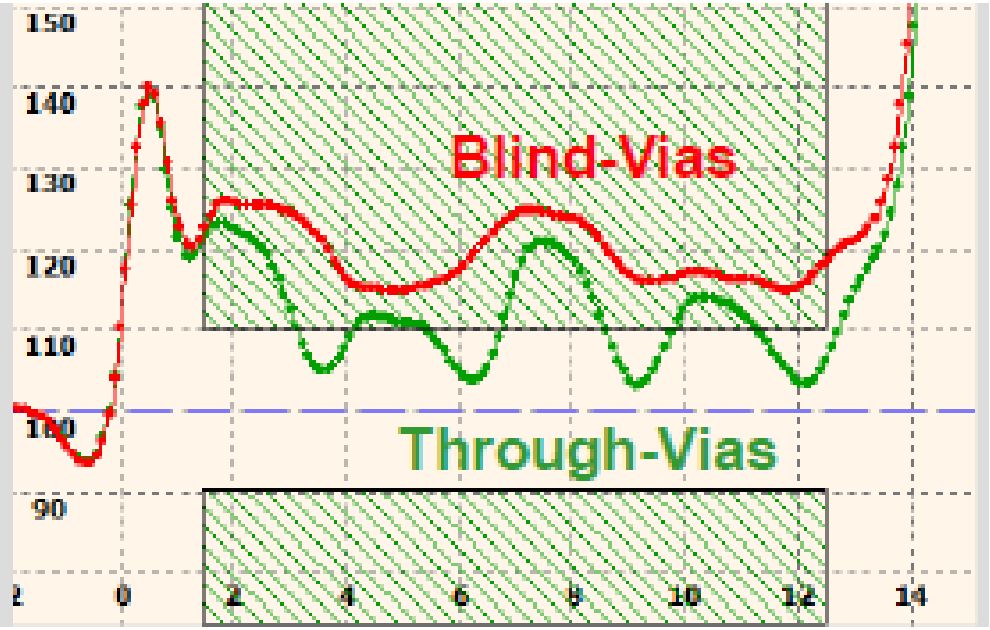
- Lower ε_r materials, net higher impedance traces and faster propagation times per given trace width & trace-to-ground separation.
- As trace width increases, trace impedance decreases (Thickness has min effect).

Differences between Microstrip and Stripline transmission lines



- Microstrip has faster propagation time.
- Stripline has better immunity to crosstalk.
- Stripline has better EMI characteristics.

Difference between Through hole Via and Microvia



With Microvias the impedance characteristics is more steady and smooth.

Source: Sequid

Skin effect

Also important, due to the "skin effect," high frequency currents cannot penetrate a conductor, and therefore, **at high-frequency all currents in conductors are surface currents**.

This affect will occur at all frequencies above 30 MHz for 1 oz. copper layers in a PCB. Therefore, a plane in a PCB is really two conductors not one conductor. There will be a current on the top surface of the plane, and there can be a different current or no current at all on the bottom surface of the plane.

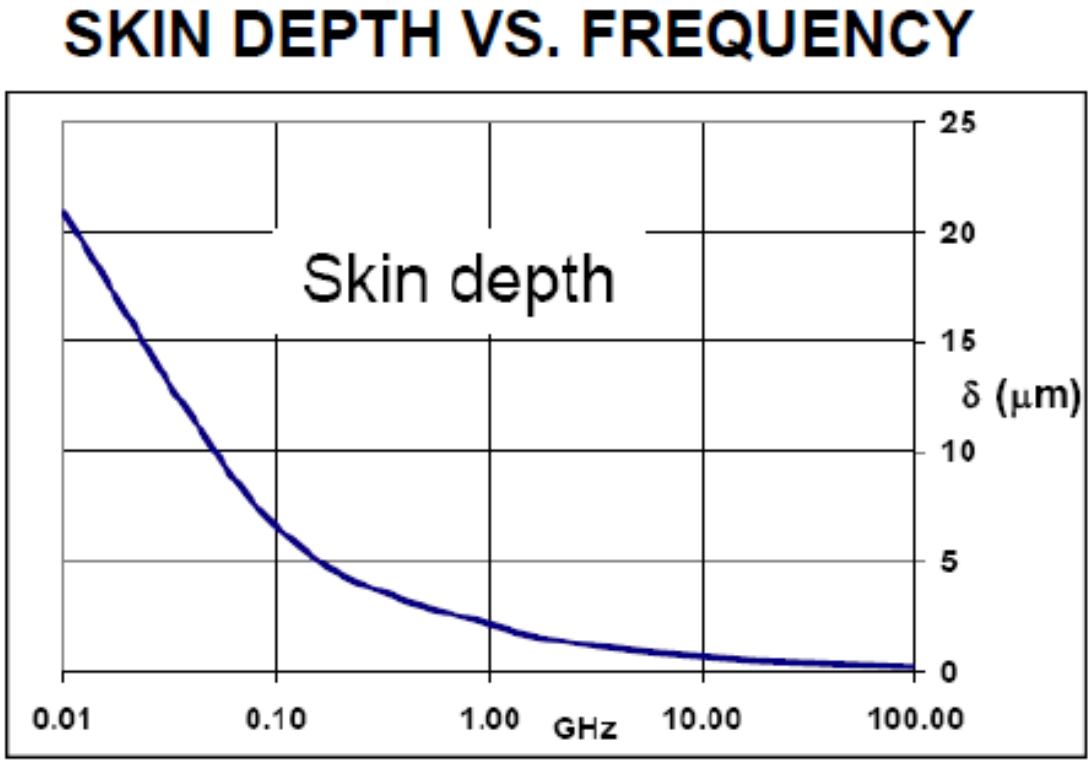
Signal layer thickness and skin effect

- Nearly all signal layers in modern designs have signals fast enough that skin effect loss and skin depth determine how thick the signal traces need to be.
- “Skin effect” is the behavior of current flow in conductors at high frequencies where the current flows near the surface of a conductor rather than all the way through it.

Signal layer thickness and skin effect

- When frequencies are high enough that the current is penetrating less than half the thickness of the conductor, making that conductor any thicker is of no value.
- For etching uniformity it is useful to make signal layers as thin as possible. (1/2 ounce being a good compromise).

Signal layer thickness and skin effect



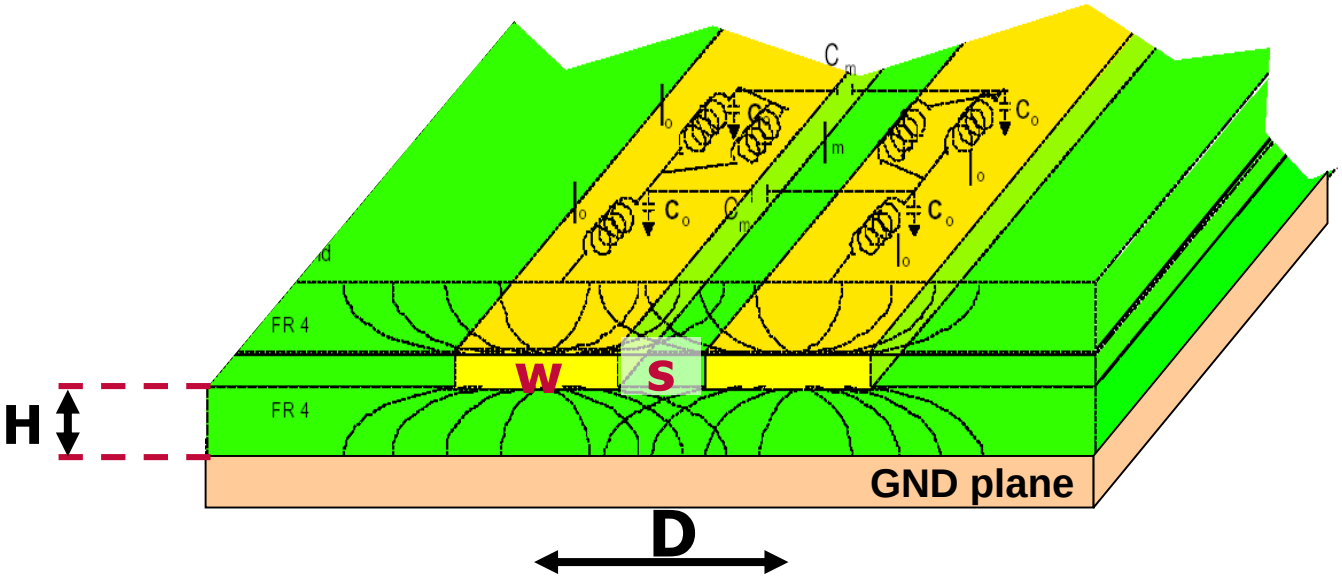
Notice that at 1 GHz, Skin depth is 2µm or 80 micro inches. Trace layers thicker than 17µm (½ oz.) copper do not help above this frequency.

17µm (½ oz.) thick signal layers are ”good enough” for high speed signals.

Source: Barry Olney

Crosstalk

Crosstalk Faktor: $k < 1 / [1 + (D/H)^2]$ (Howard Johnson)

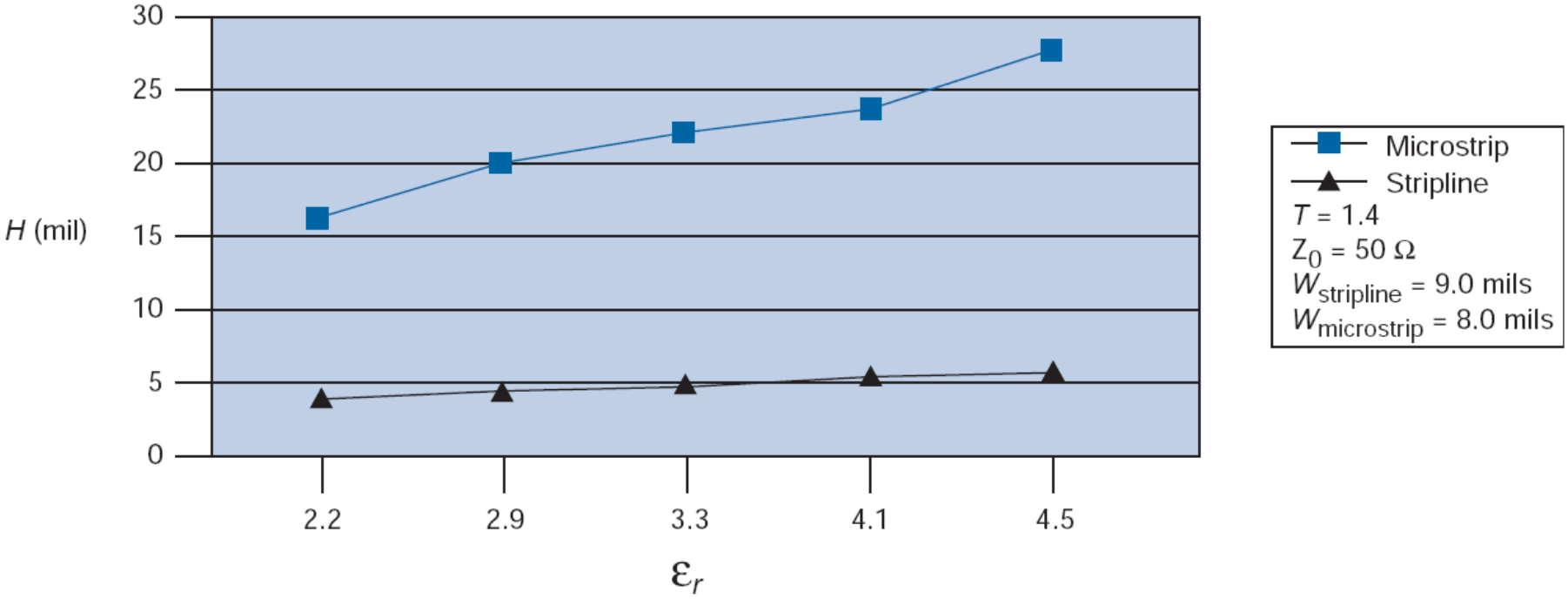


LP Layout: $D = w + s$

Für	$s = w$	$H = 2w$:	$k < 0.5$
Für	$s = 1{,}5w$	$H = 1{,}5w$:	$k < 0.26$
Für	$s = w$	$H = w$:	$k < 0.2$
Für	$s = 2w$	$H = w$:	$k < 0.1$

Source: Howard Johnson

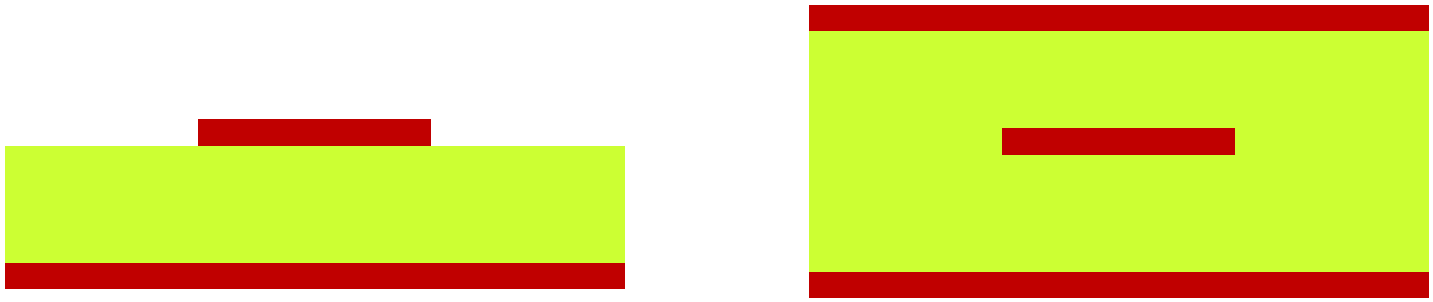
Crosstalk



The above figure shows Height (H) vs. dielectric constant (ε_r) and the difference between Microstrip and Stripline traces.

Source: Altium

Differences between Microstrip and Stripline transmission lines



- Microstrip has faster propagation time.
- Stripline has better immunity to crosstalk.
- Stripline has better EMI characteristics.

Five objectives creating a multi layer PCB

Five objectives creating multi-layer PCB

The following five objectives the designer should try to achieve:

1. A signal layer adjacent to a plane
2. Signal layers coupled to adjacent planes
3. Power and ground planes coupled together
4. High-speed signals routed on buried layers located between planes
5. Multiple ground planes

Five objectives creating a multi-layer PCB

The higher the frequencies occurring, the more important are the 5 objectives.

The most important objectives are Number 1 and Number 2.

1. A signal layer should always adjacent to a reference plane
2. Signal layers should be tightly coupled (close) to their adjacent planes

Objective number “1”

“1“ A signal layer should always be adjacent to a plane. This limits the count of signal layers embedded between planes and top and bottom layers.

Stop thinking about only ground planes, and think more about reference planes. A signal running over a reference plane, whose voltage happens to be at VCC will still return over that reference plane.

Objective number “2”

“2“ Signal layers should be tightly coupled (close) to their adjacent planes, while complying with breakdown voltage rules.

When pairing plane layers with signal layers across a piece of laminate, it is wise to use the same copper thickness on both sides to insure etching is uniform on both sides.

Objective number “3”

“3“ Power and Ground planes should be closely coupled together.

The ground planes can act as shields for the inner signal layers. You should try to make a cage like this. You'll get better results keeping your trace to plane height as low as possible.

Objective number "3"

The power to ground plane capacitance provides a ideal capacitor which helps reduce noise of extremely high frequencies.

Approximate calculation the interplane capacitance:

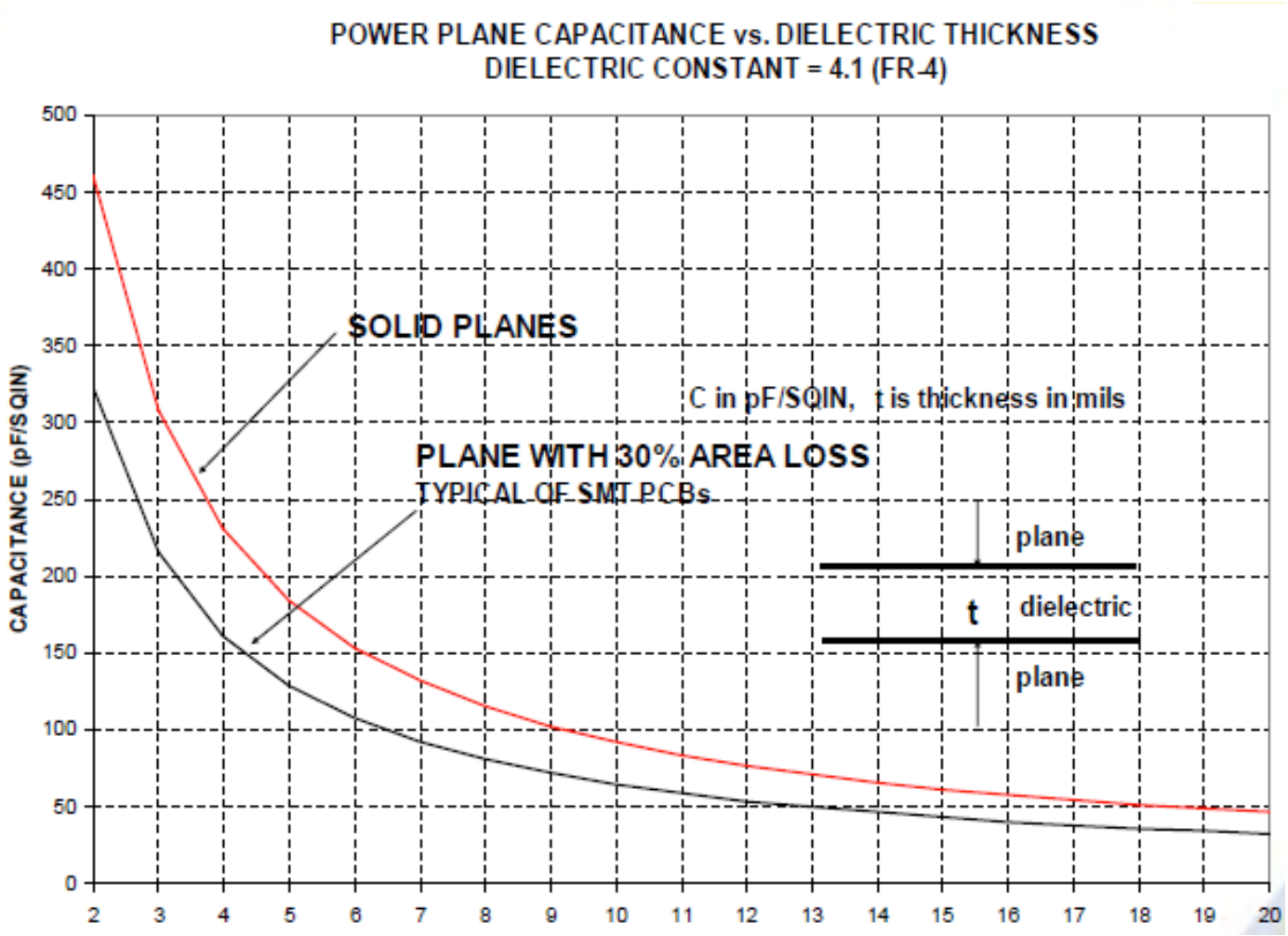
$$C_{\text{interplane}} = \frac{0.225 * A * \varepsilon_r}{d}$$

A = Area of PCB

ε_r = Dielectric Constant

d = Distance between planes

Objective number "3"



Dielectric Thickness [mils]

Source: Lee Ritchey

Objective number “3”

This high quality (low inductance) capacitance, as higher as better, is necessary to support the very fast switching transients associated with driving single ended transmission lines and the rapidly changing IC core supply currents.

The amount of plane capacitance needed is calculated as part of the PDS (Power delivery design) design.

Objective number “4”

“4“ High-speed signals should be routed on buried layers located between planes. In this way the planes can act as shields and contain the radiation from the high-speed traces.

Determine the return path of the signals (which plane will be used). Fast rise time signals take the past of least inductance which is normally the closest plane.

Objective number “5”

“5“ Multiple ground planes are very advantageous, since they will lower the reference planes impedance of the board and reduce the common-mode radiation.

Do not split the ground plane into separate planes for analog, digital, power pins. A single and contiguous ground plane is recommended.

Min. eight-layers to achieve all five objectives

An eight-layer board is the fewest number of layers that can be used to achieve all five of the above described objectives.

On four and six layers board some of the above objectives will have to be compromised. Under those conditions you will have to determine which objectives are the most important to the design at hand.

A good design with four and six layer PCBs is possible as well

The above paragraph should not be construed to mean that you can't do a good EMC design on a four- or six-layer, because you can.

It only indicates that all the objectives cannot be met simultaneously and some compromise will be necessary.

A good design with four and six layer PCBs is possible as well

Just follow the “Law of physics”.

When Laws of Physics can’t be followed, know what compromises are available.

THIS IS NOT BLACK MAGIC!!!

Steps in building a stack-up

- Determine how many signal layers are needed.
- Determine how many power planes are needed to distribute power and ground.
- Arrange signals and planes to accomplish
  - Partners for signal layers
  - Parallel plate capacitance between power and ground
- Set signal height above planes to meet cross talk requirements.

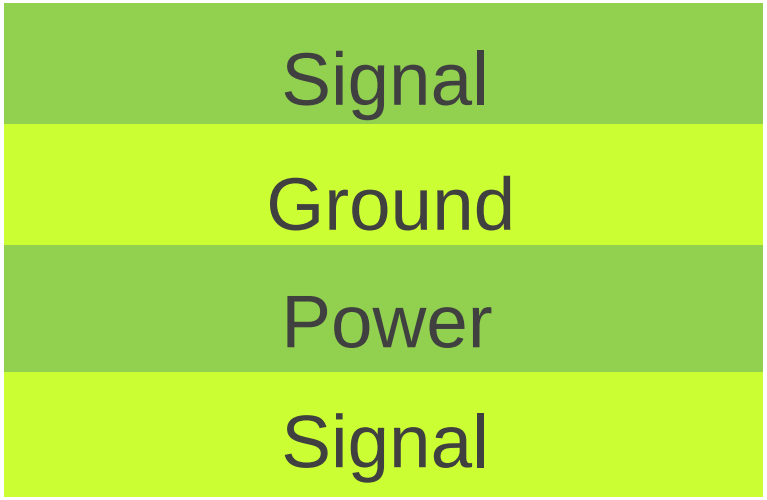
Steps in building a stack-up

- Set trace widths to meet impedance requirements.
- Set spacing between planes to meet capacitance requirements.
- Set spacing between signal layers to meet overall thickness.

5 Four layer stack-up

Four layer stack-up

The most common four-layer board configuration is shown following:



Power and ground planes may be reversed

With respect to the list of 5 objectives this stack-up only satisfies objective “1”.

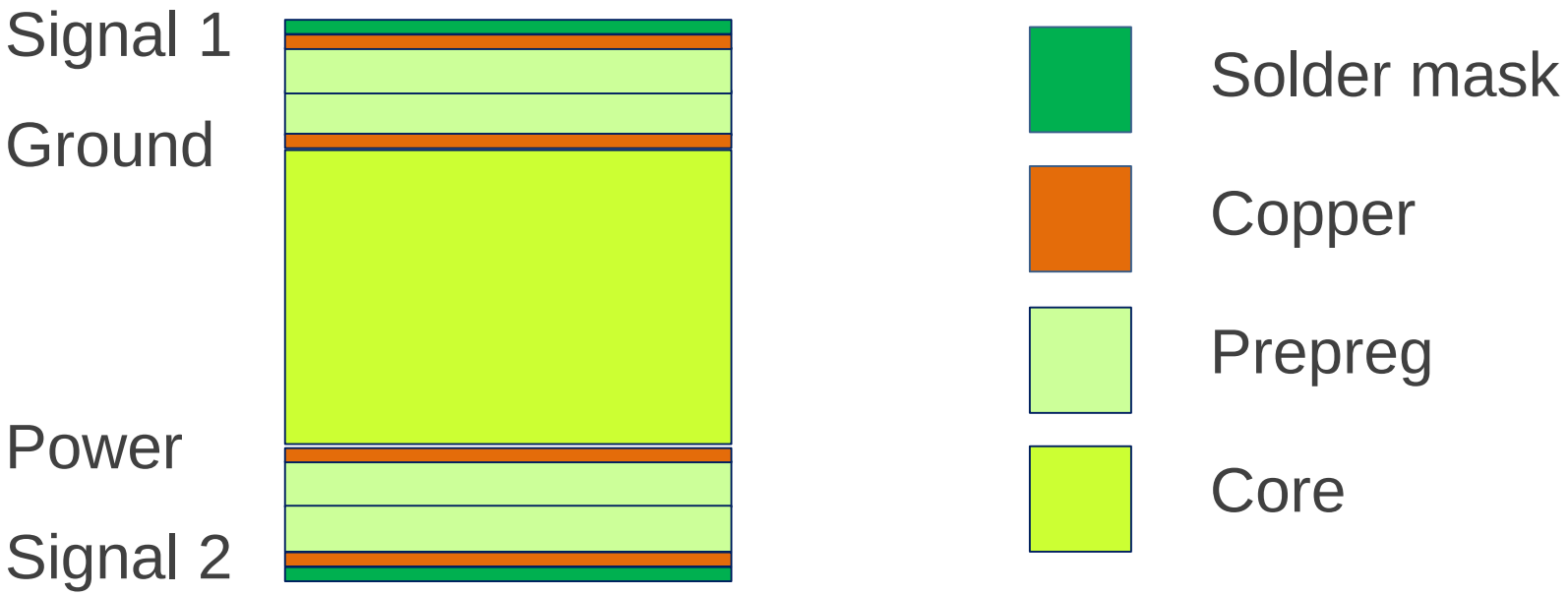
Four layer stack-up

As we can see, if the layers are equally spaced, there is a large separation between the signal layer and the current return plane.

There is as well a large separation between the power and ground planes

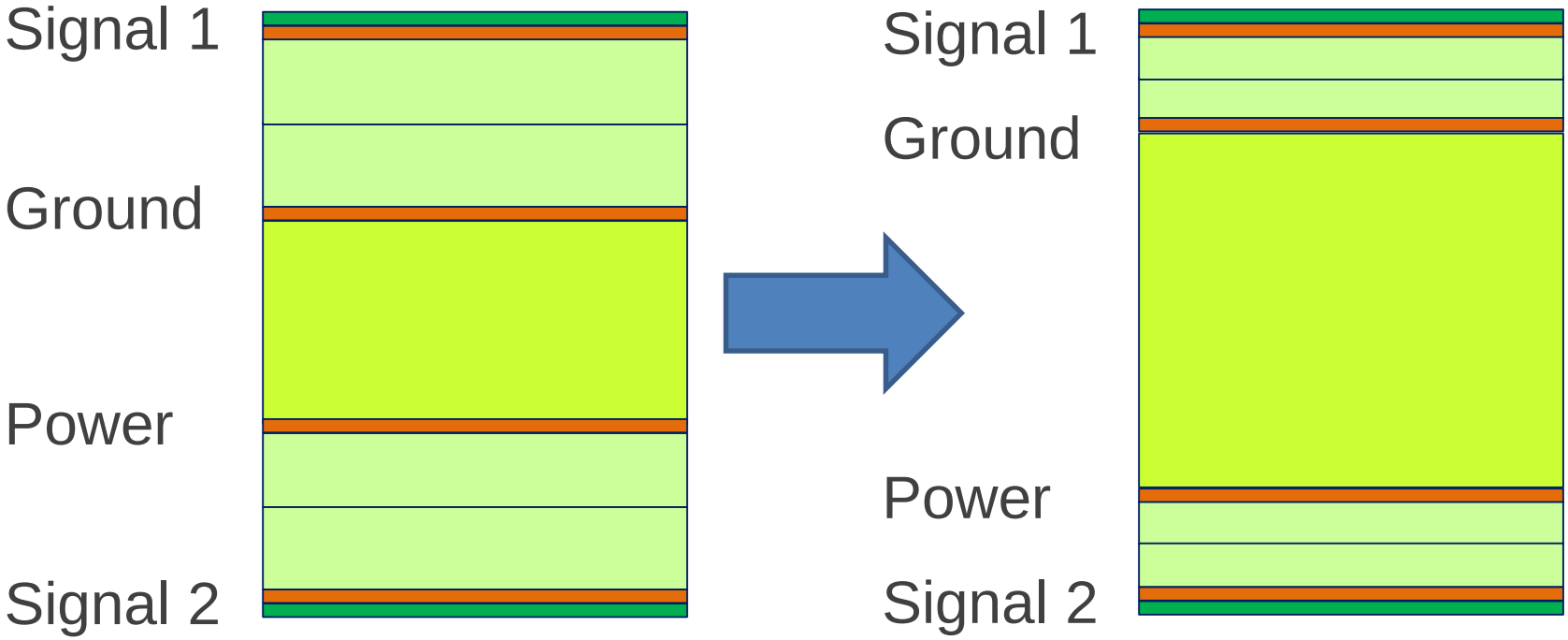
Four layer stack-up

To realize as well objective “2 “ we must space the signal layer as close to the planes as possible.



Source: Fineline

Four layer stack-up



Solder mask Copper Prepreg Core

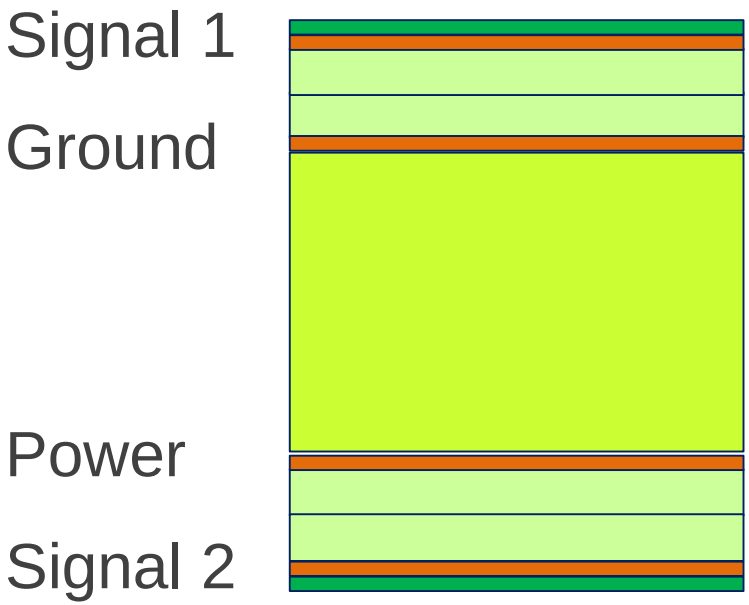
Source: Fineline

Four layer stack-up

Now in this case, it was not possible to tightly couple the ground and power plane (Obj. “ 3“) because the center core had to be used to beef-up the total board thickness. However, to improve the EMC performance of a four layer board, it is best to space the signal layers as close as possible to the planes (Obj. “ 1“ + “ 2“), and use a large core between the power and ground plane keeping the overall thickness of the substrate about 1.6mm.

Four layer stack-up

Anyway the following four layer stack-up is the Most cost-effective and most overlooked way to improve the performance of a four layer PCB.



Source: Fineline

Four layer stack-up

There are three advantages to this configuration:

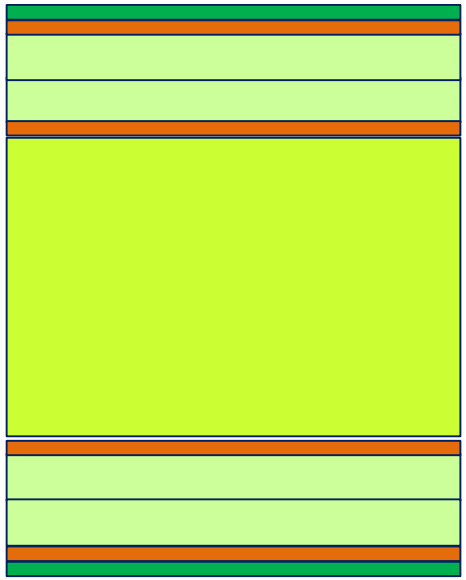
- Tight coupling between the signal and reference plane amount about ~10dB reduction in the trace loop radiation.
- There is also a reduction of plane impedance, hence reduce the common mode radiation from cables connected to the board.
- And, tight coupling will also decrease the crosstalk between traces.

Four layer stack-up

There is a other layer stack-up, often used by experienced designer:

Signal / Power

Ground



Ground

Signal / Power

In this case the power plane is replaced by a second ground plane and the power is routed as a trace on the signal layers.

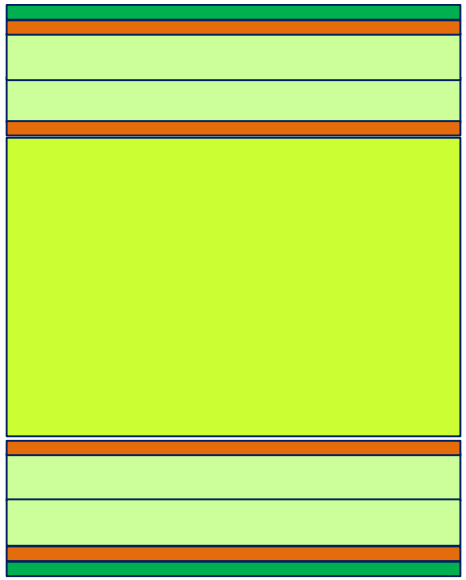
Source: Fineline

Four layer stack-up

The biggest disadvantage of his variant, the planes do not provide any shielding.

Signal / Power

Ground



Ground

Signal / Power

This configuration satisfies objectives "1", "2", and "5"

but not objectives "3" or "4".

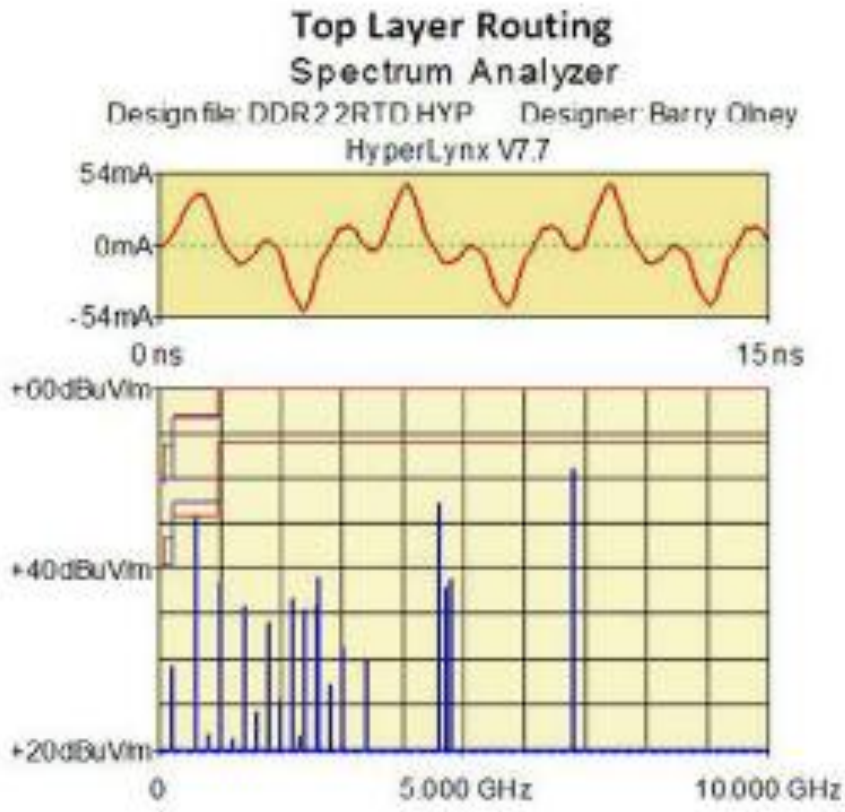
Source: Fineline

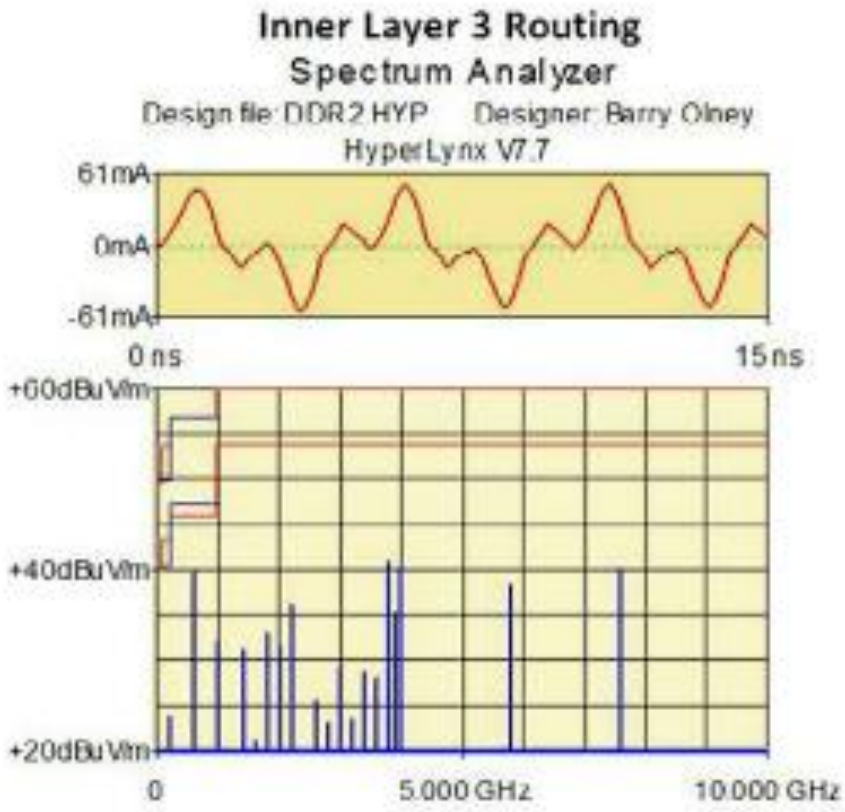
Six layer stack-up

Six layer stack-up

To use two more signal layers, has a huge advantage compare with a four layer PCB. Embedded high-speed signals between planes can reduce electromagnetic radiation by up to 10dB. Embedding signals between the planes also reduce susceptibility to radiation, as well as providing ESD protection. So, not only do we prevent noise from being radiated, but we also reduce the possibility of being affected by an external source.

Six layer stack-up





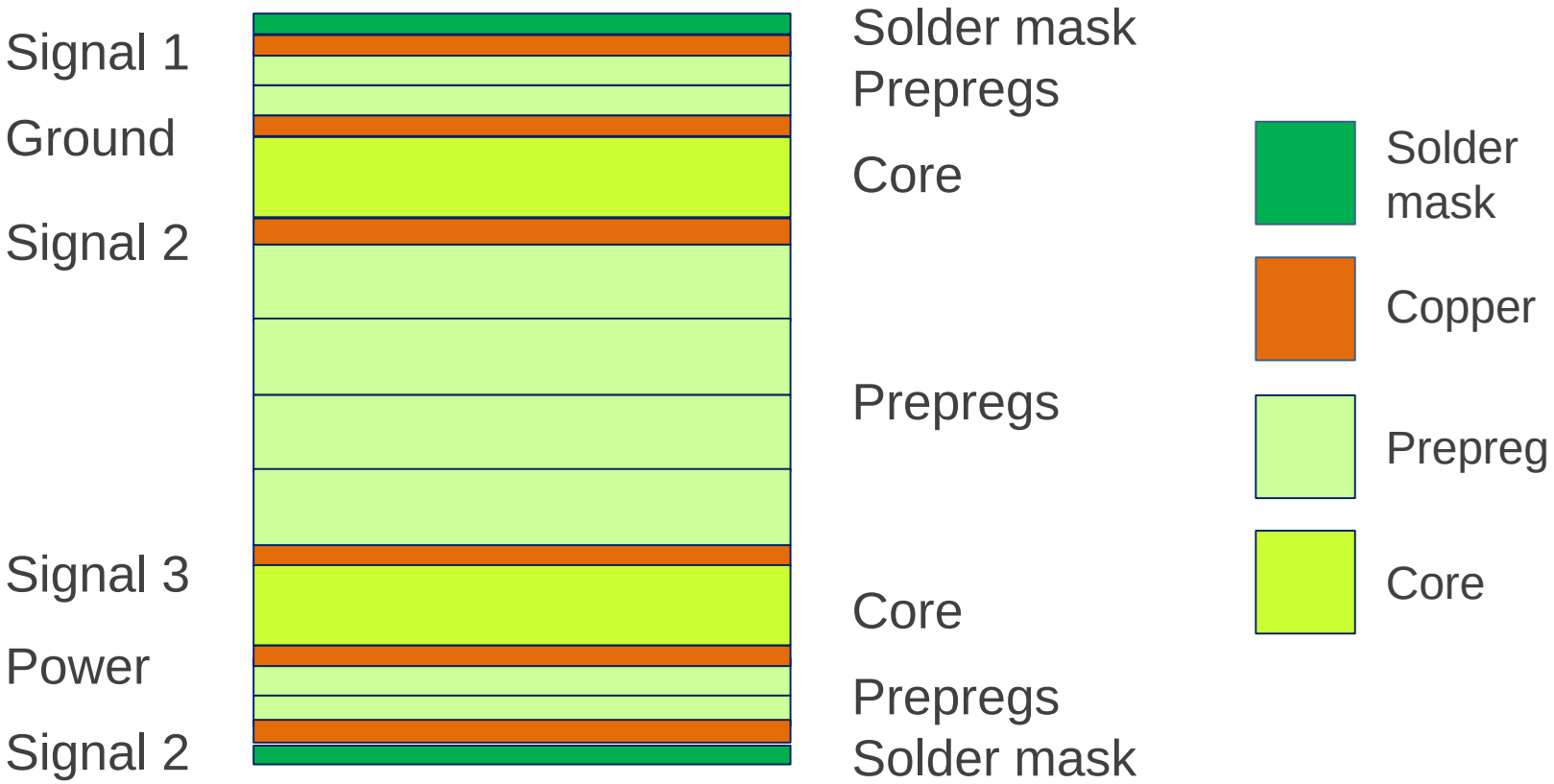
Comparison of radiation emissions from outer and inner layer routing

You can see a notable 10dB reduction of emissions.

Source: Barry Olney

Six layer stack-up

A very good designed six layer PCB:

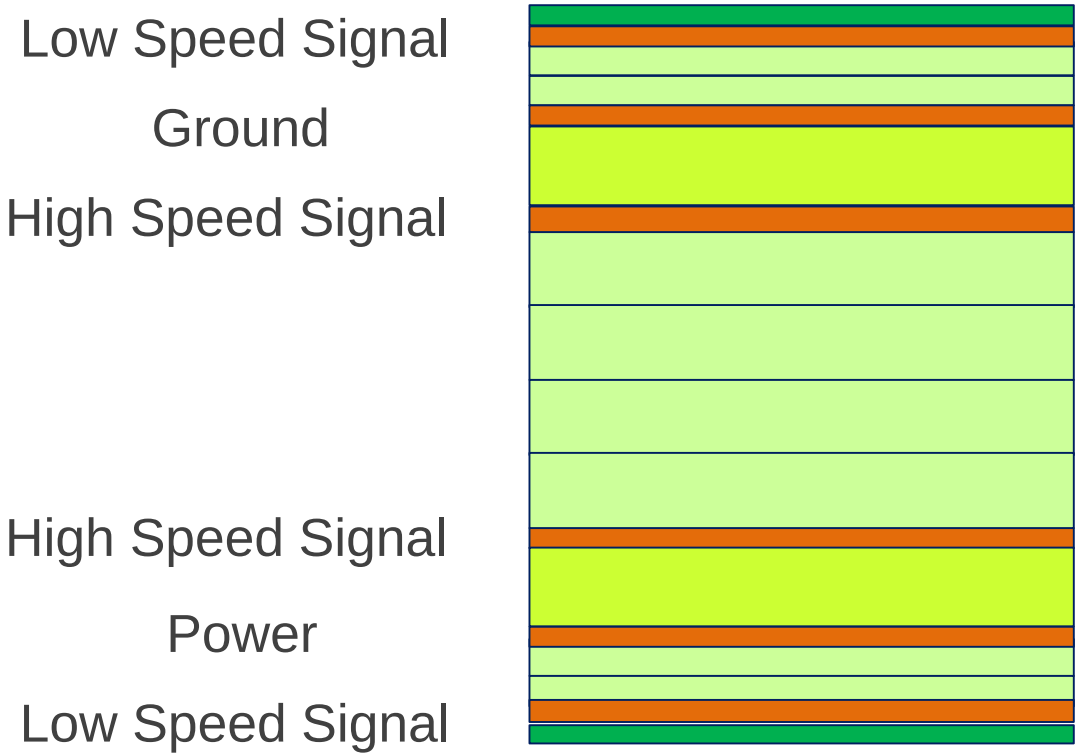


FINELINE
EXCELLENCE IN PCB

Source: Fineline

Six layer stack-up

This is probably the most common six-layer Stack-up and can be very effective in controlling emissions, if done correctly:



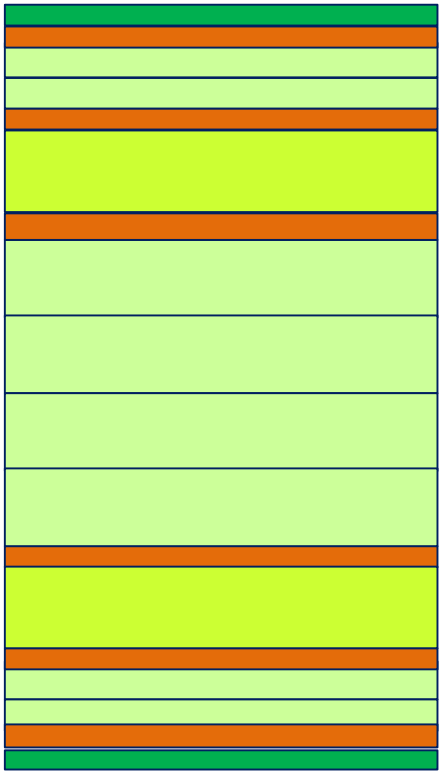
Source: Fineline

Six layer stack-up

Low Speed Signal

Ground

High Speed Signal



High Speed Signal

Power

Low Speed Signal

This configuration satisfies objectives “ 1 “, “ 2 “ and “ 4 “, but not objectives “ ~~3~~ “ and “ ~~5~~ “.

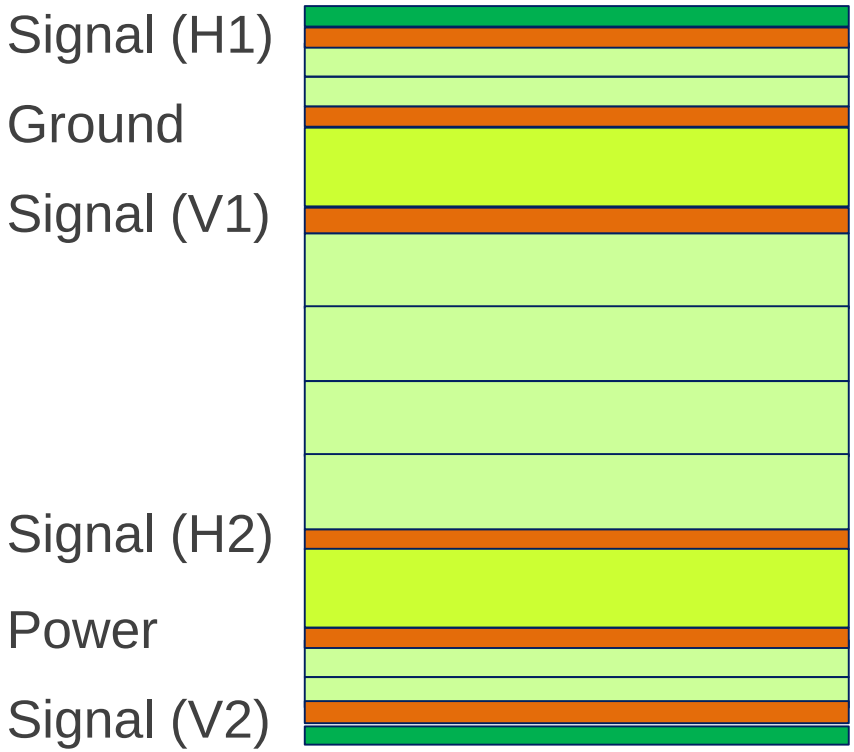
Its main drawback is the separation of the power and ground planes. Due to this separation there is no significant interplane capacitance between power and ground

FINELINE
EXCELLENCE IN PCB

Source: Fineline

Six layer stack-up

Not nearly as common, but a good performing stack-up for a six-layer board, is the following one:

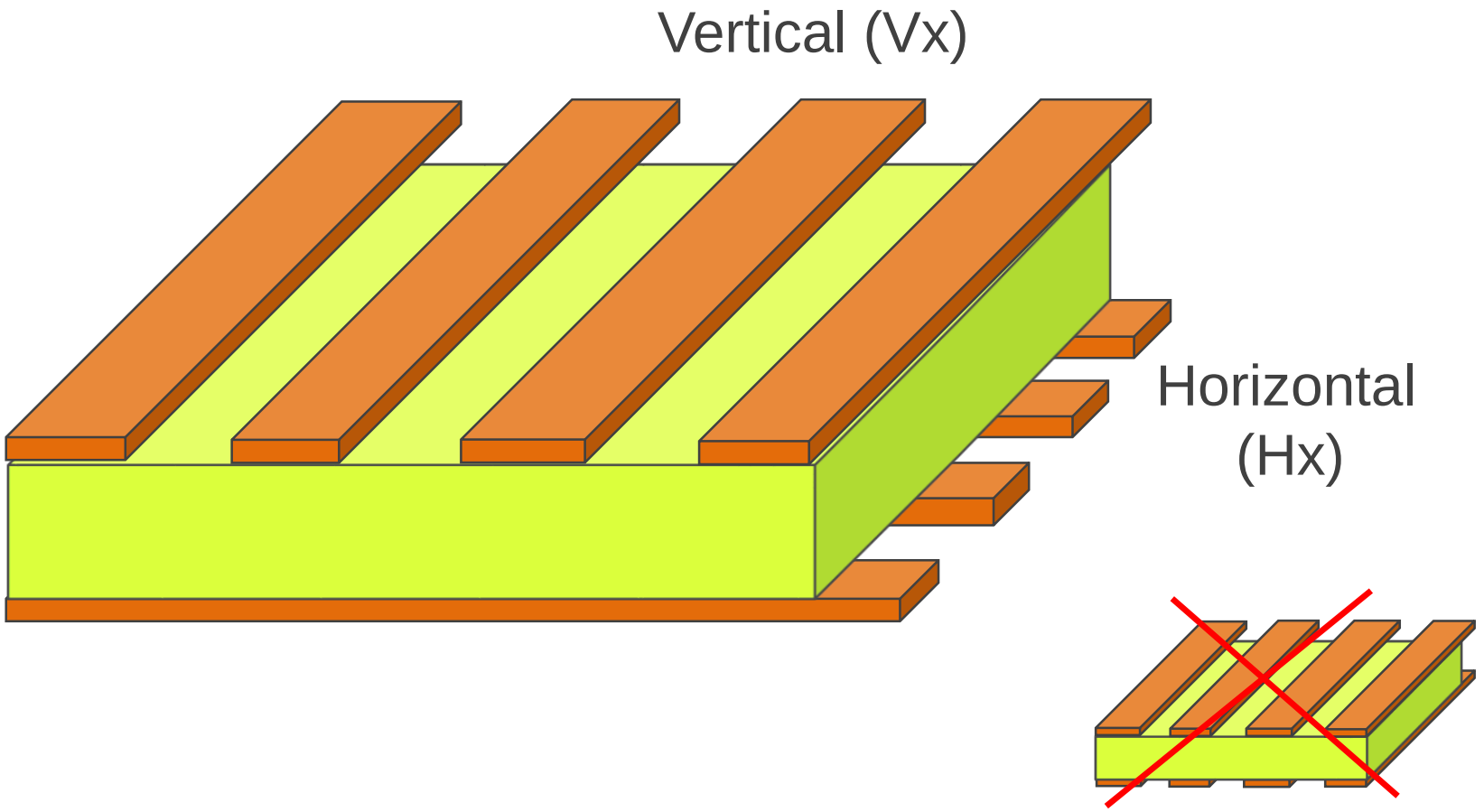


H1 indicates the horizontal routing layer for signal 1, and V1 indicates the vertical routing layer for signal 1. H2 and V2 represent the same for signal 2. This configuration has the advantage that orthogonal routed signals always reference the same plane.

Source: Fineline

Six layer Stack-up

Orthogonal track routing:

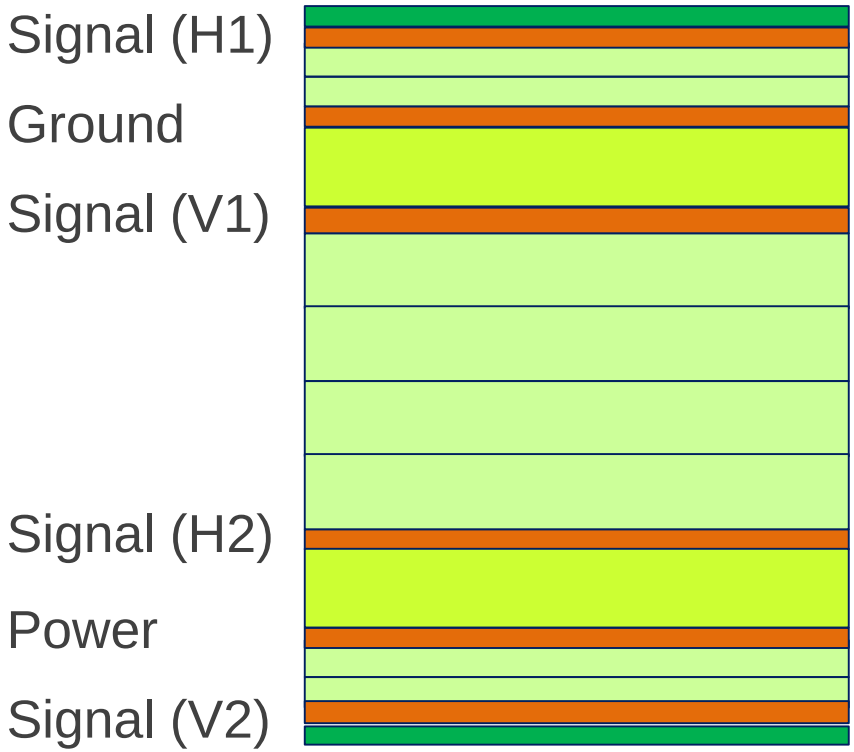


FINELINE
EXCELLENCE IN PCB

Source: Fineline

Six layer stack-up

The disadvantage is that the signals on layer one and six are not shielded.

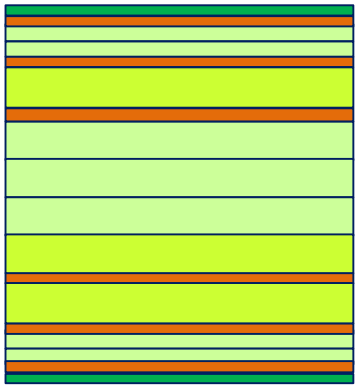


This configuration satisfies objectives “ 1 “ and “ 2 “, but not “ ~~3~~ “, “ ~~4~~ “ and “ ~~5~~ “.

Source: Fineline

Six layer stack-up

It is easier to achieve good EMC performance with a six-layer board than with a four-layer board. We also have the advantage of four signal routing layers instead of being limited to just two. The configurations showed above can be made to perform very well from an EMC point of view.



7 Eight layer stack-up

Eight layer stack-up

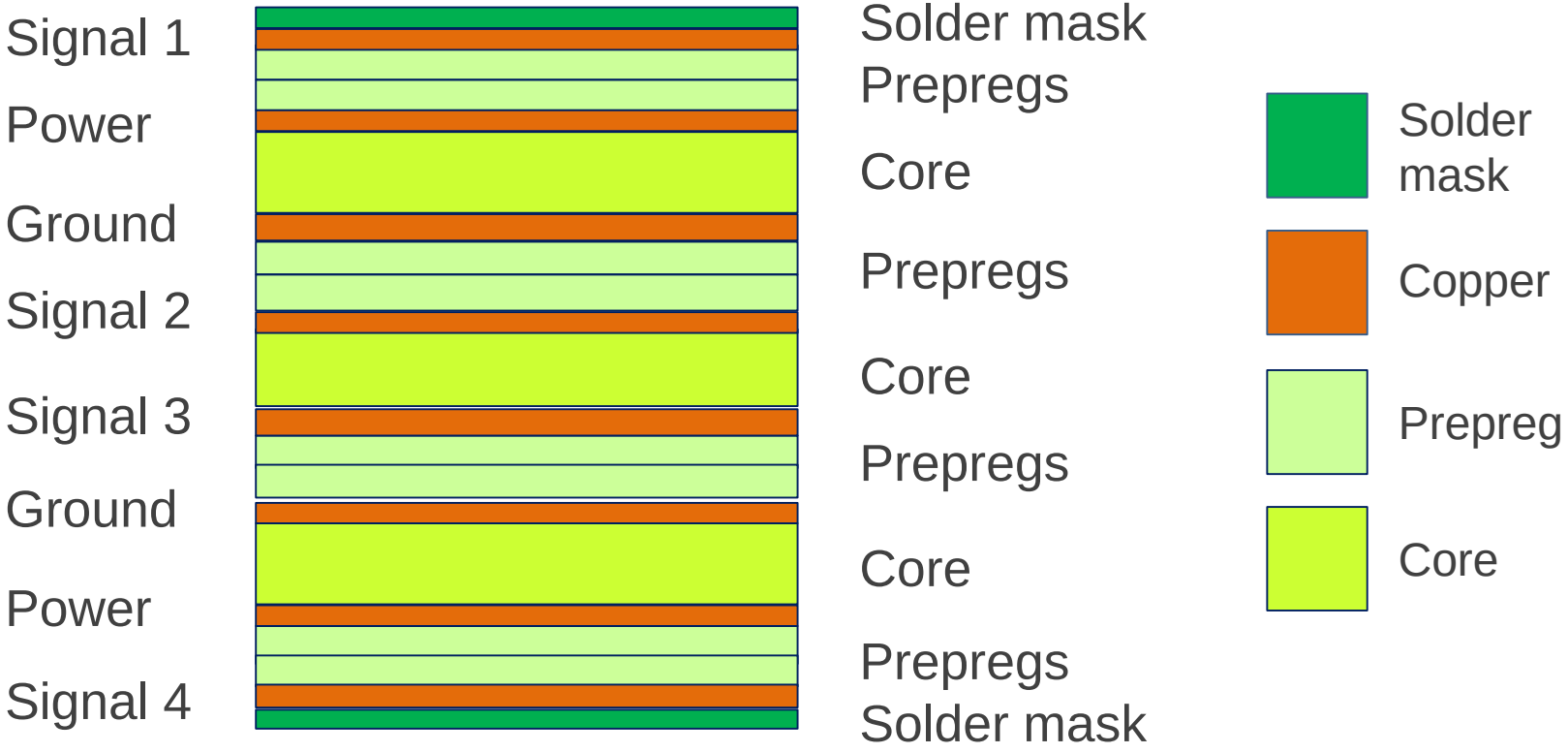
An eight-layer board provides us, for the first time, the opportunity to easily satisfy all of the five originally stated objectives. Although there are many stack-ups possible, we will only discuss a few of them that have proven themselves by providing excellent EMC performance. As stated above, eight layers is usually used to improve the EMC performance of the board, not to increase the number of routing layers.

Eight layer stack-up

Important remark:
An eight-layer board with six routing layers is definitely **not** recommended, no matter how you decide to stack-up the layers. If you need six routing layers you should be using a ten-layer board. Therefore, an eight-layer board can be thought of as a six-layer board with optimum EMC performance.

Eight layer stack-up

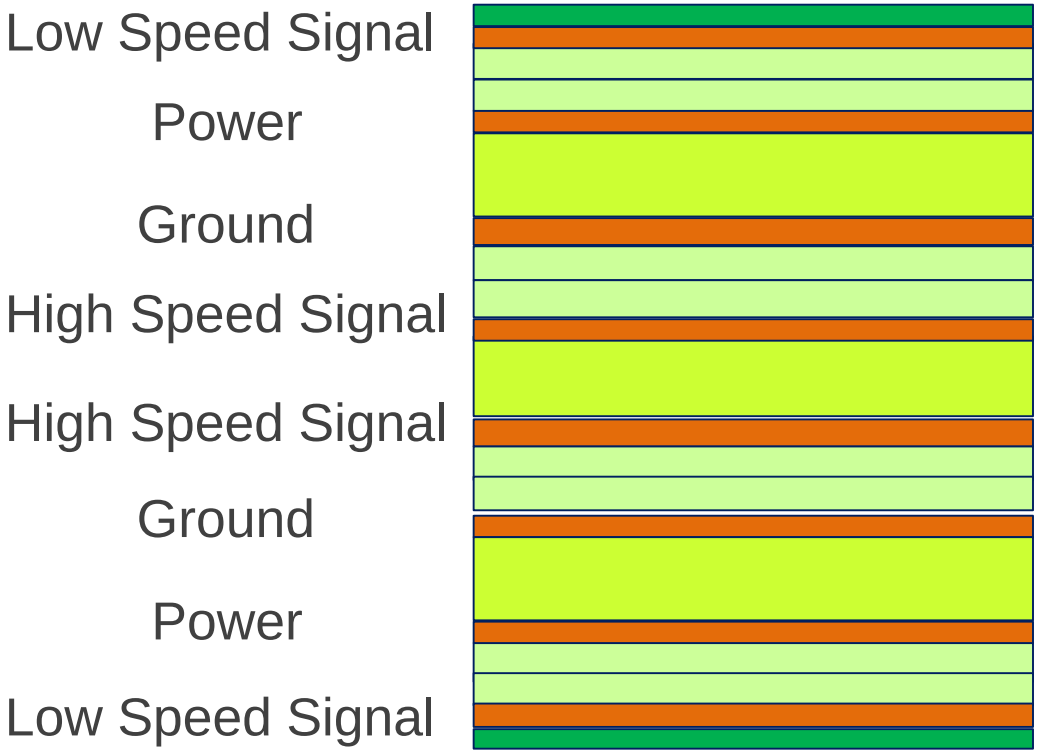
Following the basic stack-up of an eight-layer board with excellent EMC performance:



Source: Fineline

Eight layer stack-up

Following the basic stack-up of an eight-layer board with excellent EMC performance:

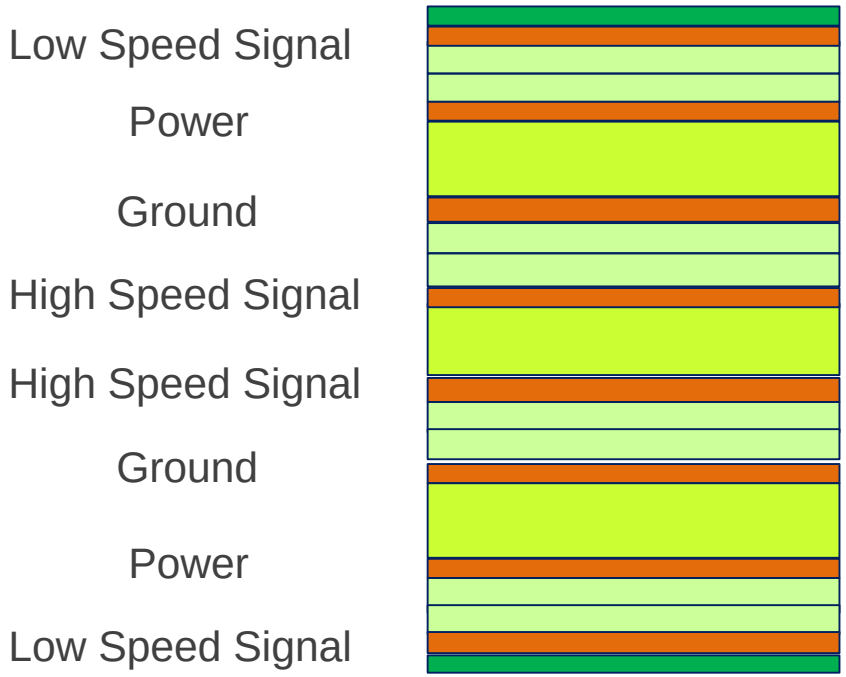


This configuration satisfies all 5 objectives!

Source: Fineline

Eight layer stack up

All signal layers are adjacent to planes, and all the layers are closely coupled together. The high-speed signals are buried between planes, therefore the planes provide shielding to reduce the emissions from these signals. In addition the board uses multiple ground planes, thus decreasing the ground impedance.

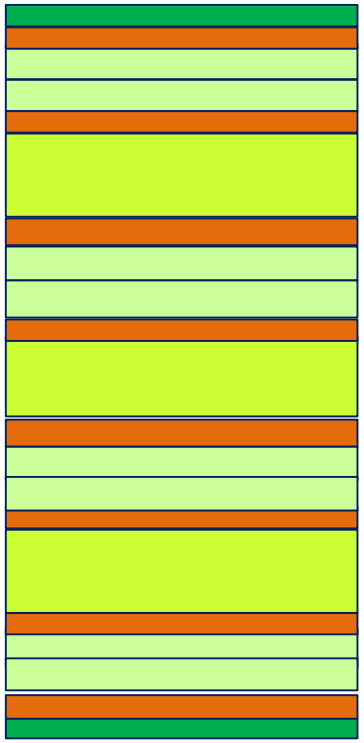


Source: Fineline

Eight layer stack-up

Another excellent configuration, is the following one:

Ground / Mounting Pad
Signal (H1)
Ground
Signal (V1)
Signal (H2)
Power
Signal (V2)
Ground / Mounting Pad



This configuration is similar to the previous One, but includes two outer layer ground planes. With this arrangement all routing layers are buried between planes and are therefore shielded.

Source: Fineline

Eight layer stack-up

H1 indicates the horizontal routing layer for signal 1, and V1 indicates the vertical routing layer for signal 1. H2 and V2 represent the same for signal 2.

Gnd / Mounting Pad

Signal (H1)

Ground

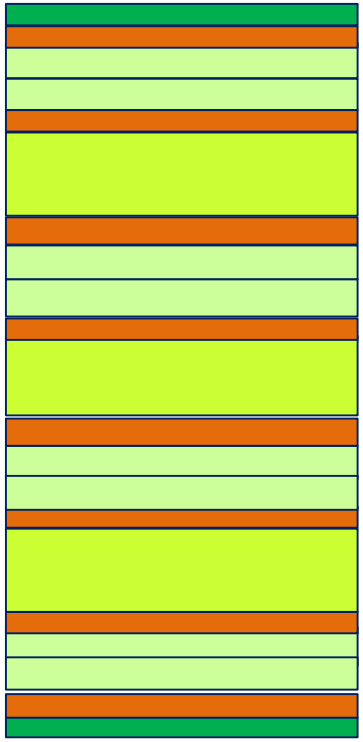
Signal (V1)

Signal (H2)

Power

Signal (V2)

Gnd / Mounting Pad



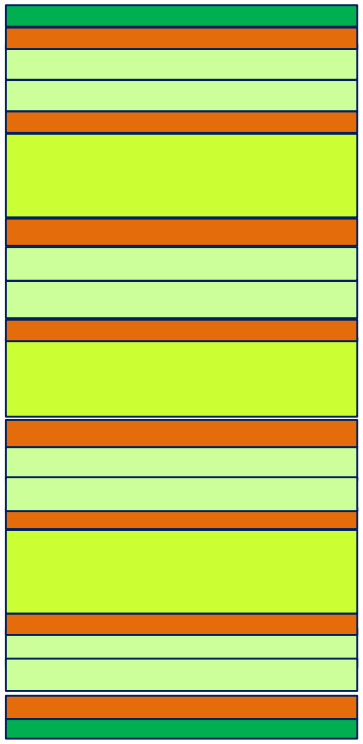
Although not commonly used, this configuration also satisfies all the five objectives presented previously, and has the added advantage of routing orthogonal signals adjacent to the same plane.

FINELINE
EXCELLENCE IN PCB

Source: Fineline

Eight layer stack-up

Again another good configuration:



This configuration satisfies objectives "1", "2", "3" and "5", but not "~~4~~".

Source: Fineline

8 Ten layer stack-up

Ten layer stack-up

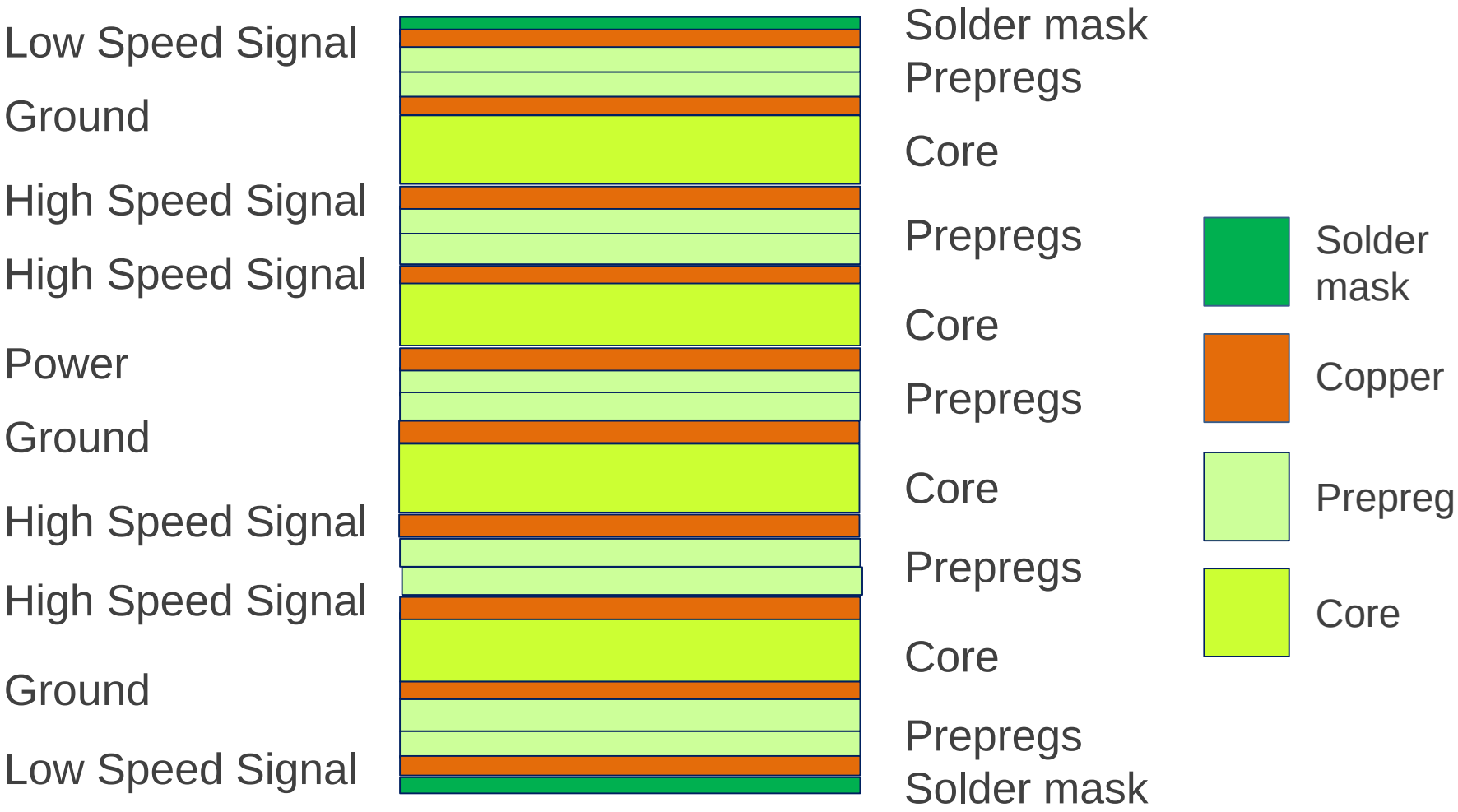
A ten-layer board should be used when six routing layers are required. Ten-layer boards, therefore, usually have six signal layers and four planes.

Having more than six signal layers on a ten-layer board is **not** recommended.

Ten-layers is also the largest number of layers that can usually be conveniently fabricated in a 1.6mm thick board.

Ten layer stack-up

A very common ten layer stack-up:



FINELINE
EXCELLENCE IN PCB

Source: Fineline

Ten layer stack-up

A very common and nearly ideal stack-up for a ten-layer board is shown in previous figure.

The reason that this stack-up has such good performance is:

- the tight coupling of the signal and return planes,
- the shielding of the high-speed signal layers,
- the existence of multiple ground planes,
- as well as a tightly coupled power/ground plane pair in the center of the board.

Ten layer stack-up

High-speed signals normally would be routed on the signal layers buried between planes (layers 3-4 and 7-8 in this case).

The common way to pair orthogonally routed signals in this configuration would be to pair layers 1 & 10 (carrying only low-frequency signals), as well as pairing layers 3 & 4, and layers 7 & 8 (both carrying high-speed signals). By paring signals in this manner, the planes on layers 2 and 9 provide shielding to the high-frequency signal traces on the inner layers.

Ten layer stack-up

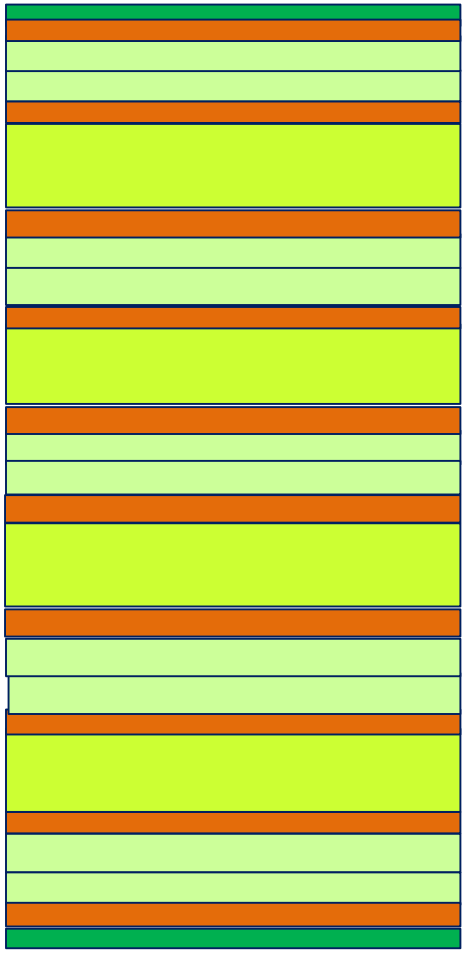
In addition the signals on layers 3 & 4 are isolated from the signals on layers 7 & 8 by the center power/ground plane pair.

For example, high-speed clocks might be routed on one of these pairs, and high-speed address and data buses routed on the other pair. In this way the bus lines are protected, against being contaminated with clock noise, by the intervening planes.

This configuration satisfies all of the five original objectives.

Ten layer stack-up

Another common ten layer stack-up:



Source: Fineline

Ten layer stack-up

This configuration gives up the closely spaced power/ground plane pair. In return it provides three signal- routing-layer pairs shielded by the ground planes on the outer layers of the board, and isolated from each other by the internal power and ground plane. All signal layers are shielded and isolated from each other in this configuration.

This configuration satisfies objectives “1“, “2“ “4“ and “5“, but not “3“.

Ten layer stack-up

A third common ten layer stack-up:

Low Speed Signal

Power

Signal (H1)

Ground

Signal (V1)

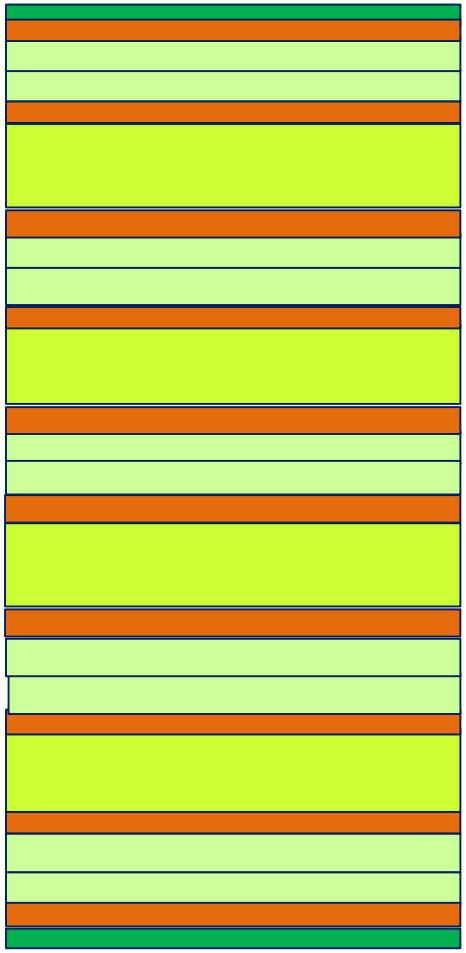
Signal (H2)

Ground

Signal (V2)

Ground or Power

Low Speed Signal



Solder mask

Prepregs

Core

Prepregs

Core

Prepregs

Core

Prepregs

Core

Prepregs

Solder mask

Solder mask

Copper

Prepreg

Core

FINELINE
EXCELLENCE IN PCB

Source: Fineline

Ten layer stack-up

This stack-up allows the routing of orthogonal signals adjacent to the same plane, but in the process also has to give up the closely spaced power/ground. It, however, has the additional advantage that orthogonal routed signals always reference the same plane.

This configuration satisfies objectives “1“, “2“ “4“ and “5“, but not “3“.

9 Summery

Summery

A good PCB stack-up:

- reduces radiation,
- improves signal quality,
- and helps aid in the decoupling of the power bus.

No one stack-up is best, there is a number of viable options in each case and some compromise of objectives is usually necessary.

Summary

- PCB stack-up design is an integral part of the signal integrity engineering process.
- PCB stack up design is far too complex to be left in the hands of the fabricator. It is not that fabricators are not capable of designing stack-ups, their skill set does not cover all the areas that are important.
- PCB stack-up design is a joint effort between SI engineers and fabricators. Neither can do it alone.

Summary

- PCB stack-up design requires detailed knowledge of the materials used to fabricate PCBs as well as the fabrication process itself.
- PCB stack-up design is not a difficult process given good materials data and design tools.

Choosing a PCB manufacturer as a design partner

- PCB stack-up design is a combination of manufacturing engineering and electrical engineering.
- Successful stack-up design required close cooperation between electrical engineers and fabrication engineers.
- Therefore, it is advisable for the design engineer to seek out a fabricator whose capabilities are in line with the complexity of the PCB being designed.

Choosing a PCB manufacturer as a design partner

- Once this alliance is established, the design engineer needs to propose a stack-up that meets the electrical requirements and have it reviewed by the fabricator for feasibility.

References

Barry Olney: “The dumping Ground”

Henry W. Ott: “Electromagnetic Compatibility Engineering”

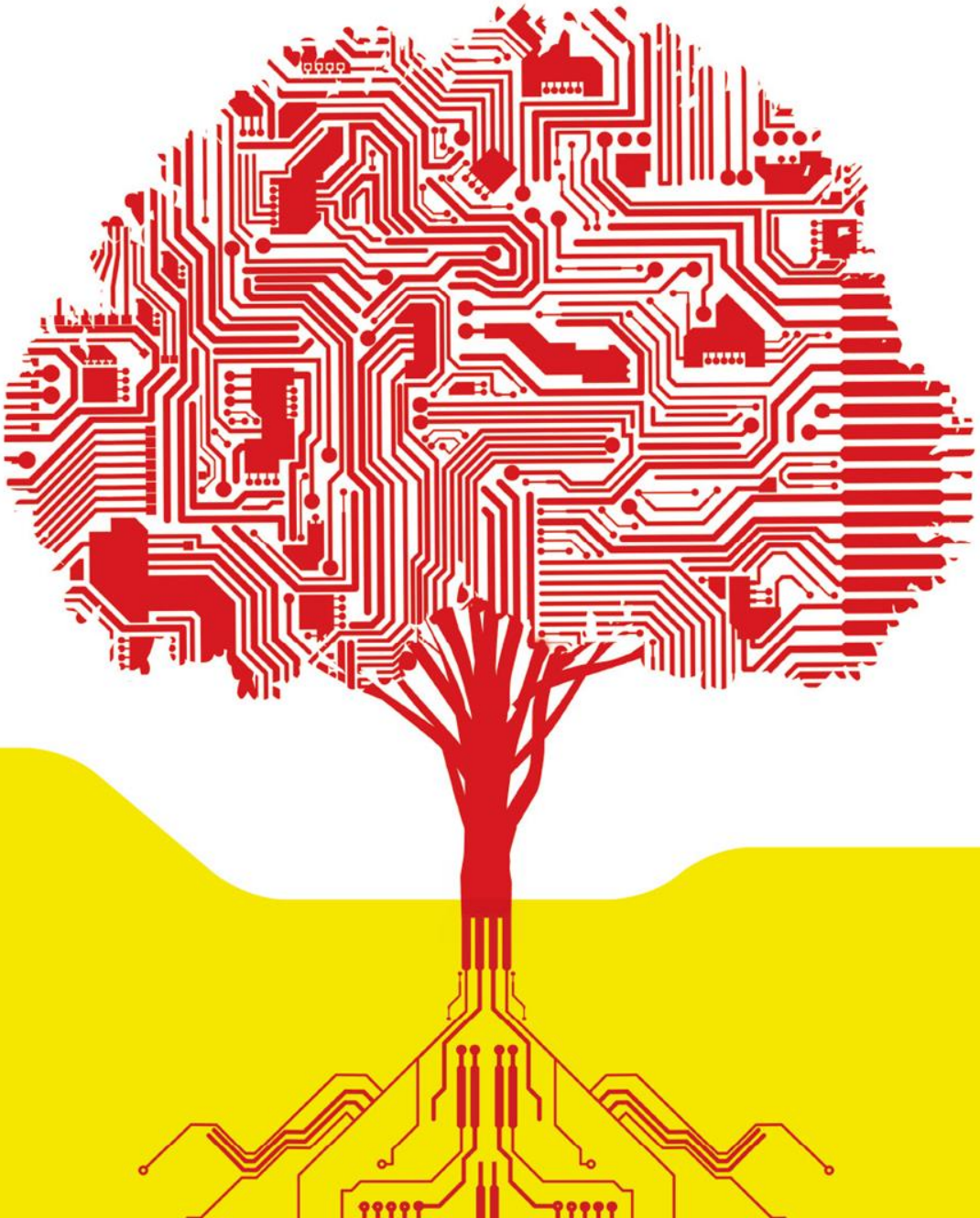
Lee W. Ritchey: “Speeding Etch”

Arnold Wiemers: “Strategien für den Aufbau von Multilayern unter dem Aspekt der Zuverlässigkeit”

Arnold Wiemers: “Was modern Multilayer-Systeme leisten können”

CIRCUITS OF EXPERTISE

Thank you



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EXCELLENCE IN PCB