The "Ground" Myth

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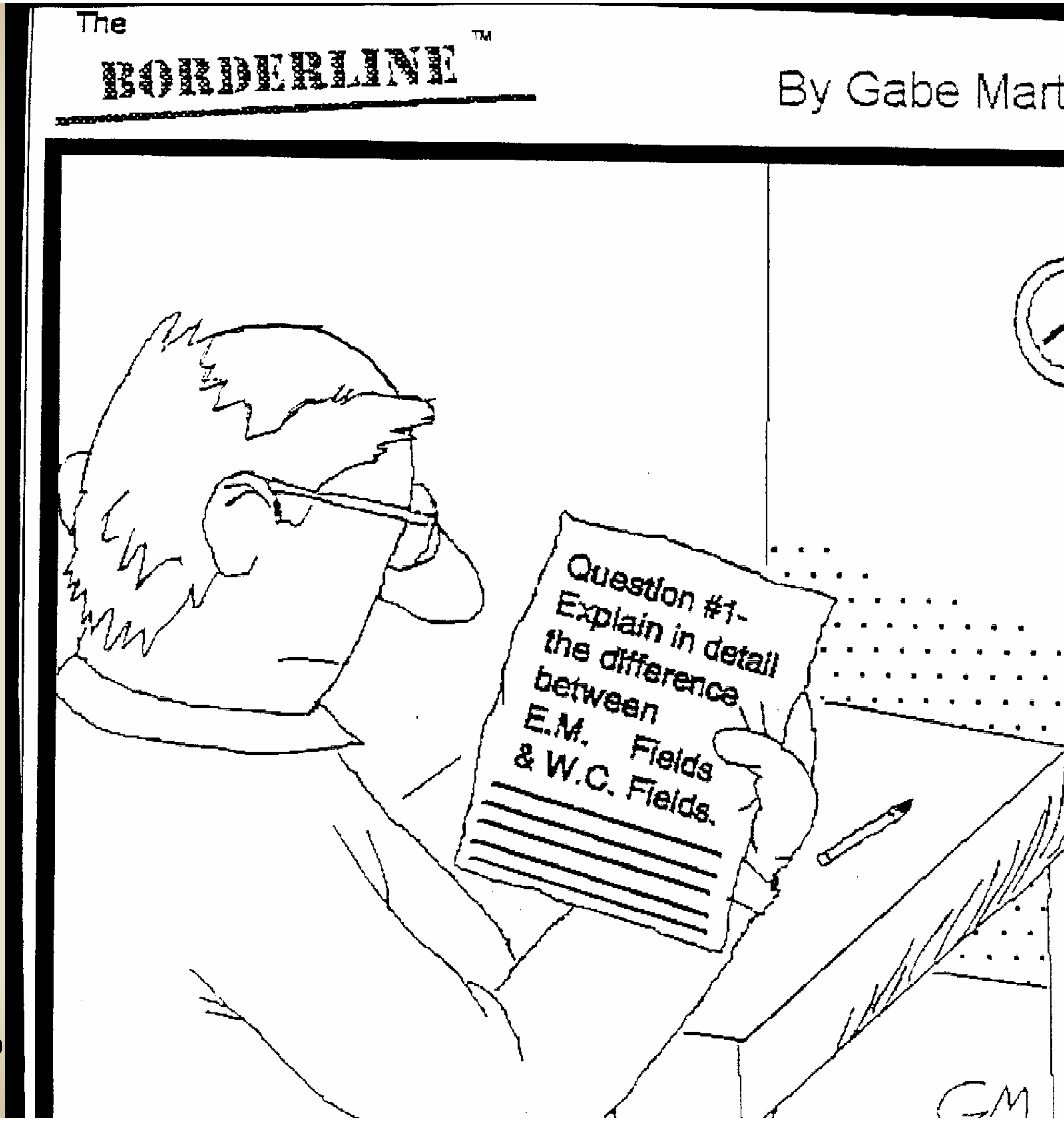
IEEE

Introduction

- Electromagnetics can be scary
  - Universities *LOVE* messy math
- EM is not hard, unless you want to do the messy math
- Goal:
  - Intuitive understanding
  - Understand the basic fundamentals
  - Understand how to read the math


The BORDERLINE™
By Gabe Mart
Question #1- Explain in detail the difference between E.M. Fields & W.C. Fields.
GM

Overview

- What does the derivative mean?
- What does integration mean?
- Weird vector notation
- In the beginning – Faraday and Maxwell
- Inductance
- “Ground”
- Primary cause of EMI problems on PCBs

Derivative

- How fast is *something* changing?

$$\frac{d}{dt}\left[something\right]$$

Changing with respect to time

$$\frac{d}{dx}\left[something\right]$$

Changing with respect to position (x)

Partial Derivative

- How fast is *something* changing for one variable?

$$\frac{\partial}{\partial t}\left[something(t,x)\right]$$

Changing with respect to time (as ‘x’ is constant)

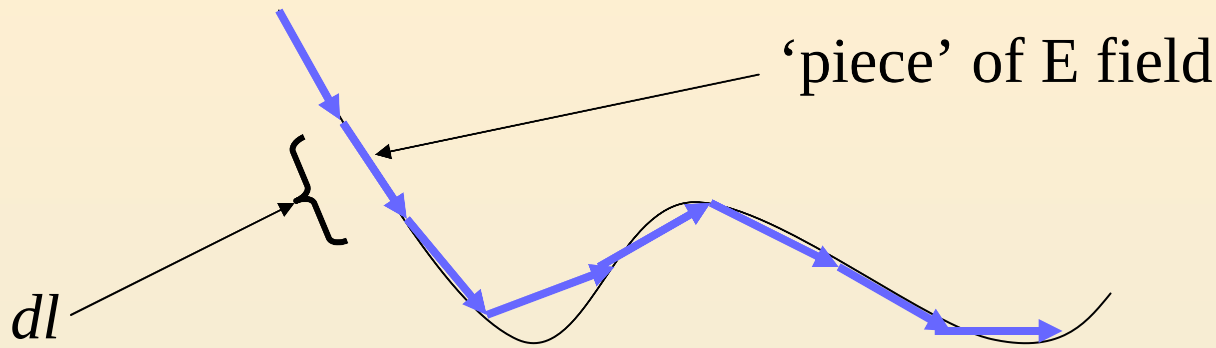
$$\frac{\partial}{\partial x}\left[something(t,x)\right]$$

Changing with respect to position (x) (as time is constant)

Integration

- Simply the sum of parts (when the parts are very small)
  - Line Integral --- sum of small line segments
  - Surface Integral -- sum of small surface patches
  - Volume Integral -- sum of small volume blocks

Line Integral
(find the length of the path)

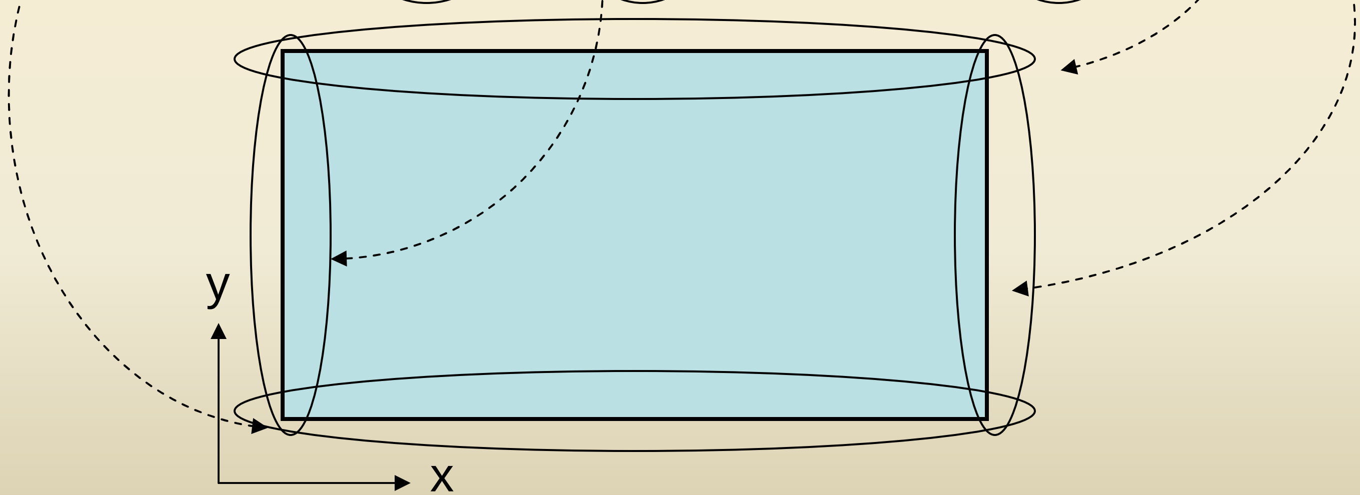


$$V = -\int_{start}^{stop} (\vec{E} \bullet dl)$$

Line Integral -- Closed

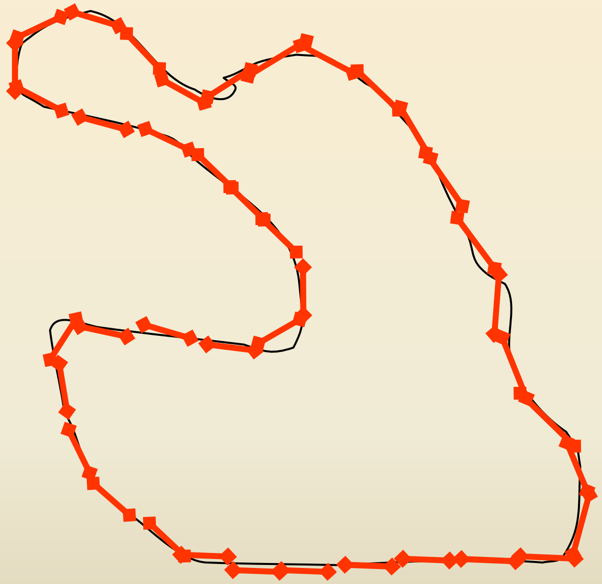
$$Circumference = \oint path\ around\ box$$

$$= \int_{x=0}^{x=l} dx + \int_{y=0}^{y=w} dy + \int_{x=l}^{x=0} dx + \int_{y=w}^{y=0} dy$$

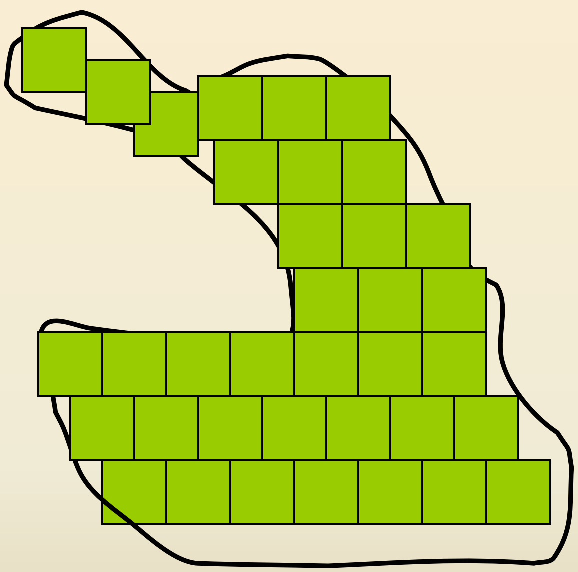


Line Integral -- Closed

- Closed line integrals find the path length
- And/or the amount of some quantity along that closed path length



Surface Integral
(find the area of the surface)



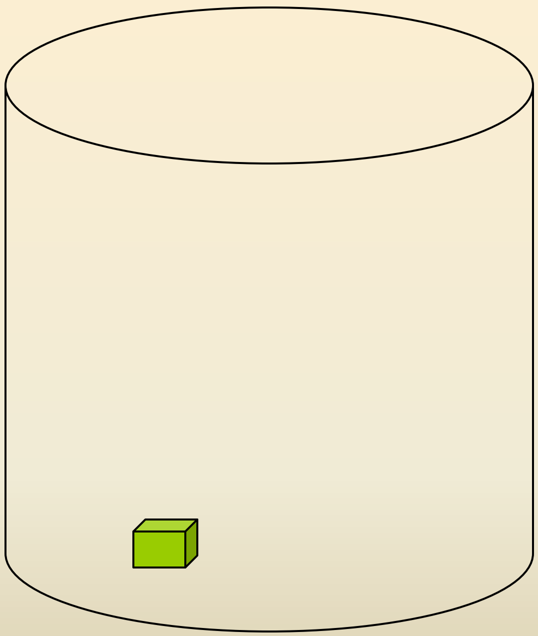
$$Area = \int da$$

$$da = dx * dy$$

$$Area = \iint dx * dy$$

As *dx* and *dy* become smaller and smaller, the area is better calculated

Volume Integral
(find the volume of an object)



$$Volume = \int dv$$

$$dv = dx * dy * dz$$

$$Volume = \iiint [dx * dy * dz]$$

Electromagnetics
In the Beginning

- Electric and Magnetic effects not connected
- Electric and magnetic effects were due to 'action from a distance'
- Faraday was the 1st to propose a relationship between electric lines of force and time-changing magnetic fields
  - Faraday was very good at experiments and 'figuring out' how things work

Maxwell

- Maxwell was impressed with Faraday's ideas
- Discovered the mathematical link between the "electro" and the "magnetic"
- Scotland's greatest contribution to the world (next to Scotch)

"Maxwell's Equations"

- Maxwell's original work included 20 equations!
- Heaviside reduced them to the existing four equations
  - Heaviside refused to call the equations his own
- Hertz is credited with proving they are correct

Maxwell's Equations are NOT Hard!

$$\nabla \times H = J + \frac{\partial D}{\partial t}$$

$$\nabla \times E = -\frac{\partial B}{\partial t}$$

Maxwell's Equations are not Hard!

- Change in H-field across space ≈ Change in E-field (at that point) with time
- Change in E-field across space ≈ Change in H-field (at that point) with time
- (Roughly speaking, and ignoring constants)

Current Flow

- Most important concept of EMC
- Current flow through metal changes as frequency increases
- DC current
  - Uses entire conductor
  - Only resistance inhibits current
- High Frequency
  - Only small part of conductor (near surface) is used
  - *Resistance* is small part of current inhibitor
  - ***<u>Inductance</u>*** is major part of current inhibitor

Skin Depth

- High frequency current flows only near the metal surface at high frequencies

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

Frequency	Skin Depth	Skin Depth
60 Hz	260 mils	8.5 mm
1 KHz	82 mils	2.09 mm
10 KHz	26 mils	0.66 mm
100 KHz	8.2 mils	0.21 mm
1 MHz	2.6 mils	0.066 mm
10 MHz	0.82 mils	0.021 mm
100 MHz	0.26 mils	0.0066 mm
1 GHz	0.0823 mils	0.0021 mm

Inductance

- Current flow through metal => inductance!
- Fundamental element in EVERYTHING
- Loop area first order concern
- Inductive impedance increases with frequency and is MAJOR concern at high frequencies

$$X_L = 2\pi f L$$

Current Loop => Inductance

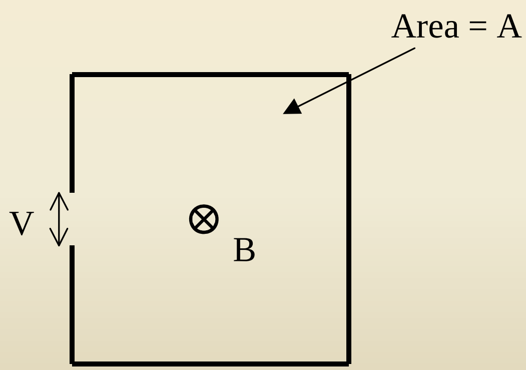
Courtesy of Elya Joffe

Inductance Definition

- Faraday's Law

$$\oint \overline{E} \cdot dl = -\iint \frac{\partial \overline{B}}{\partial t} \cdot d\overline{S}$$

- For a simple rectangular loop



$$V = -A\frac{\partial B}{\partial t}$$

The minus sign means that the induced voltage will work against the current that originally created the magnetic field!

Self Inductance

- Isolated circular loop

$$L \approx \mu_0 a \left(\ln \frac{8a}{r_0} - 2 \right)$$

- Isolated rectangular loop

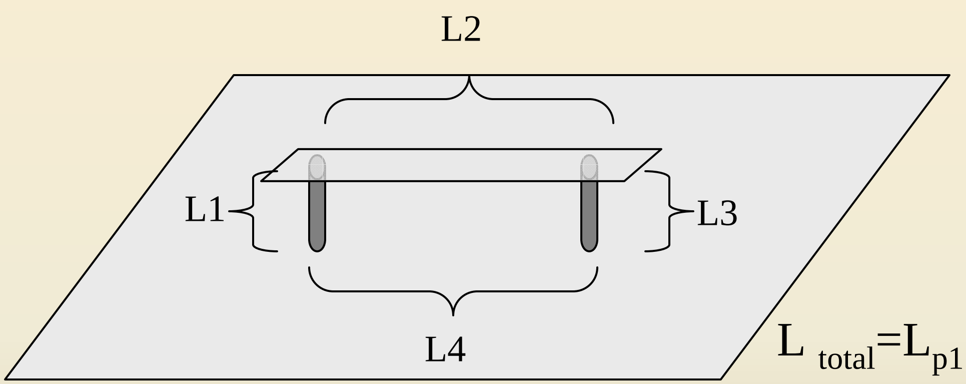
$$L = \frac{2\mu_0 a}{\pi} \ln\left(\frac{p + \sqrt{1+p^2}}{1+\sqrt{2}} + \frac{1}{p} - 1 + \sqrt{2} - \frac{1}{p}\sqrt{1+p^2} \right)$$

Note that inductance is directly influenced by loop ***<u>AREA</u>*** and only less influenced by conductor size!

$$p = \frac{length\ of\ side}{wire\ radius}$$

Partial Inductance

- Simply a way to break the overall <u>loop</u> into pieces in order to find total inductance



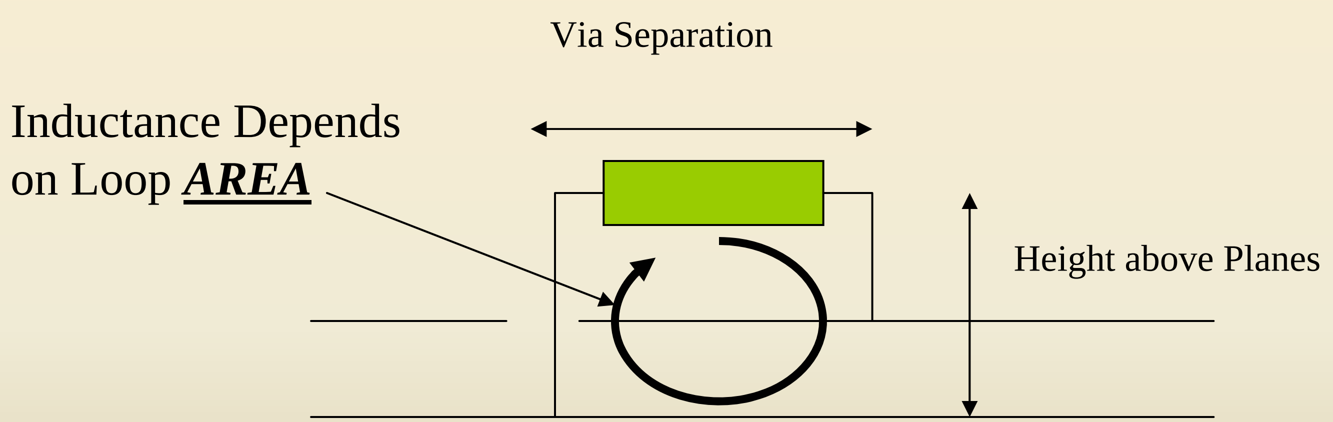
$$L_{total} = L_{p11} + L_{p22} + L_{p33} + L_{p44} - 2L_{p13} - 2L_{p24}$$

Important Points About Inductance

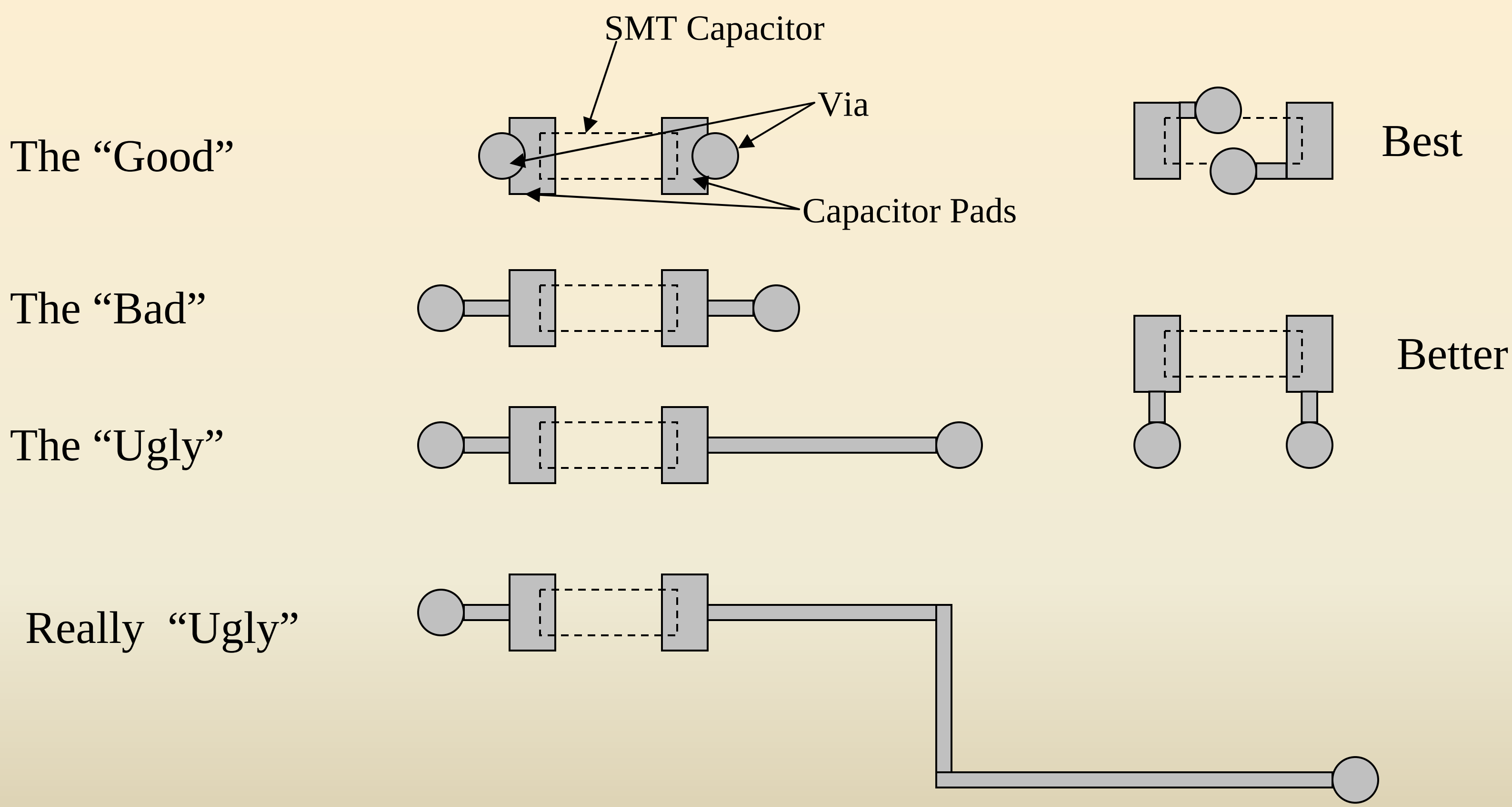
- Inductance is everywhere
- Loop area most important
- Inductance is everywhere

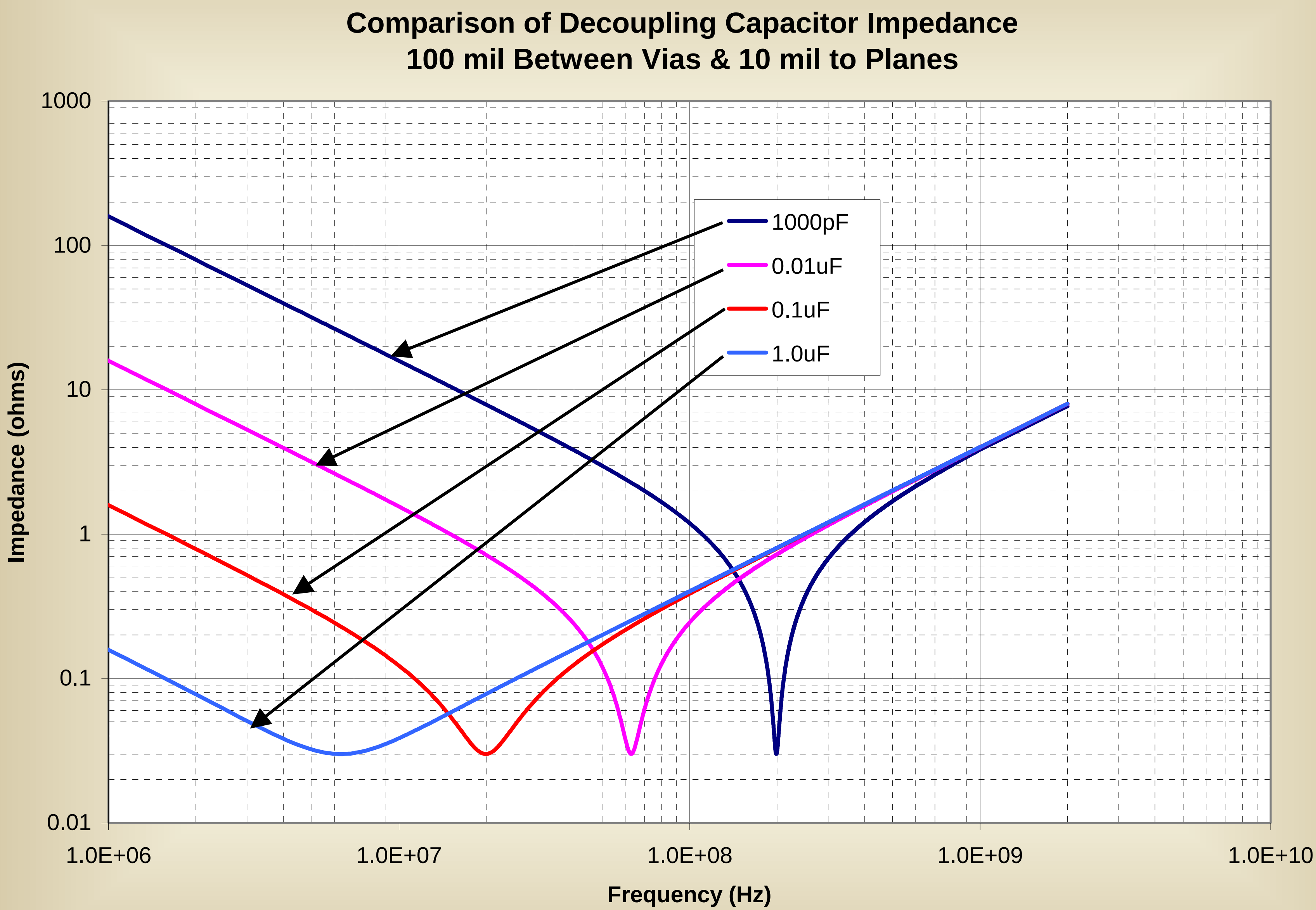
Decoupling Capacitor Mounting

- Keep as to planes as close to capacitor pads as possible

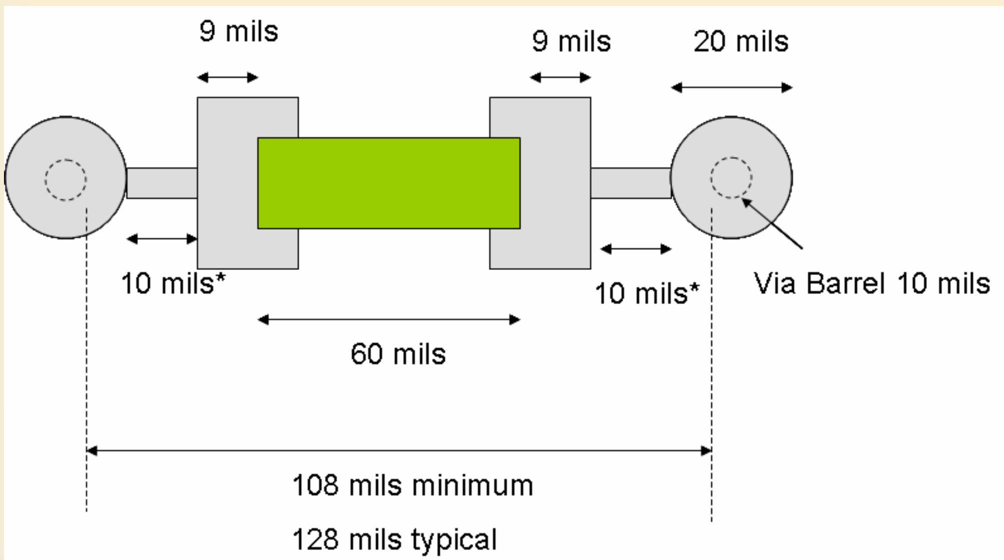


Via Configuration Can Change Inductance

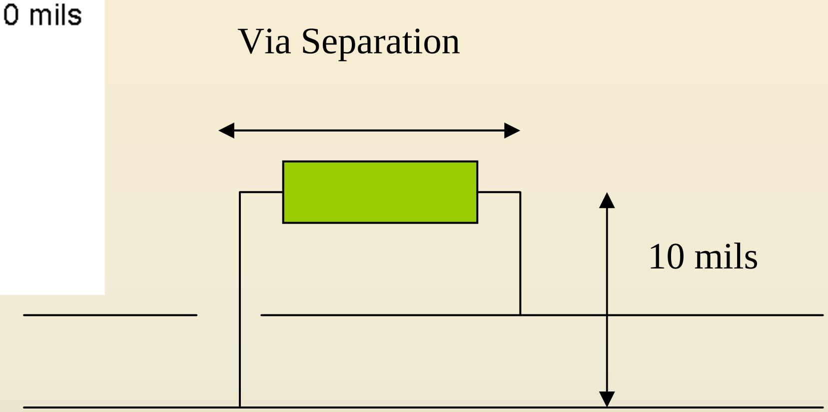



Comparison of Decoupling Capacitor Impedance
100 mil Between Vias & 10 mil to Planes
Impedance (ohms)
1000
100
10
1
0.1
0.01
1.0E+06
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)
1000pF
0.01uF
0.1uF
1.0uF

Comparison of Decoupling Capacitor Via Separation Distance Effects



0603 Typical
Minimum
Dimensions



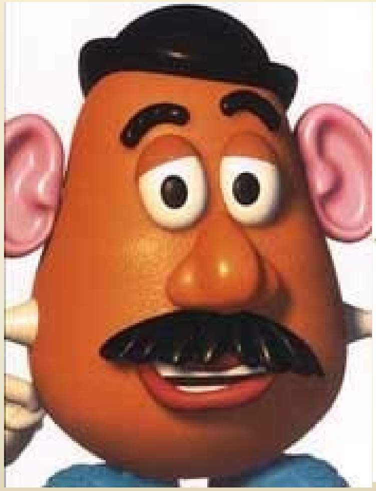
Connection Inductance for Typical Capacitor Configurations

Distance into board to planes (mils)	**0805 typical/minimum (148 mils between via barrels)**	**0603 typical/minimum (128 mils between via barrels)**	**0402 typical/minimum (106 mils between via barrels)**
10	1.2 nH	1.1 nH	0.9 nH
20	1.8 nH	1.6 nH	1.3 nH
30	2.2 nH	1.9 nH	1.6 nH
40	2.5 nH	2.2 nH	1.9 nH
50	2.8 nH	2.5 nH	2.1 nH
60	3.1 nH	2.7 nH	2.3 nH
70	3.4 nH	3.0 nH	2.6 nH
80	3.6 nH	3.2 nH	2.8 nH
90	3.9 nH	3.5 nH	3.0 nH
100	4.2 nH	3.7 nH	3.2 nH

‘Ground’

- **Ground is a place where potatoes and carrots thrive!**
- ‘Earth’ or ‘reference’ is more descriptive
- Original use of “GROUND”
- Inductance is everywhere

$$X_L = 2\pi f L$$



What we Really Mean when we say ‘Ground’

- Signal Reference
- Power Reference
- Safety Earth
- Chassis Shield Reference

‘Ground’ is NOT a Current Sink!

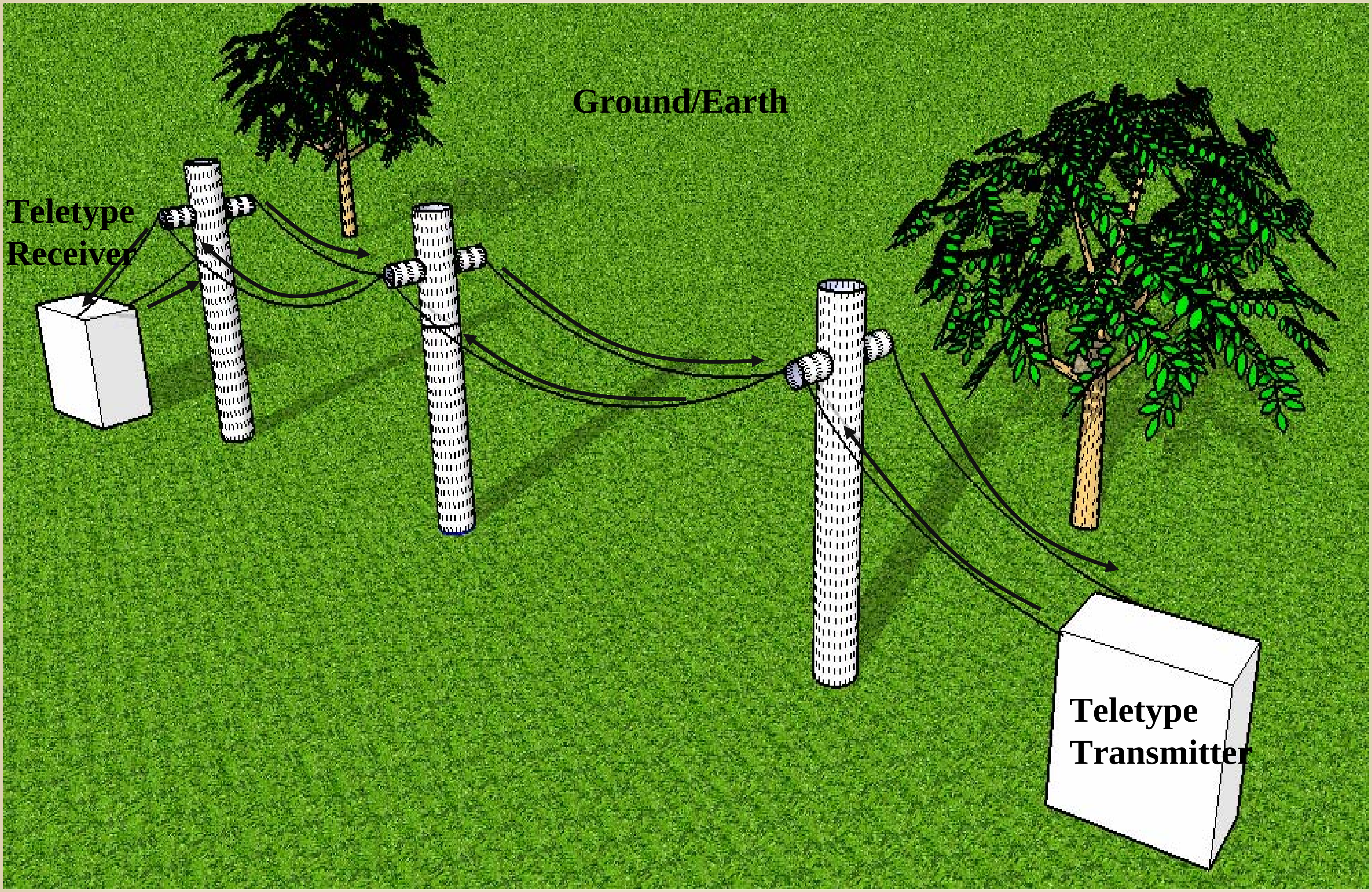
- Current leaves a driver on a trace and must return (somehow) to its source
- This seems basic, but it is often forgotten, and is most often the cause of EMC problems

‘Grounding’ Needs Low Impedance at Highest Frequency

- Steel Reference Plate
  - 4 milliohms/sq @ 100KHz
  - 40 milliohms/sq @ 10 MHz
  - 400 milliohms/sq @ 1 GHz
- A typical via is about 2 nH
  - @ 100 MHz   Z = 1.3 ohms
  - @ 500 MHz   Z = 6.5 ohms
  - @ 1000 MHz   Z = 13 ohms
  - @ 2000 MHz   Z = 26 ohms

Where did the Term “GROUND” Originate?

- Original Teletype connections
- Lightning Protection


Ground/Earth
Teletype
Receiver
Teletype
Transmitter

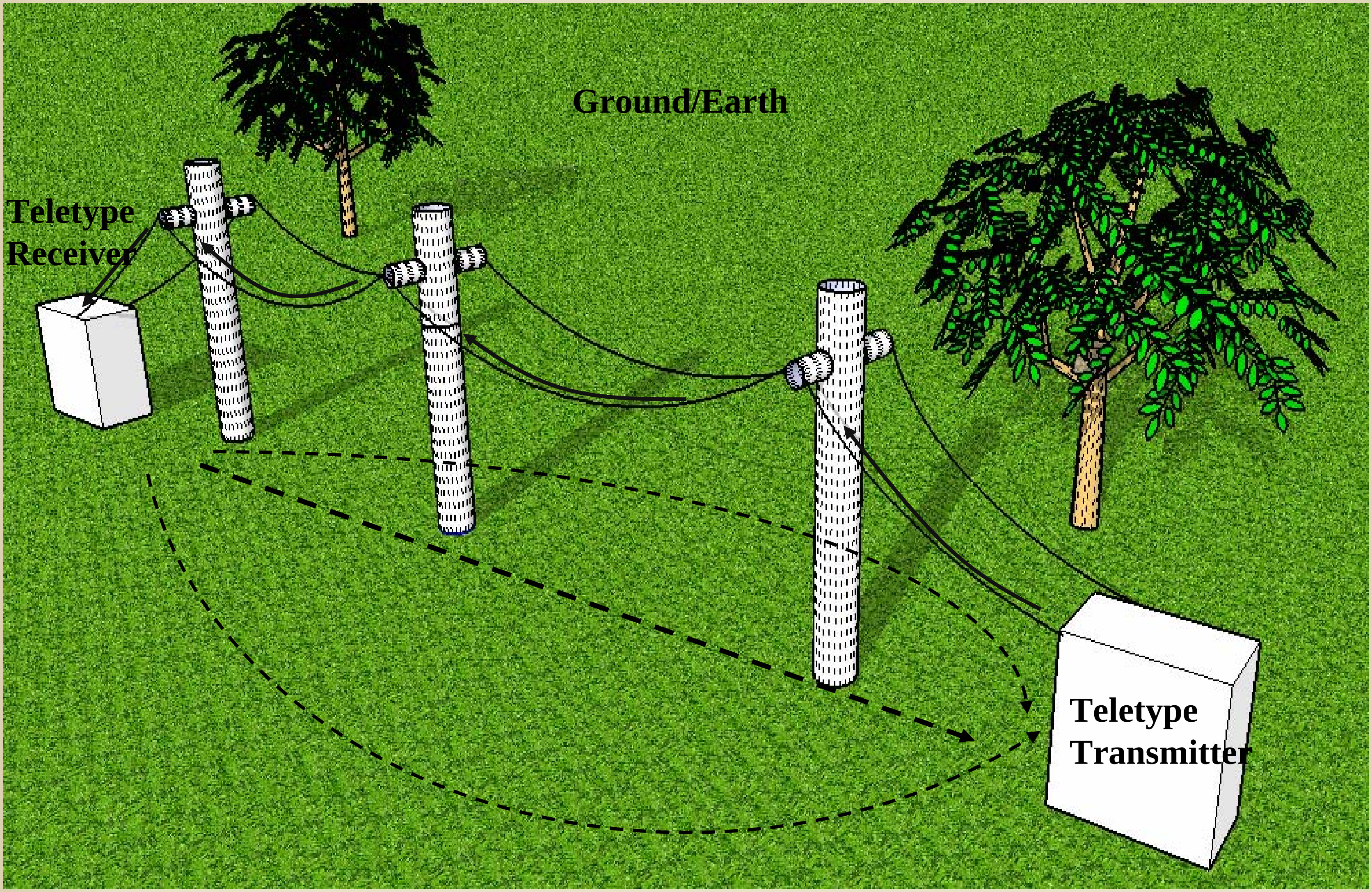
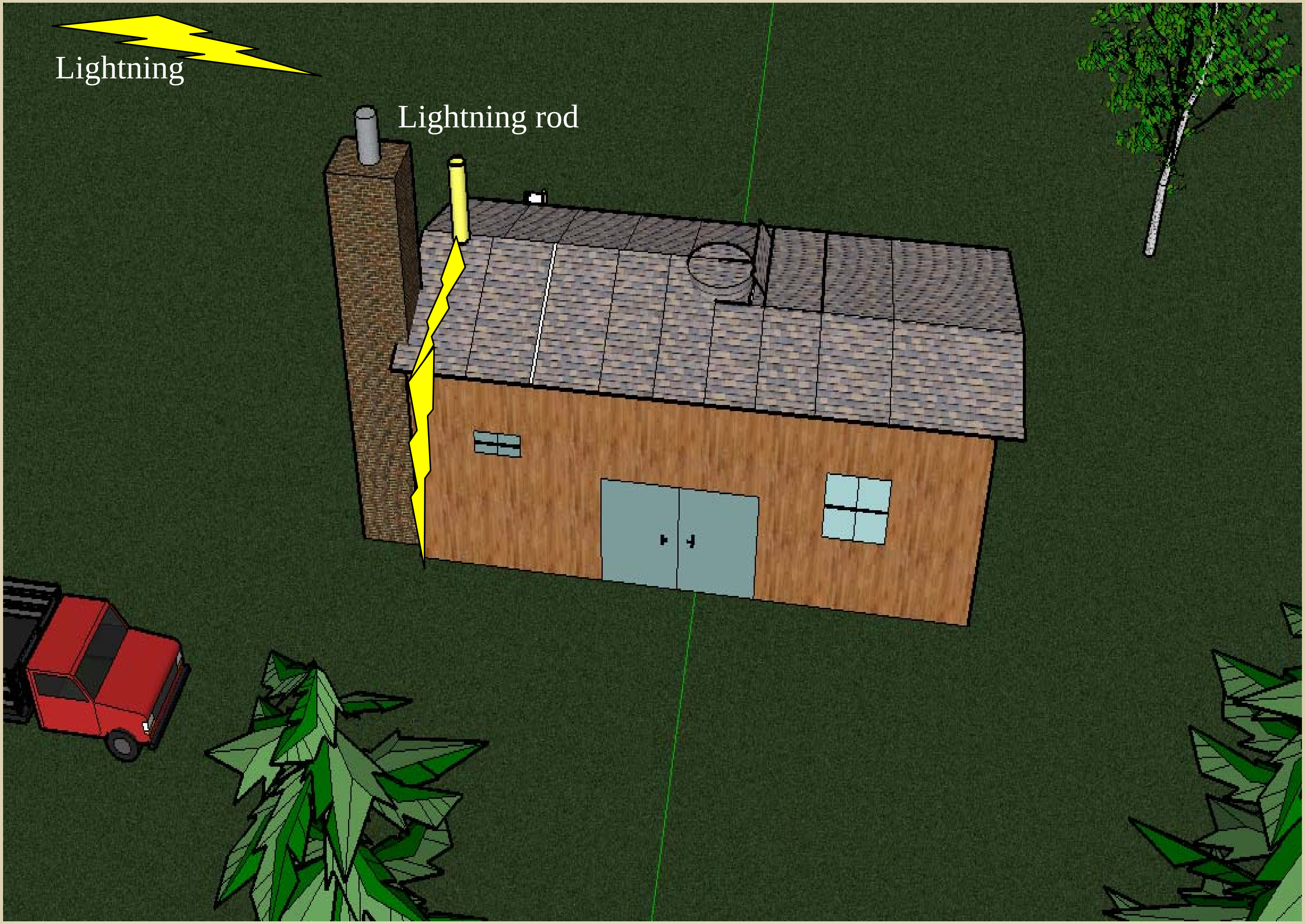

Ground/Earth
Teletype
Receiver
Teletype
Transmitter

FIG 7

Lightning striking house

Lightning effect without rod

Lightning effect with rod



What we Really Mean when we say ‘Ground’

- Signal Reference
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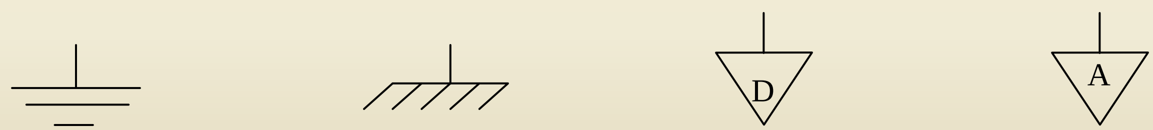
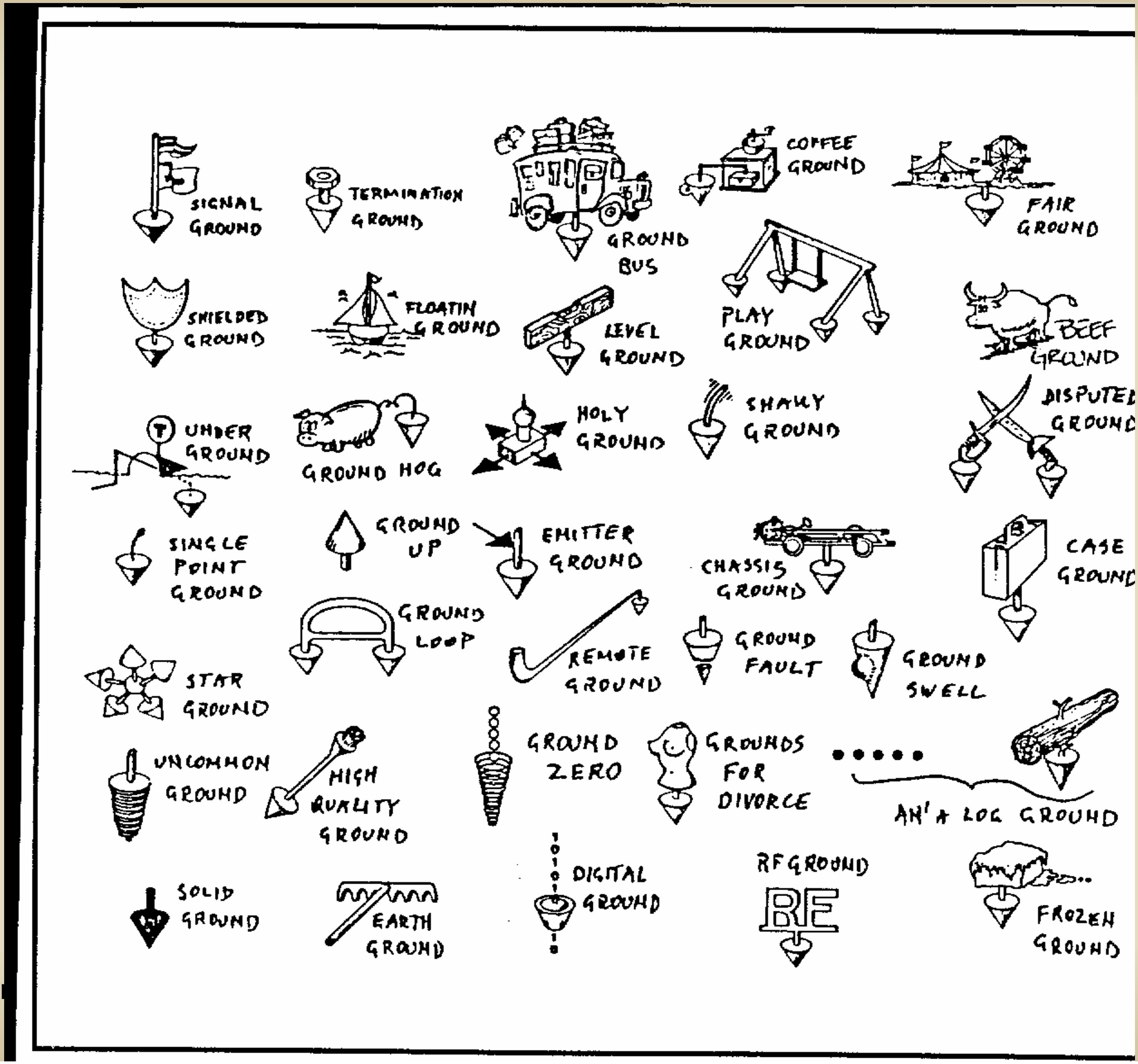
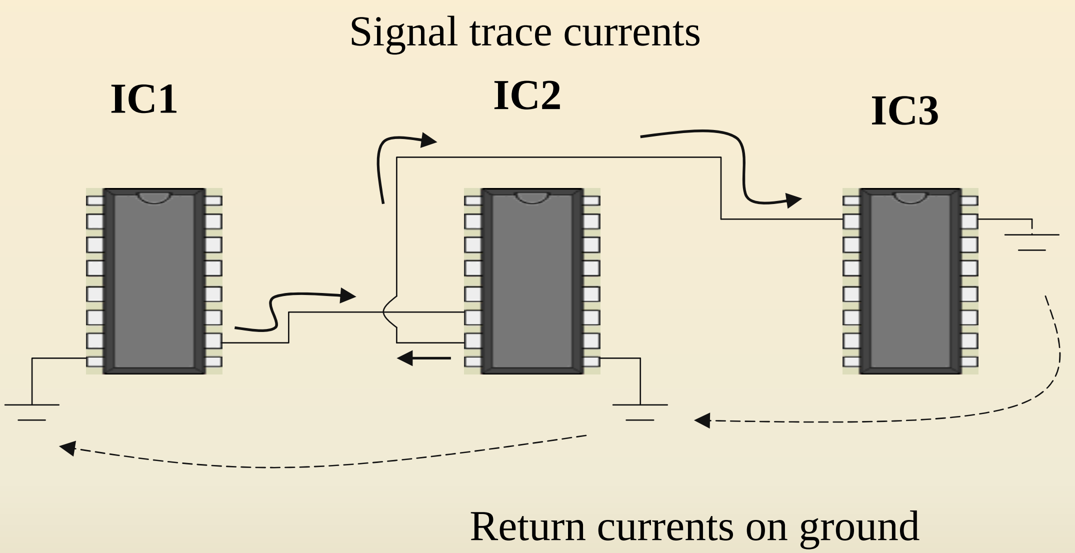


Circuit “Ground” | Chassis “Ground” | Digital “Ground” | Analog “Ground”

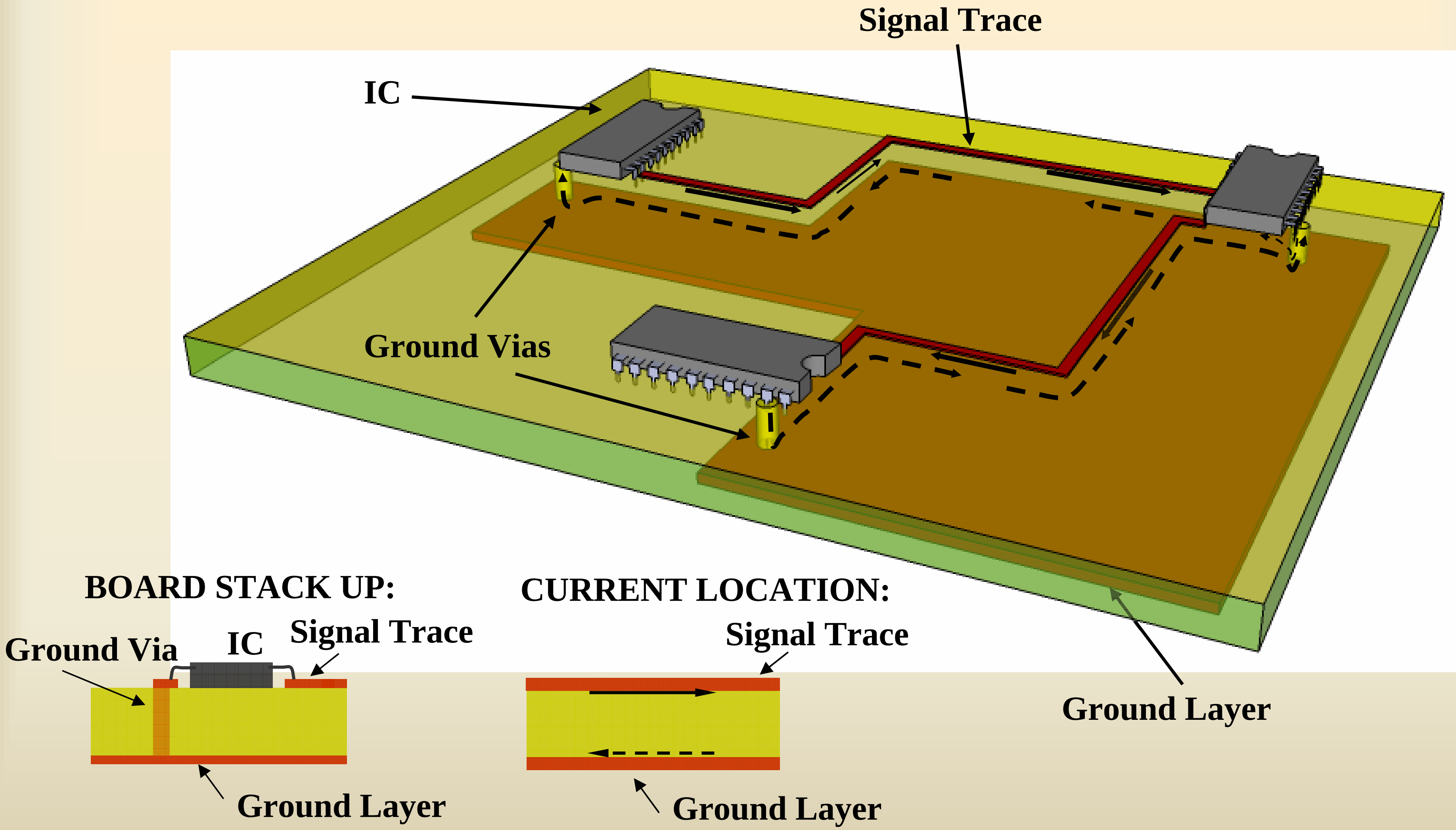


SIGNAL GROUND
TERMINATION GROUND
GROUND BUS
COFFEE GROUND
FAIR GROUND
SHIELDED GROUND
FLOATIN GROUND
LEVEL GROUND
PLAY GROUND
BEEF GROUND
UNDER GROUND
GROUND HOG
HOLY GROUND
SHAKY GROUND
DISPUTED GROUND
SINGLE POINT GROUND
GROUND UP
EMITTER GROUND
CHASSIS GROUND
CASE GROUND
GROUND LOOP
REMOTE GROUND
GROUND FAULT
GROUND SWELL
STAR GROUND
UNCOMMON GROUND
HIGH QUALITY GROUND
GROUND ZERO
GROUNDS FOR DIVORCE
AN' A LOG GROUND
SOLID GROUND
EARTH GROUND
DIGITAL GROUND
RF GROUND
RF
FROZEN GROUND

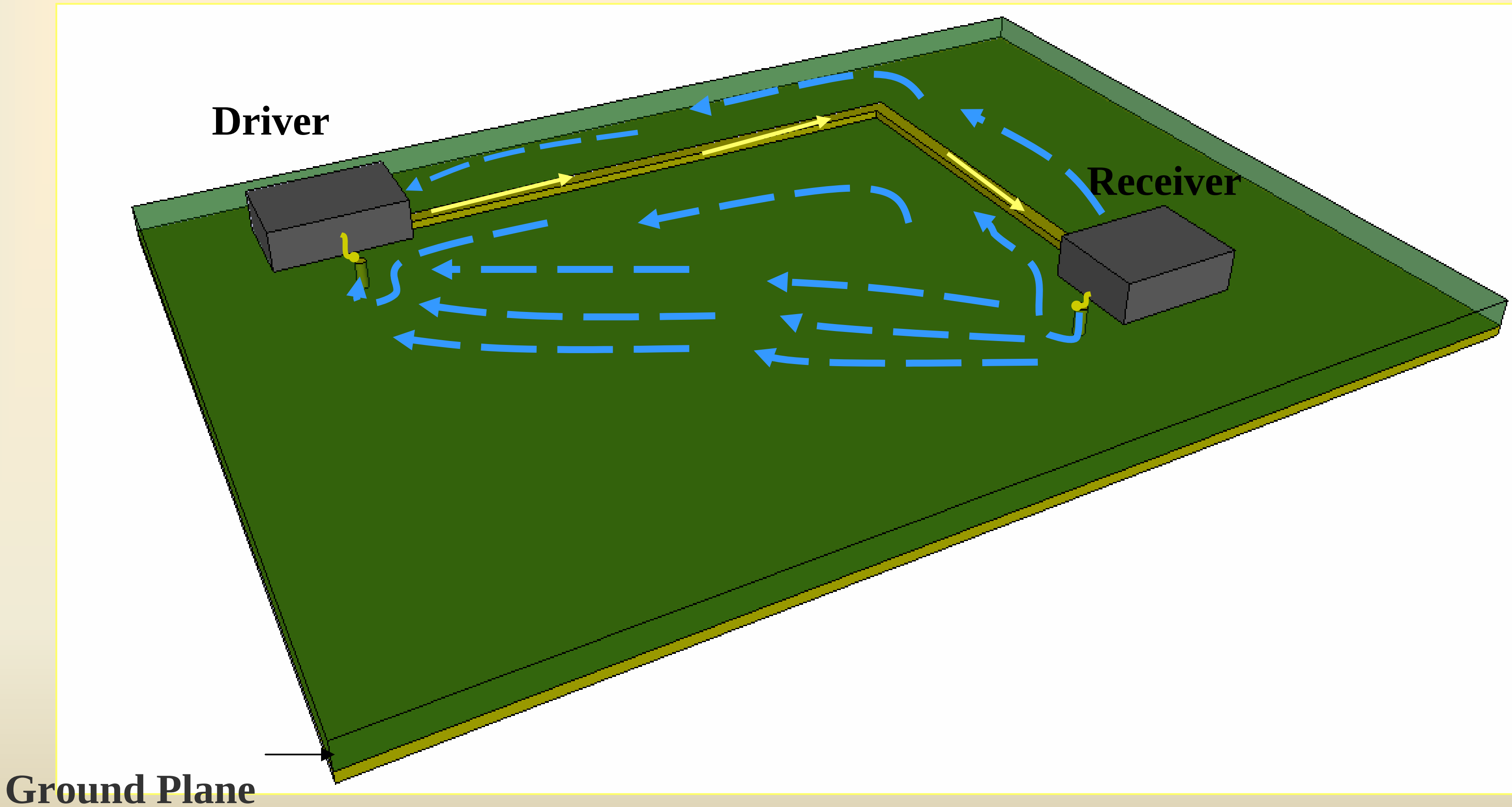
Schematic with return current shown



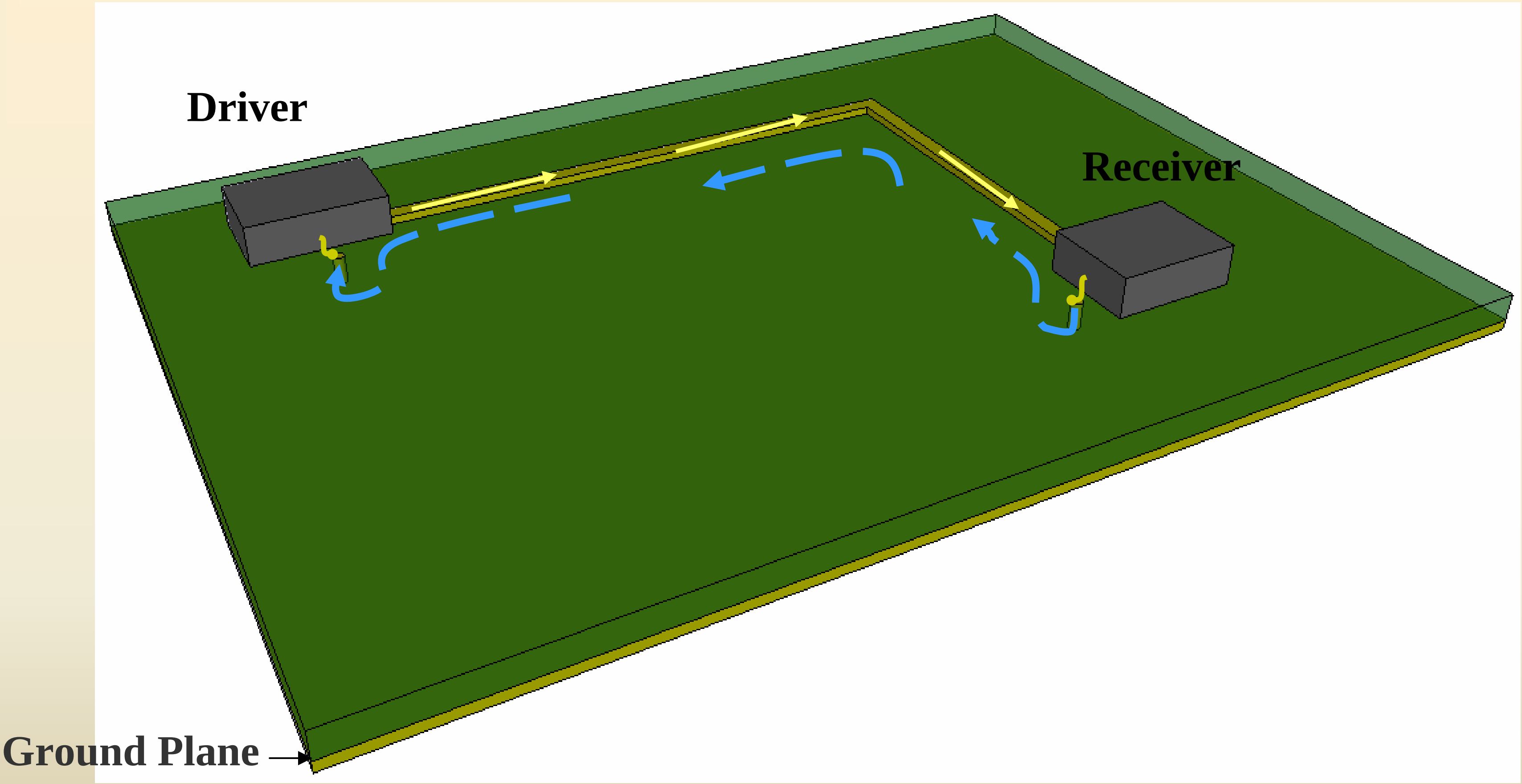
Actual Current Return is 3-Dimensional



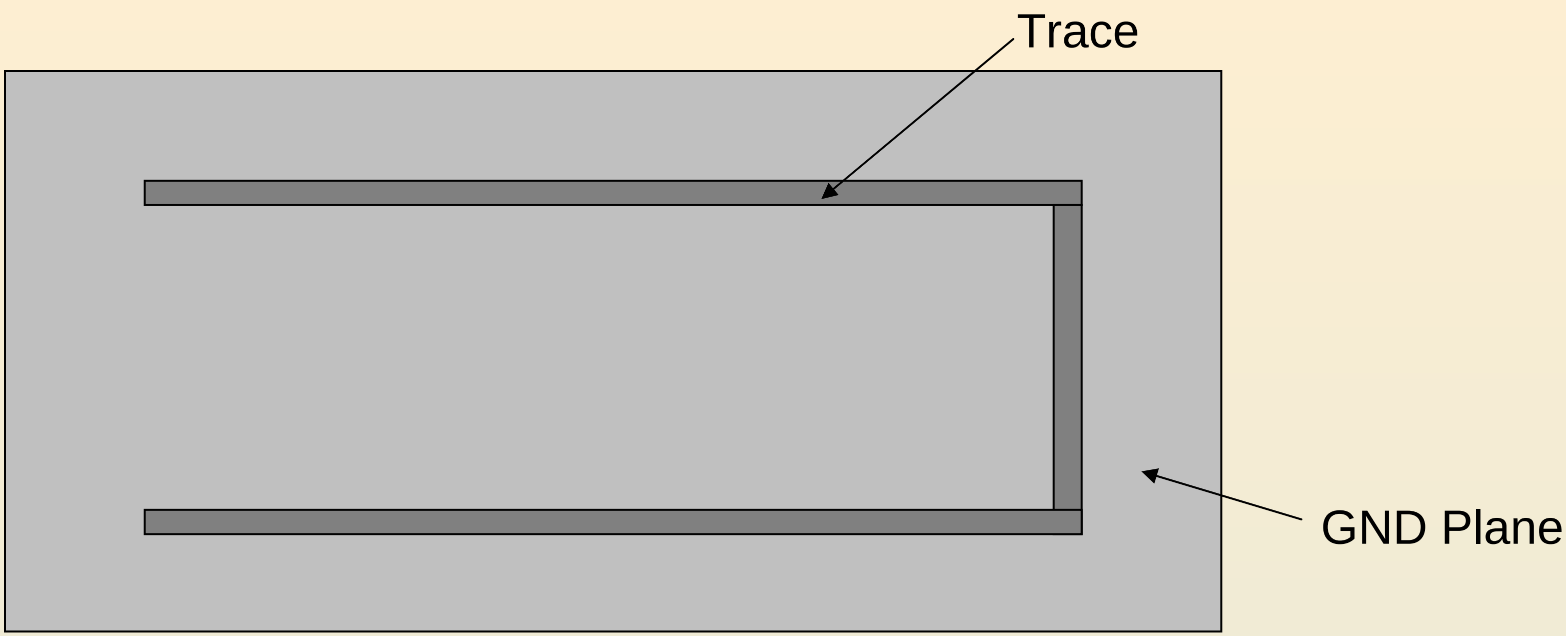
Low Frequency Return Currents Take Path of Least ***Resistance***



High Frequency Return Currents Take Path of Least ***<u>Inductance</u>***



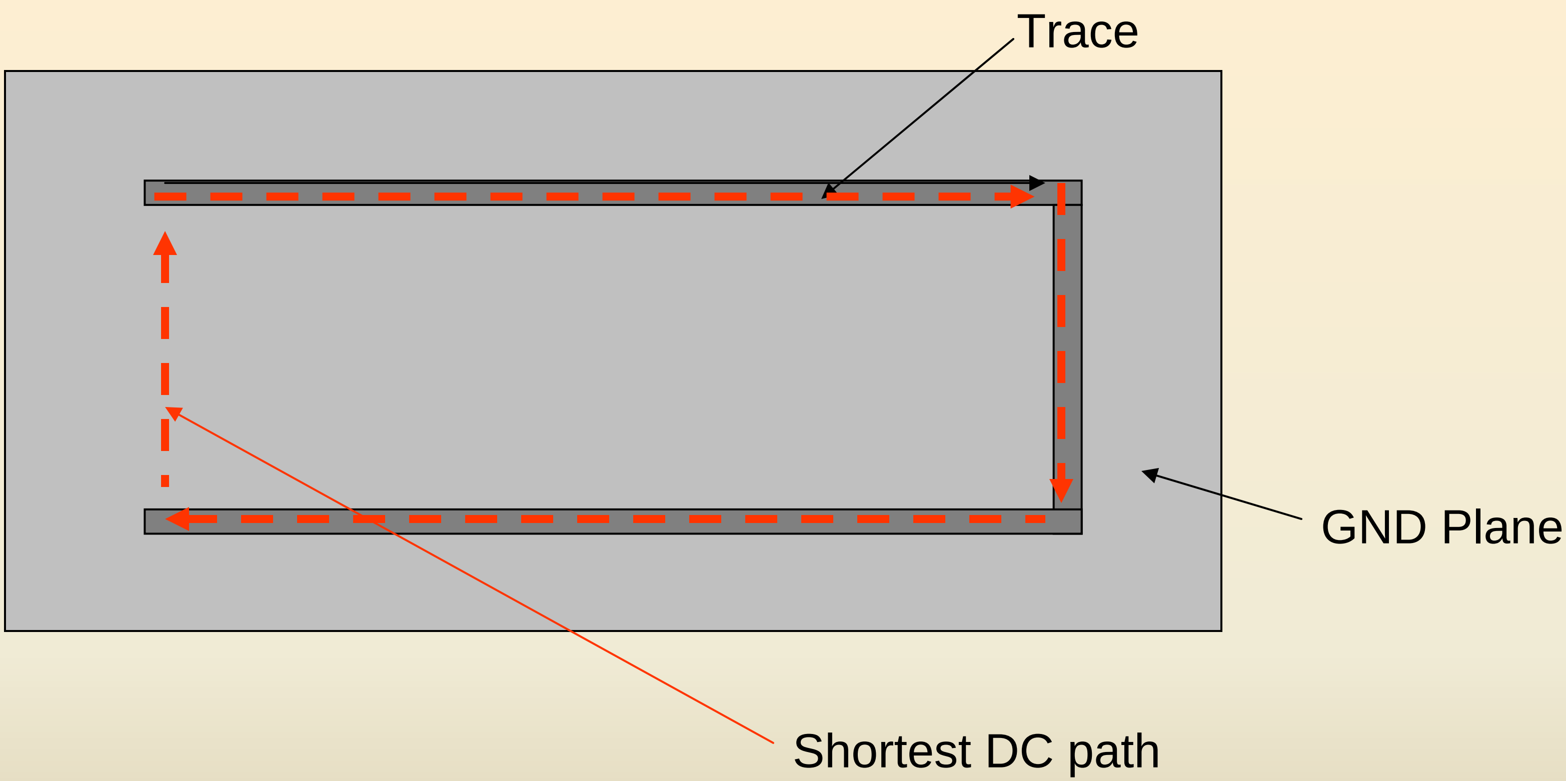
PCB Example for Return Current Impedance



22” trace

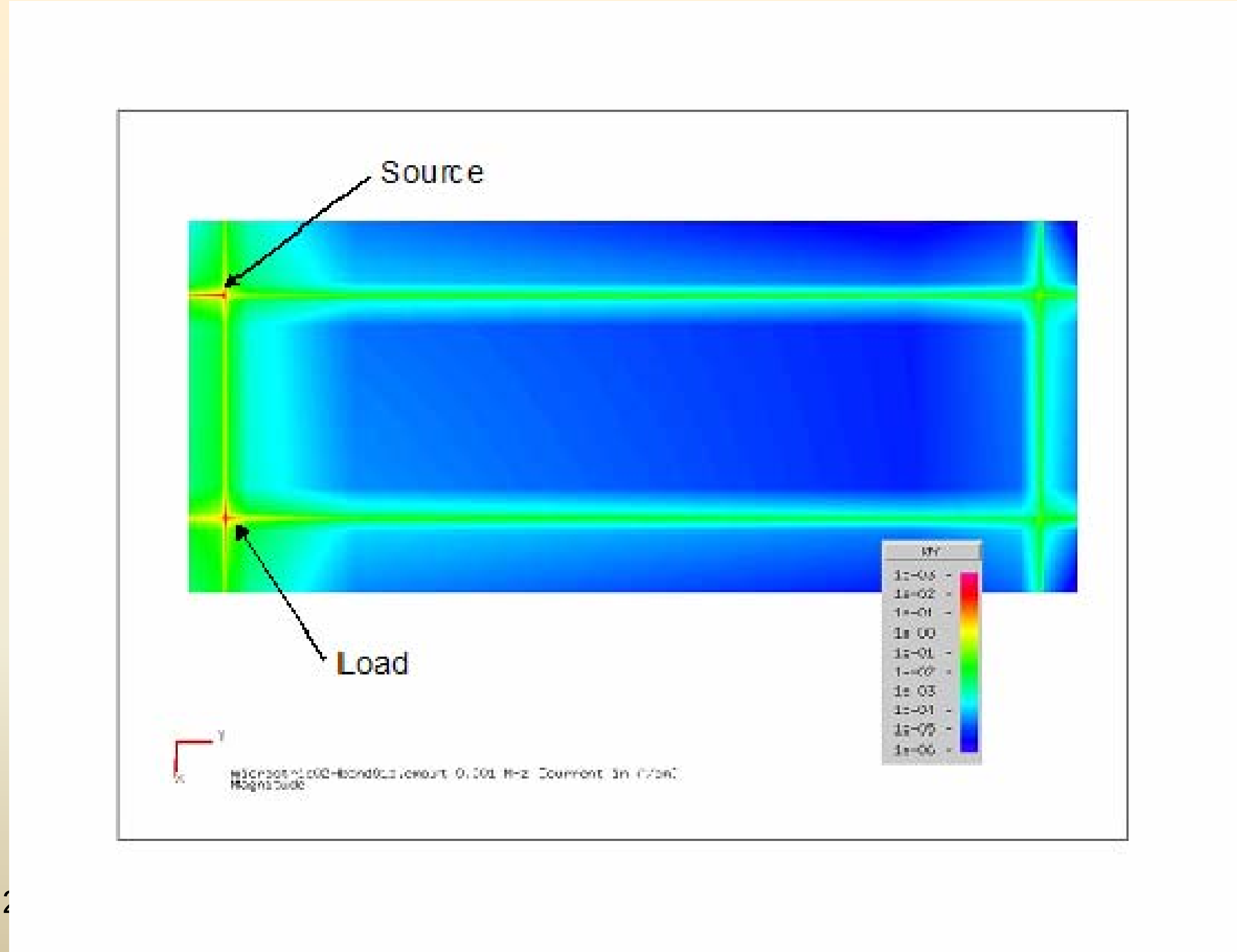
10 mils wide, 1 mil thick, 10 mils above GND plane

PCB Example for Return Current Impedance

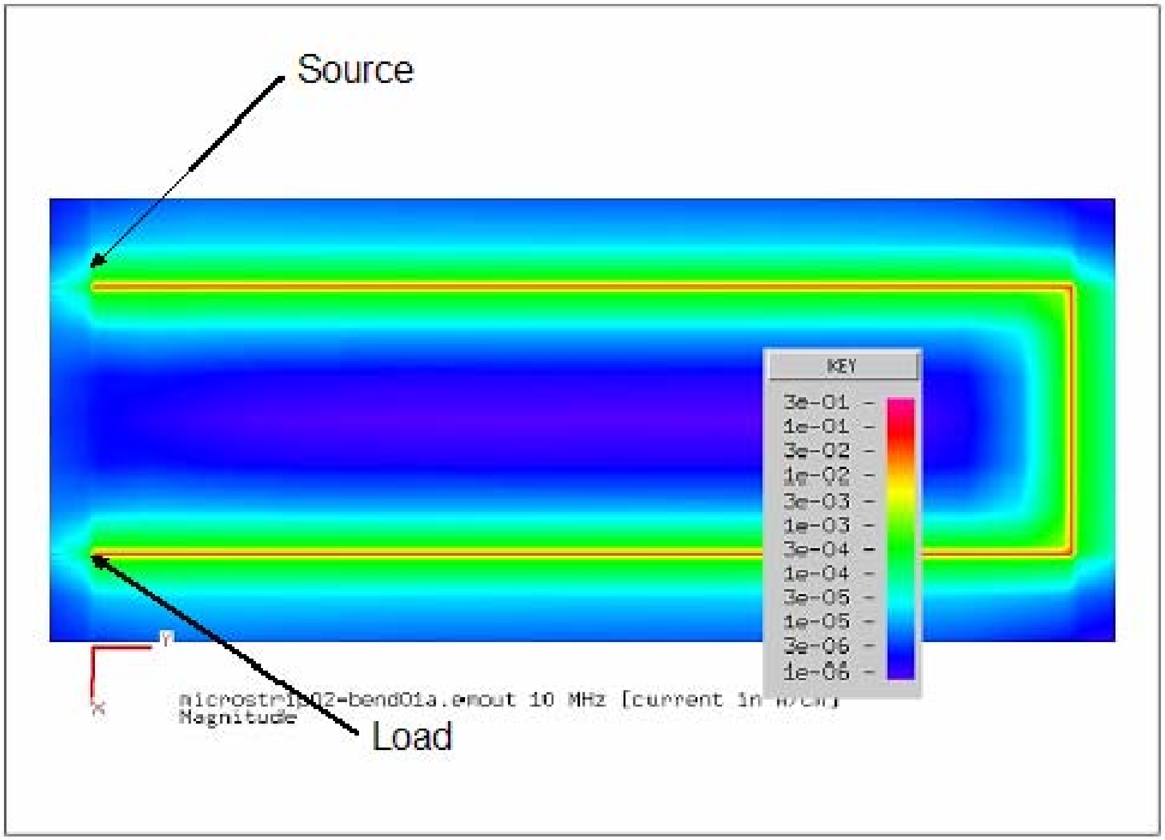


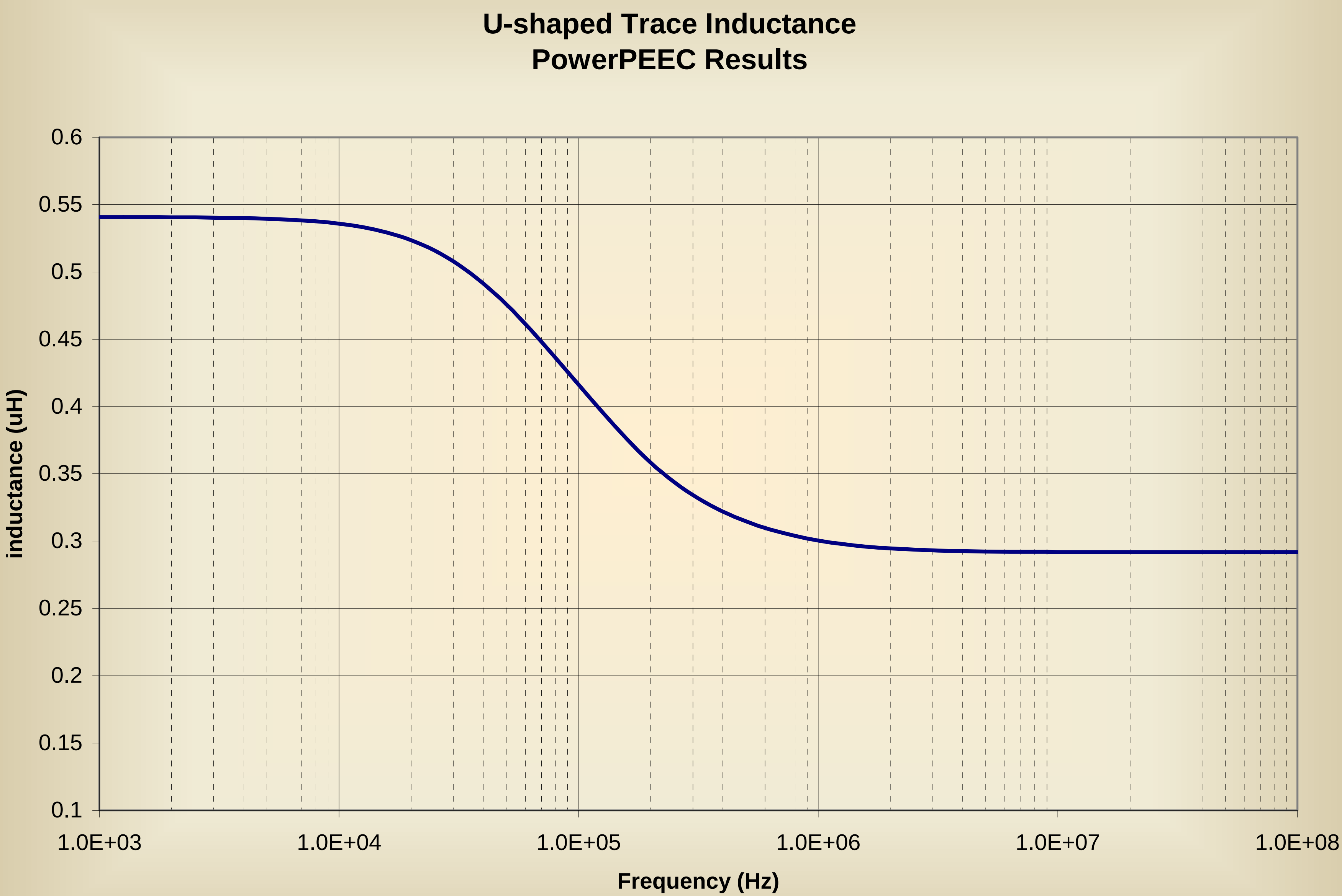
For longest DC path, current returns under trace

MoM Results for Current Density Frequency = 1 KHz

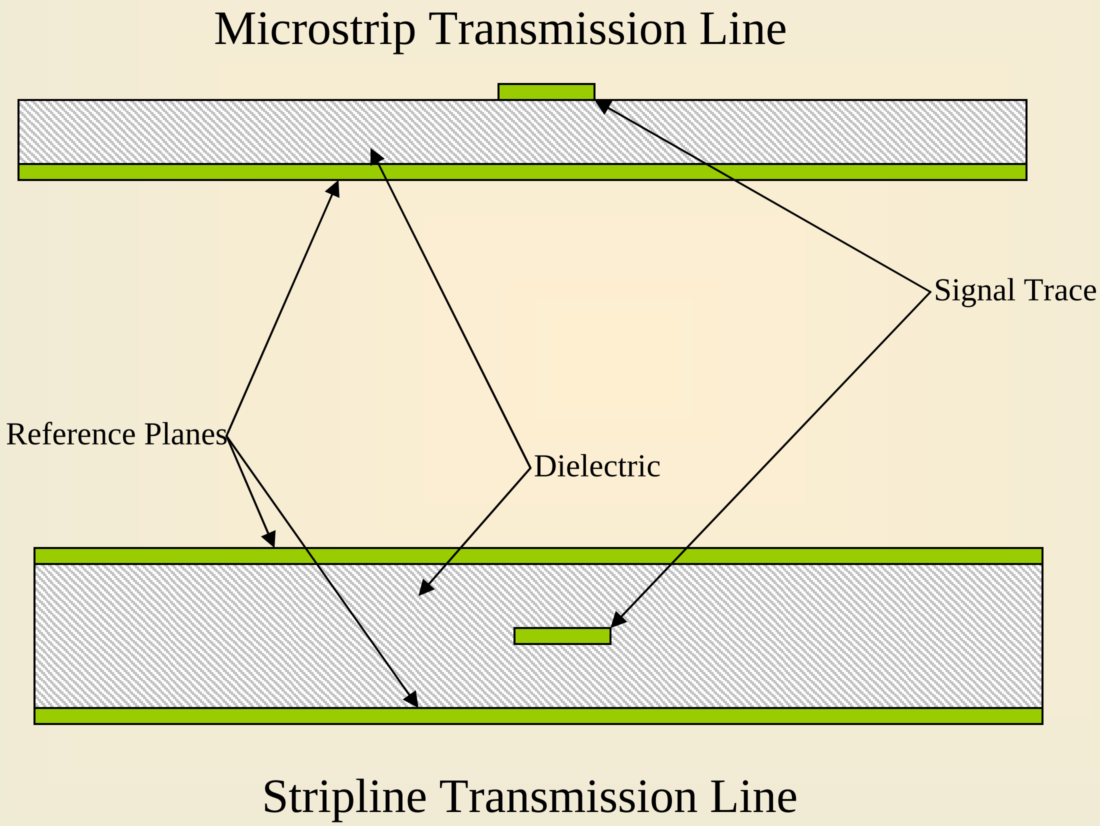


MoM Results for Current Density Frequency = 1 MHz

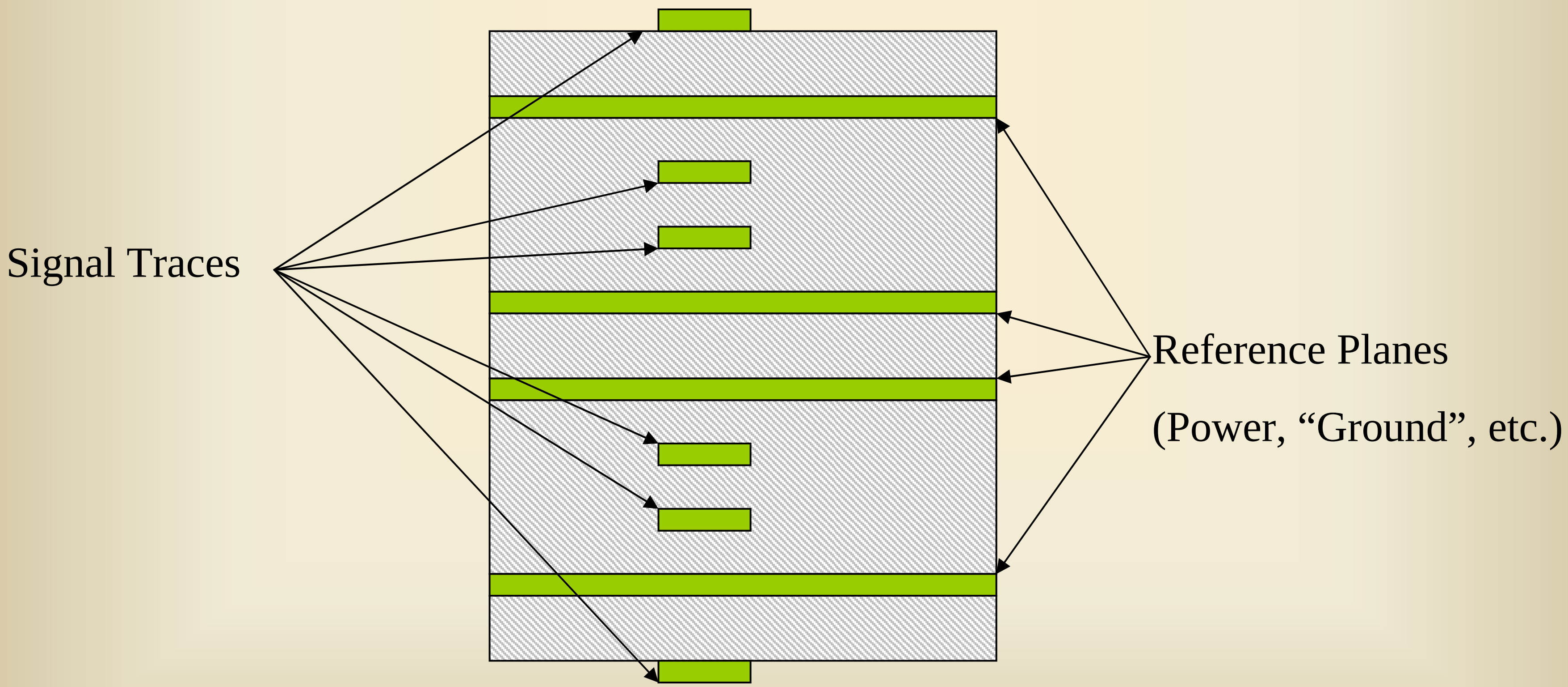



U-shaped Trace Inductance
PowerPEEC Results
inductance (uH)
0.6
0.55
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
1.0E+03
1.0E+04
1.0E+05
1.0E+06
1.0E+07
1.0E+08
Frequency (Hz)

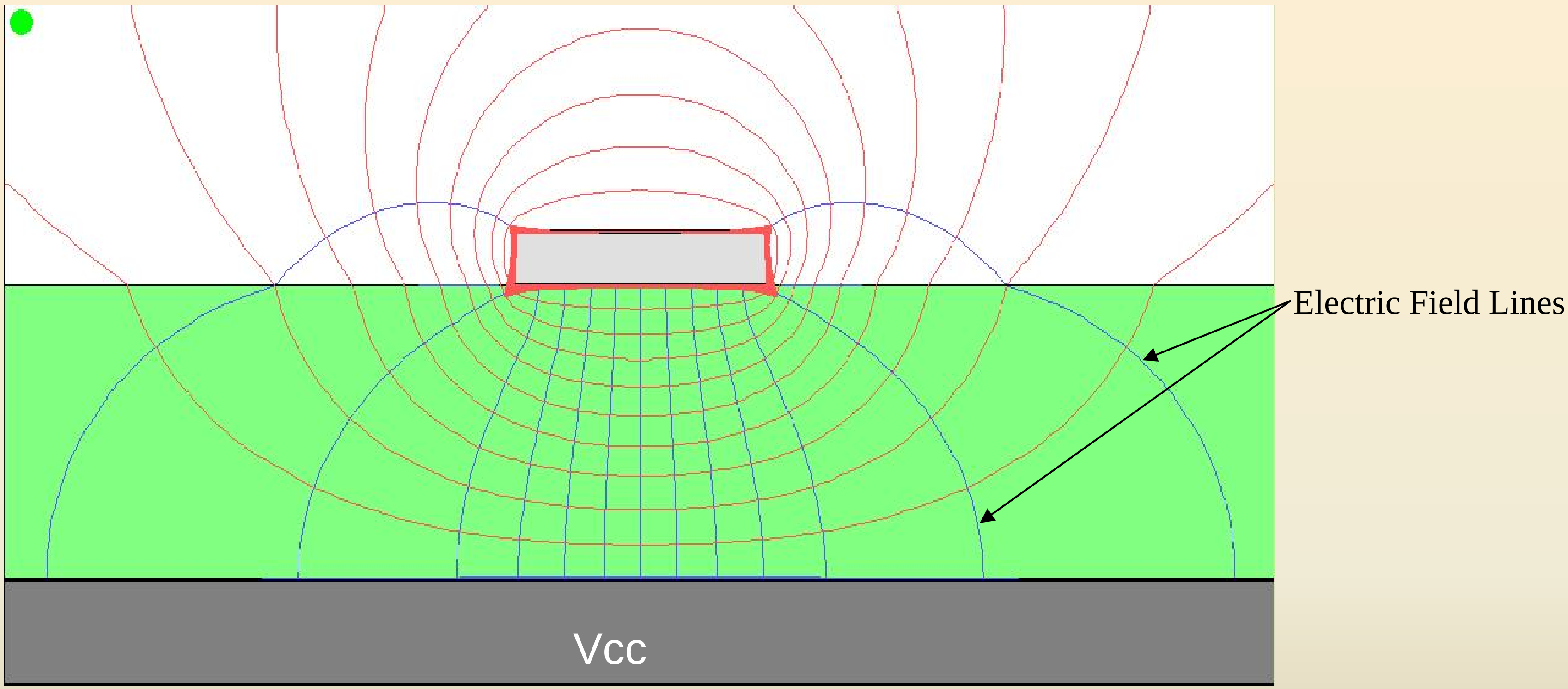
Traces/nets over a Reference Plane



Traces/nets and Reference Planes in Many Layer Board Stackup



Microstrip Electric/Magnetic Field Lines
(8mil wide trace, 8 mils above plane, 65 ohm)

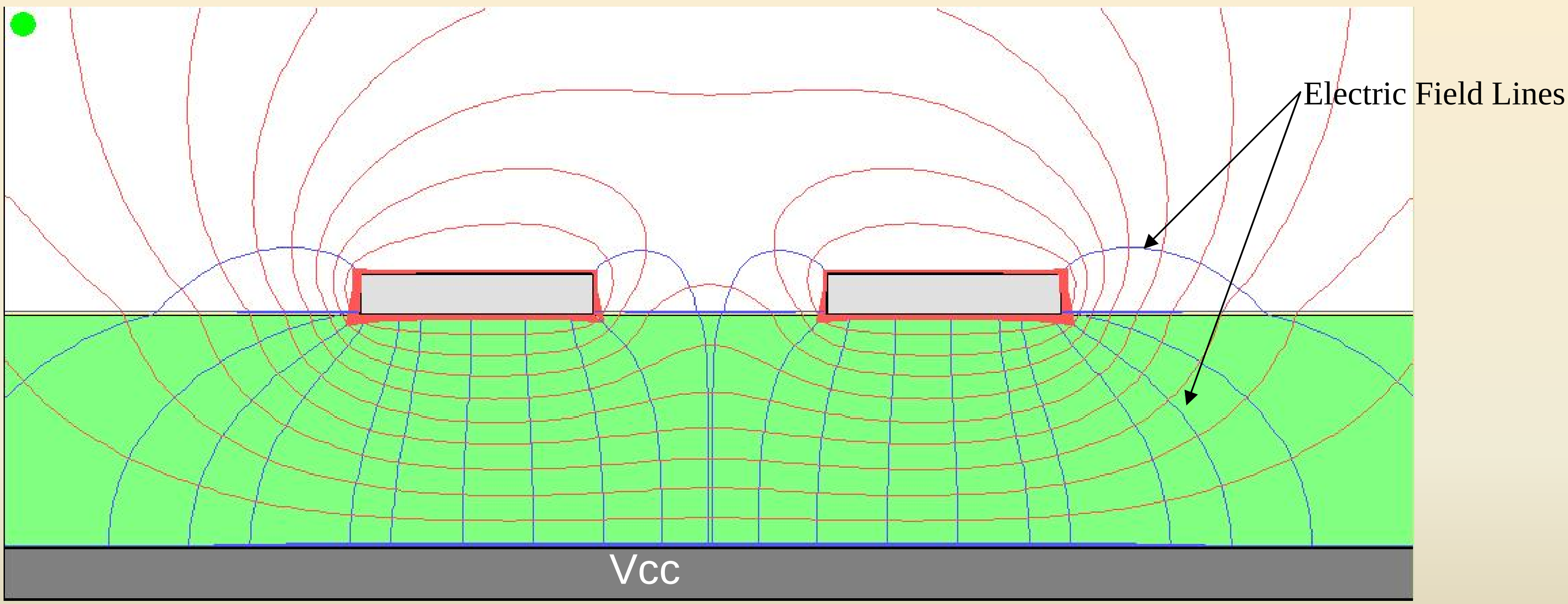


Courtesy of Hyperlynx

Microstrip Electric/Magnetic Field Lines

Common Mode

8 mil wide trace, 8 mils above plane, 65/115 ohm)

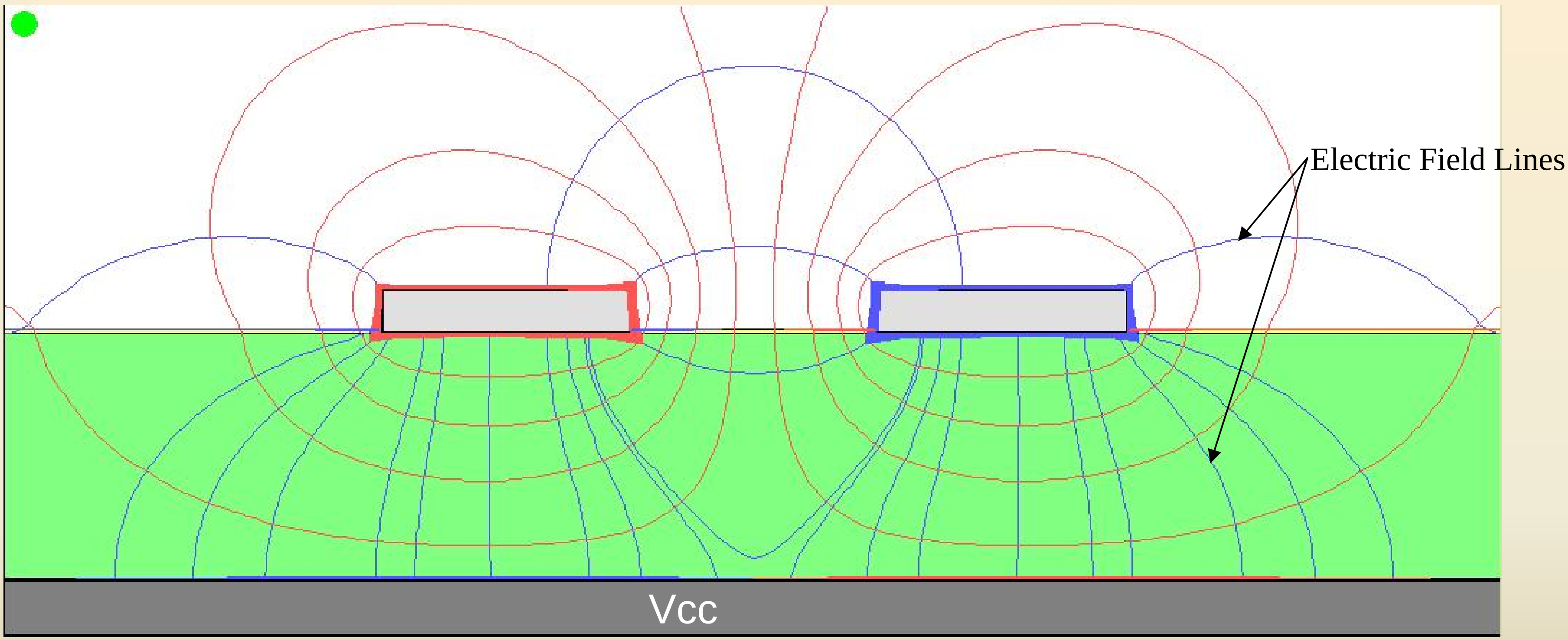


Courtesy of Hyperlynx

Microstrip Electric/Magnetic Field Lines

Differential Mode

8 mil wide trace, 8 mils above plane, 65/115 ohm)



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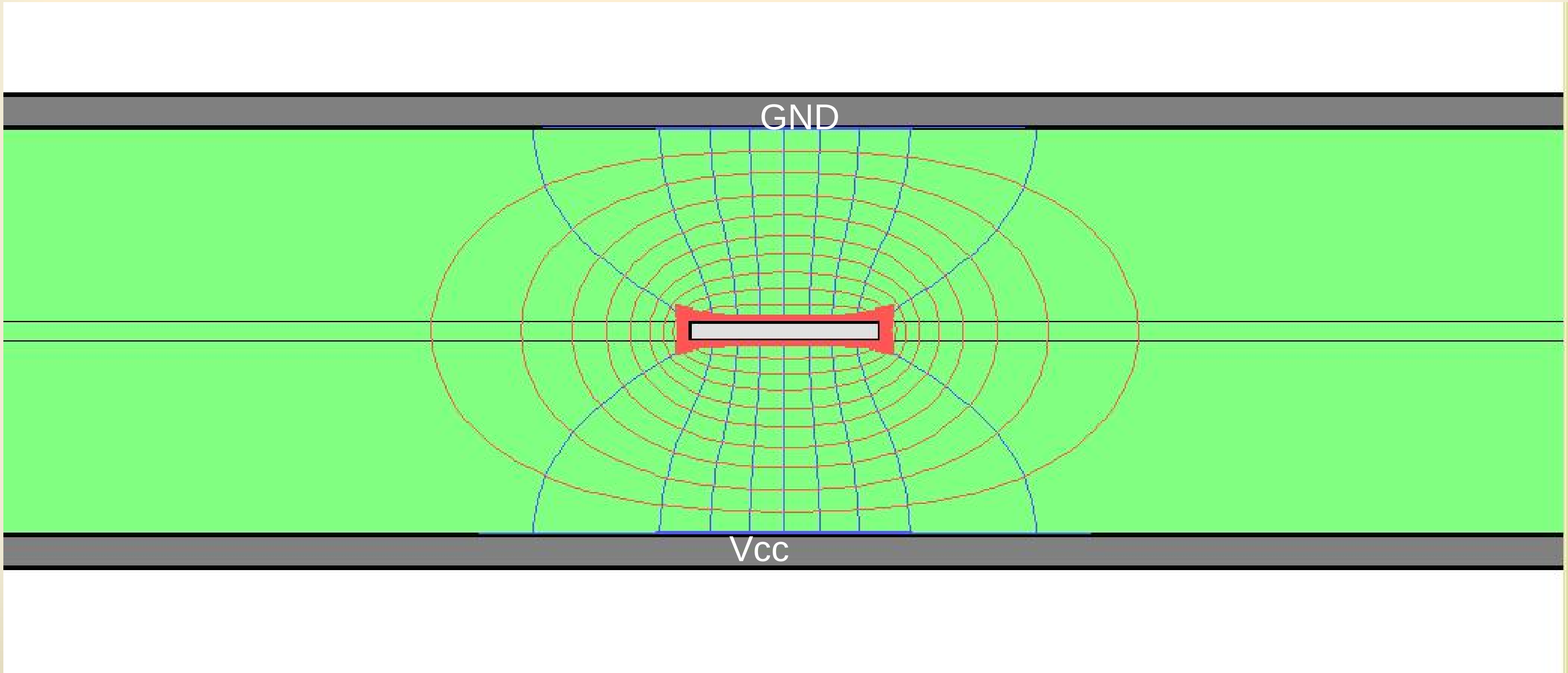
Electric/Magnetic Field Lines
Symmetrical Stripline



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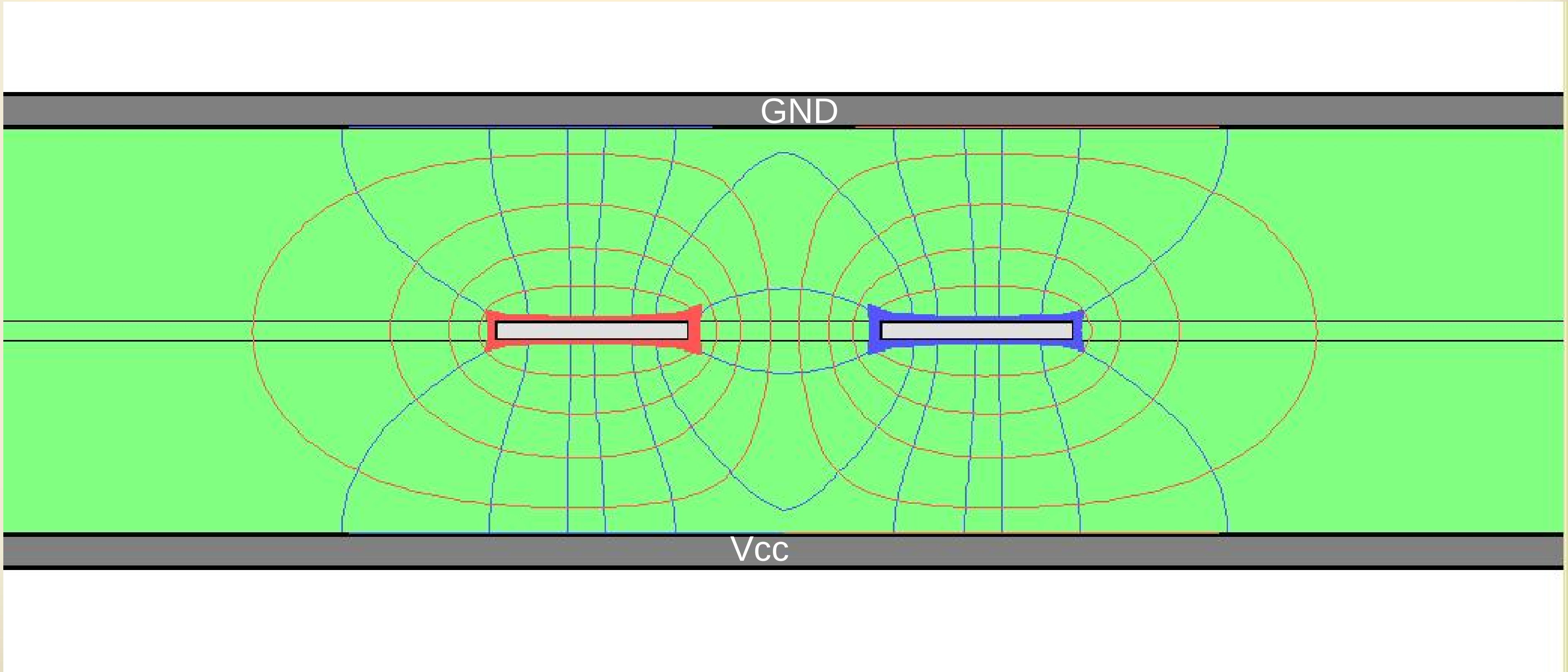
Electric/Magnetic Field Lines
Symmetrical Stripline (Differential)



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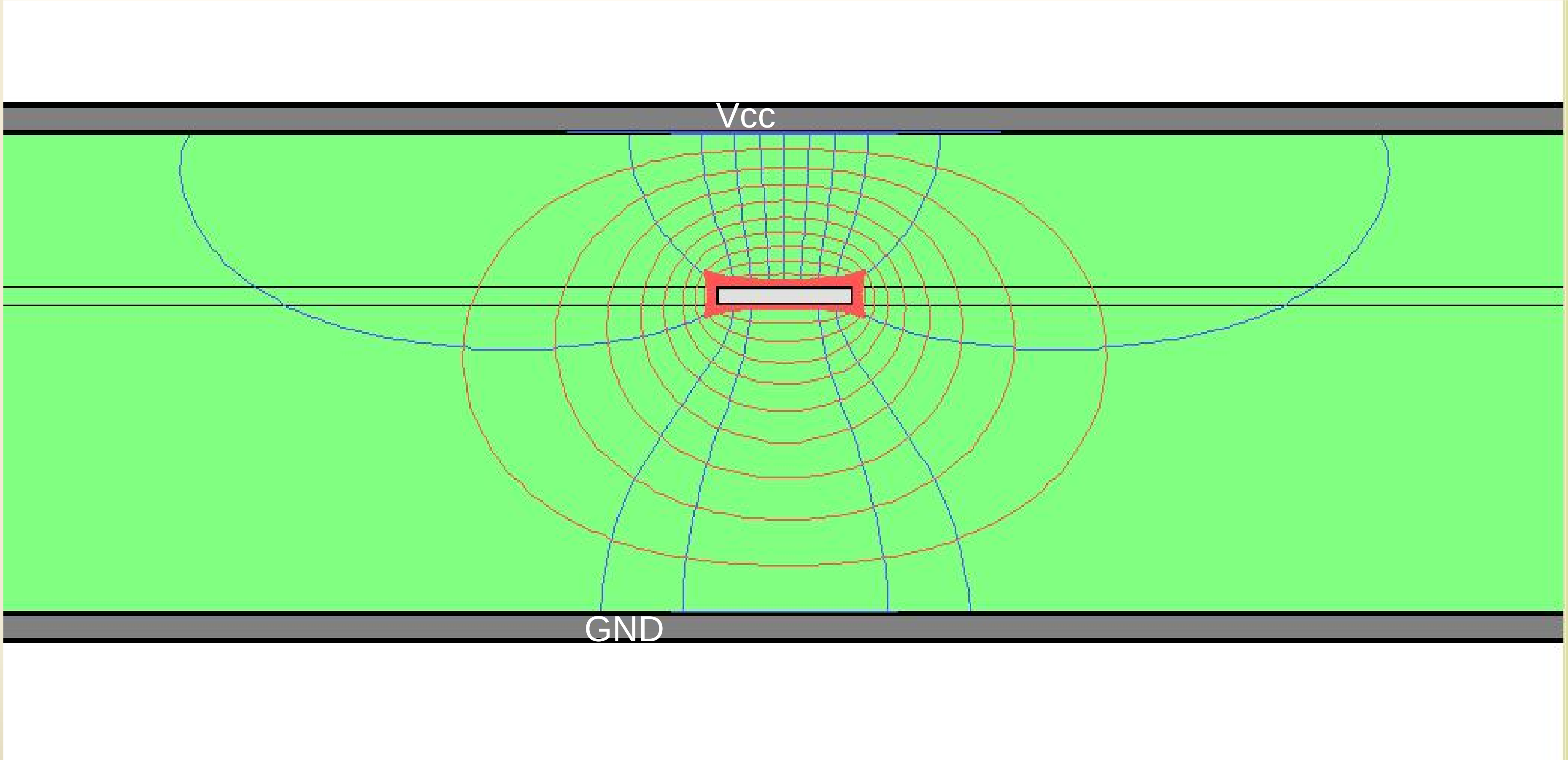
Electric/Magnetic Field Lines

Asymmetrical Stripline



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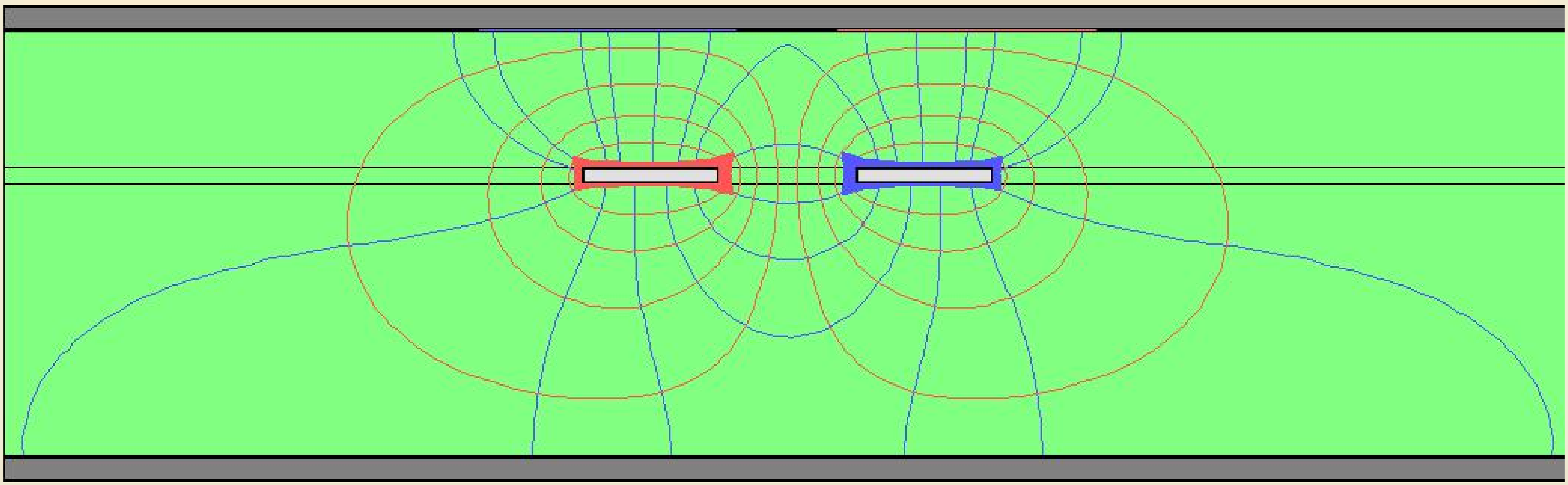
Electric/Magnetic Field Lines

Asymmetrical Stripline (Differential)



Courtesy of Hyperlynx

What About Pseudo-Differential Nets?

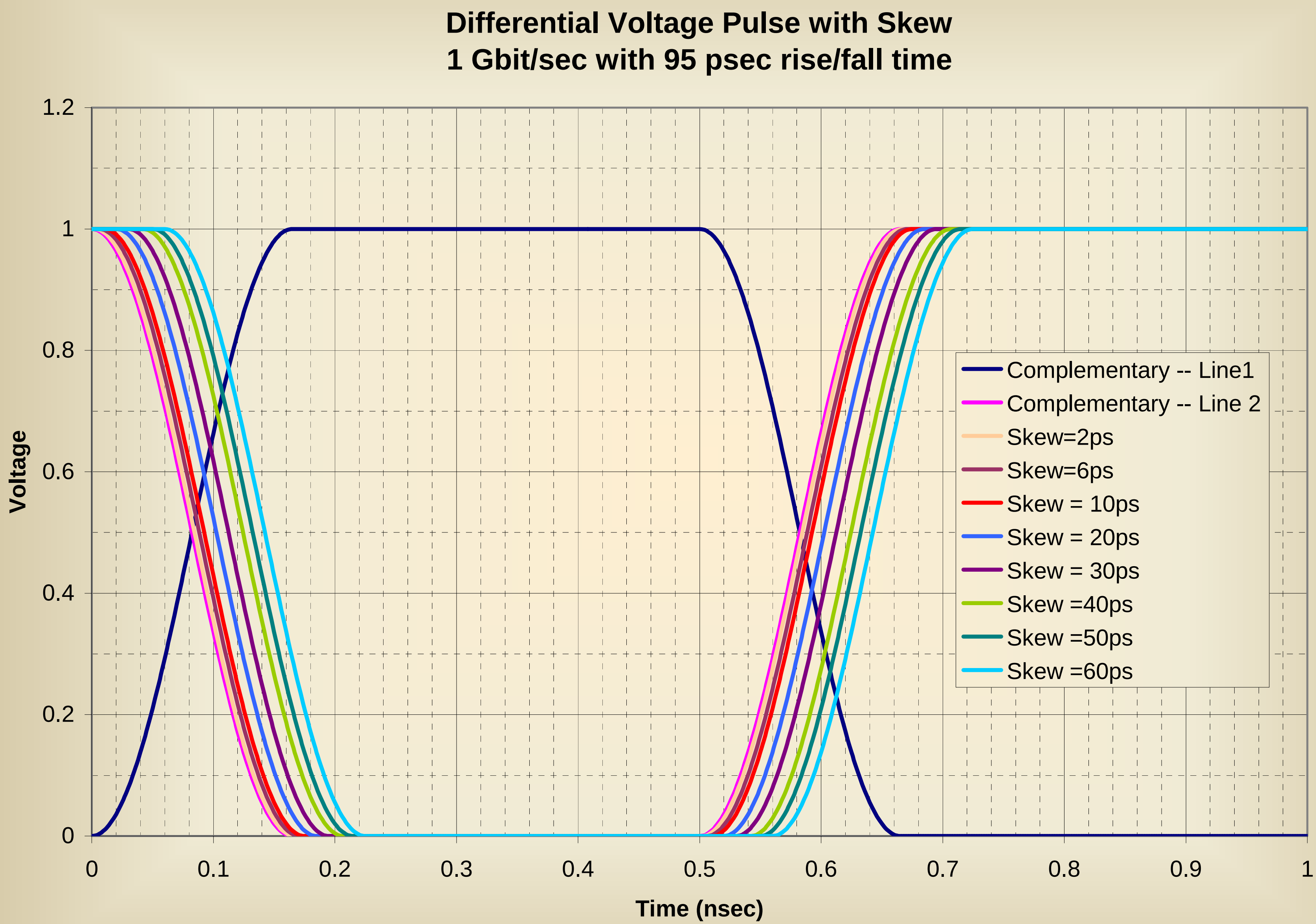
- So-called differential traces are NOT truly differential
  - Two complementary single-ended drivers
    - Relative to ‘ground’
  - Receiver is differential
    - Senses difference between two nets (independent of ‘ground’)
    - Provides good immunity to common mode noise
    - Good for signal quality/integrity

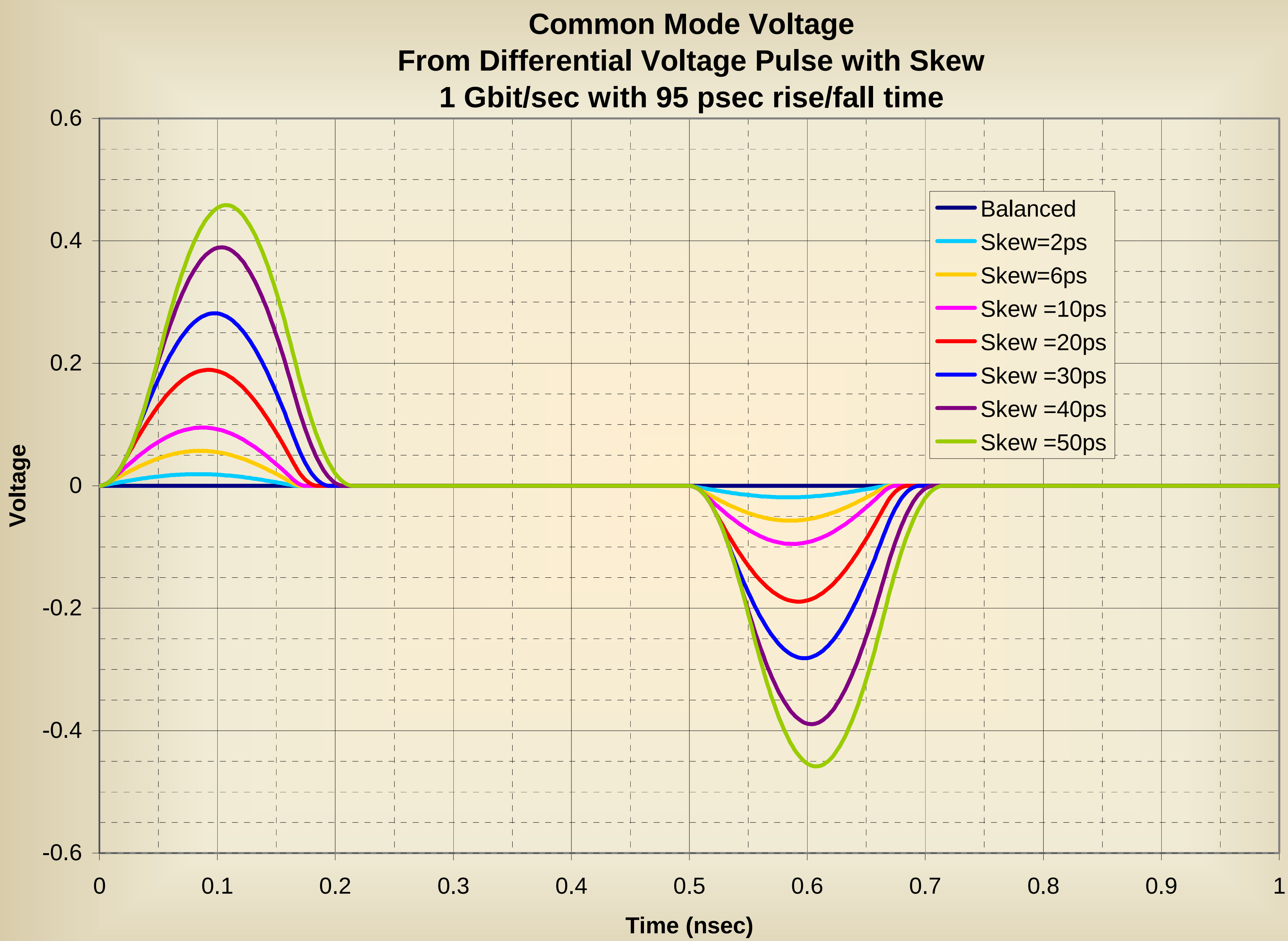
Pseudo-Differential Nets Current in Nearby Plane

- Balanced/Differential currents have matching current in nearby plane
  - No issue for discontinuities
- Any unbalanced (common mode) currents have return currents in nearby plane that must return to source!
  - All normal concerns for single-ended nets apply!

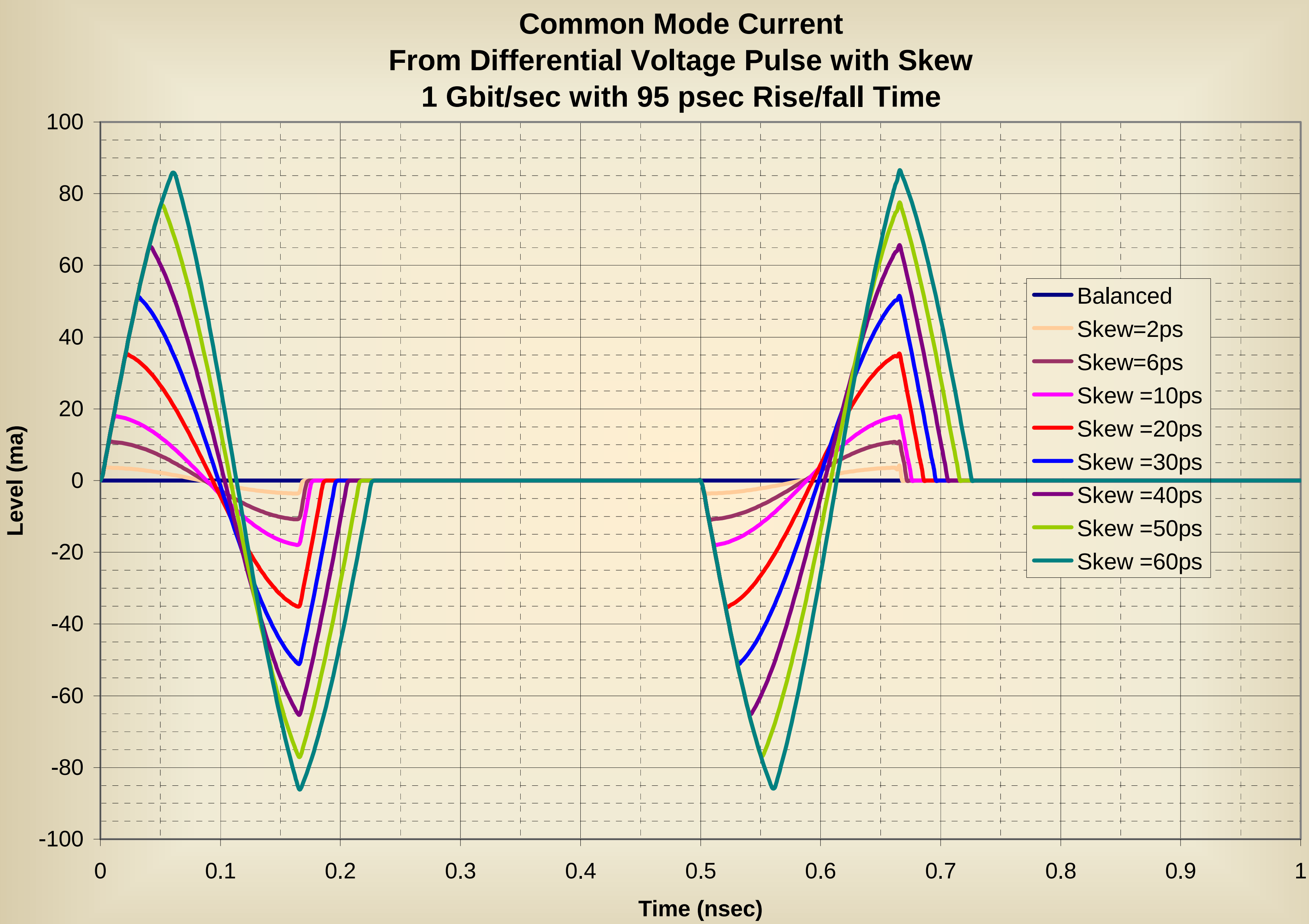
Pseudo-Differential Nets

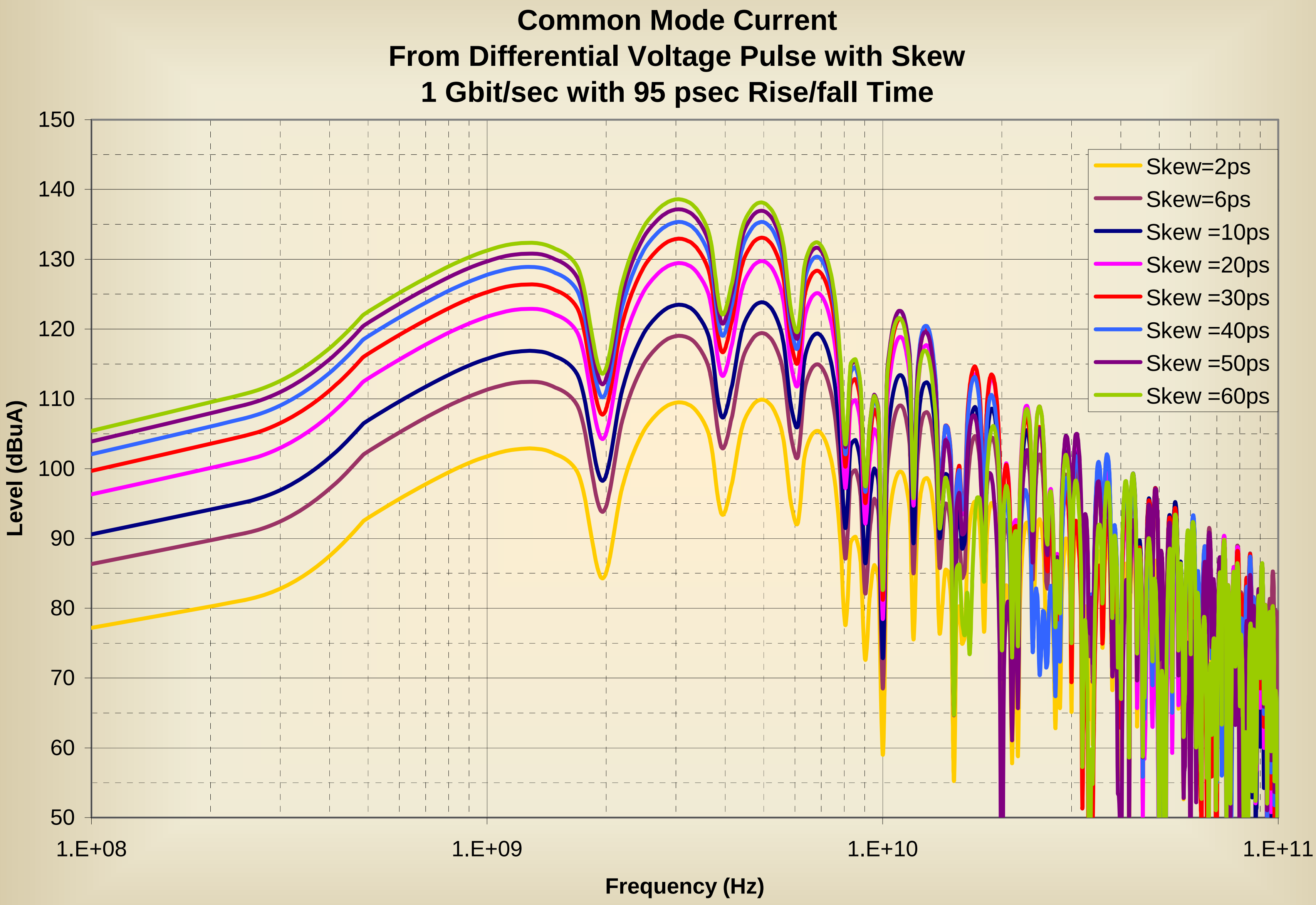
- Not really ‘differential’, since more closely coupled to nearby plane than each other
- Slew and rise/fall variation cause common mode currents!

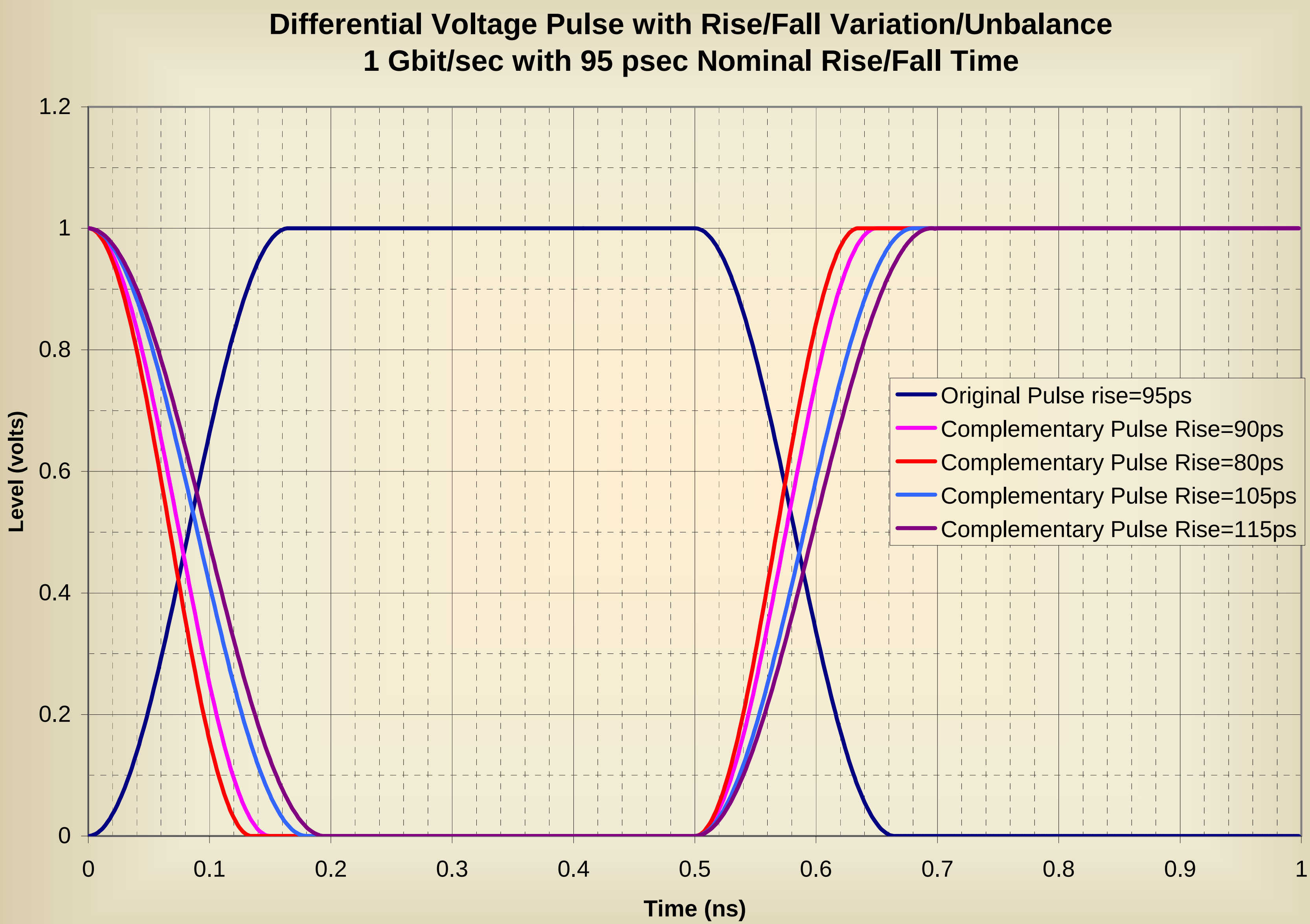

Differential Voltage Pulse with Skew
1 Gbit/sec with 95 psec rise/fall time
1.2
1
0.8
0.6
0.4
0.2
0
Voltage
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Time (nsec)
Complementary -- Line1
Complementary -- Line 2
Skew=2ps
Skew=6ps
Skew = 10ps
Skew = 20ps
Skew = 30ps
Skew =40ps
Skew =50ps
Skew =60ps

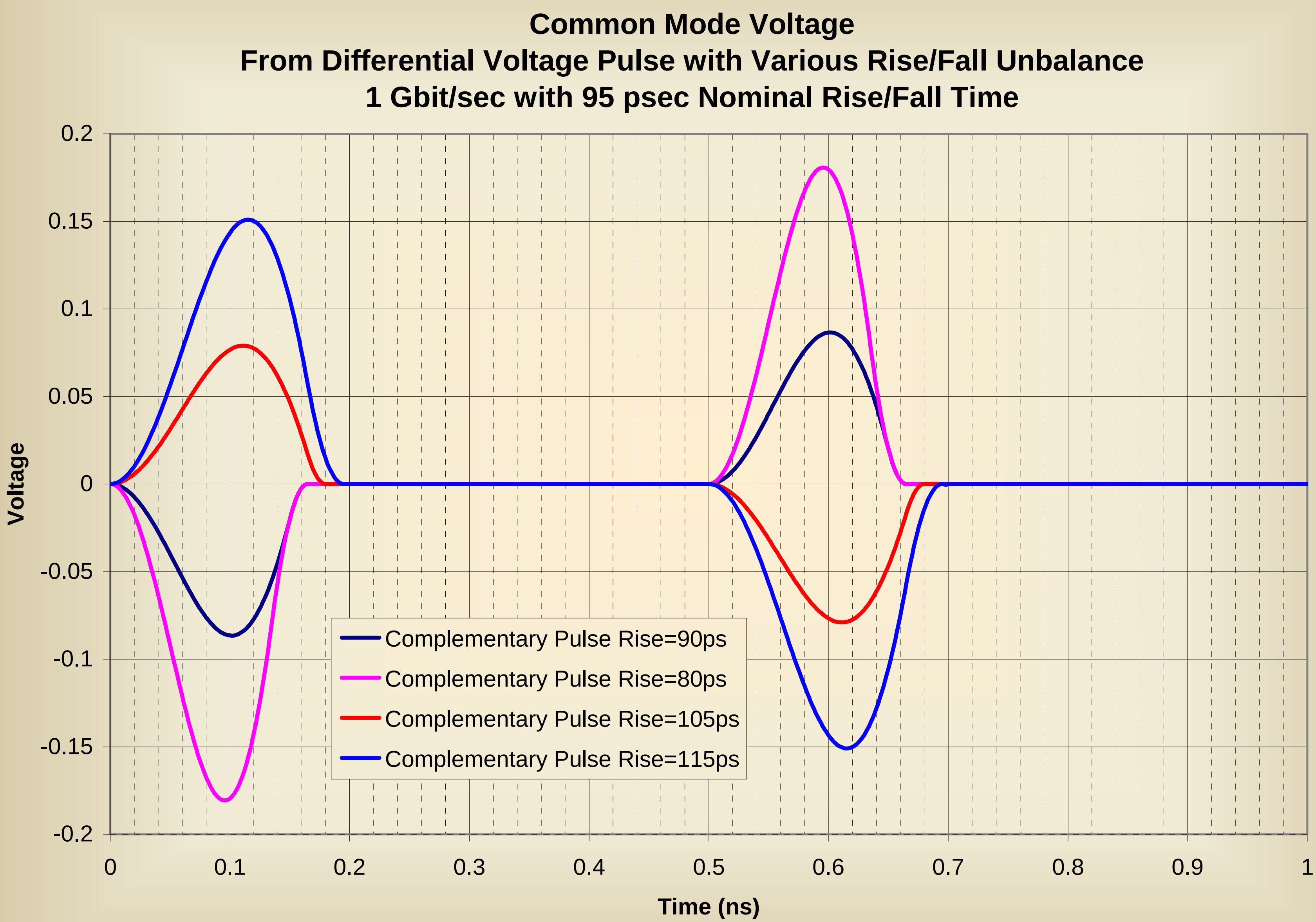


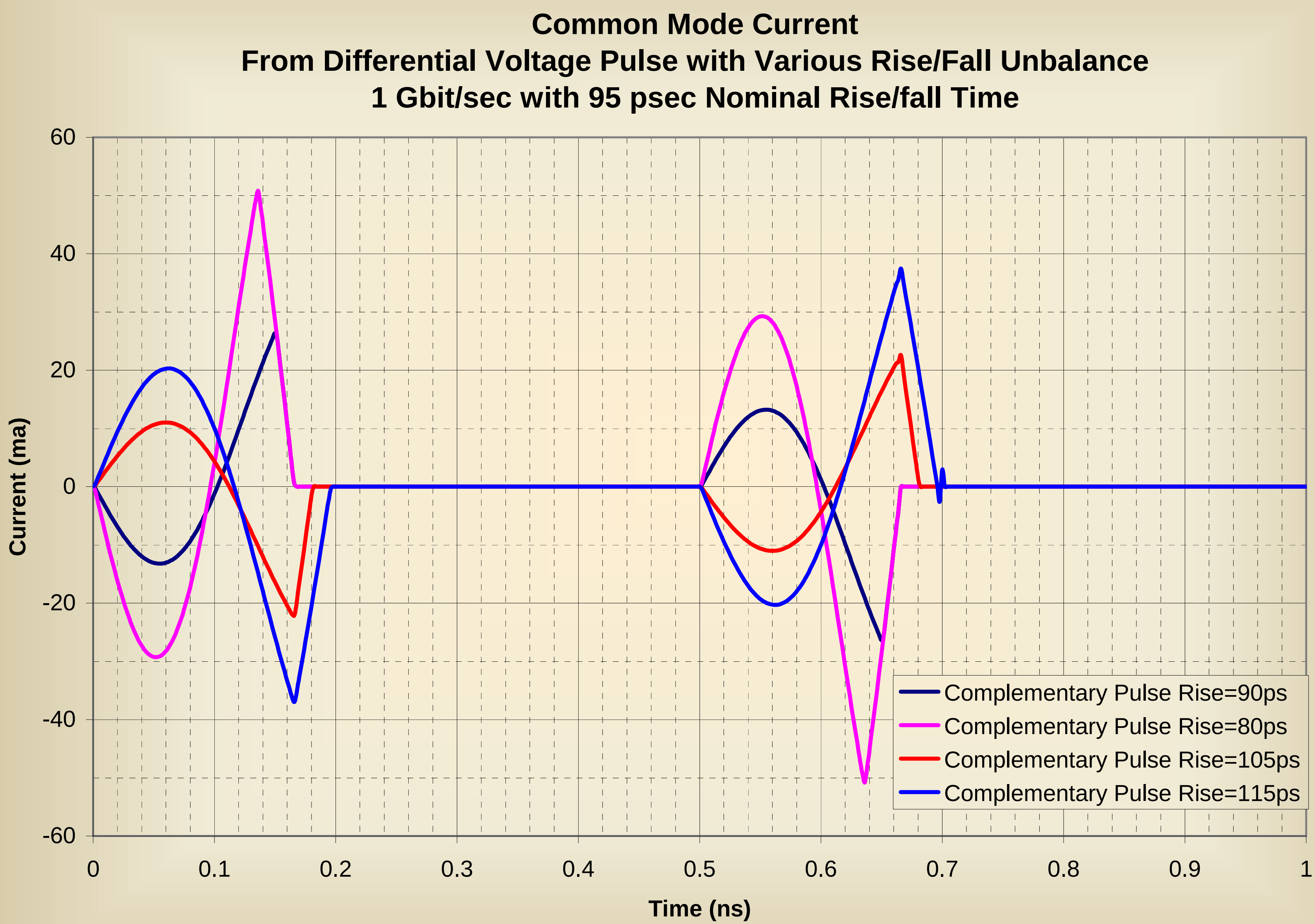
Common Mode Voltage
From Differential Voltage Pulse with Skew
1 Gbit/sec with 95 psec rise/fall time
Voltage
Time (nsec)
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Balanced
Skew=2ps
Skew=6ps
Skew =10ps
Skew =20ps
Skew =30ps
Skew =40ps
Skew =50ps


Common Mode Current
From Differential Voltage Pulse with Skew
1 Gbit/sec with 95 psec Rise/fall Time
Level (ma)
Time (nsec)
100
80
60
40
20
0
-20
-40
-60
-80
-100
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Balanced
Skew=2ps
Skew=6ps
Skew =10ps
Skew =20ps
Skew =30ps
Skew =40ps
Skew =50ps
Skew =60ps

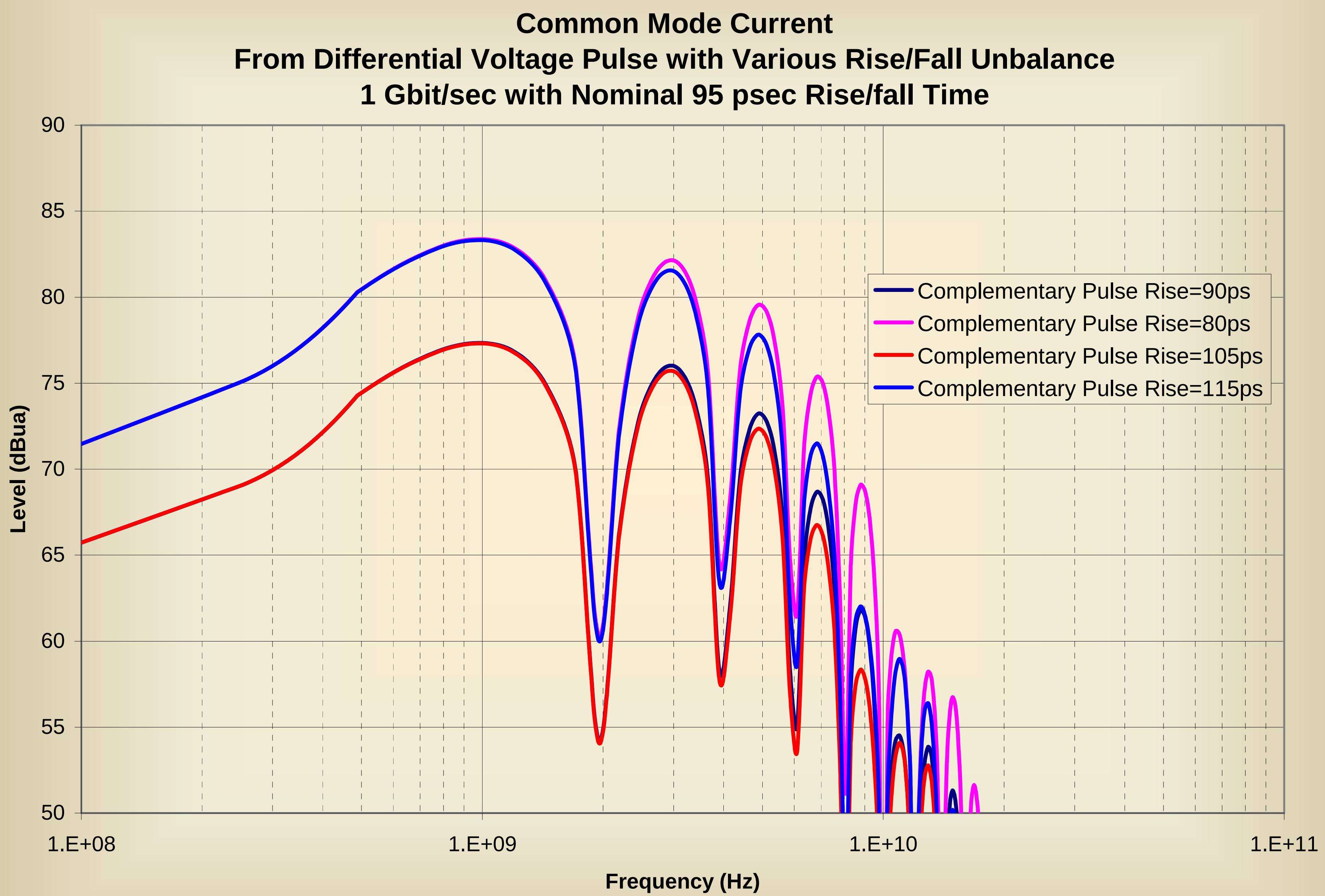

Common Mode Current
From Differential Voltage Pulse with Skew
1 Gbit/sec with 95 psec Rise/fall Time
Level (dBuA)
Frequency (Hz)
150
140
130
120
110
100
90
80
70
60
50
1.E+08
1.E+09
1.E+10
1.E+11
Skew=2ps
Skew=6ps
Skew =10ps
Skew =20ps
Skew =30ps
Skew =40ps
Skew =50ps
Skew =60ps


Differential Voltage Pulse with Rise/Fall Variation/Unbalance
1 Gbit/sec with 95 psec Nominal Rise/Fall Time
Level (volts)
Time (ns)
0
0.2
0.4
0.6
0.8
1
1.2
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Original Pulse rise=95ps
Complementary Pulse Rise=90ps
Complementary Pulse Rise=80ps
Complementary Pulse Rise=105ps
Complementary Pulse Rise=115ps


Common Mode Voltage
From Differential Voltage Pulse with Various Rise/Fall Unbalance
1 Gbit/sec with 95 psec Nominal Rise/Fall Time
Voltage
Time (ns)
0.2
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-0.2
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Complementary Pulse Rise=90ps
Complementary Pulse Rise=80ps
Complementary Pulse Rise=105ps
Complementary Pulse Rise=115ps

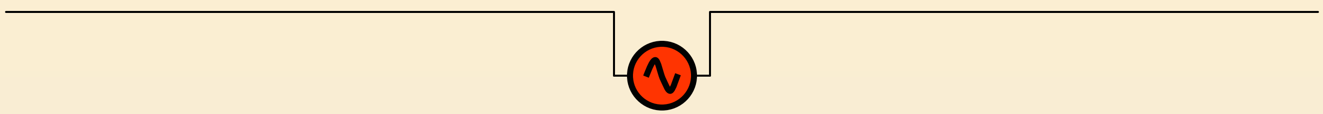


Common Mode Current
From Differential Voltage Pulse with Various Rise/Fall Unbalance
1 Gbit/sec with 95 psec Nominal Rise/fall Time
60
40
20
0
-20
-40
-60
Current (ma)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Time (ns)
Complementary Pulse Rise=90ps
Complementary Pulse Rise=80ps
Complementary Pulse Rise=105ps
Complementary Pulse Rise=115ps

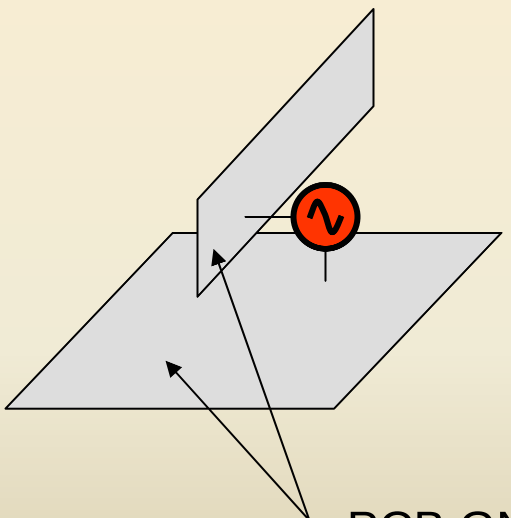

Common Mode Current
From Differential Voltage Pulse with Various Rise/Fall Unbalance
1 Gbit/sec with Nominal 95 psec Rise/fall Time
90
85
80
75
70
65
60
55
50
Level (dBua)
1.E+08
1.E+09
1.E+10
1.E+11
Frequency (Hz)
Complementary Pulse Rise=90ps
Complementary Pulse Rise=80ps
Complementary Pulse Rise=105ps
Complementary Pulse Rise=115ps

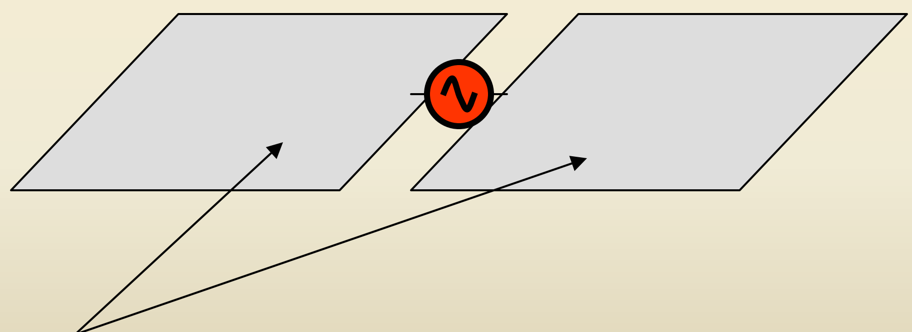
Antenna Structures

Dipole antenna



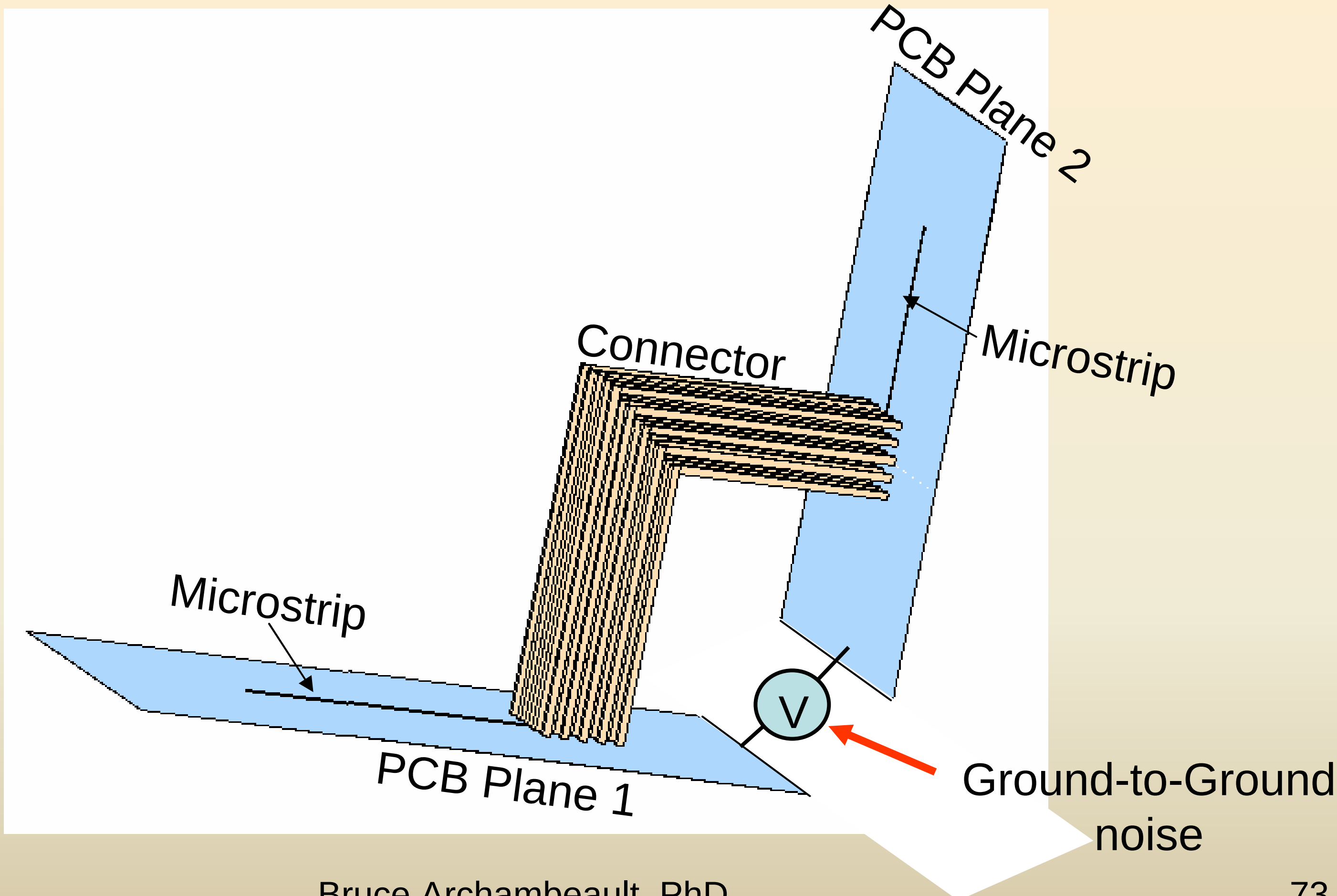
Non-Dipole antenna



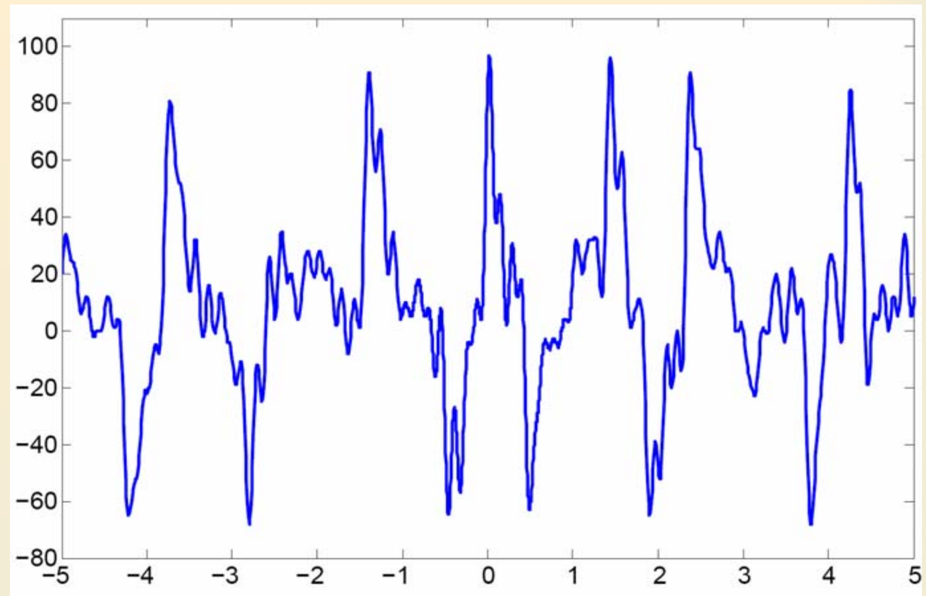


PCB GND planes

Board-to-Board Differential Pair Issues



Example Measured Differential Individual Signal-to-GND

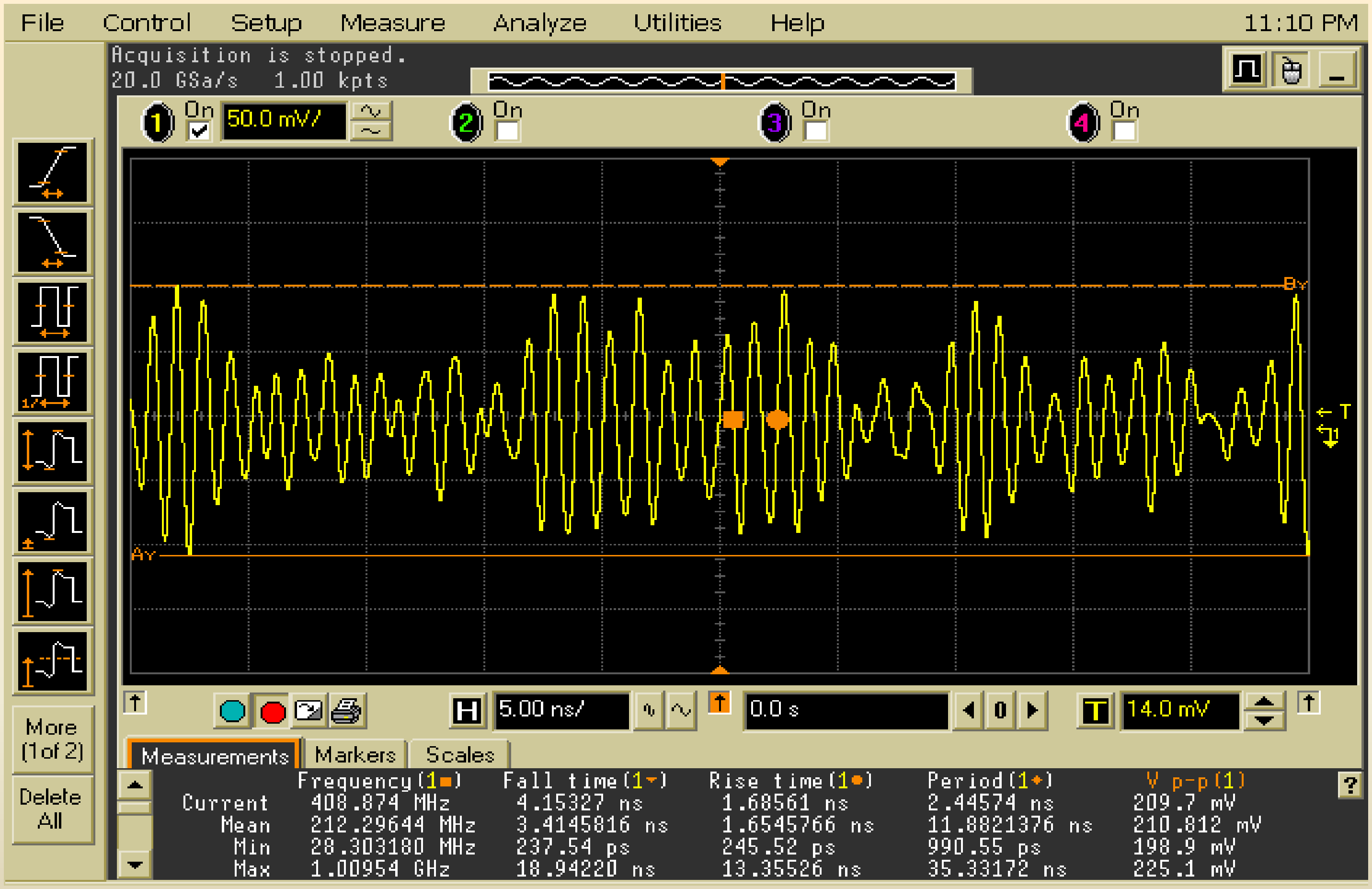


500 mV P-P (each)

Individual Differential Signals ADDED

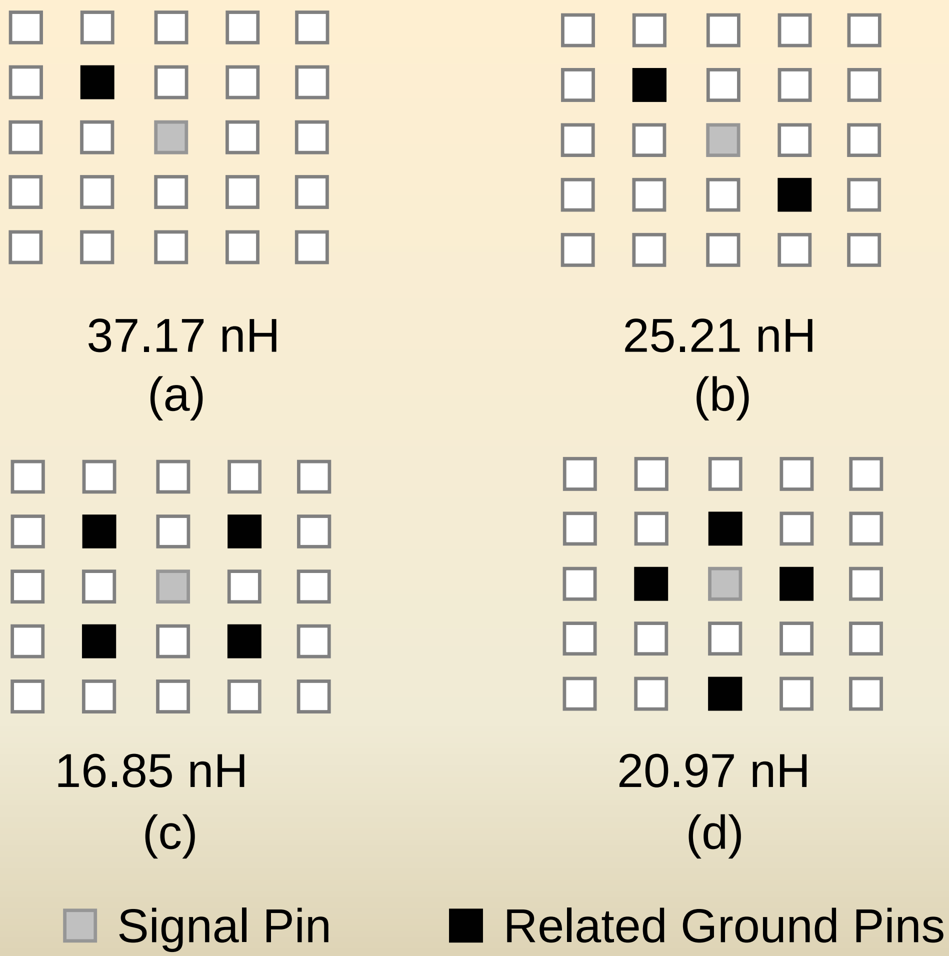
Common Mode Noise 170 mV P-P

Measured GND-to-GND Voltage

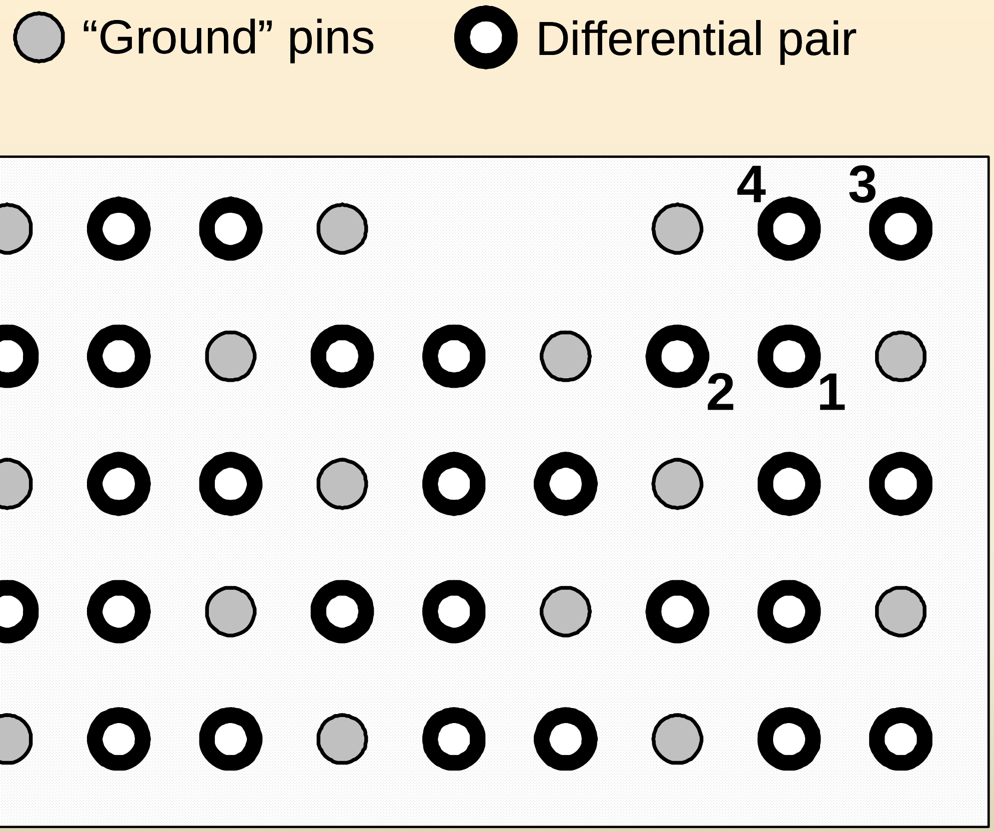


205 mV P-P

Pin Assignment Controls Inductance for CM signals



Different pins within Same Pair may have Different Loop Inductance for CM



pin 1 -- 26.6nH

pin 2 -- 23.6nH

pin 3 -- 31.8nH

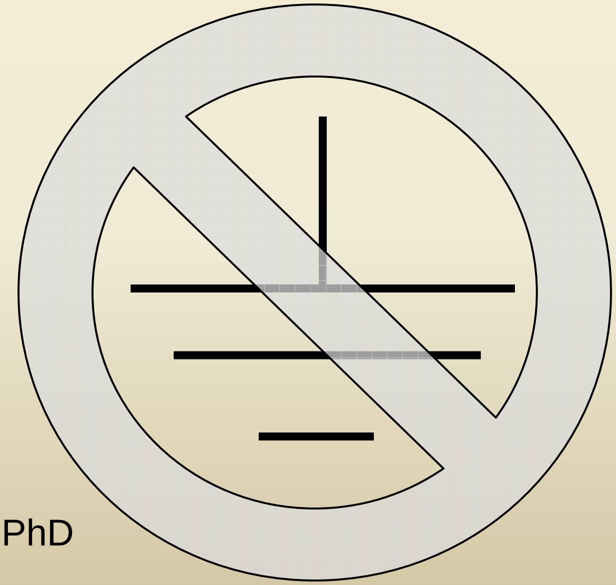
pin 4 -- 28.8nH

Pseudo-Differential Net Summary

- Small amounts of skew can cause significant common mode current
- Small amount of rise/fall time deviation can cause significant amount of common mode current
- Discontinuities (vias, crossing split planes, etc) and convert significant amount of differential current into common mode current

Return Current vs. “Ground”

- For high frequency signals, “Ground” is a concept that does not exist
- The important question is “where does the <u>*return current*</u> flow?”



Referencing Nets
(Where does the Return Current Flow??)

- Microstrip/Stripline across split in reference plane
- Microstrip/Stripline through via (change reference planes)
- Mother/Daughter card

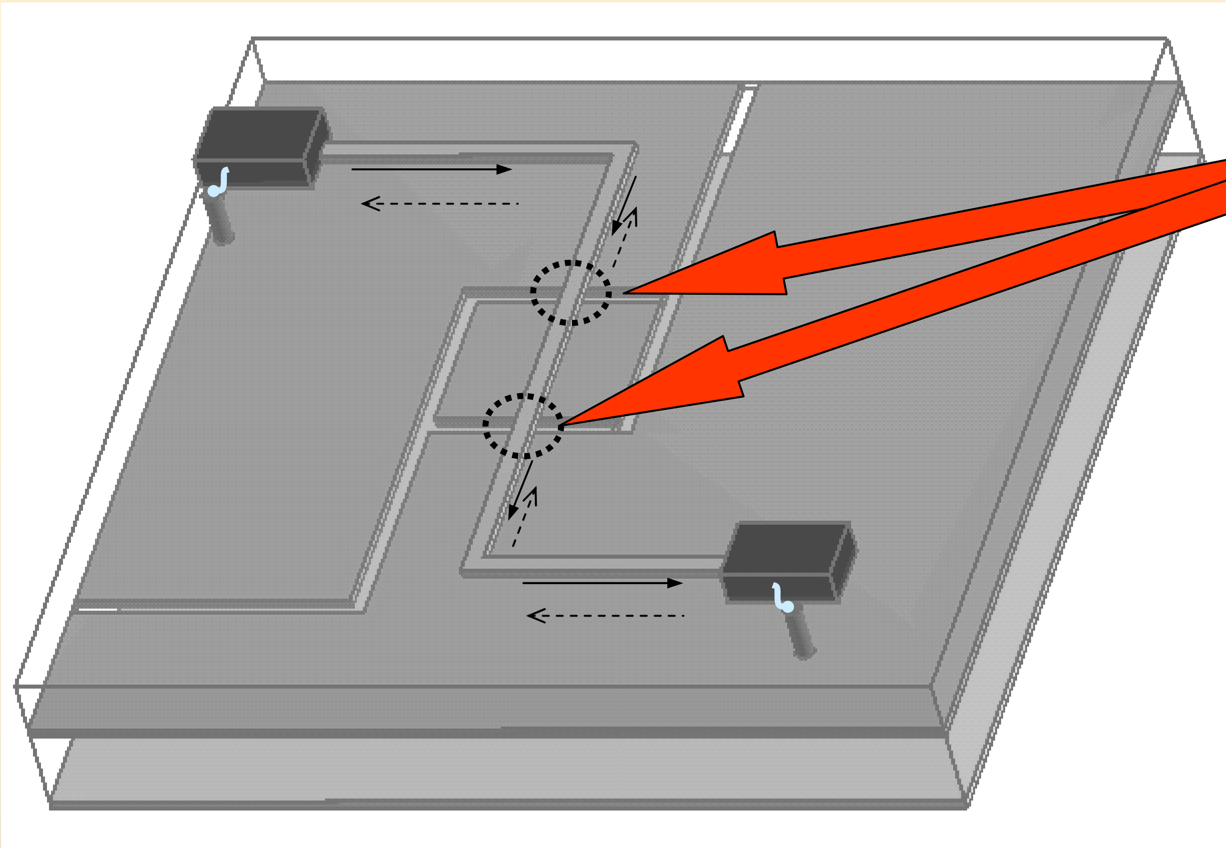
Microstrip/Stripline Across Split in Reference Plane

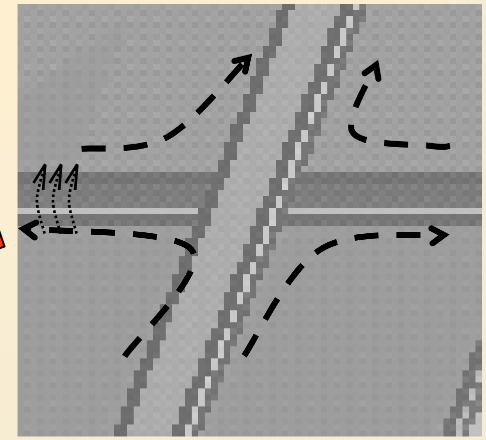
- Don’t Cross Splits with Critical Signals!!!
  - Bad practice
  - Stitching capacitor required across split to allow return current flow
    - must be close to crossing
    - must have low inductance
    - limited frequency effect --- due to inductance
  - Major source of Common Mode current!

Splits in Reference Plane

- Power planes often have splits
- Return current path interrupted
- Consider spectrum of clock signal
- Consider stitching capacitor impedance
- High frequency harmonics not returned directly

Split Reference Plane Example



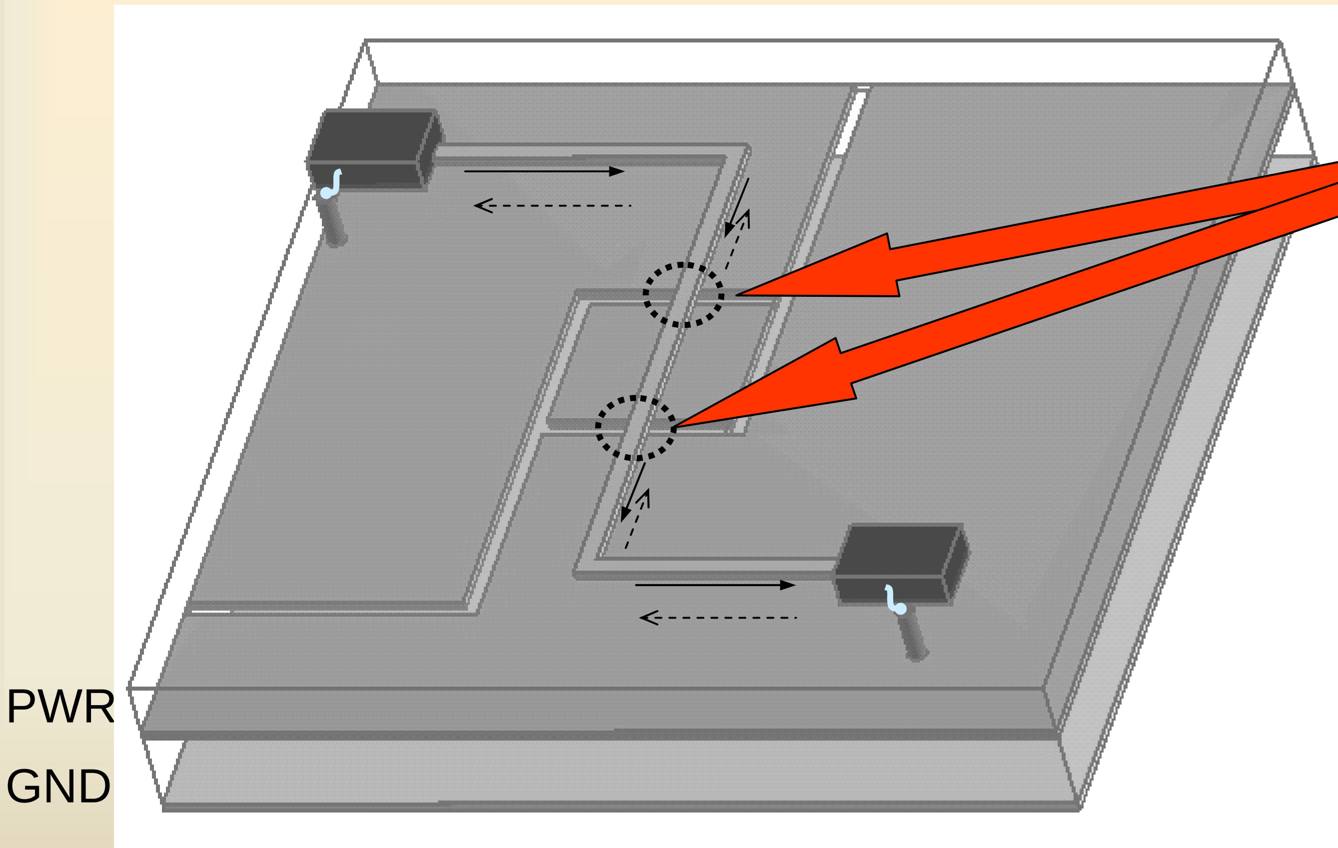


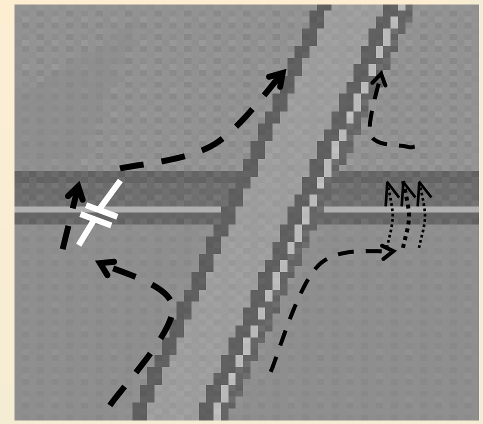
PWR

GND

Split Reference Plane Example

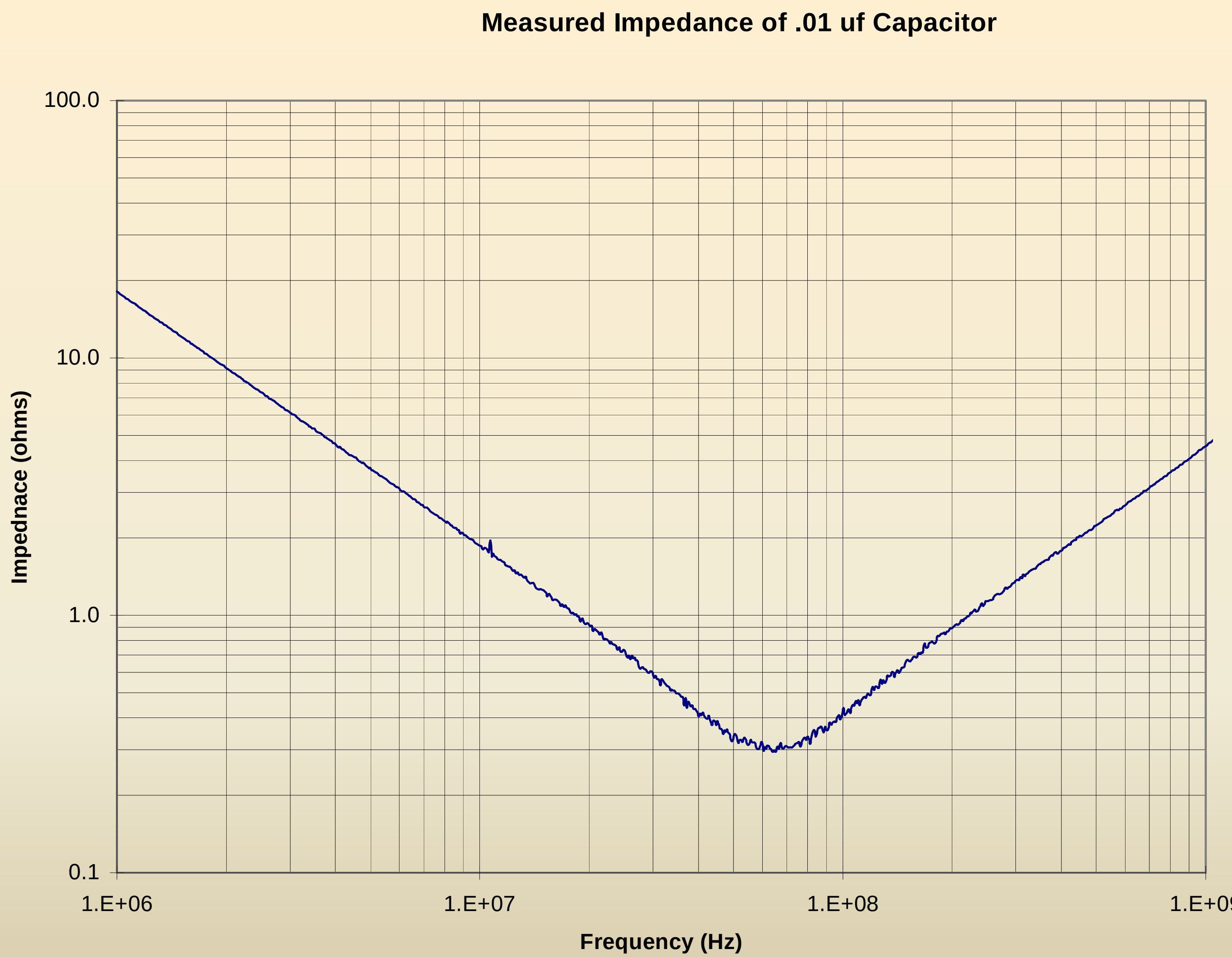
With Stitching Capacitors



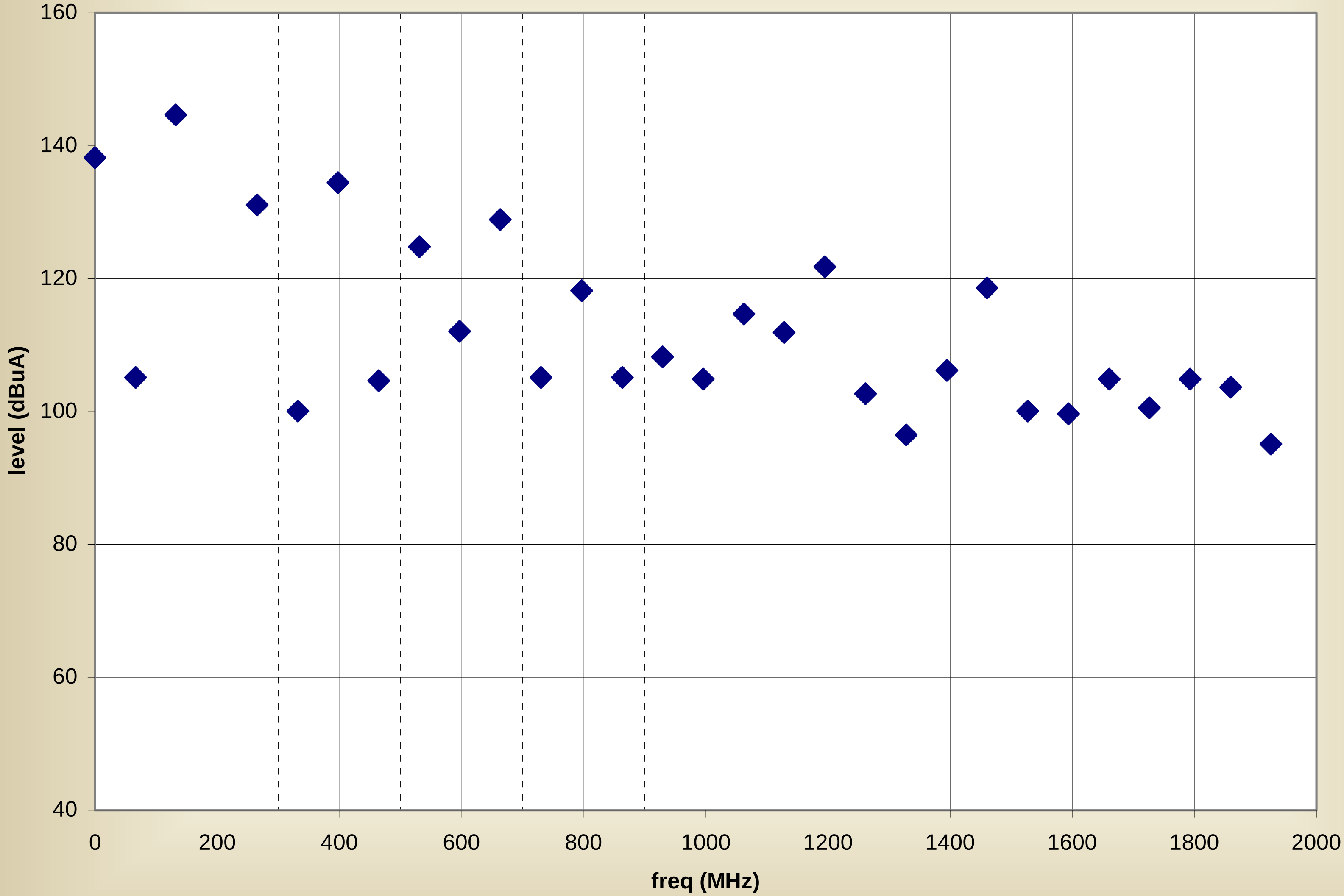


Stitching Capacitors Allow Return current to Cross Splits ???

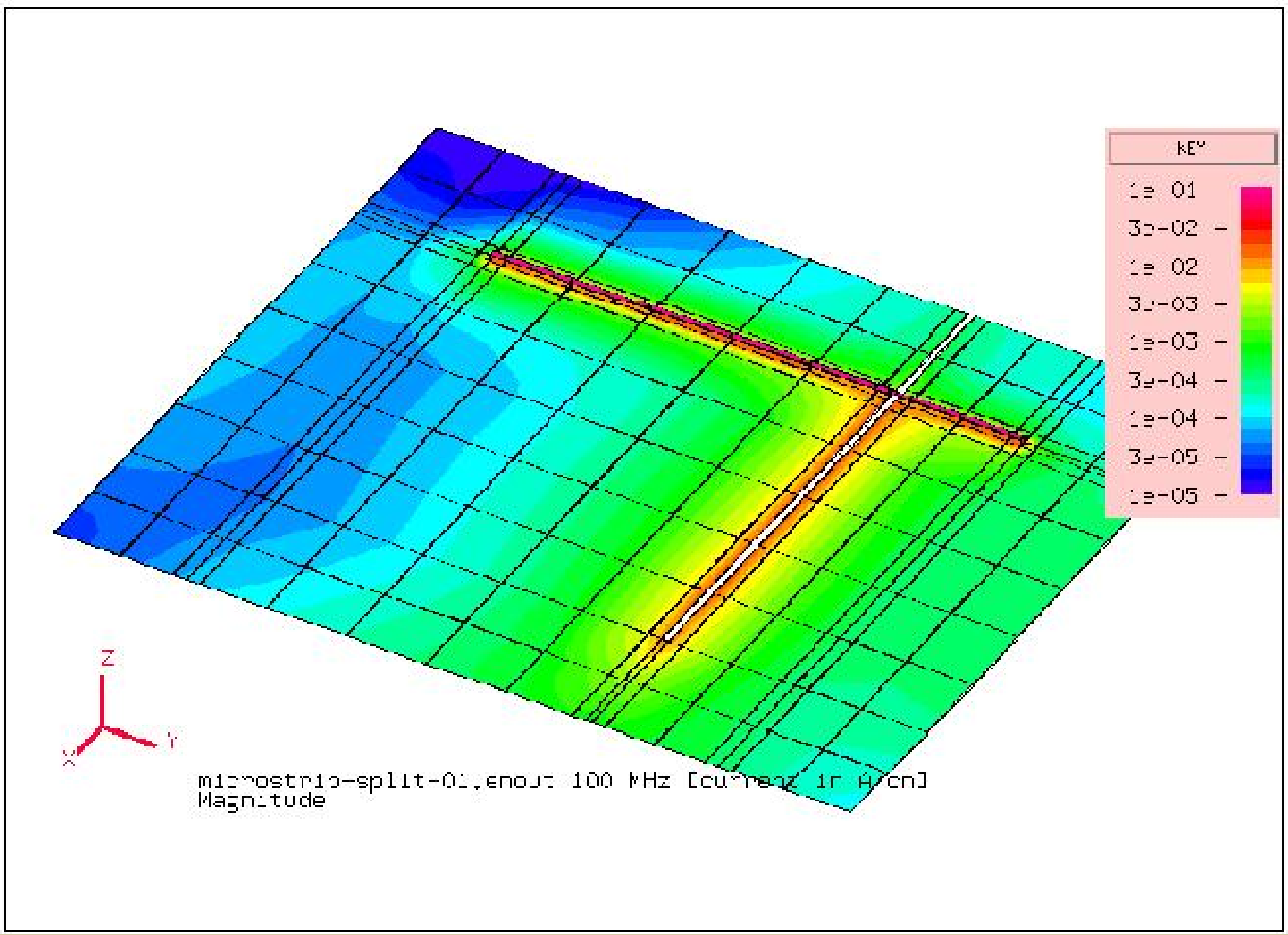
Capacitor Impedance



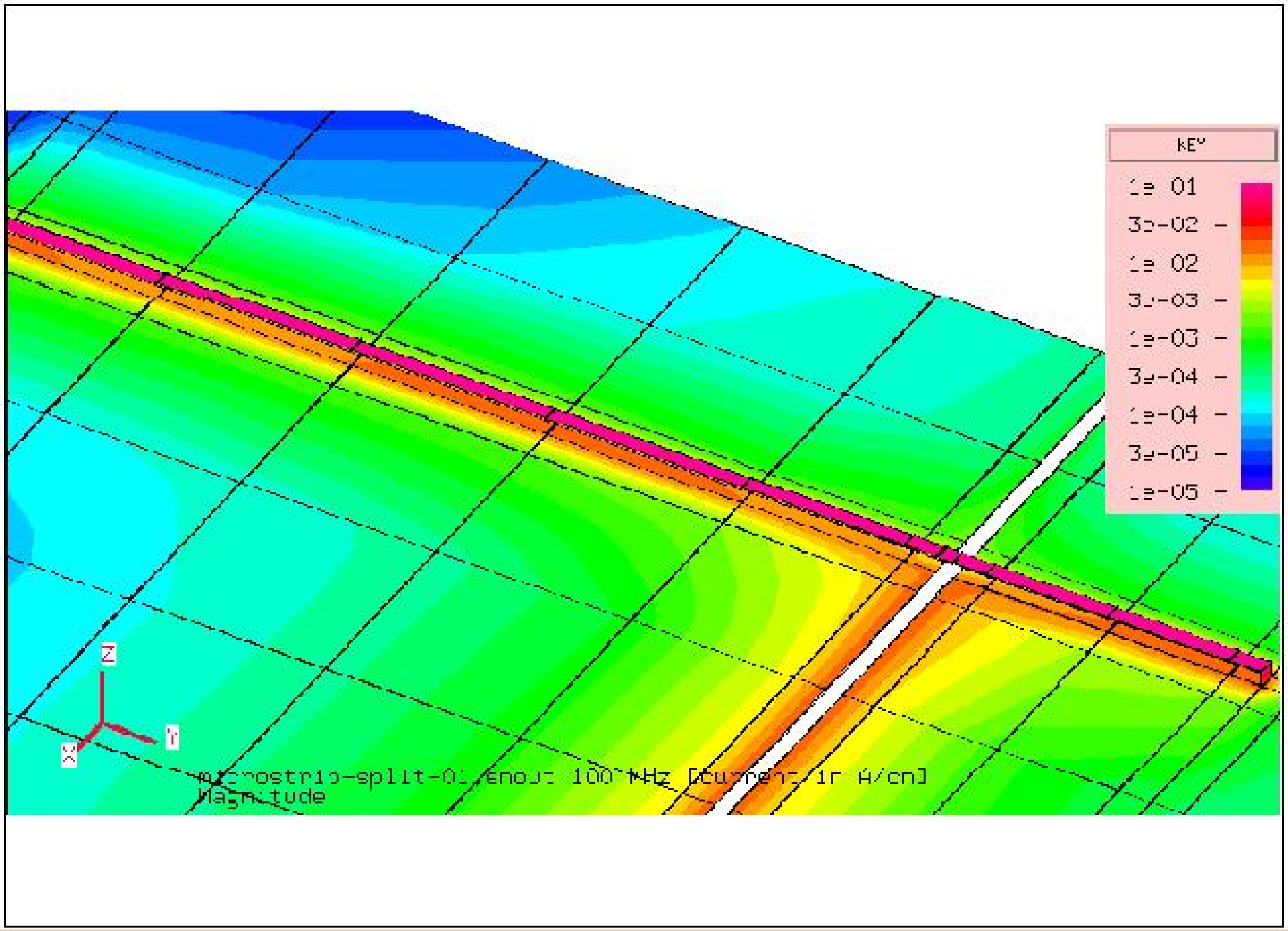
Frequency Domain Amplitude of Intentional Current Harmonic Amplitude From Clock Net



MoM Microstrip Model Current Distribution Example



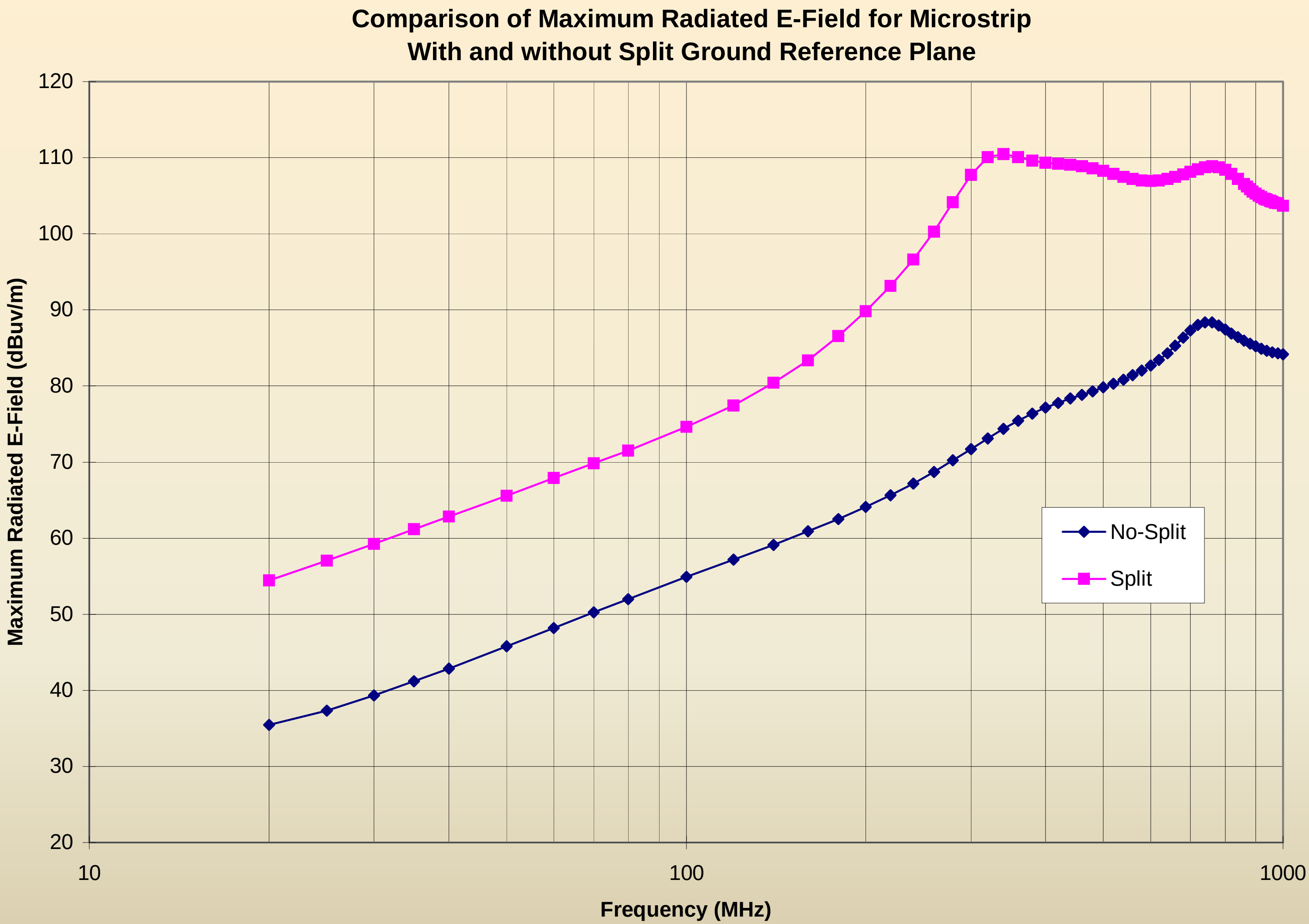
MoM Microstrip Model Current Distribution Example



Emissions From Board

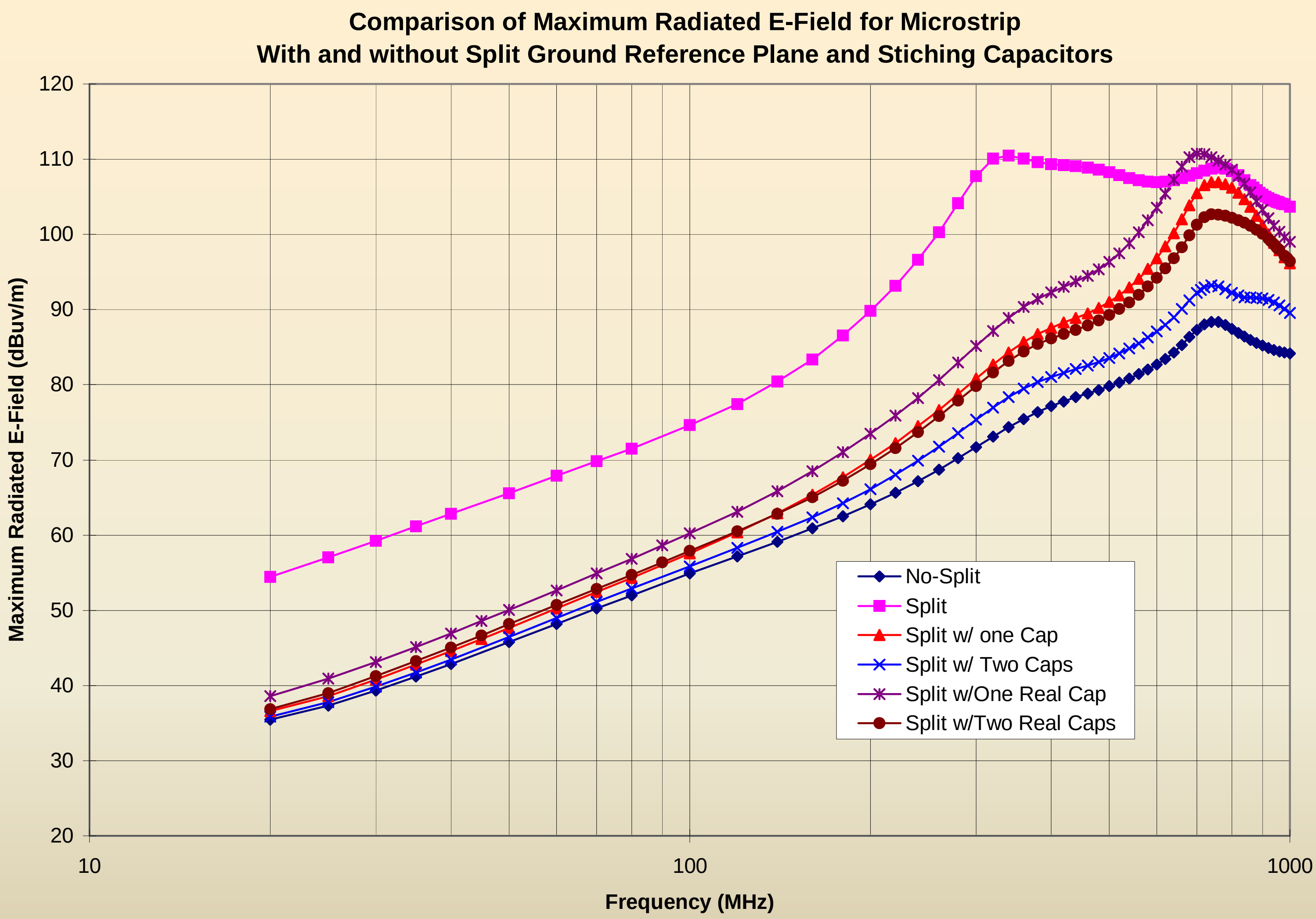
- Far field emissions not important unless it is an unshielded product
- Near field emissions above board **<u>ARE</u>** important
- Example of emissions from board with critical net crossing split reference plane

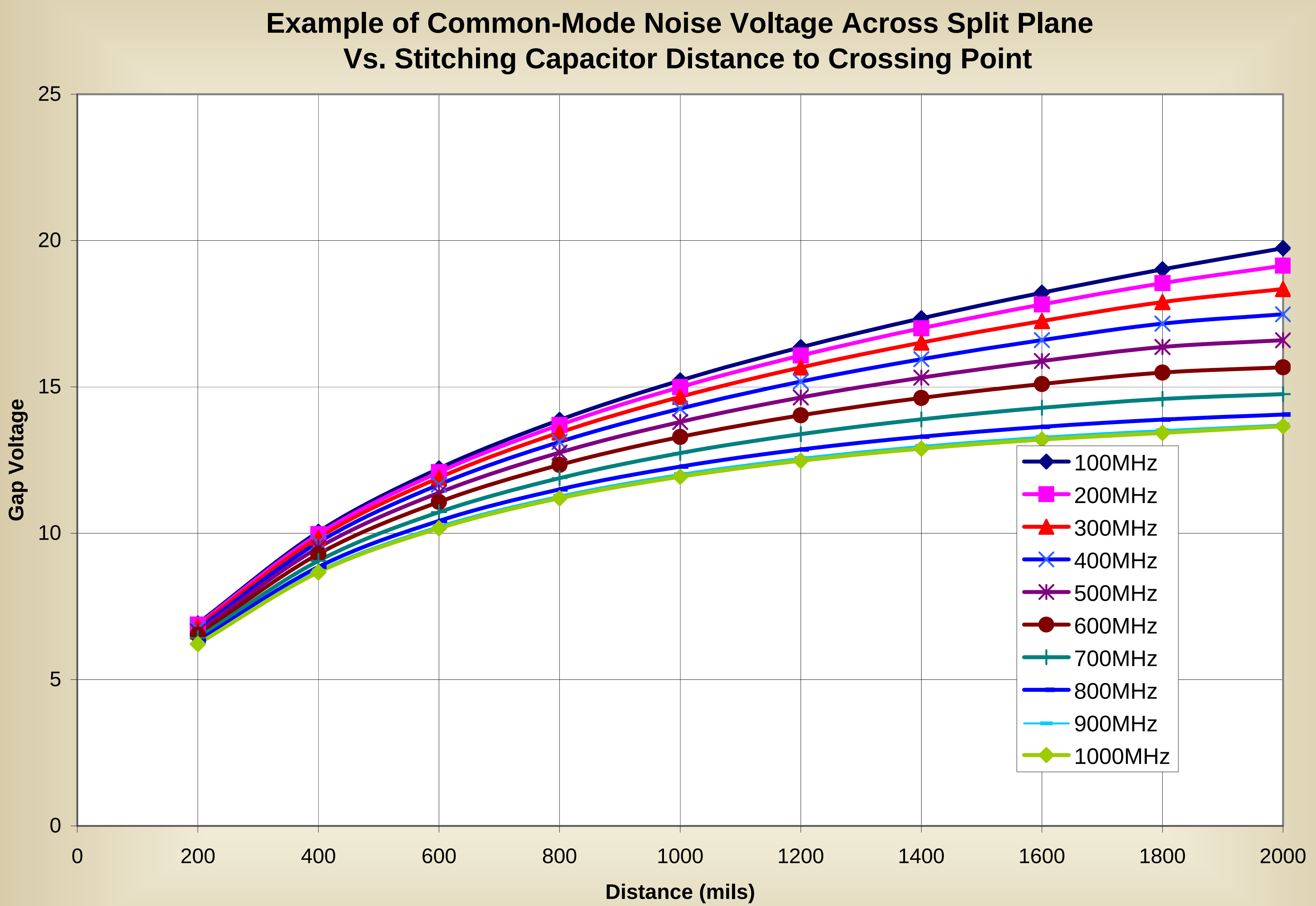
Near Field Radiation from Microstrip on Board with Split in Reference Plane



With "Perfectly Connected" Stitching Capacitors Across Split

Stitching Caps with Via Inductance

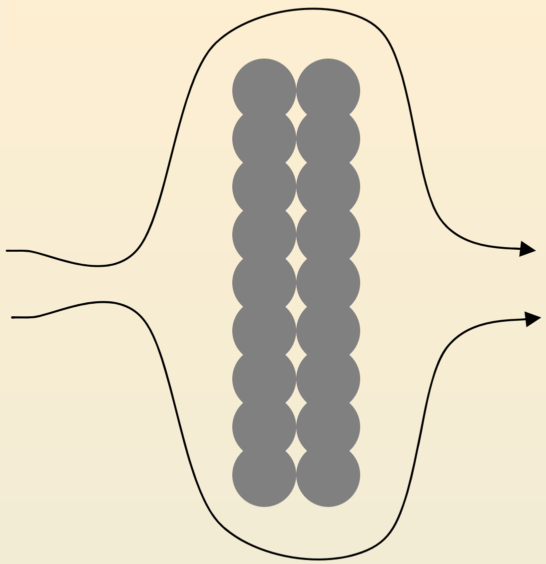



Example of Common-Mode Noise Voltage Across Split Plane
Vs. Stitching Capacitor Distance to Crossing Point
Gap Voltage
25
20
15
10
5
0
0
200
400
600
800
1000
1200
1400
1600
1800
2000
Distance (mils)
100MHz
200MHz
300MHz
400MHz
500MHz
600MHz
700MHz
800MHz
900MHz
1000MHz

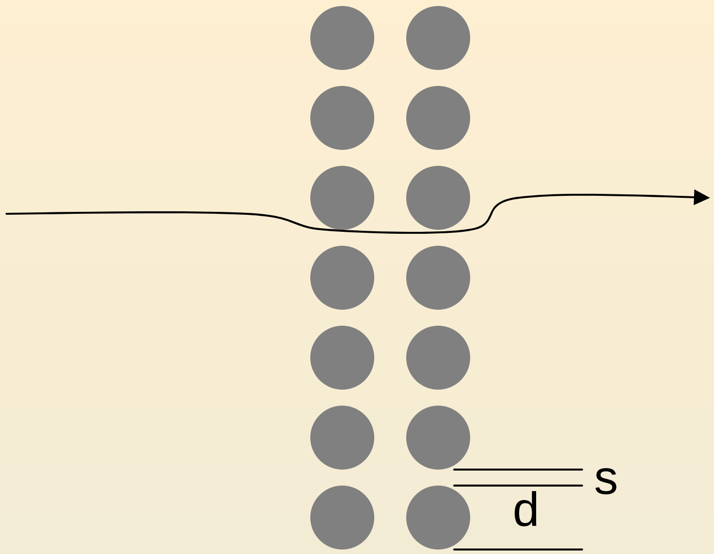
Are Stitching Capacitors Effective ???

- YES, at low frequencies
- No, at high frequencies
- Need to limit the high frequency current spectrum
- Need to avoid split crossings with ALL critical signals

Pin Field Via Keepouts??



Return Current must go around entire keep out area --- just as bad as a slot

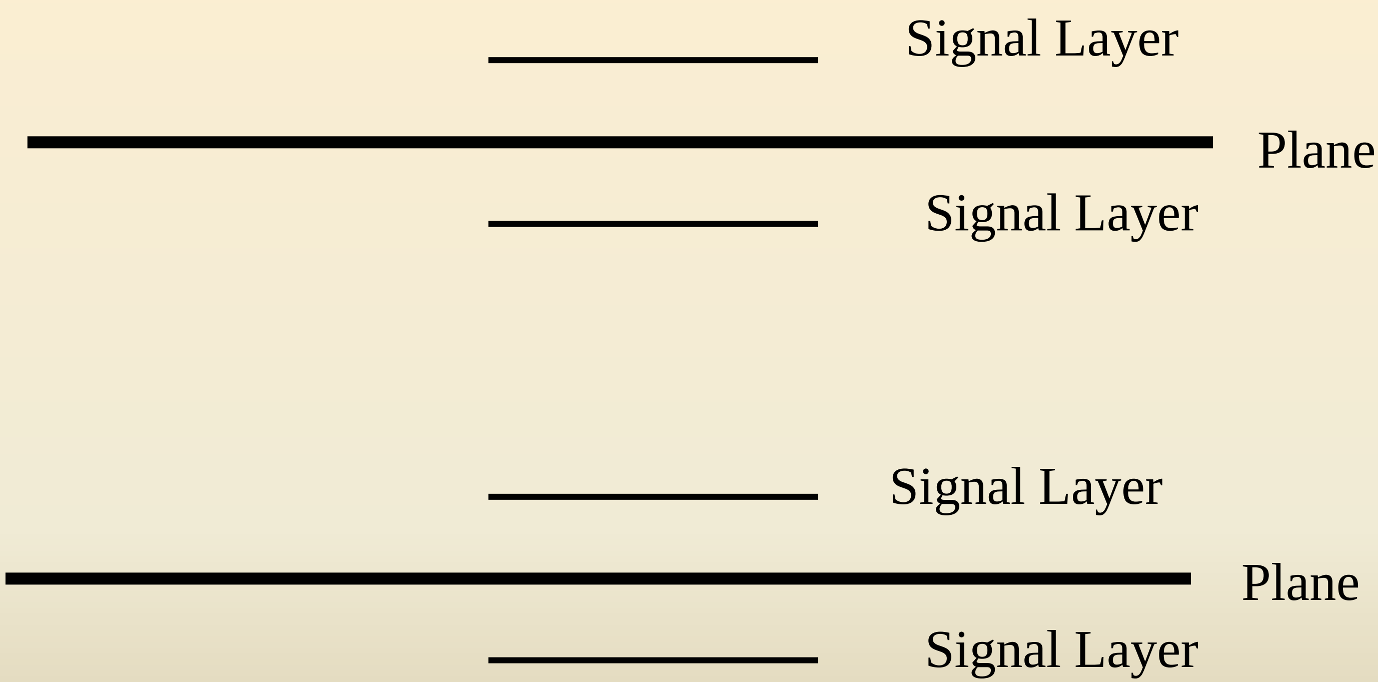


Return current path deviation minimal

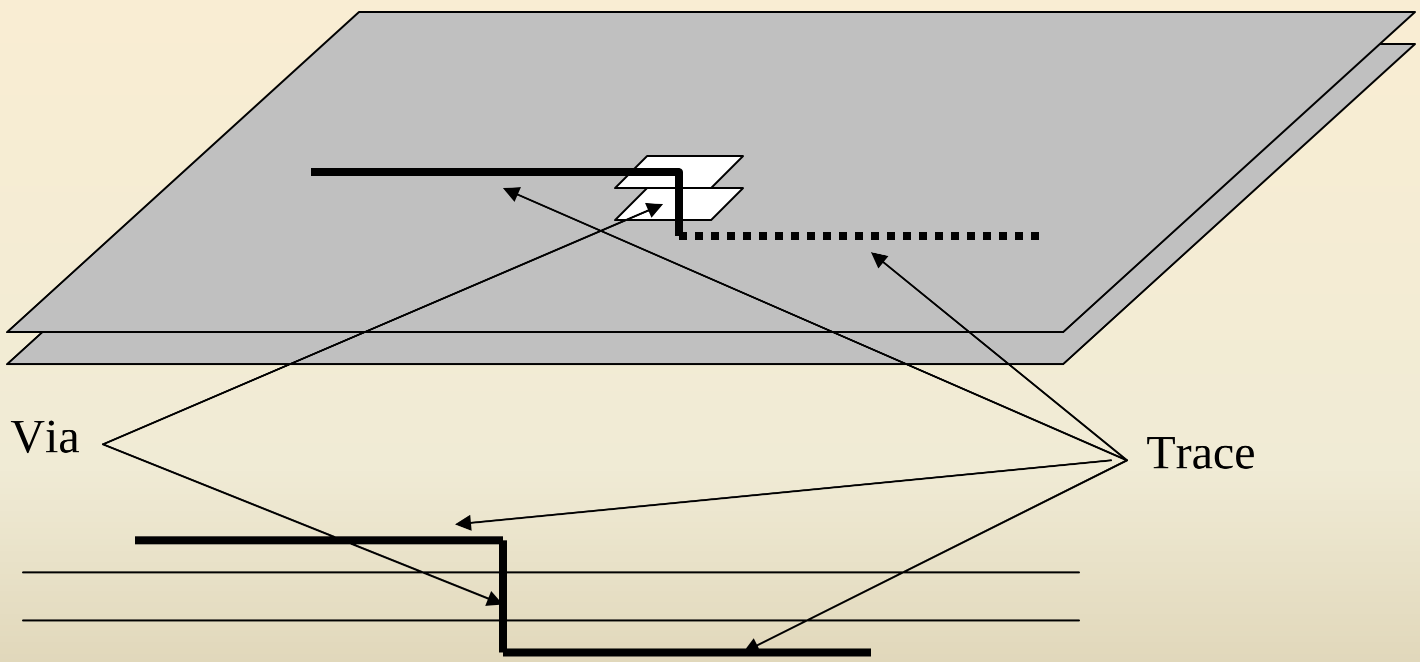
Recommend s/d > 1/3

Changing Reference Planes

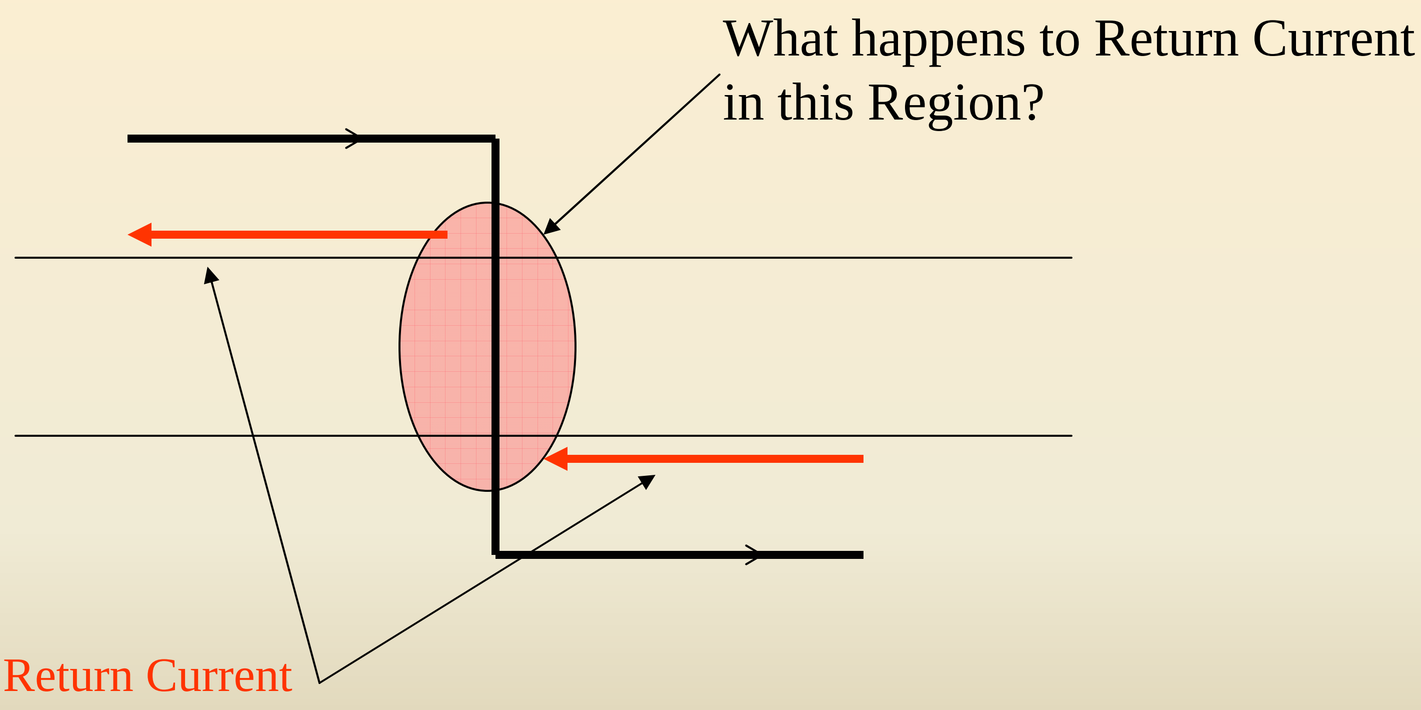
Six-Layer PCB Stackup Example



Microstrip/Stripline through via (change reference planes)



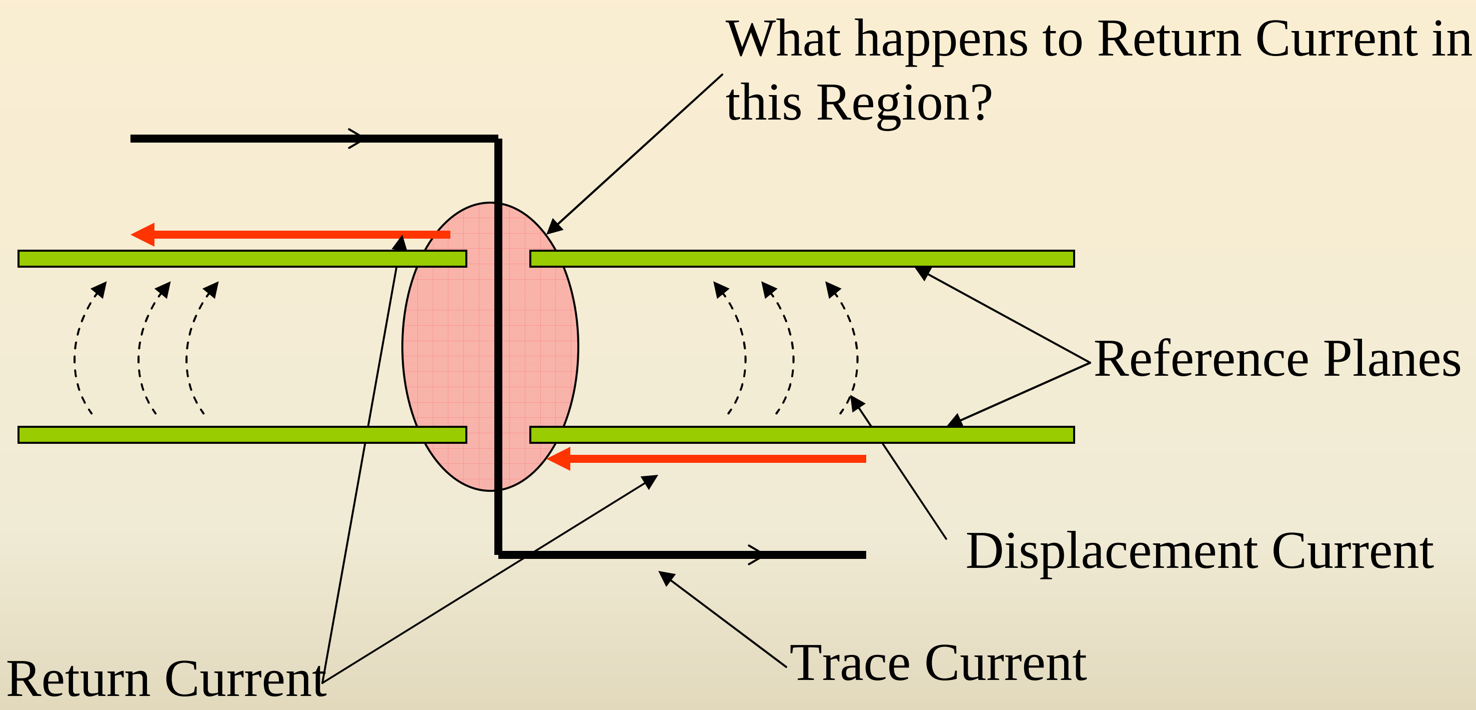
How can the Return Current Flow When Signal Line Goes Through Via??



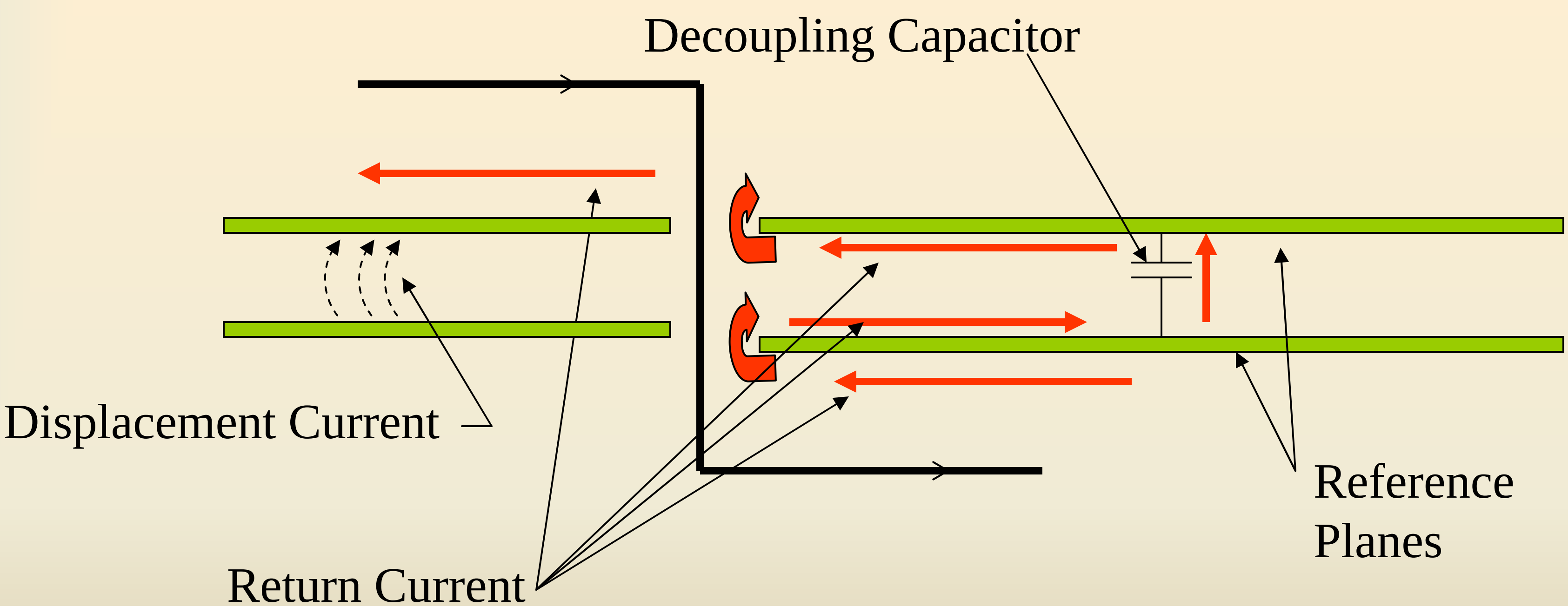
How can the Return Current Flow When Signal Line Goes Through Via??

- Current can NOT go from one side of the plane to the other through the plane
  - skin depth
- Current must go around plane at via hole, through decoupling capacitor, around second plane at the second via hole!
- Use displacement current between planes

Return Current Across Reference Plane Change

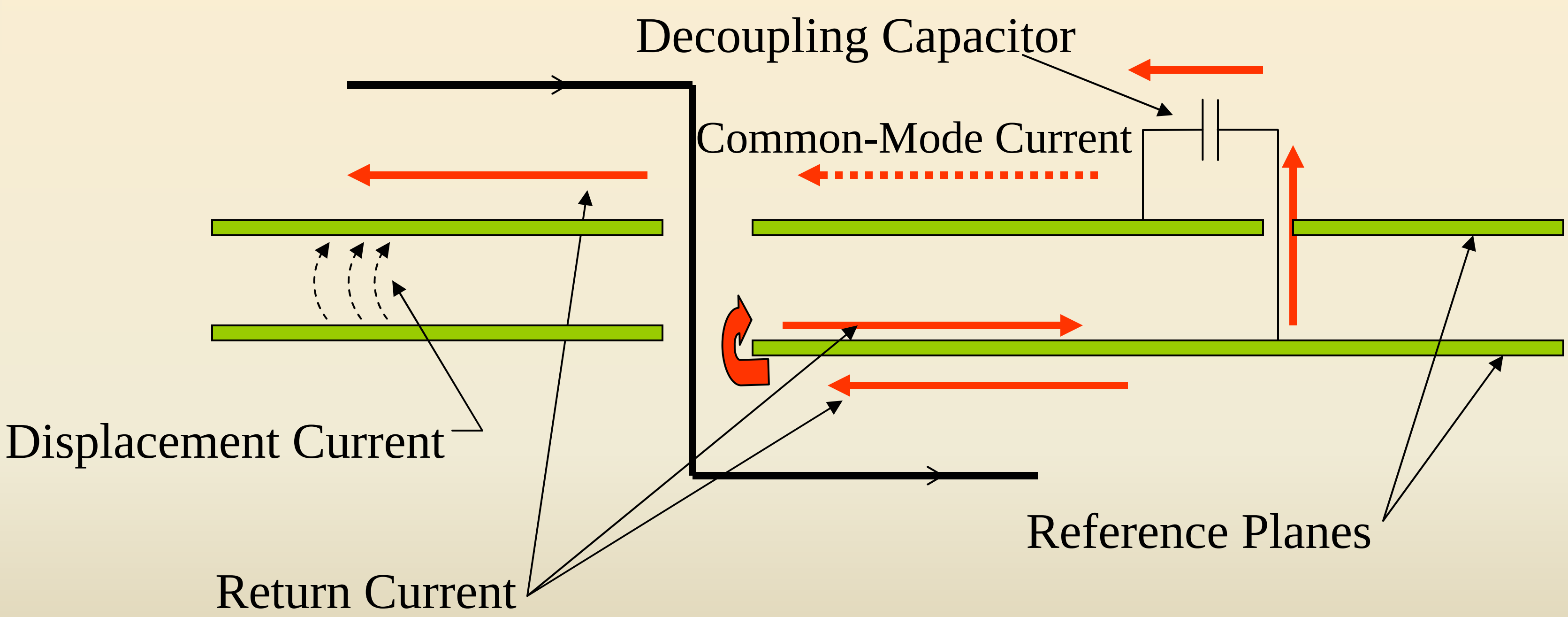


Return Current Across Reference Plane Change
With Decoupling Capacitor



Return Current Across Reference Plane Change

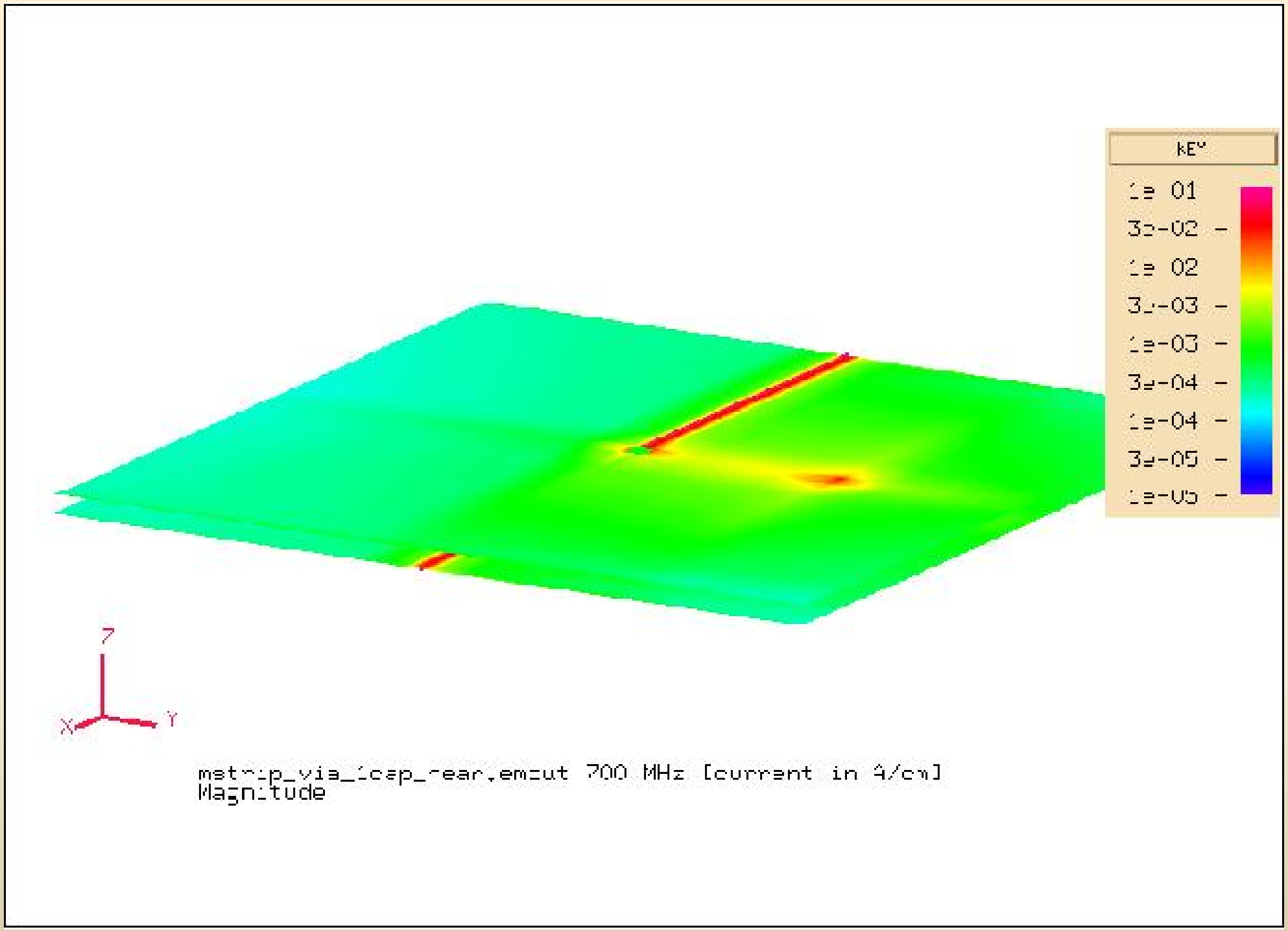
With Decoupling Capacitor (on Top)



Location of Decoupling Capacitors (Relative to Via) is Important!

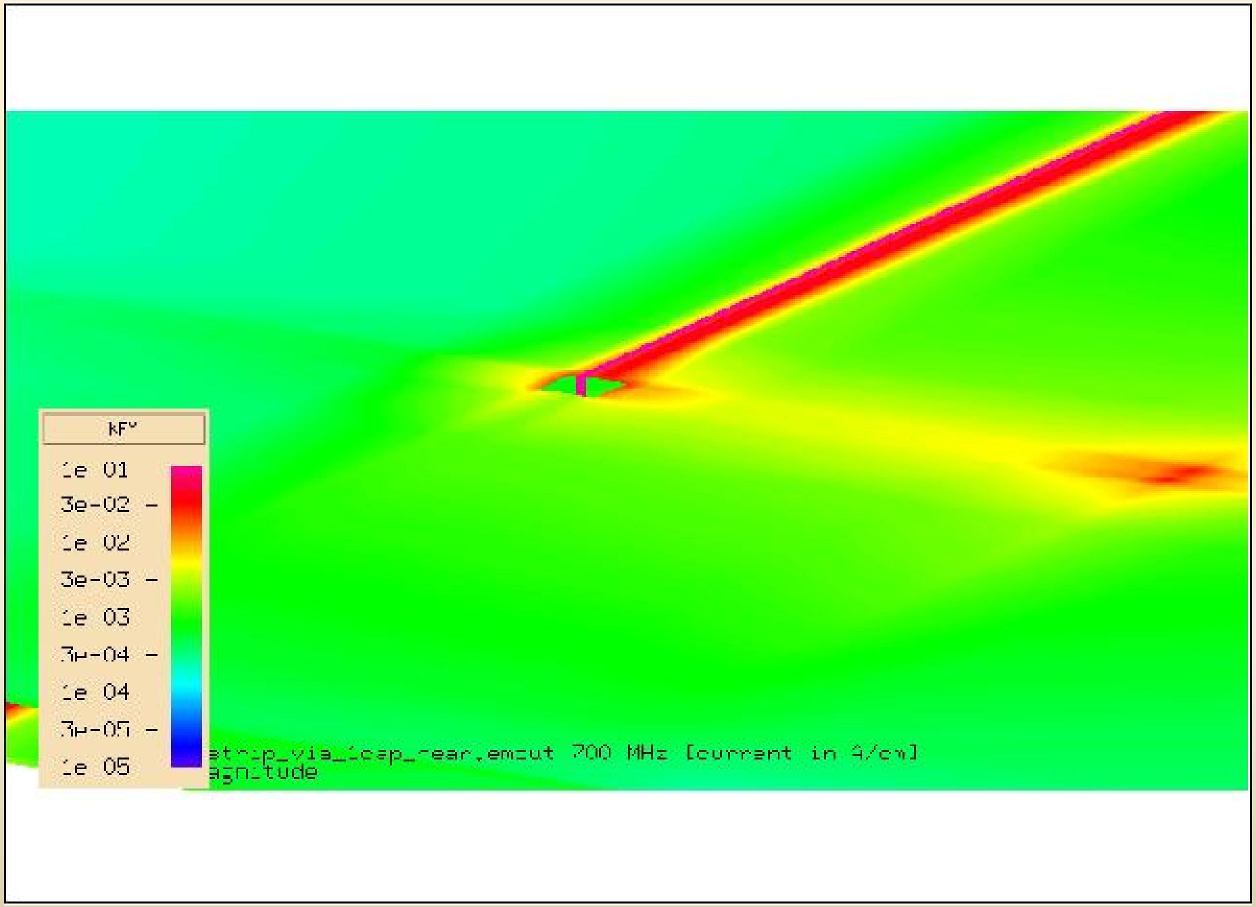
- One Decoupling Capacitor at 0.5”
- Two Decoupling Capacitors at 0.5”
- Two Decoupling Capacitors at 0.25”

RF Current @ 700 MHz with One Capacitor 0.5” from Via

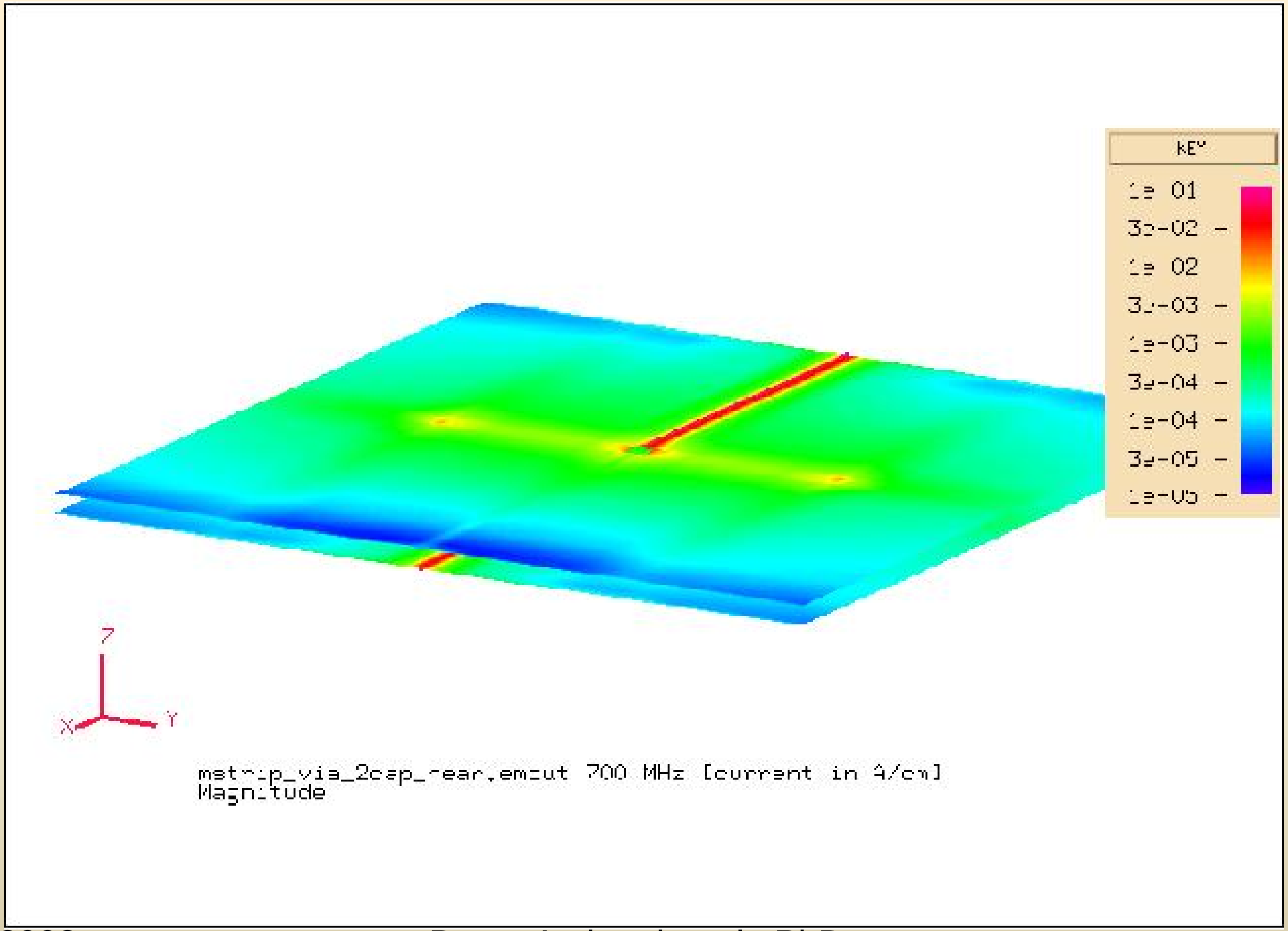


RF Current @ 700 MHz with One Capacitor 0.5” from Via

(expanded view)

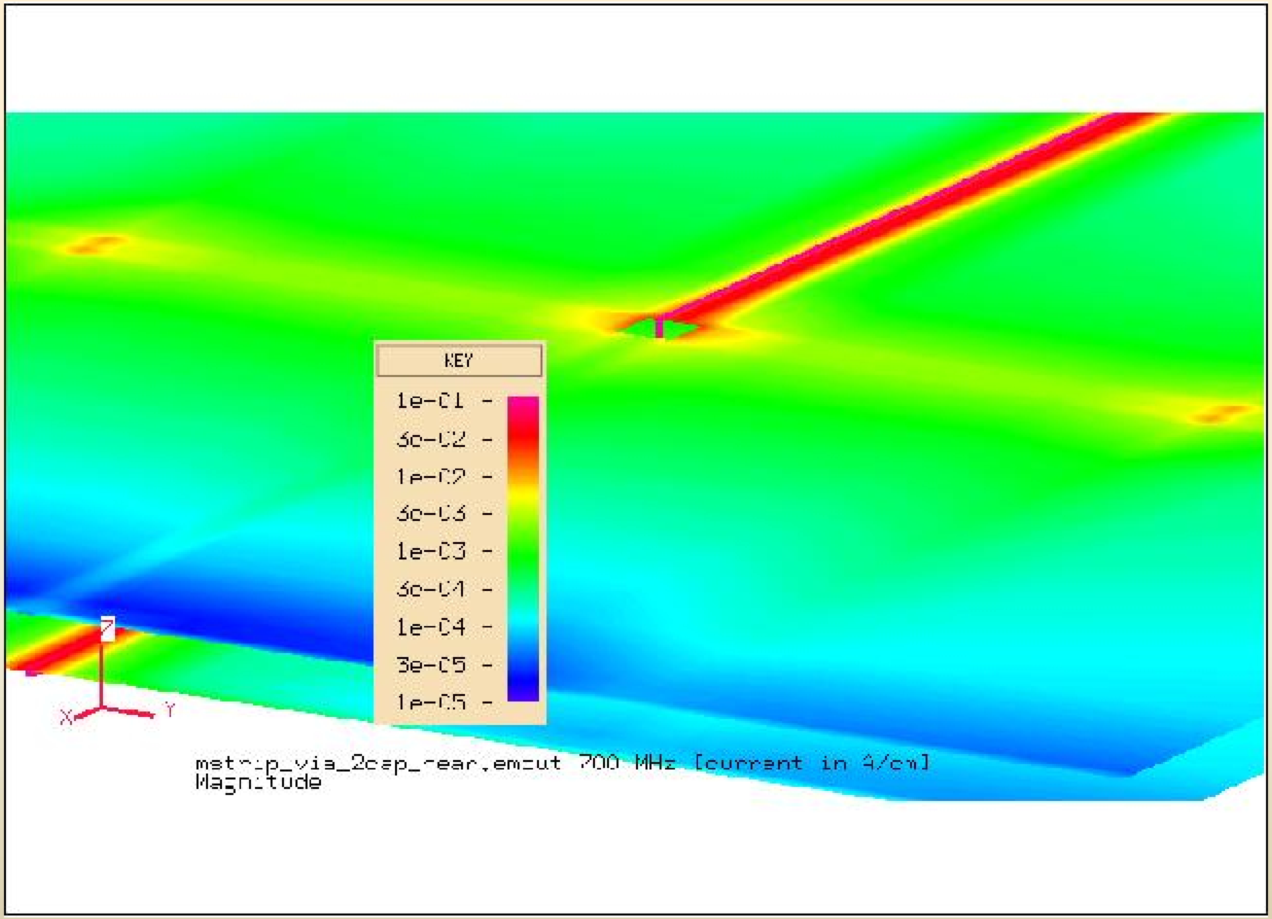


RF Current @ 700 MHz with Two Capacitors 0.5” from Via

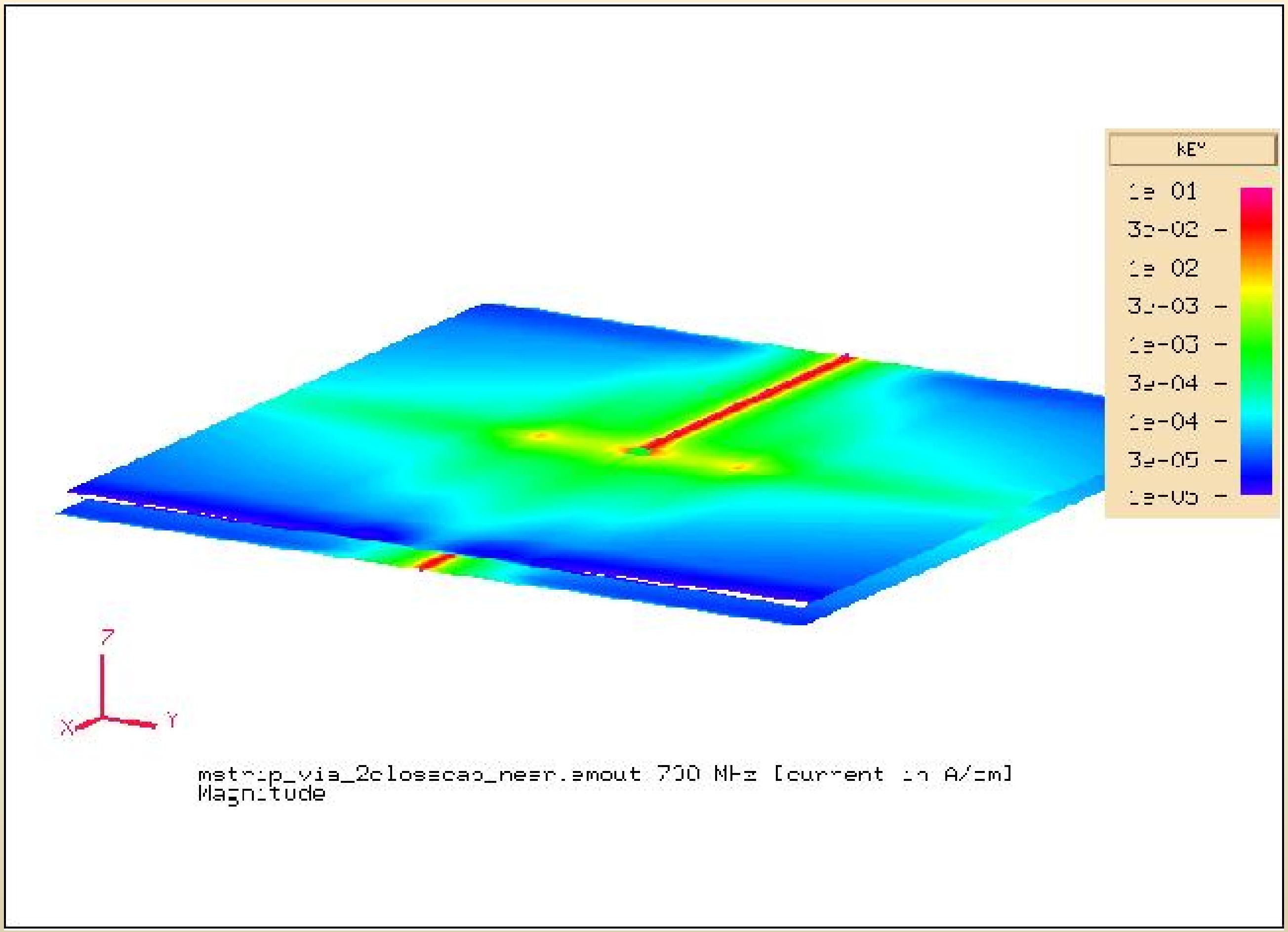


RF Current @ 700 MHz with One Capacitor 0.5” from Via

(Expanded view)

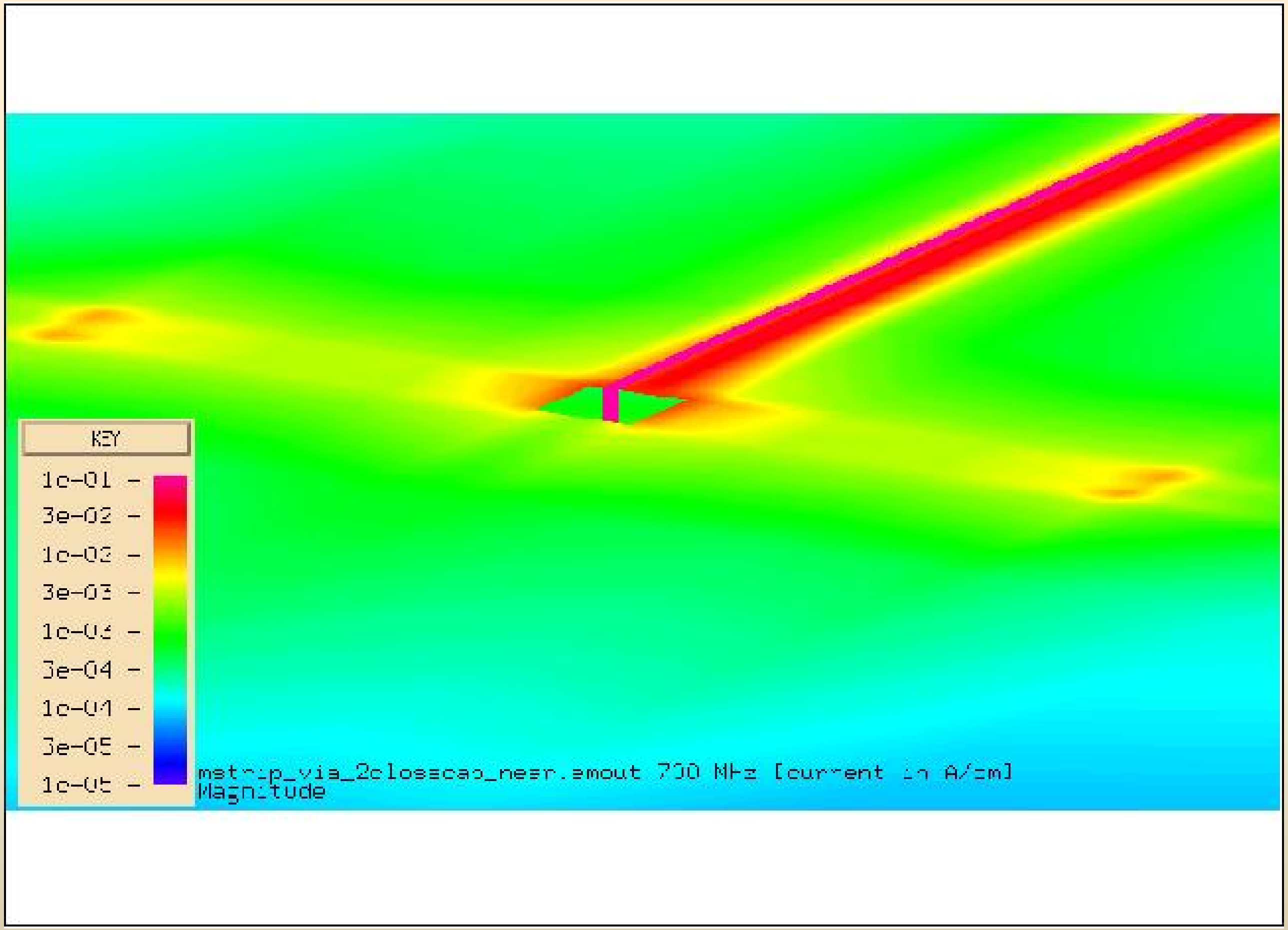


RF Current @ 700 MHz with Two Capacitors 0.25” from Via



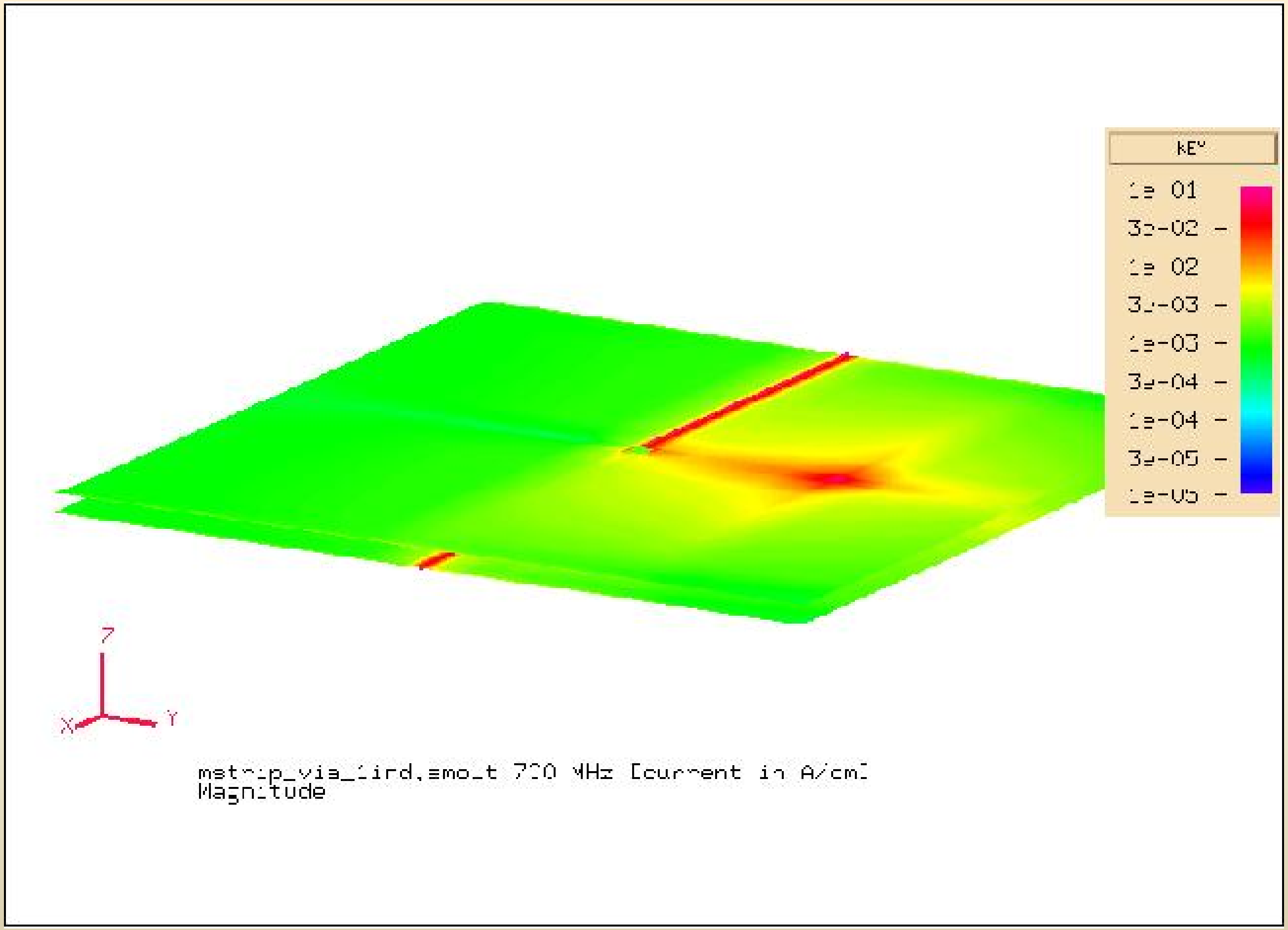
108

RF Current @ 700 MHz with Two Capacitors 0.25” from Via
(expanded view)

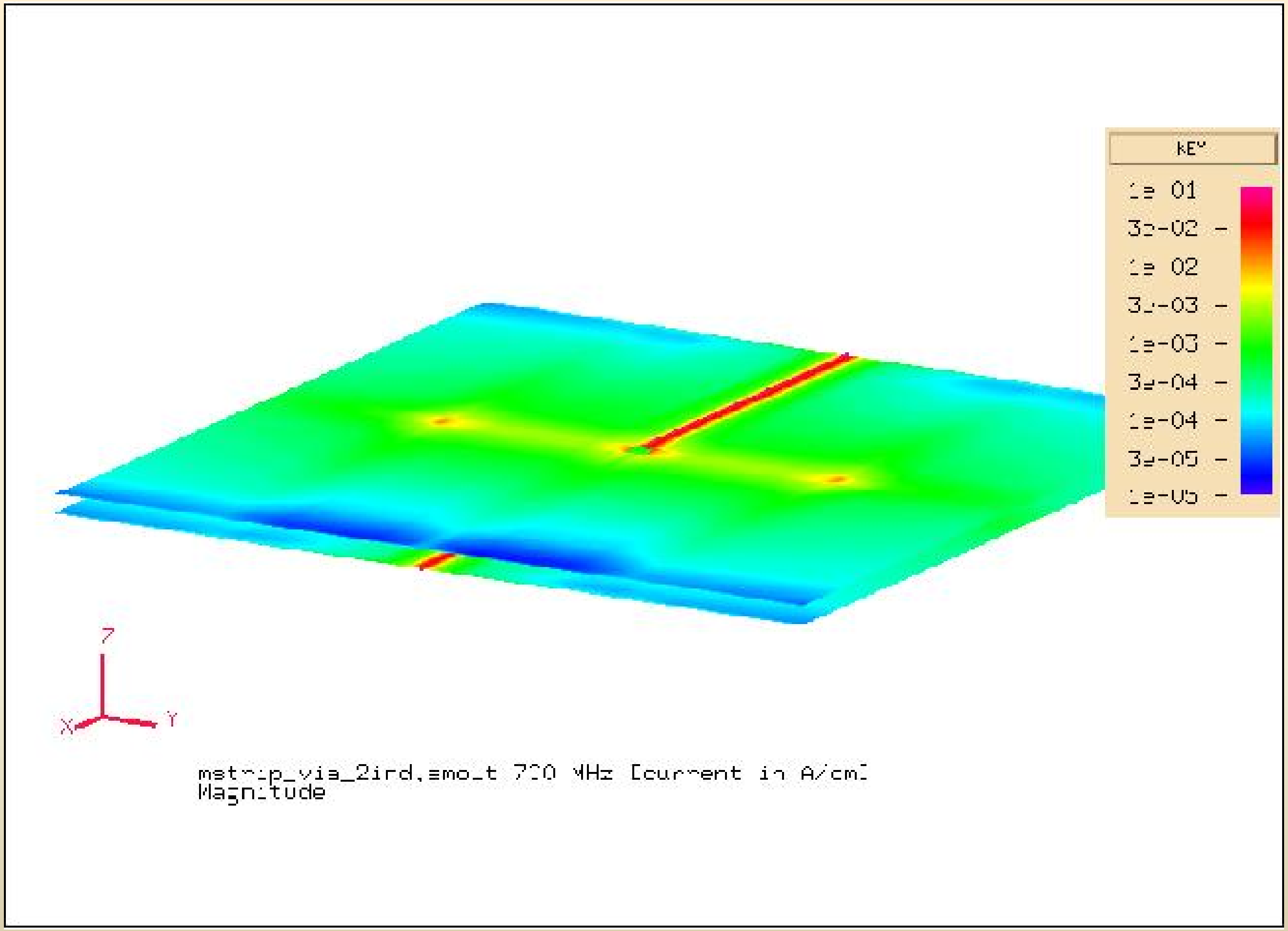


109

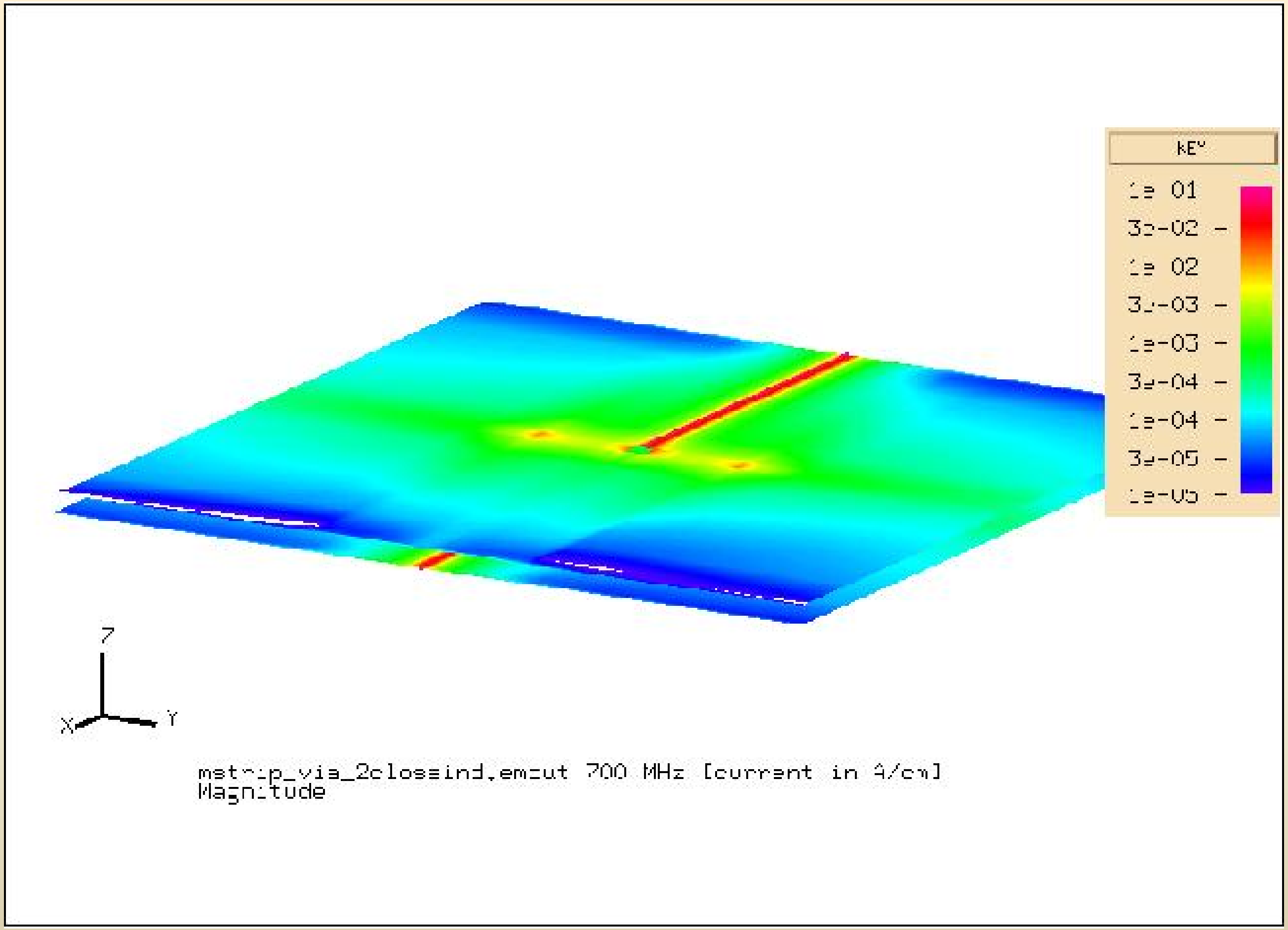
RF Current @ 700 MHz with One REAL Capacitor 0.5” from Via



RF Current @ 700 MHz with Two REAL Capacitors 0.5” from Via



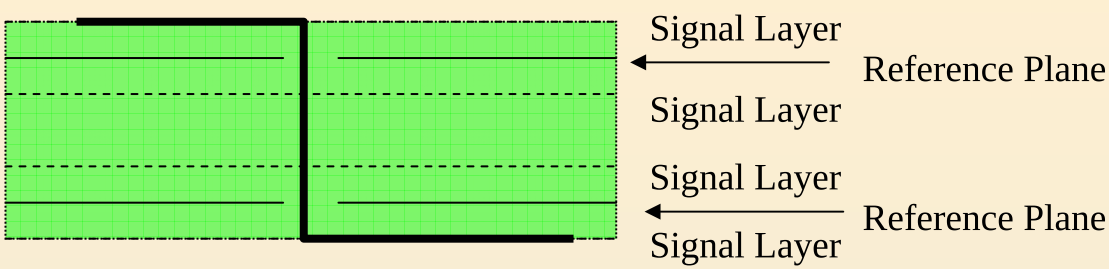
RF Current @ 700 MHz with Two REAL Capacitors 0.25” from Via



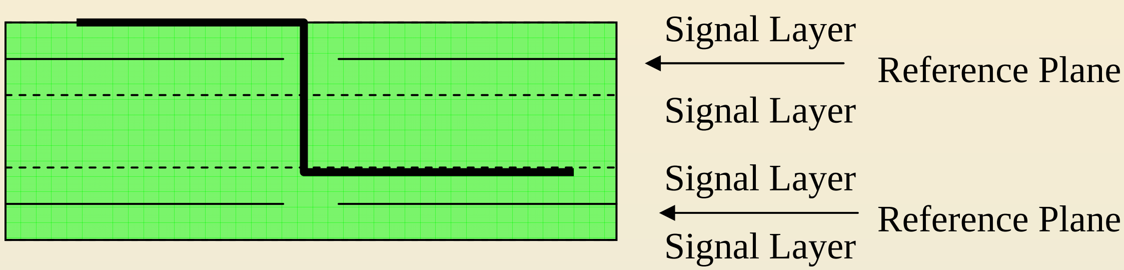
Possible Routing Options

Six-Layer Board

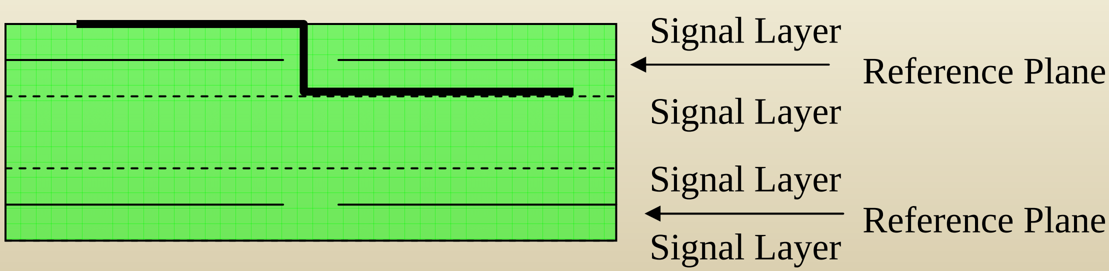
Bad



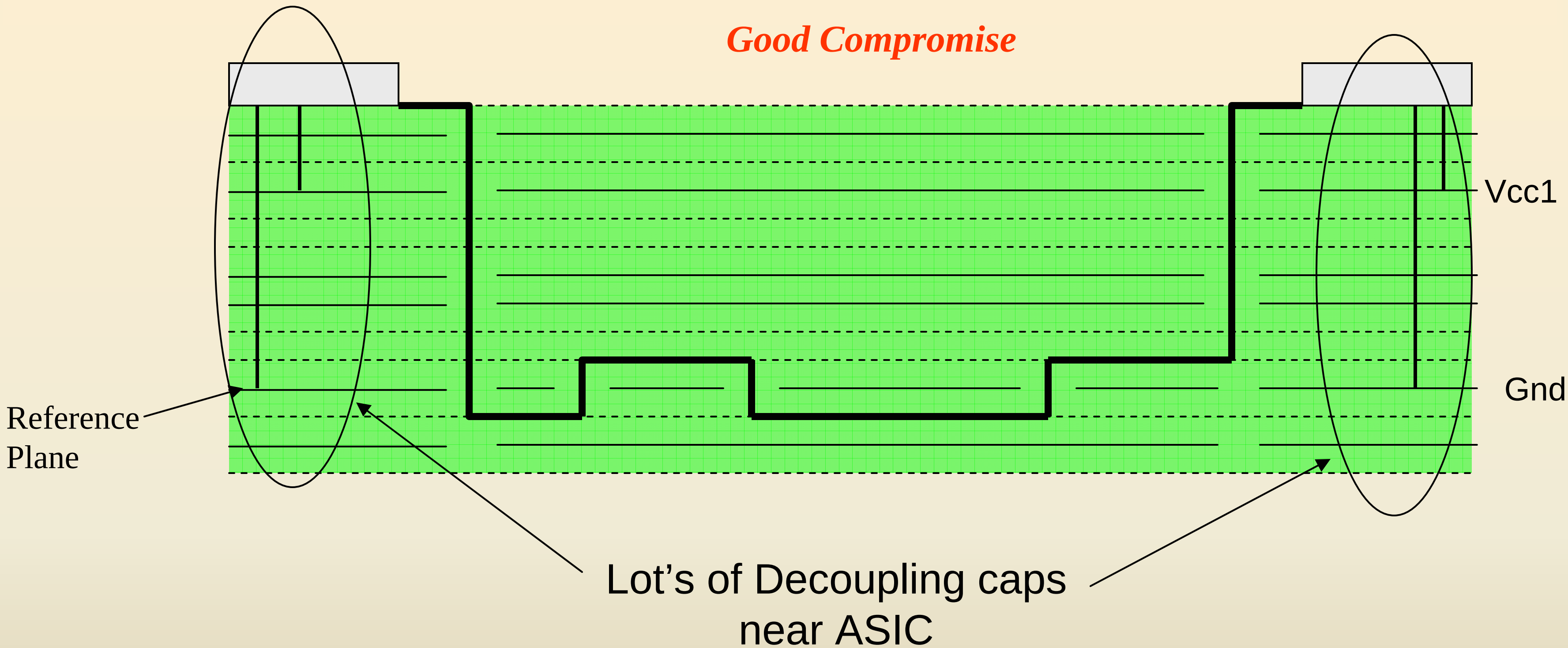
Bad



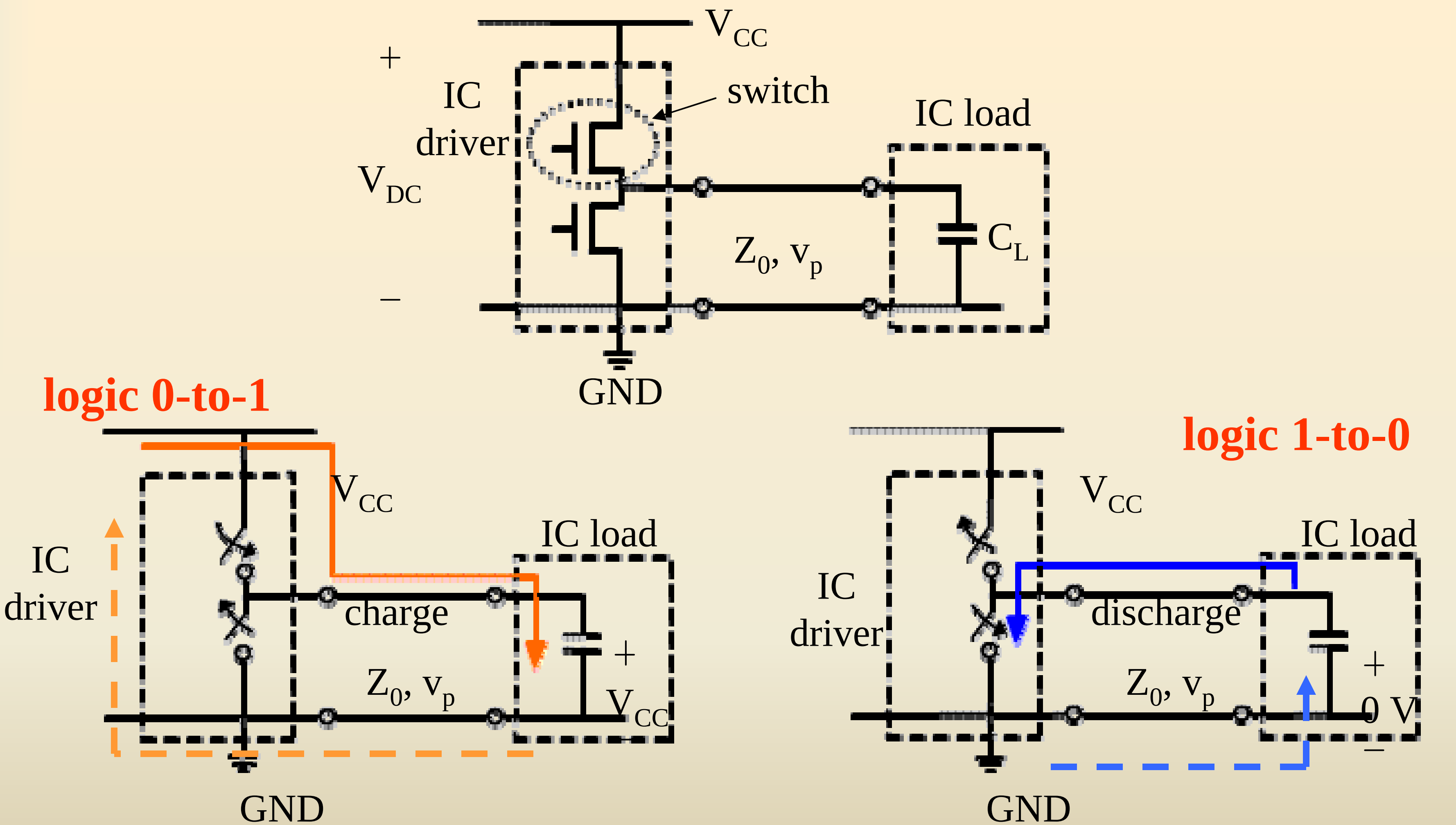
Good



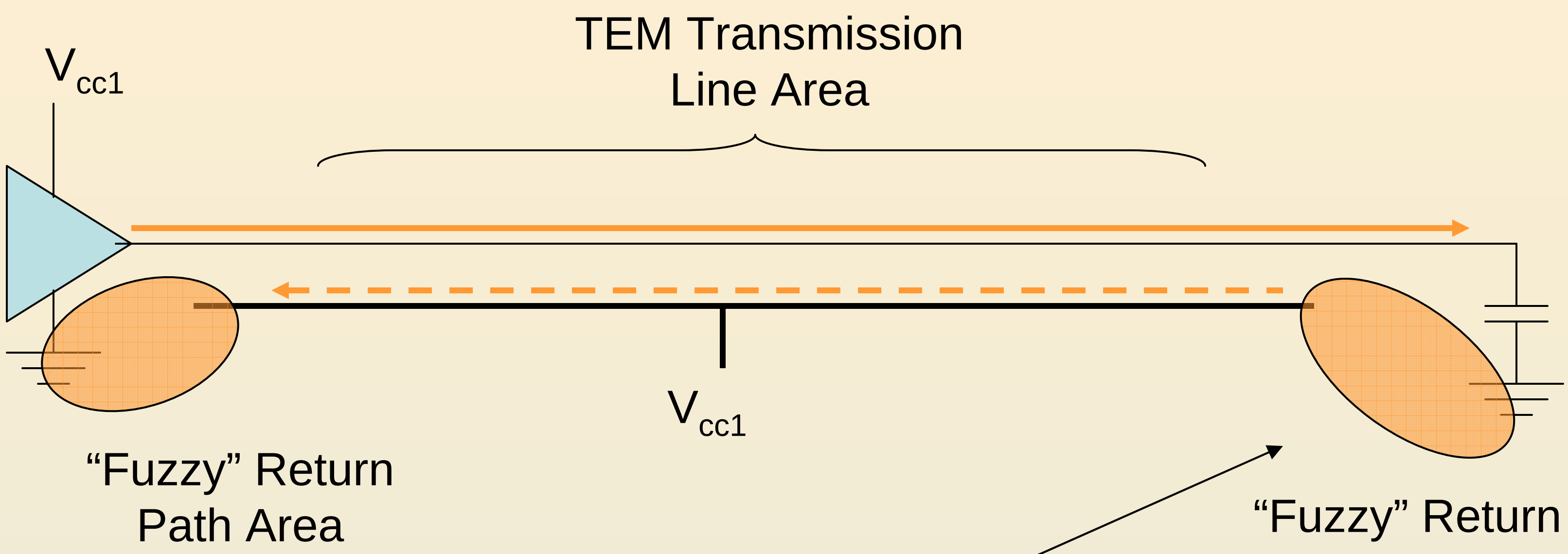
Compromise Routing Option for Many Layer Boards



Typical Driver/Receiver Currents



Suppose The Trace is Routed Next to Power (not Gnd)

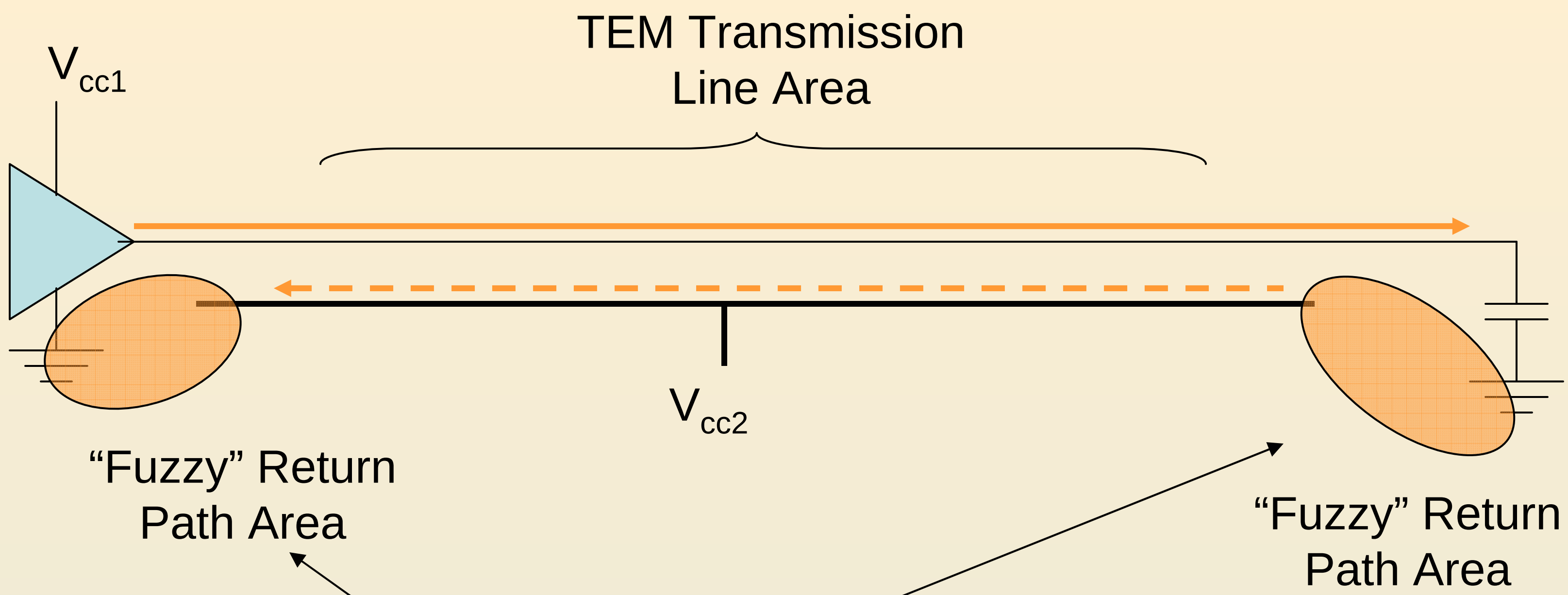


Return Path Options:

-- Decoupling Capacitors

-- Distributed Displacement Current

Suppose The Trace is Routed Next to a *DIFFERENT* Power (not Gnd)



Return Path Options:

-- Decoupling Capacitors ??? *May not be any nearby*!!

-- Distributed Displacement Current – *Increased current spread*!!!

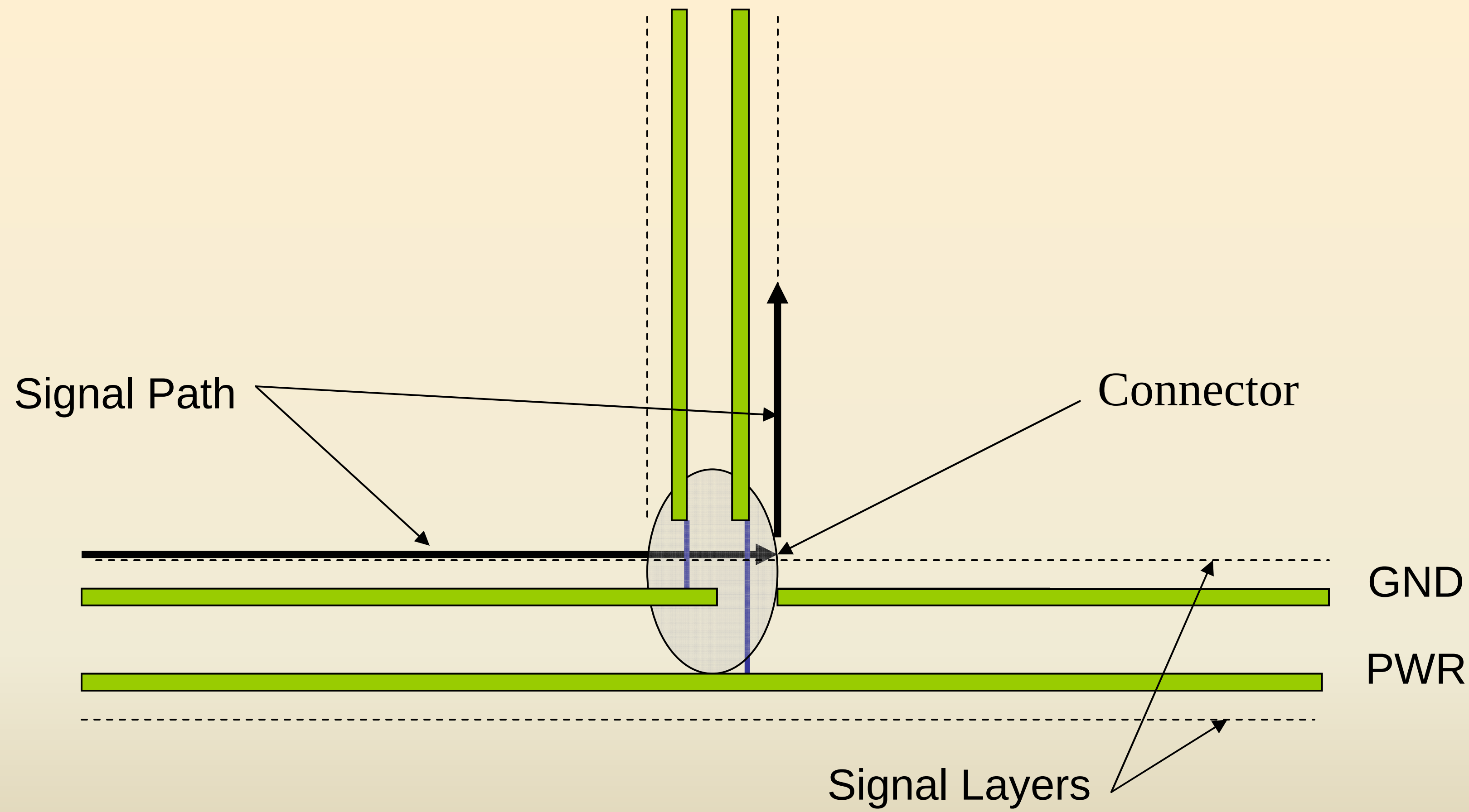
Via Summary

- ✓ Route critical signals on either side of ONE reference plane
- ✓ Drop critical signal net to selected layer close to driver/receiver
  - ✓ Many decoupling capacitors to help return currents
- ✓ Do NOT change reference planes on critical nets unless ABSOLUTELY NECESSARY!!
- ✓ Make sure at least 2 decoupling capacitors within 0.2” of via with critical signals

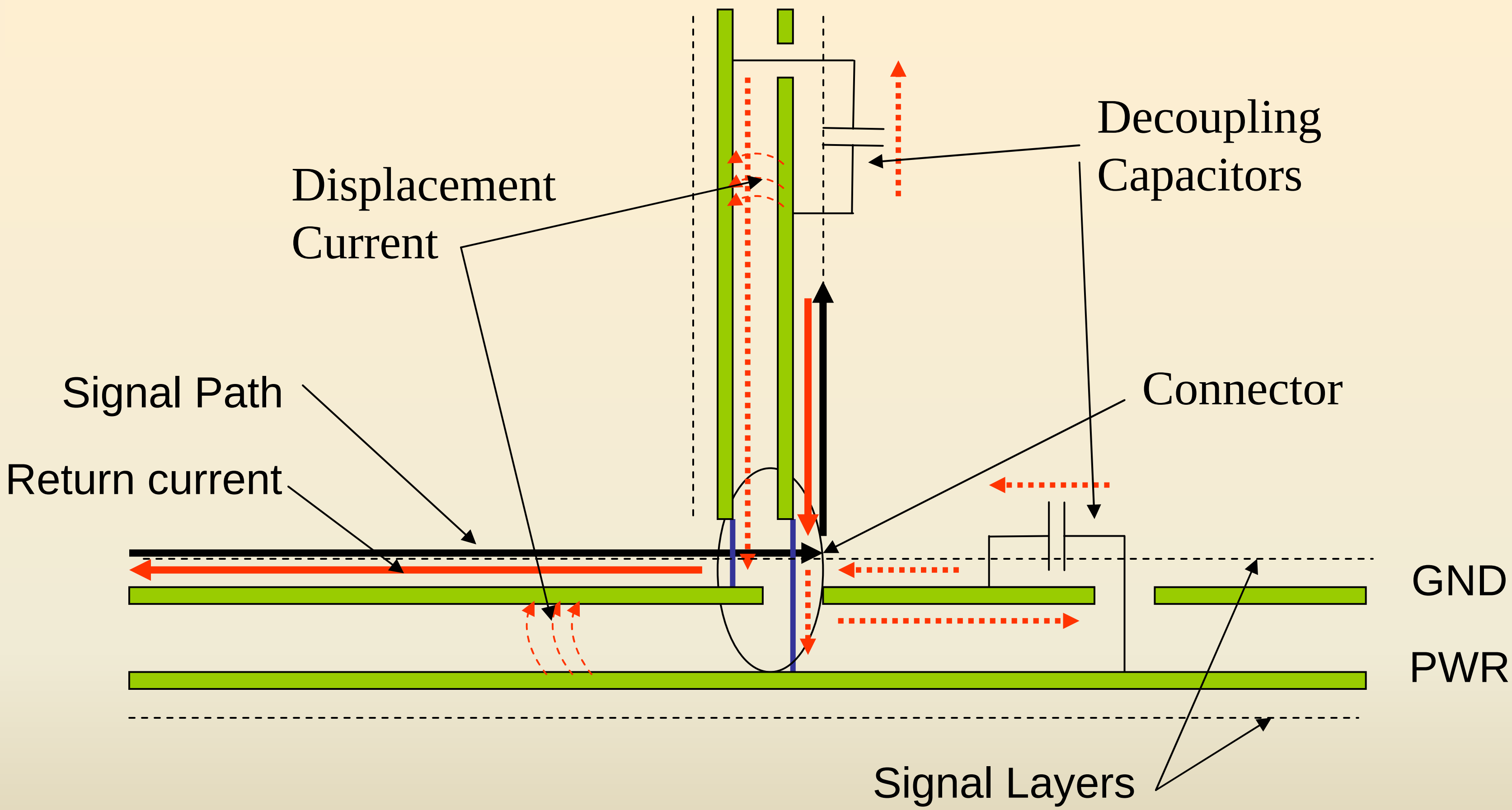
Mother/Daughter Board Connector Crossing

- Critical Signals must be referenced to same plane on both sides of the connector

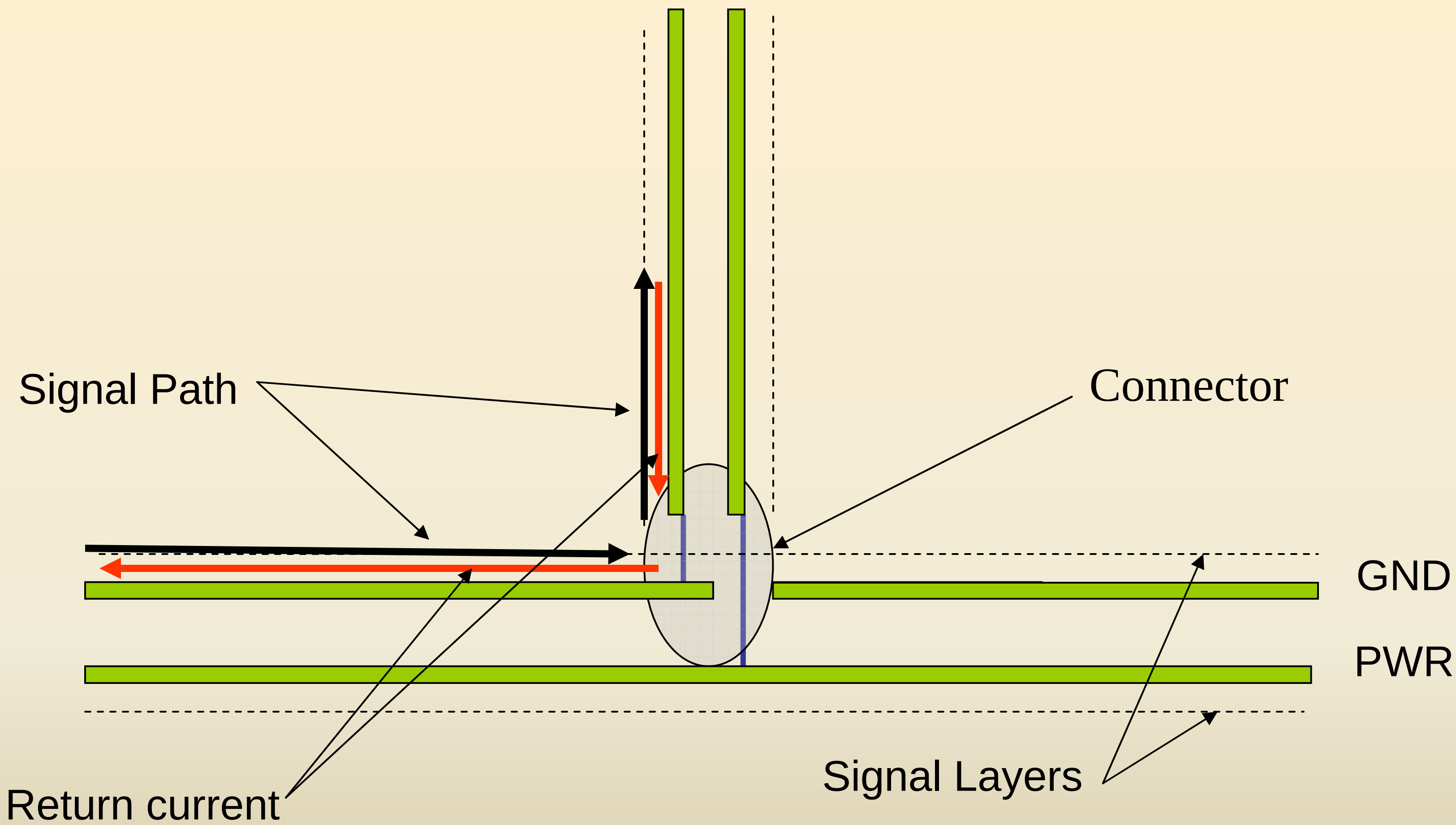
Mother/Daughter Board Connector Crossing



Return Current from Improper Referencing Across Connector



Return Current from Proper Referencing Across Connector



How Many “Ground” Pins Across Connector ???

- Nothing ***MAGICAL*** about “ground”
- Return current flow!
- Choose the number of power and “ground” pins based on the number of signal lines referenced to power or “ground” planes
- Insure signals are referenced against same planes on either side of connector

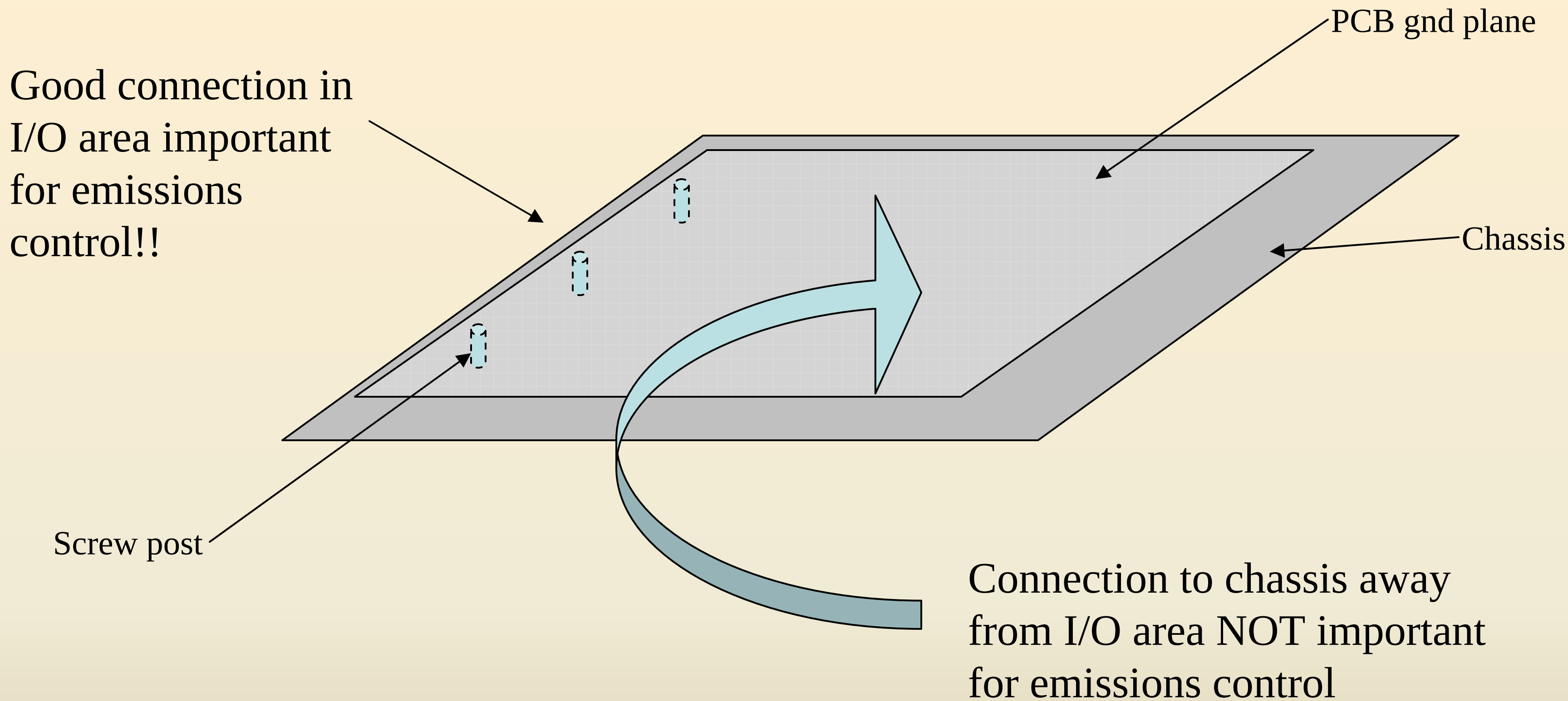
Think about Return Currents!!

- ✓ Reference plane should be continuous under all critical traces
- ✓ When Vias are necessary make sure there are two close decoupling capacitors
- ✓ When crossing a connector to a second board, make sure the critical trace is referenced to the same reference plane as the primary board

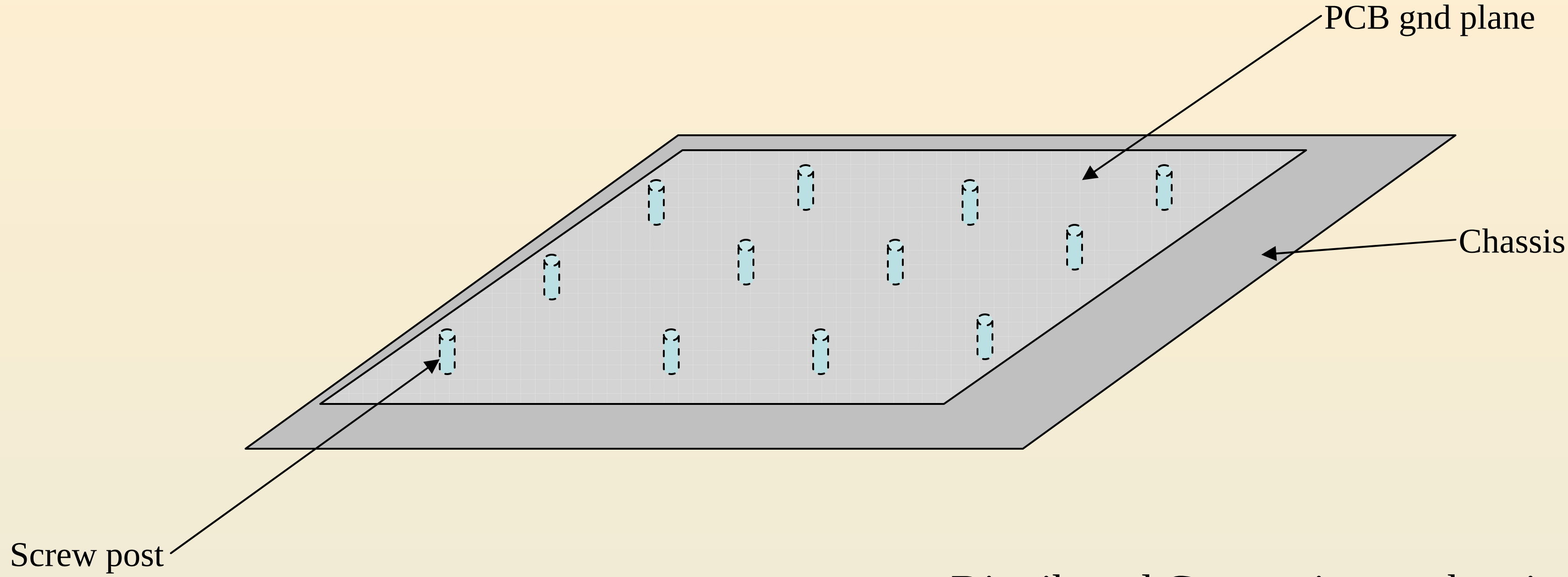
Ground-Reference Plane Noise
(Voltage Difference Across Plane)

- Connection of large PC ‘ground’ planes to chassis important
  - ESD current can result in voltage difference across ‘ground’ plane
  - Looks like input pulse to circuits
  - More connection to chassis will reduce this voltage difference

Connection to Chassis

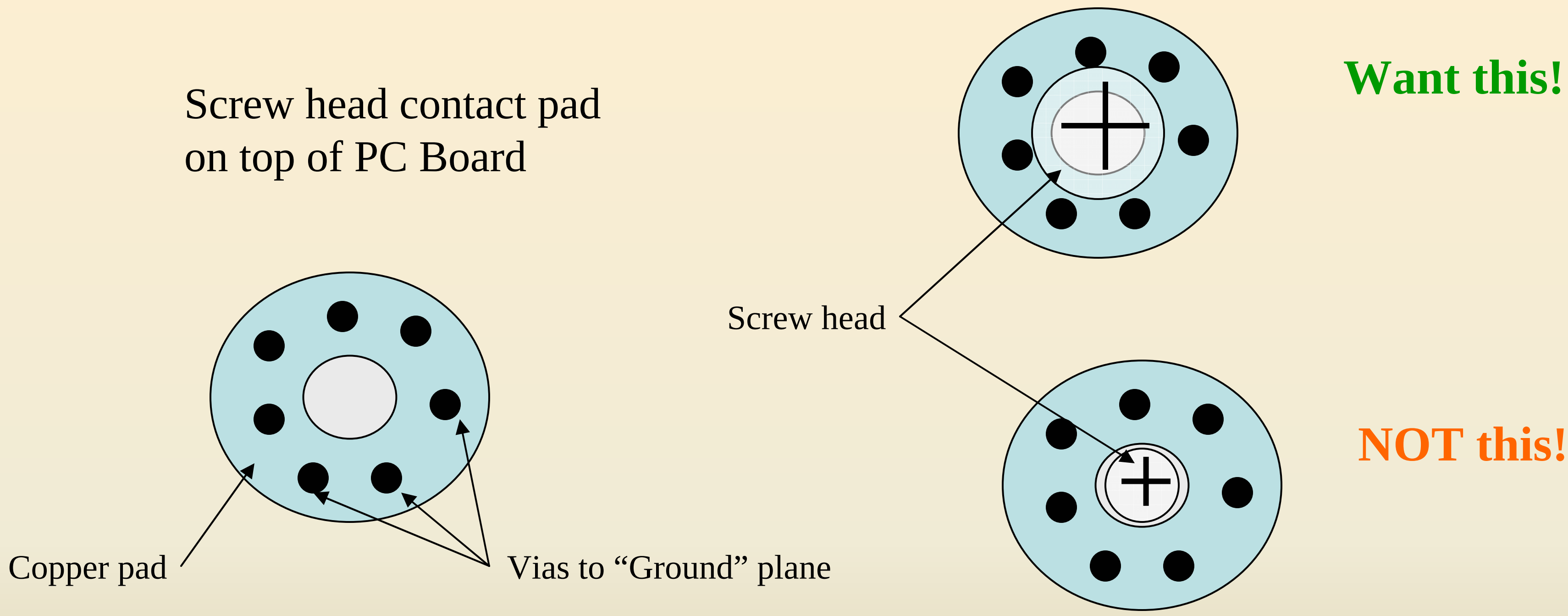


Connection to Chassis for ESD Control

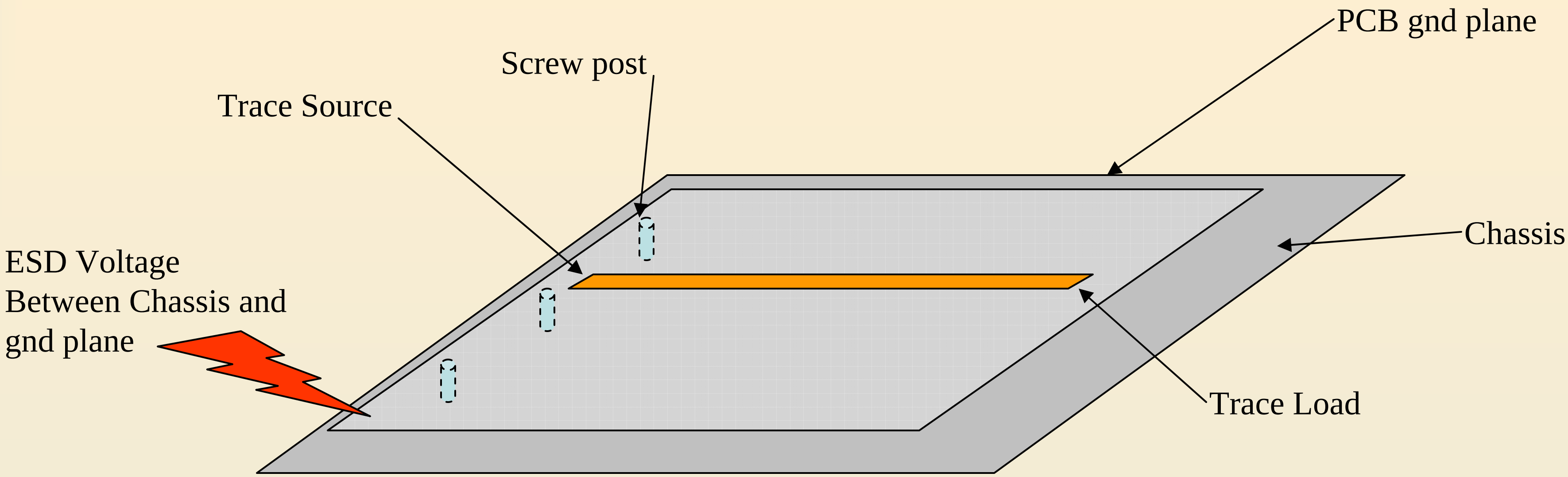


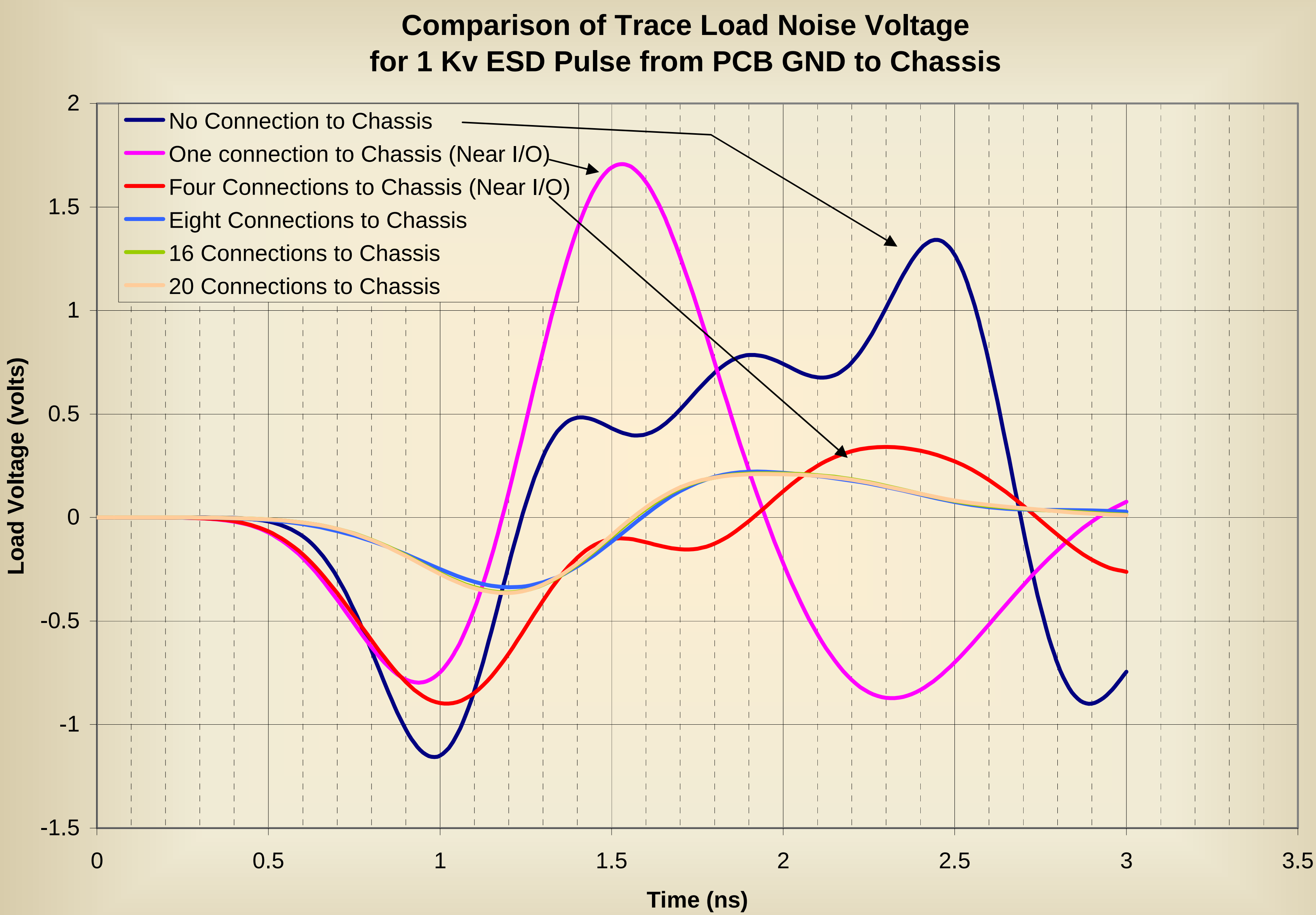
Distributed Connection to chassis away from I/O area very important for ESD control

Contacts for Chassis Connection

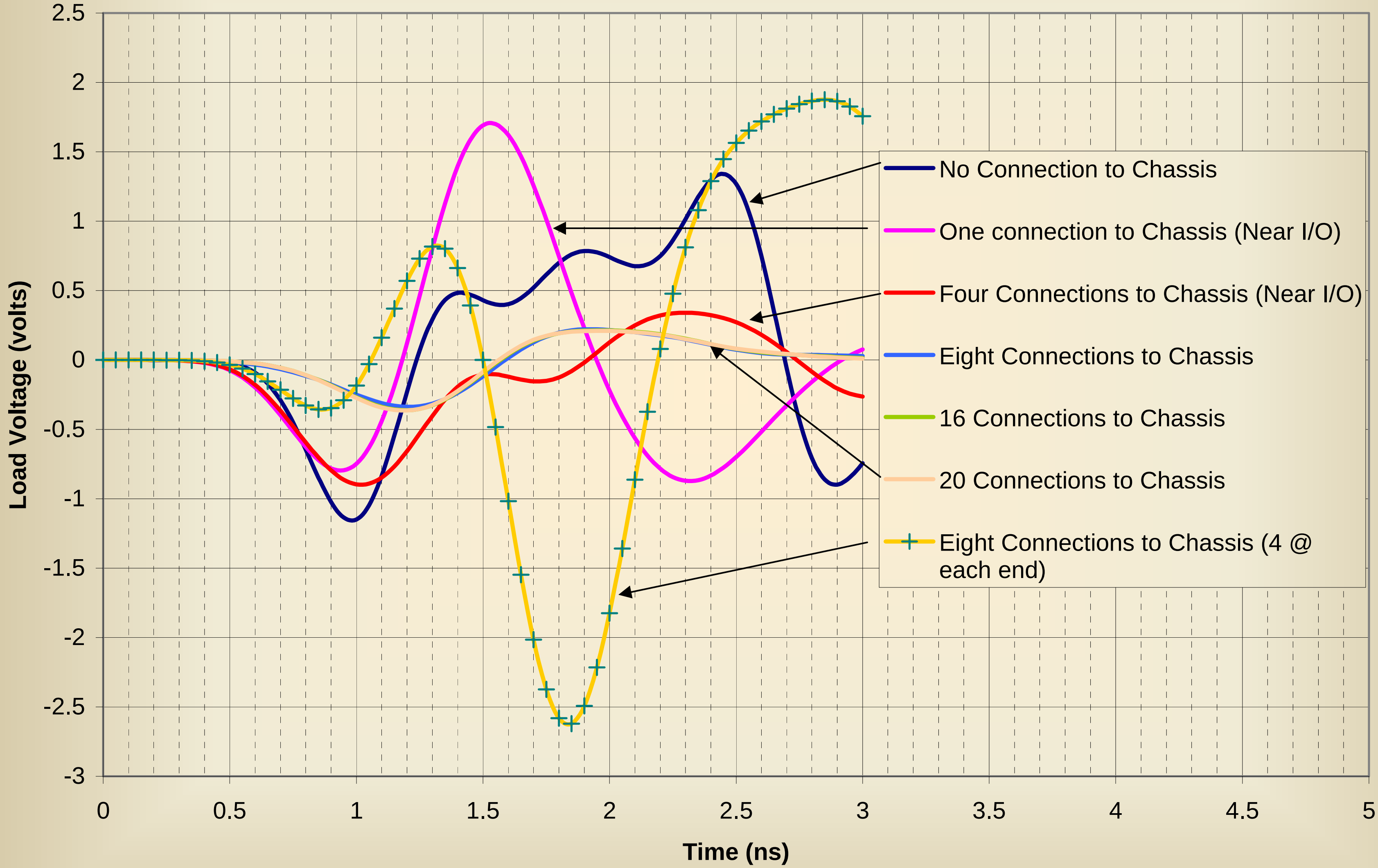


Model for Current Simulations

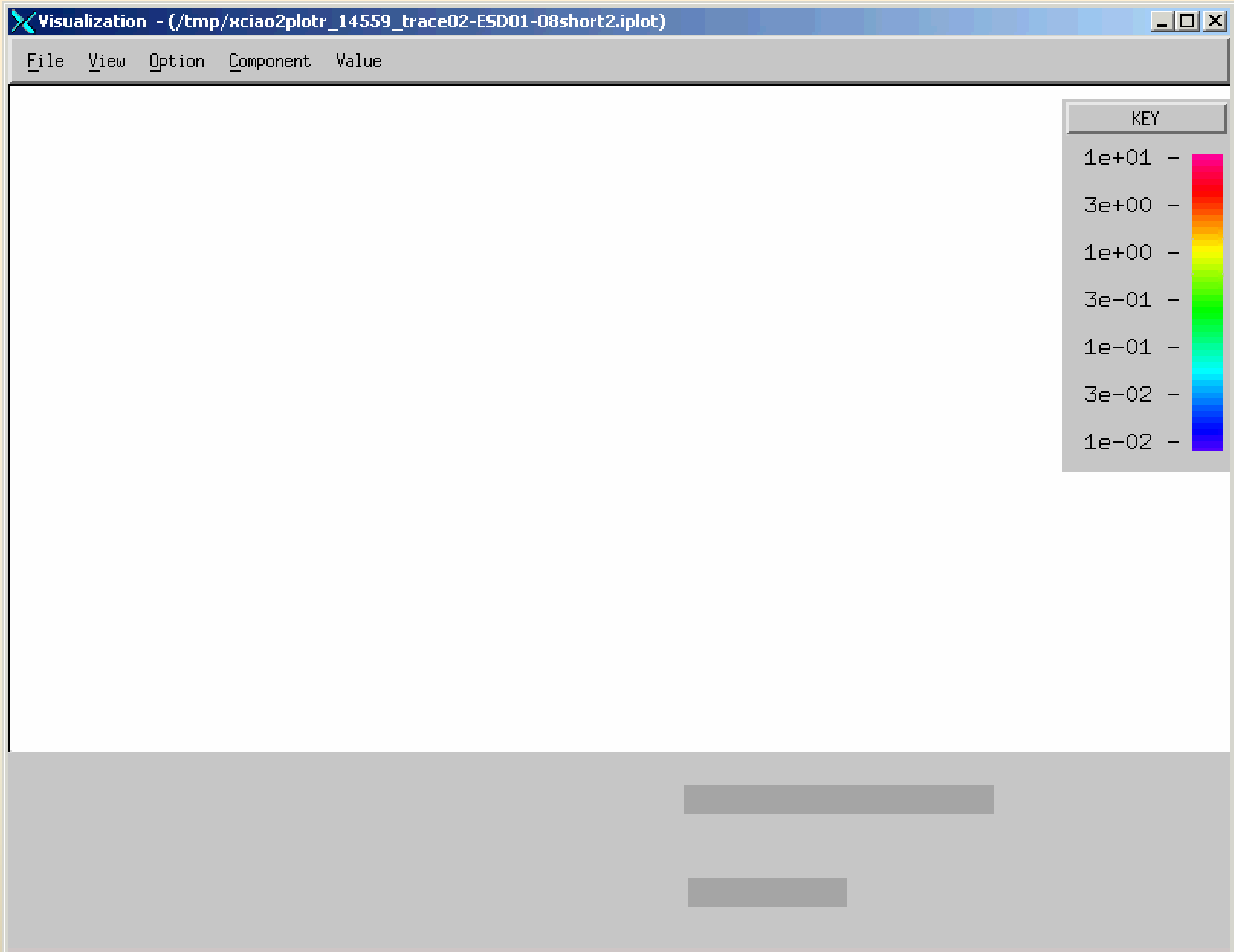



Comparison of Trace Load Noise Voltage
for 1 Kv ESD Pulse from PCB GND to Chassis
No Connection to Chassis
One connection to Chassis (Near I/O)
Four Connections to Chassis (Near I/O)
Eight Connections to Chassis
16 Connections to Chassis
20 Connections to Chassis
Load Voltage (volts)
Time (ns)
2
1.5
1
0.5
0
-0.5
-1
-1.5
0
0.5
1
1.5
2
2.5
3
3.5

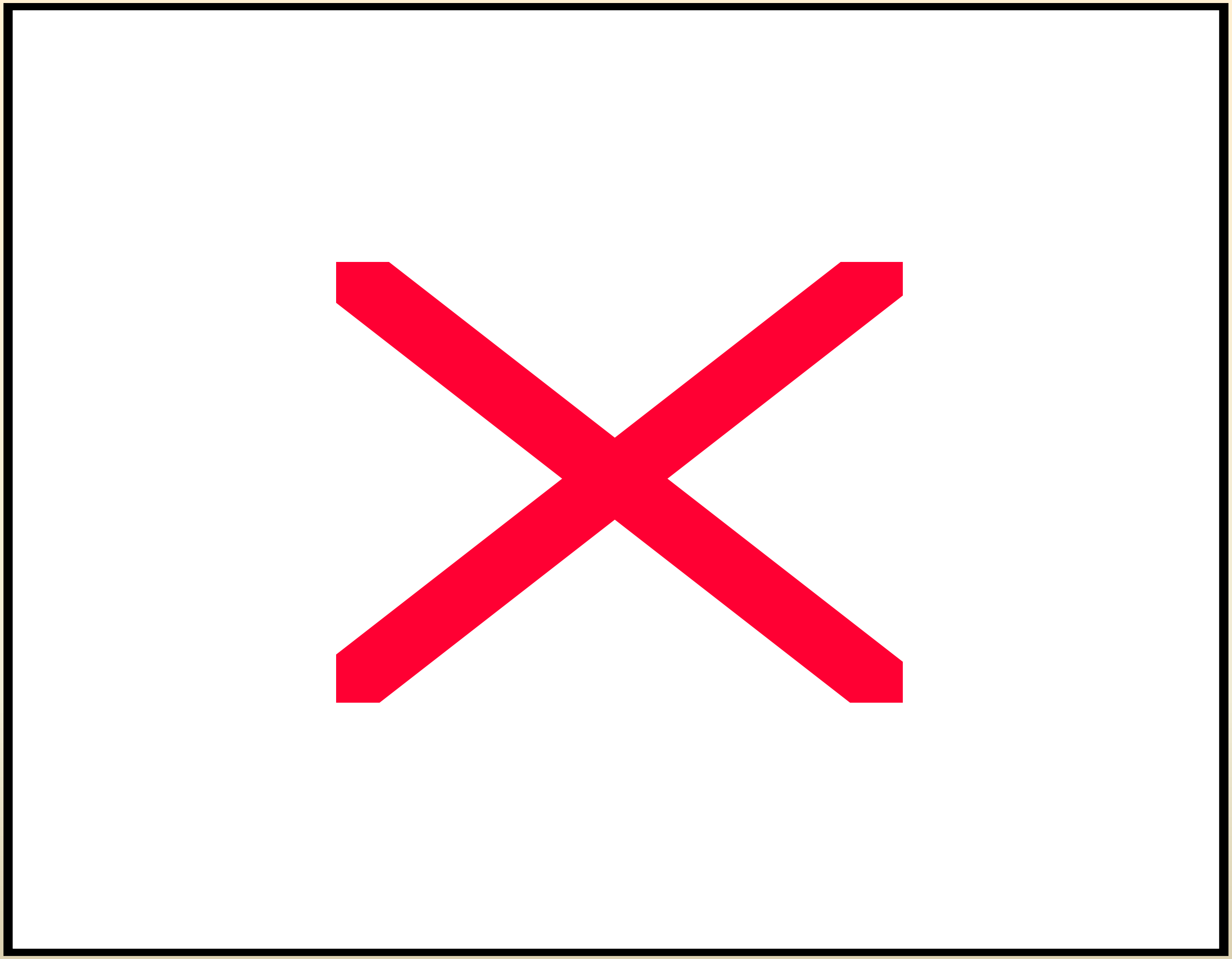
Comparison of Trace Load Noise Voltage for 1 Kv ESD Pulse from PCB GND to Chassis



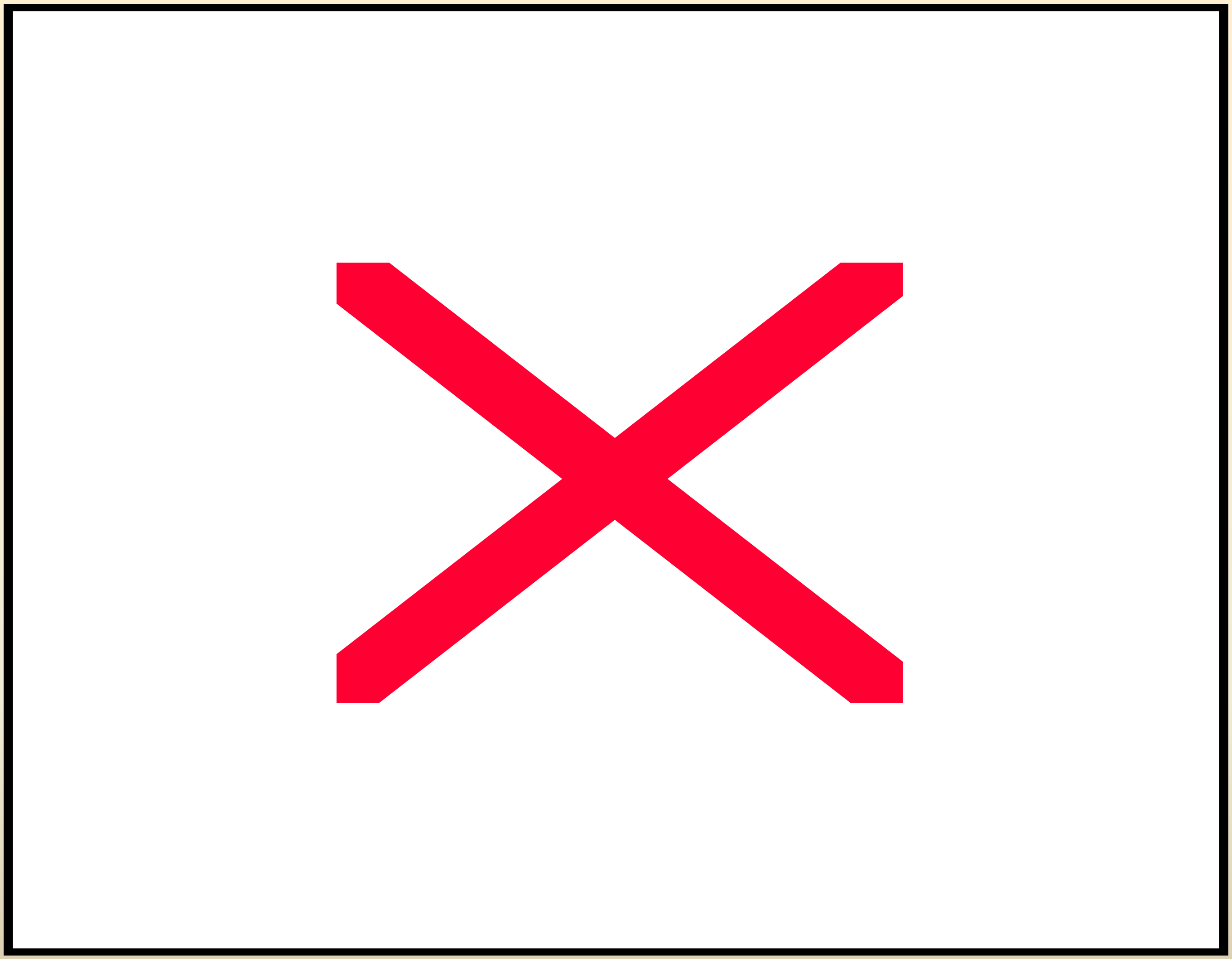
Current Flow w/One Screw Post



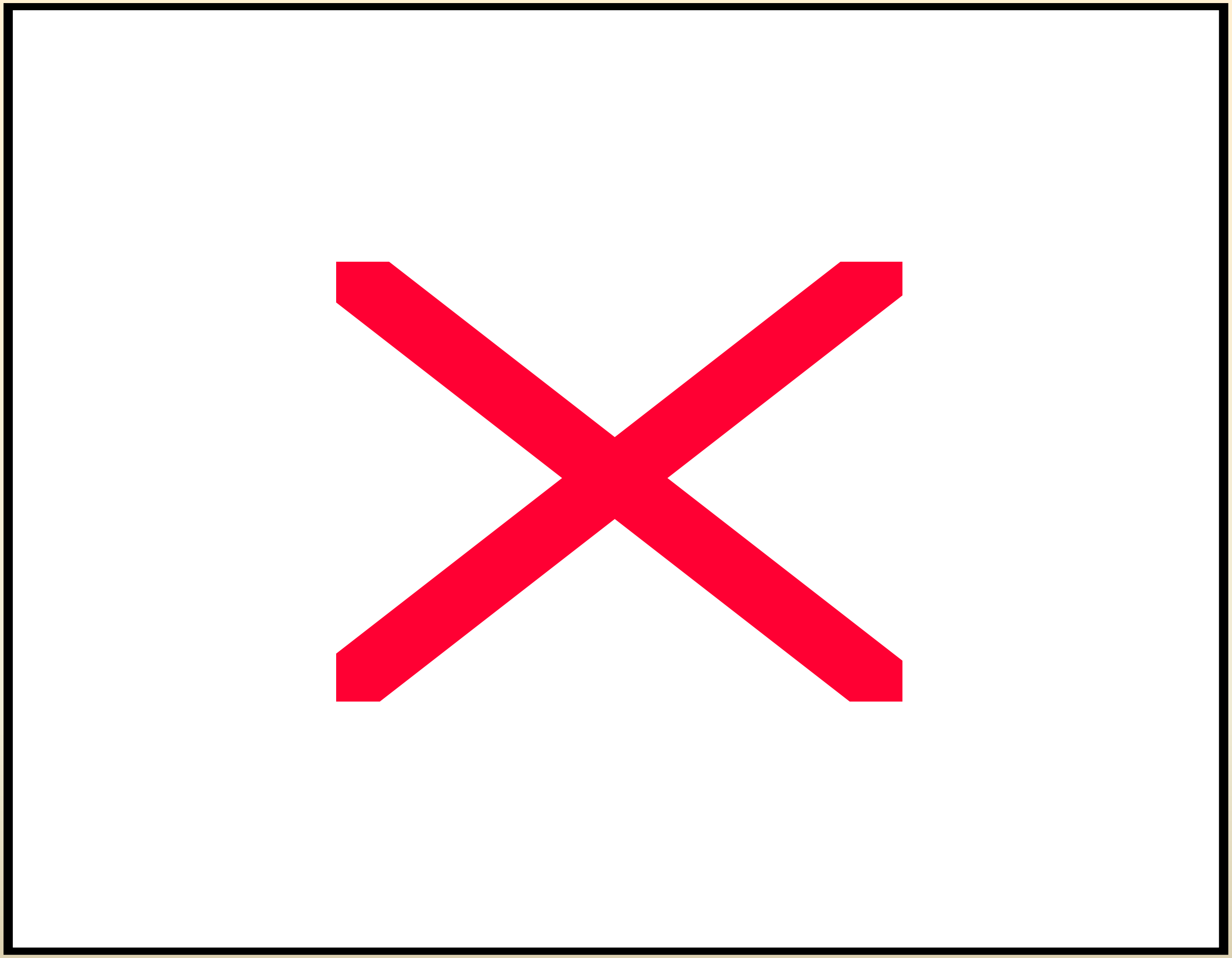
Current Flow w/Eight Screw Posts



Current Flow w/20 Screw Posts



Current Flow w/Eight Screw Posts (4 each end)



Number **ONE** Problem

- Intentional signal ***return current***

Where to Go for More?

- Limited selection of EMC design books
  - Beware of some popular books!!!
  - “PCB Design for Real-World EMI Control” (good choice)
    - Bruce Archambeault
- EMC ‘experts’
  - Experience is important
  - Again, beware ---- ask questions and understand WHY
- Cookbooks do not work! Every case is special and different