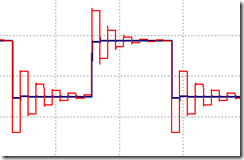
**Driver’s Output Impedance From IBIS**

[with 18 comments](https://blog.lamsimenterprises.com/2010/12/22/drivers-output-impedance-from-ibis/#comments)

In a recent post from the SI-list I subscribe to asks a question; “How do you find the driver impedance information from the IBIS file?” Most of the time we want this information so that we can explore mitigation techniques to control reflections caused by impedance discontinuities of the transmission path.

IBIS stands for Input/Output Buffer Information Specification and is controlled by the [IBIS Open Forum](http://www.vhdl.org/ibis/) organization. It is a device modeling technique used in simulation to provide a simple table based; non-proprietary buffer model derived from a real semi-conductor device. IBIS models can be used to characterize I/V output curves, rising/falling waveforms and pin parasitics of the device packaging.

[[](https://bertsimonovich.files.wordpress.com/2010/12/image7.png)](https://bertsimonovich.files.wordpress.com/2010/12/image7.png)When a driver’s output impedance is not matched to the transmission line characteristic impedance (Zo), there are reflections which causes ringing at the receiver as shown by the red waveform in the figure on the left. Terminating the transmission line at the receiver using a pull-up or pull-down resistor to match Zo is one way to cure this. Although this approach works fine, it is not the preferred method because the resistor value would be in the 45-70 Ohm range to match the typical single-ended transmission line impedances found in modern PCB designs. Such a low resistance causes additional loading on the driver resulting in higher power dissipation.

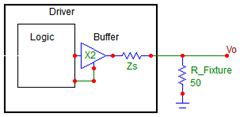
A better method is to add a series resistor at the end of the driver to make up the difference in impedance. For example if the buffer’s output impedance is 20 Ohms driving a 50 Ohm transmission line, you would add a 30 Ohm resistor in series with the output.

Because the buffer is a semi-conductor, it’s output impedance could vary based on rising/falling edge transitions, manufacturing process (slow, typical, fast), and the load it is driving. Since IBIS models are ASCII based, you can simply use your favourite text editor to view and quickly estimate the output impedance when driving 50 Ohms using two of the four V-T waveform tables.

Here’s how:

The output impedance is often different for the rising edge compared to the falling edge. To determine the output impedance of a low to high transition you would use the pull-down [Rising Waveform]; R\_fixture = 50; V\_fixture = 0.000 table. A sample of what this table looks like is shown below:

**[Rising Waveform]  
R\_fixture = 50.0000  
V\_fixture = 0.000**  
| time           V(typ)                V(min)               V(max)  
|  
0.000S          0.000V              0.000V                0.000V  
0.2000nS      0.000V              0.000V              -1.7835uV  
0.4000nS      -1.1143mV       -8.0018uV        -7.8340mV  
0.6000nS       0.1336V           -5.4161mV         0.9354V  
0.8000nS       1.1220V           -12.5300mV       2.3940V  
\*                   \*                        \*                        \*  
\*                   \*                        \*                        \*  
9.6000nS       2.5680V             2.1880V            2.7880V  
9.8000nS       2.5680V             2.1880V            2.7880V  
**10.0000nS  2.5680V         2.1880V        2.7880V**

[[](https://bertsimonovich.files.wordpress.com/2010/12/image11.png)](https://bertsimonovich.files.wordpress.com/2010/12/image11.png)The first three lines of the table tells us that the rising waveform has a 50 Ohm resistor connected to the buffer output and pulled-down to 0V as shown by the equivalent circuit on the right.

The combination of the output impedance (Zs) and the 50 Ohm load forms a simple voltage divider network described by the following equation:

[clip_image002](https://bertsimonovich.files.wordpress.com/2010/12/clip_image002.gif)

Where:

*VO* = Voltage at the output pin of the buffer  
*VDC* = Supply voltage  
*Zs* = Buffer impedance

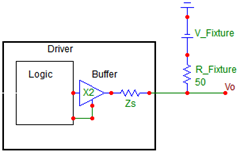
Solving for *Zs*, we end up with the following equation:

[clip_image002[5]](https://bertsimonovich.files.wordpress.com/2010/12/clip_image0025.gif)

If *VDC* is 3.3V, and *VO* is **2.568V** using the typical voltage at 10 nS from the V-T table above, the output impedance for the rising edge into 50 Ohms is equal to **14.25 Ohms**.

To determine the output impedance of a high to low transition you would use the pull-up [Falling Waveform]; table similar to the following example:

**[Falling Waveform]  
R\_fixture = 50.0000  
V\_fixture = 3.3000  
V\_fixture\_min = 3.0000  
V\_fixture\_max = 3.4500**| time           V(typ)              V(min)              V(max)  
|  
**0.000S       3.3000V         3.0000V         3.4500V**0.2000nS       3.3000V             3.0000V             3.4500V  
0.4000nS       3.2995V             3.0000V             3.4500V  
\*                   \*                        \*                        \*  
\*                   \*                        \*                        \*  
9.4000nS       0.5598V             0.6824V             0.4812V  
9.6000nS       0.5598V             0.6824V             0.4812V  
9.8000nS       0.5598V             0.6824V             0.4812V  
**10.0000nS  0.5598V         0.6824V         0.4812V**

[[](https://bertsimonovich.files.wordpress.com/2010/12/image6.png)](https://bertsimonovich.files.wordpress.com/2010/12/image6.png)

This time, the table tells us the falling waveform has a 50 Ohm resistor connected to the buffer output and pulled-up to V\_fixture as shown by the equivalent circuit on the right.

The output impedance is calculated by the following equation:

[clip_image002[11]](https://bertsimonovich.files.wordpress.com/2010/12/clip_image00211.gif)

Where:

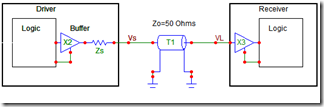
*VO* = Output voltage when the driver is sinking current  
*V\_Fix* = Voltage of the test fixture

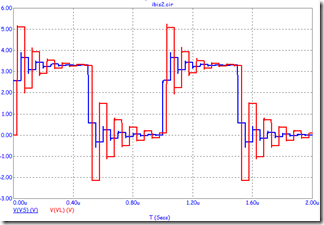
Using typical values for ***V\_Fix* = 3.3V** and ***VO* = 0.5598V** at 10nS,  ***Zs* = 10.21 Ohms**.

As you can see for this particular IBIS model, the output impedance varies depending on the edge transition. For a rising edge, the output impedance is 14.25 ohms and 10.21 Ohms for a falling edge when using the typical values. The impedances will also vary under min/max conditions.

If your load is something other than 50 Ohms, you should NOT rely on this simple method for signoff. Instead you should simulate it if the design is critical. Sometimes though we need a quick ball park number to gain some insight of a particular design or to give us some intuition of what to expect from simulation.

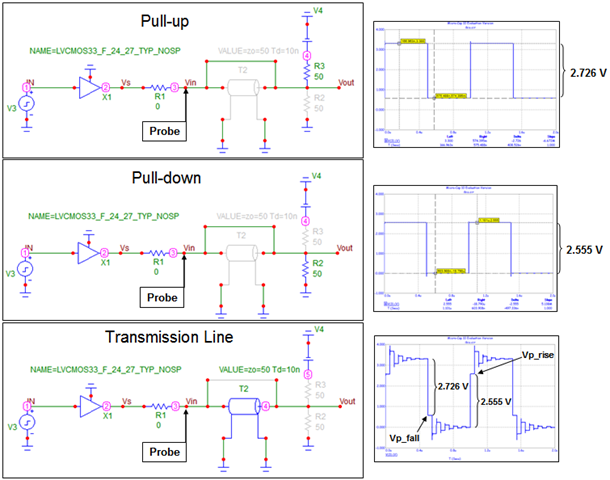
You can validate this methodology using any Spice-like simulator which supports IBIS models. There are many to choose from like HSPICE, Hyperlynx, Cadence Spectraquest, Ansoft Designer from ANSYS and Agilent ADS to name a few. Chances are if you work for a large company, you already have access to some of these tools. If you are a student or someone just starting to learn about signal integrity, there is an alternative available. Fortunately, [Spectrum Software](http://www.spectrum-soft.com/index.shtm) offers Micro-cap 10; a free trial of its SPICE software you can use. Although it is limited to the number of components, nodes and performance, it is more than adequate for this and other signal integrity studies. Personally, I found it quite easy to pick up and get productive fairly quickly.

[[](https://bertsimonovich.files.wordpress.com/2010/12/image3.png)](https://bertsimonovich.files.wordpress.com/2010/12/image3.png)For the purpose of the analysis, the output buffer and it’s impedance (Zs) can be simplified as shown by the schematic on the left. When the buffer drives a 50 Ohm transmission line, you typically see the waveforms at the driver’s output (blue) and receiver’s input (red) as shown in the following plot:

[[](https://bertsimonovich.files.wordpress.com/2010/12/image18.png)](https://bertsimonovich.files.wordpress.com/2010/12/image18.png)The initial step in the rising and falling edges of the blue waveform (Vs) is due to the voltage divider action between Zs and Zo. Let us call these steps as a “porch” and designate the voltages as Vp\_rise/Vp\_fall for the rising and falling porches respectively.

Vp\_rise is equivalent to the maximum voltage of Rising Waveform table found in the IBIS model. Vp\_fall is equivalent to the minimum voltage of Falling Waveform table.

The analysis is best summarized by the following Figure:

[](https://bertsimonovich.files.wordpress.com/2010/12/image4.png)

A common circuit topology was built using the schematic editor. The respective greyed-out devices are disabled during simulation making it a convenient way of switching them in and out for the different topologies. R1 is reserved for the series termination resistor and is set to 0 Ohms initially. Once the output impedance is determined, R1 is set to the difference between Zo and the output impedance Zs.

The top topology simulates the Pull-up test fixture and used to verify the Falling Waveform table in the IBIS model. Similarly, the center topology simulates the Pull-down test fixture for the Rising Waveform table. The bottom topology has the output buffer driving a real world 50 Ohm transmission line.

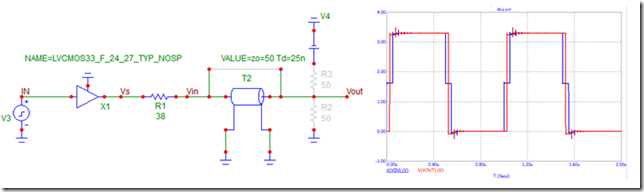
The results of the simulations are shown adjacent to their respective topologies. Referring to the last case, Vp\_rise=**2.555V** and Vp\_fall=3.3V-2.726V=**0.574V** .  As you can see there is excellent correlation when you compare them against the IBIS model’s voltages of  **2.568V** and  **0.5598V** respectively. Using the simulated voltages and solving for Zs, we get **14.58 Ohms** and **10.53 Ohms** respectively.

Because Zs is different for the rise time and fall time, you can never perfectly compensate for the impedance mismatch. The best approach is sometimes to take the average value between the two. In this case Zs\_avg=**12.56 Ohms**.

Once Zs is known, the series resistor can be calculated as follows:

[clip_image002[1]](https://bertsimonovich.files.wordpress.com/2010/12/clip_image0021.gif)

When 38 ohms is substituted in the transmission line topology, the waveform is clean with minimum reflections as shown by the following results:

[](https://bertsimonovich.files.wordpress.com/2010/12/image5.png)

In conclusion, the methodology presented here is a simple and effective way to predict the driver’s output impedance from an IBIS model. Try it next time someone asks you the question, “How do you find the driver impedance information from the IBIS file?”