ECSE-534
Analog Microelectronics
Assignment #2

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***Abstract*—A CMOS amplifier was designed, simulated, and analyzed using Cadence to meet a set of specifications. The amplifier was found to have a DC gain of $65.9\,\mathrm{dB}$, poles at $7.4\,\mathrm{kHz}$ and $85\,\mathrm{MHz}$, distortion of $0.05\,\%$ when swinging at half the supply range in a unity-gain configuration, input-referred spot noise of $40.0\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at $1\,\mathrm{MHz}$, and a static power dissipation of $150.7\,\mu\mathrm{W}$. All of these criteria exceed the given specifications.**

I. Introduction

THIS report follows the design, simulation, and analysis of a CMOS amplifier using a 0.13 micron process from IBM. We used Cadence and Analog Environment to simulate the design in said process. The amplifier was required to meet the following specs:

- DC gain $\geq 60\,\mathrm{dB}$.
- Amplifier poles at approx. $10\,\mathrm{kHz}$ and $100\,\mathrm{MHz}$. Others above this.
- Output voltage swings of at least $50\,\%$ of the supply full scale with a distortion less than $0.2\,\%$ in a unity-gain configuration.
- Input-referred PSD Noise Voltage less than $100\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at $1\,\mathrm{MHz}$.
- Static power dissipation less than $200\,\mu\mathrm{W}$.

In addition, we were assigned a supply voltage of $1.2\,\mathrm{V}$, a common mode input voltage of $0.5\,\mathrm{V}$, and a load capacitance of $0.5\,\mathrm{pF}$. To meet these specifications, we first used a hand analysis to determine a feasible topology and some design goals. Then, we used a first order simulation, with biasing done using ideal voltage and current sources, to determine the bias points of our amplifier. Afterwards, we used the insight gained from the simulation to replace the ideal sources with transistors and a bias network. Finally, we analyzed the performance of the amplifier and confirmed that it meets the specs.

II. Initial Design

We first had to decide on a topology. Since the maximum DC gain of a transistor in the given process is around $30\,\mathrm{V/V}$, a simple two-stage op-amp was deemed insufficient. In fact, at least three stages are required to obtain the desired gain. In order to minimize the complexity of the frequency response and maximize our input swing, we therefore chose to implement a folded-cascode stage followed by a common source stage as our topology. A schematic of the essential components is shown in Figure 1.

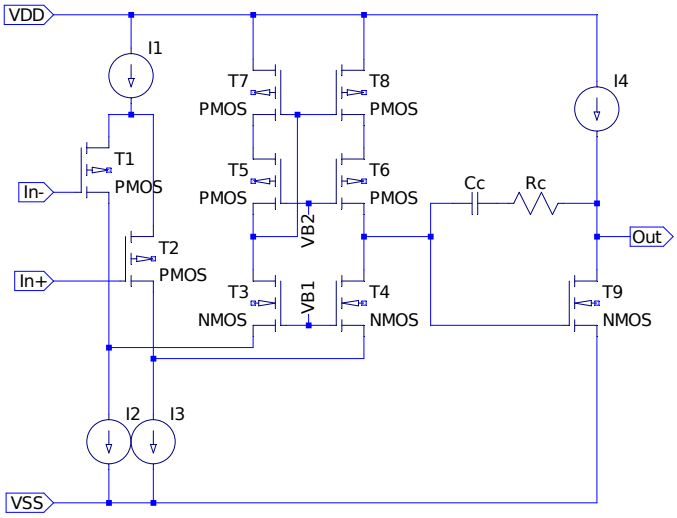

Fig. 1. A schematic of the topology used for the amplifier.

We next analyzed said amplifier using a simple small signal model, as shown in Figure 2. The parameters in the model are given by

$$G_{m1} = g_{m2}$$

$$R_{o1} = (r_{o2} g_{m4} r_{o4}) \parallel (r_{o8} g_{m6} r_{o6})$$

$$G_{m2} = g_{m9}$$

$$R_{o2} = r_{o9}$$

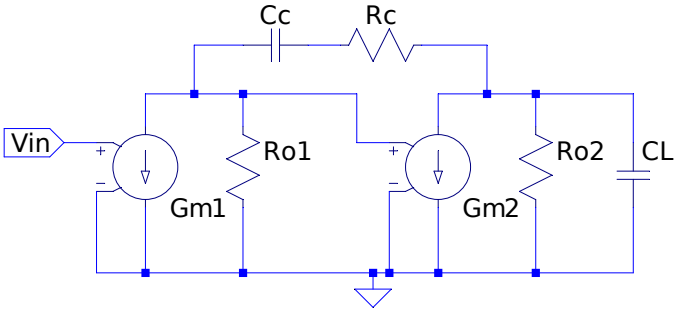

Fig. 2. A small signal model of the amplifier in Figure 1.

It can be shown [1] that the gain, poles, and zero of the amplifier can be approximated as

$$A = G_{m1} R_{o1} G_{m2} R_{o2}$$

$$f_{p1} = G_{m1}/(2\pi C_c A)$$

$$f_{p2} = G_{m2}/(2\pi C_L)$$

$$f_{z1} = 1/(2\pi C_c(1/G_{m1} - R_c))$$

Using $C_L = 0.5\,\text{pF}$, we obtain $G_{m2} \approx 310\,\mu\text{A/V}$. Taking $C_c = 0.5\,\text{pF}$ and $A = 5000\,\text{V/V}$ for good measure, we also obtain $G_{m1} \approx 160\,\mu\text{A/V}$. Finally, placing the zero at $1.2f_{p2}$ (in the left half-plane) to smooth out the step response, we obtain $R_c \approx 8.9\,\text{k}\Omega$. Using these parameters as a rough guide, we proceed to performing a first order simulation to find the bias points.

III. First Order Simulation

To determine the bias conditions, we replaced current sources I_1, I_2, and I_3 in Figure 1 with $0.2\,\text{V}$ voltage sources, meant to represent current mirror transistors operating with $V_{DS} \approx 0.2\,\text{V}$. We chose to use a length of $L = 0.4\,\mu\text{m}$ for each transistor, several times the minimum length for the process, for adequate analog performance. We then swept the widths W_1 and W_2 until we obtained $g_{m1} = g_{m2} \approx 160\,\mu\text{A/V}$. With these in hand, we set $V_{B1} = 0.55\,\text{V}$ and $V_{B2} = 0.6\,\text{V}$ to allow for the proper biasing of transistors T_3 to T_8. Then, we set $W_5 = W_6 = W_7 = W_8 = 0.4\,\mu\text{m}$ and swept W_3 and W_4 until we obtained a gate voltage for T_9 of $V_{G9} \approx 0.5\,\text{V}$. Finally, we swept both I_4 and W_9 until we obtained $V_{Out} \approx 0.5\,\text{V}$ and $g_{m9} \approx 310\,\mu\text{A/V}$ to meet our design goals and obtain sufficient output swing. The resulting dimensions are shown in Table I, and the resulting currents are shown in Table II. We note with the current setup, we've only used $114\,\mu\text{W}$ of the power budget, indicating that this criterion is likely to be met with this design.

TABLE I
TRANSISTOR DIMENSIONS OBTAINED AFTER A FIRST ORDER SIMULATION OF THE AMPLIFIER.

	T1	T2	T3	T4	T5	T6	T7	T8	T9
W (μm)	3.5	3.5	0.65	0.65	0.4	0.4	0.4	0.4	1.4
L (μm)	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4

TABLE II
BIAS CURRENTS OBTAINED AFTER A FIRST ORDER SIMULATION OF THE AMPLIFIER.

	I_1	I_2	I_3	I_4
I (μA)	37.5	21.3	21.3	52.0

We next performed a pole-zero analysis to see if our design is on the right track to meet the required pole placement. Using our previously calculated values for C_c and R_c, we obtained poles at $5.6\,\text{kHz}$ and $108\,\text{MHz}$, as well as a zero at $55\,\text{MHz}$. These are close enough to the specifications for now, and we will tweak them later when we introduce an actual bias network.

IV. Biasing

We then replaced the ideal sources with a bias circuit. The completed amplifier is shown in Figure 3. Transistors T_{14}, T_{15} and resistor R_b generate a reference current that is then mirrored throughout the amplifier to create bias conditions. For the bias network, we only used multiples of a unit size transistor to facilitate matching during layout. Our unit size was $W = 0.4\,\mu\text{m}$, $L = 0.4\,\mu\text{m}$. With this in mind, we chose T_{14} and T_{15} to be composed of 10 unit size transistors each, and we swept R_b to obtain a bias current of $10\,\mu\text{A}$. This allowed us to allocate currents in multiples of $1\,\mu\text{A}$. We thus obtained $R_b = 47\,\text{k}\Omega$.

Transistors T_{16}, T_{17}, and T_{18} create the bias voltage V_{B1}. In order to stabilize the circuit, this voltage is referenced from the sources of T_3 and T_4. This provides negative feedback which lowers V_{B1} if the drain voltages of T_{11} and T_{12} drop. Transistors T_{19} and T_{20} create the bias voltage V_{B2}. Finally, transistors T_{10} to T_{13} generate the bias currents I_1 to I_4.

We first set the bias network to provide the bias conditions determined in the previous simulation. Then, we corrected for any deviations in order to obtain the proper bias points. One exception was T_9. During closed loop testing, we found that this transistor should be set at a lower current in order to maximize the swing. However, this bias condition would lead to triode operation in open loop. This is not actually a problem since we can insert an offset voltage during open loop testing and negative feedback fixes the bias point during closed loop testing. The final transistor dimensions are shown in Tables III and IV.

TABLE III
FINAL TRANSISTOR DIMENSIONS (PART 1).

	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10
W (μm)	3.5	3.5	0.4	0.4	2.4	2.4	0.4	0.4	1.2	13.6
L (μm)	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4

TABLE IV
FINAL TRANSISTOR DIMENSIONS (PART 2).

	T11	T12	T13	T14	T15	T16	T17	T18	T19	T20
W (μm)	8.0	8.0	24.0	4.0	4.0	2.8	20.0	20.0	1.6	0.4
L (μm)	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4

We then reexamined the frequency response of the amplifier. We swept C_c and R_c to obtain the required poles and zeros, and found $C_c = 1\,\text{pF}$ and $R_c = 3\,\text{k}\Omega$. Using these values, we obtained poles at $7.4\,\text{kHz}$ and $85\,\text{MHz}$, and a zero at $102\,\text{MHz}$, which meets the specifications.

V. DC Analysis

Next, we measured the DC properties of the amplifier using the setup shown in Figure 4, where the $1.2\,\text{V}$ power supply has been omitted for clarity.

We first set the common mode voltage V_{cm} to $0.5\,\text{V}$ and swept the differential mode voltage V_d from $-5\,\text{mV}$ to $5\,\text{mV}$. The results are shown in Figure 5. From this figure, we can see that the offset voltage is $V_{os} = 335\,\mu\text{V}$. We can also see that

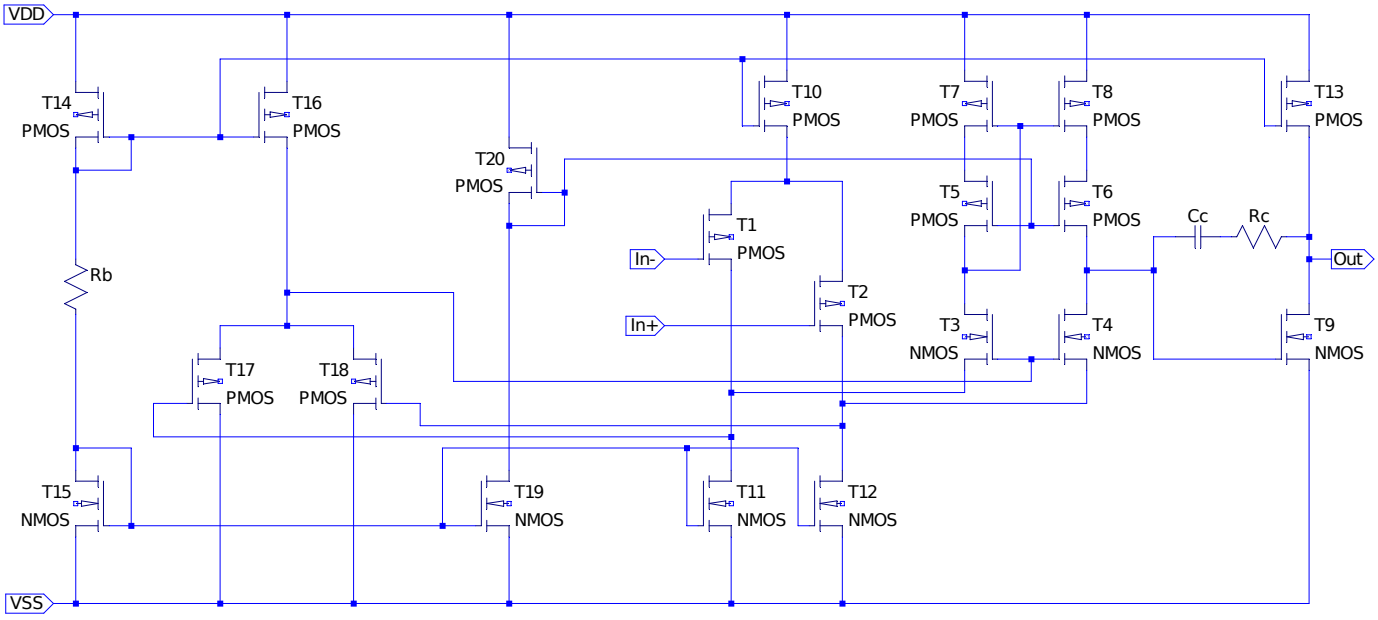

Fig. 3. A schematic of the complete amplifier with bias network included.

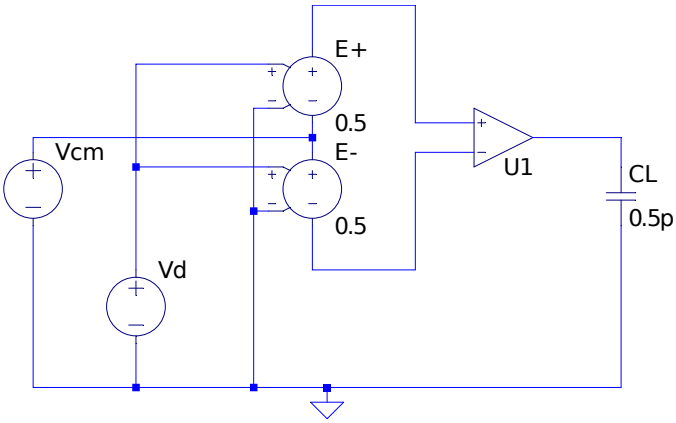

Fig. 4. A schematic of the setup used for taking open loop measurements of the amplifier.

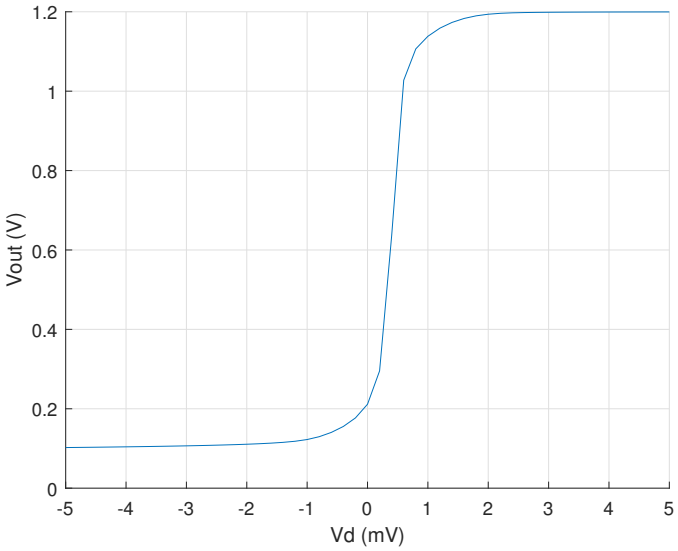

Fig. 5. DC differential mode transfer characteristic of the amplifier.

the output voltage range is $0.295\,\mathrm{V}$ to $1.03\,\mathrm{V}$, corresponding to an input voltage range of $0.2\,\mathrm{mV}$ to $0.6\,\mathrm{mV}$.

We next measured the common mode transfer characteristic by sweeping V_{cm} over the entire supply range with $V_d = 0\,\mathrm{V}$. We also corrected the offset voltage by adding a source between the two input terminals with voltage V_{os}. The results are shown in Figure 6. From this figure, we can see that the input common mode voltage can range from $0\,\mathrm{V}$ to about $1\,\mathrm{V}$. This is to be expected from the PMOS input stage, which limits the upper common mode level but allows lower common mode levels beyond even $0\,\mathrm{V}$. However, we do see that there are some non-linearities around $0.6\,\mathrm{V}$, which might produce distortion for large input signals.

We also analyzed the power dissipation of the amplifier. During the DC analysis, the amplifier drew a current of $125.6\,\mu\mathrm{A}$, which corresponds to a static power dissipation of $150.7\,\mu\mathrm{W}$. Thus, we have met the power dissipation goal of $200\,\mu\mathrm{W}$.

VI. AC Analysis

We next measured the AC properties of the amplifier using the same setup as in Figure 4 with the offset corrected. We first measured the differential mode frequency response, and the results are shown in Figure 7. From this figure, we can see that the DC gain is $65.9\,\mathrm{dB}$, which meets the specification of DC gain $\geq 60\,\mathrm{dB}$. A pole-zero analysis showed that the amplifier has its first two poles at $7.4\,\mathrm{kHz}$ and $85\,\mathrm{MHz}$, which are both close to the targets of $10\,\mathrm{kHz}$ and $100\,\mathrm{MHz}$, respectively. In addition, the first zero is at $102\,\mathrm{MHz}$, which is around 1.2 times the second pole, thus ensuring a smooth frequency response, as we will see later. We can also see that our unity-gain bandwidth is $14.4\,\mathrm{MHz}$.

Next, we measured the AC noise of the amplifier using the

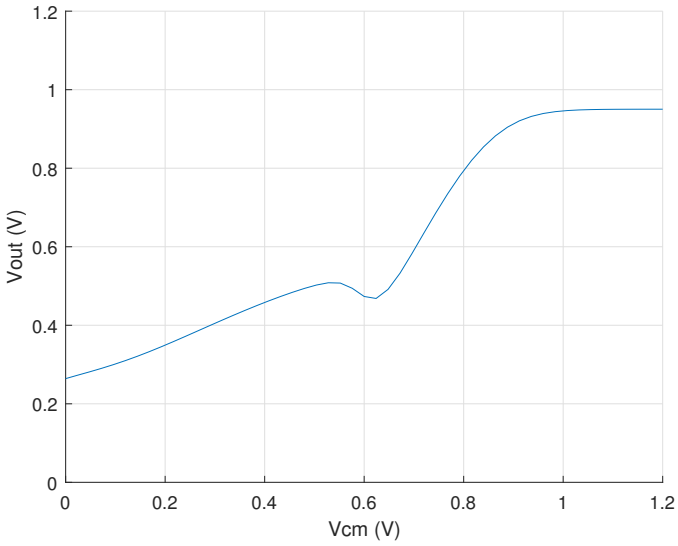

Fig. 6. DC common mode transfer characteristic of the amplifier.

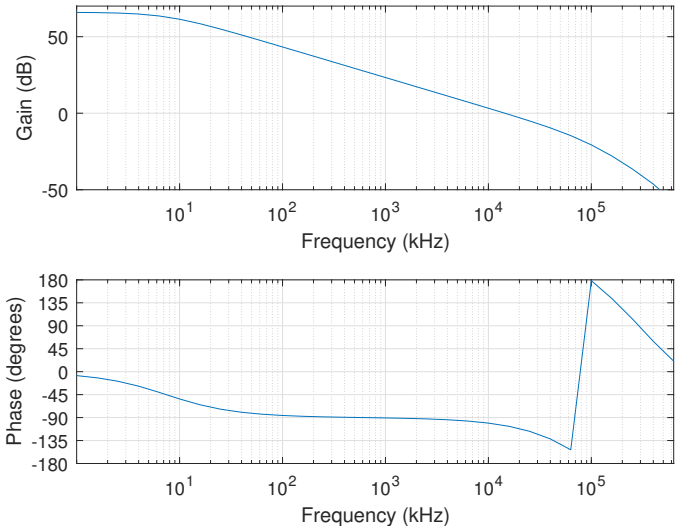

Fig. 7. AC differential mode frequency response of the amplifier.

same setup. Using V_d as our noise source, we obtained the output-referred spectral noise density shown in Figure 8. The noise was measured from $10\,\mathrm{Hz}$ to $1\,\mathrm{MHz}$, with the RMS value calculated to be $108\,\mathrm{mV}$ over this bandwidth. We note that the noise is dominated by flicker noise. In addition, we measured the input-referred spot noise at $1\,\mathrm{MHz}$, and found $40.0\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. This satisfies the upper limit of $100\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ given in the specifications.

VII. Transient Analysis

We next measured the closed loop transient behaviour of the amplifier using the setup shown in Figure 9, where the $1.2\,\mathrm{V}$ supply has been omitted for clarity.

First, we input a fast $100\,\mathrm{mV}$ pulse to the circuit, starting at a DC bias point of $0.5\,\mathrm{V}$. The resulting output is shown in Figure 10. From this graph, we can measure the rise time as $24.5\,\mathrm{ns}$. Since there is no overshoot, there is no real measure of the settling time.

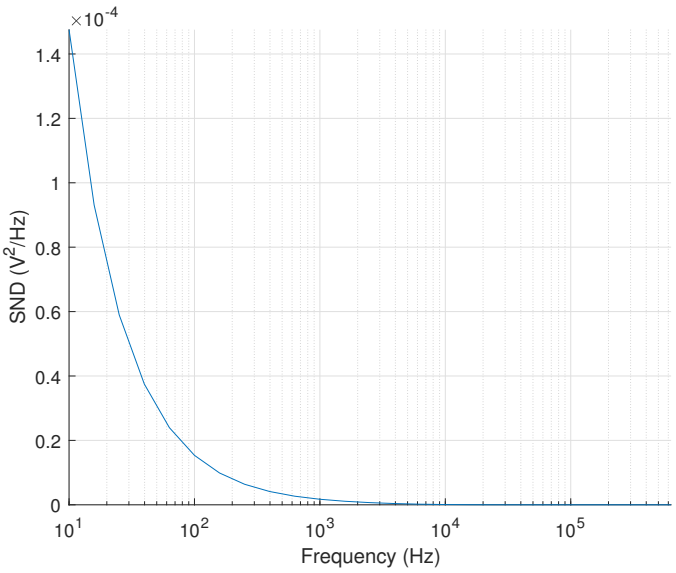

Fig. 8. Output-referred AC noise of the amplifier.

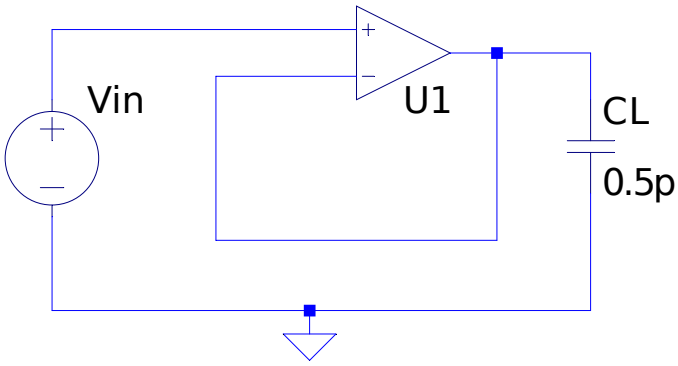

Fig. 9. A schematic of the setup used for taking closed loop measurements of the amplifier.

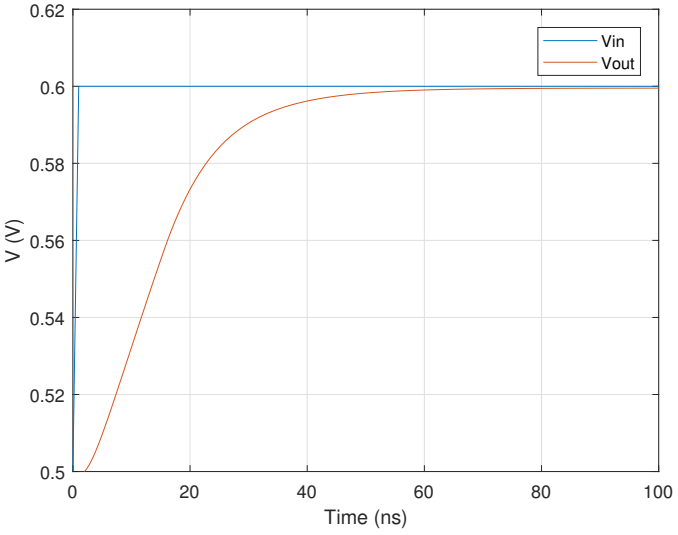

Fig. 10. Transient step response of the amplifier.

Next, we measured the distortion present when we input a $0.6\,\mathrm{V}$ peak-peak sine wave centered around the common mode

point of $0.5\,\mathrm{V}$. This corresponds to a swing of half the supply range. The resulting output is shown in Figure 11. From this figure, we can measure the total harmonic distortion as $0.05\,\%$. Thus, we have exceeded the specification of $0.2\,\%$ distortion at a swing equal to half the supply range. Therefore, the amplifier meets all the requirements.

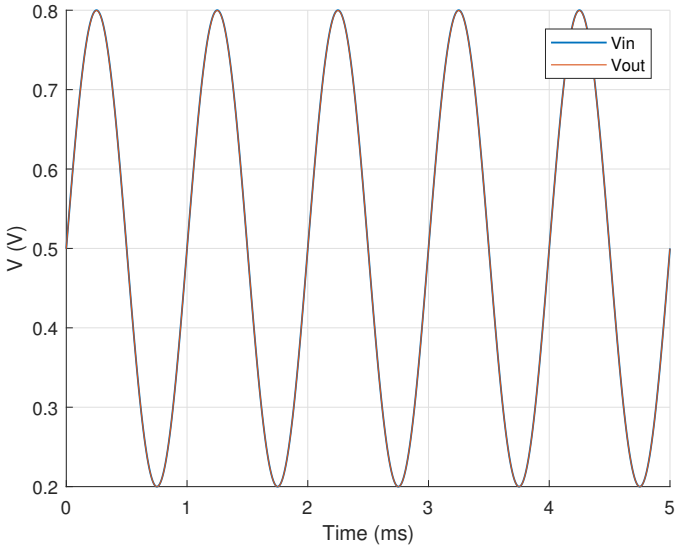

Fig. 11. Transient response of the amplifier to a $1\,\mathrm{kHz}$, $300\,\mathrm{mV}$ amplitude sine wave input.

Finally, we measured the maximum input/output swing in the unity-gain configuration. To this end, we input a $1.6\,\mathrm{V}$ peak-peak, $1\,\mathrm{kHz}$ sine wave centered around a DC bias point of $0.5\,\mathrm{V}$ and observed the output. The result is shown in Figure 12. This graph shows a maximum input/output swing of $0.1\,\mathrm{V}$ to $0.92\,\mathrm{V}$. We note that the lower limit is given by the output transistor T_9 exiting saturation, while the upper limit is given by the input biasing transistor T_{10} exiting saturation, which explains why the swing is greater in the lower limit.

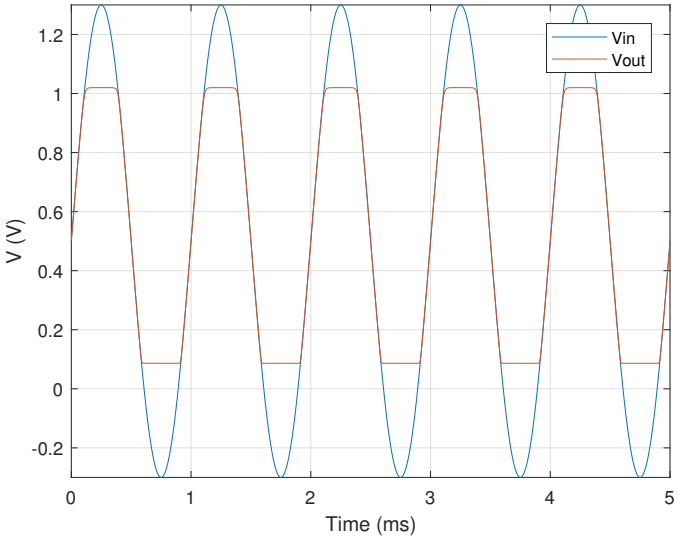

Fig. 12. Transient response of the amplifier to a large $1\,\mathrm{kHz}$ sine wave input.

VIII. Conclusions

In conclusion, we designed, simulated, and analyzed an operational amplifier that meets several specifications, including a DC gain greater than $60\,\mathrm{dB}$, poles at approximately $10\,\mathrm{kHz}$ and $100\,\mathrm{MHz}$, low distortion when swinging at half the supply range, low input-referred noise, and a static power dissipation of less than $200\,\mu\mathrm{W}$.

References

[1] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, seventh edition ed., ser. The Oxford series in electrical and computer engineering. Oxford University Press.