ANALOG MICROELECTRONICS (304-534A)
Assignment # 1

Simulation Test Benches In Cadence

Handout Date: Wednesday, September 6th, 2017
Due Date: Wednesday, September 20th, 2017

Conditions:

Assignment is to be performed ***individually*** by the student.

Objectives:

The objective of this assignment is to learn how to use Cadence to simulate electronic circuit behavior and extract meaningful circuit information. You are not responsible for optimizing the amplifier's behavior.

Simulation Problem:

A CMOS amplifier shown in Fig. 1 has been designed for unity-gain stability in a 0.13 micron CMOS process from IBM. A single 1.2 V power supply is to be used, the compensation capacitor C_c is to be set a 1 pF and the load capacitance C_L is to be set at 2 pF. The circuit uses a simple biasing scheme involving the external resistor R_{Bias}. Select a value for R_{Bias} such that the drain current of M5 is between 100 μA - 150 μA.. The rest of the component values can be found from Table 1. Enter this circuit into cadence using the schematic capture tool in Analog Artist and perform the various simulations described below.

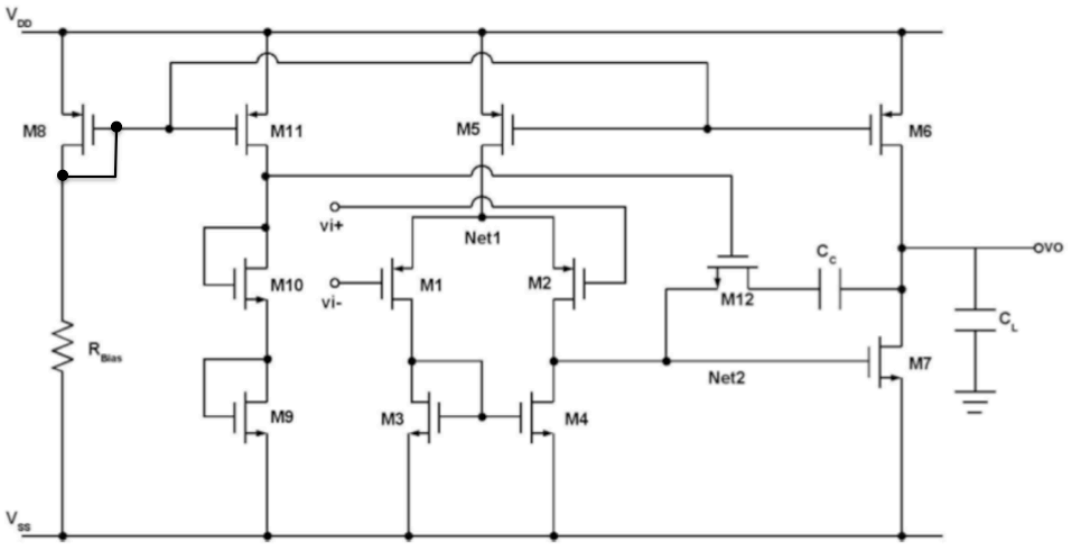

Fig. 1 - Circuit schematic

Table 1- Dimension of the transistors

	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9	M_{10}	M_{11}	M_{12}
W (μm)	70	70	40	40	107	97	105	3.5	1.2	2.5	2	5
L (nm)	300	300	500	500	1000	400	300	300	800	500	300	300

Circuit Simulation Requirements:

- The following analyses should be performed to describe the operation of the amplifier:
  - *DC analysis*: check for large-signal common-mode (CM) and differential-mode (DM) transfer characteristics, voltage offset, input and output voltage ranges.
  - *AC analysis*: check CM and DM LF gain, unity-gain bandwidth (UGBW) and phase margin, pole-zero locations of open loop amplifier, spectral noise spectral densities and the corresponding RMS thermal noise level.
  - *Transient*: check op amp closed-loop behavior such as slew rate, rise/settling time, and maximum input/output swing. Also, measure distortion behavior to sinusoidal CM and DM signals.
- Use Cadence and Analog Environment as the tool for all your simulations.

Important: The op amp may not perform all of its expected behaviors very well. This is the subject of another assignment.

Tutorials:

- Several Cadence tutorials are provided on class website to aid the student. Please refer to these documents before beginning this assignment.
- Make sure you follow the **simulation methodology** described in the reference textbook, Spice for Microelectronics, 2nd Edition, Roberts & Sedra. (some discussion also found in appendix of notes).

Items To Considers In Write-Up:

- Include plots to substantiate the simulated performance you report.
- Provide clear descriptions of the entire test benches used to extract the above mentioned op amp parameters.

Write-Up Guidelines:

All assignments and project reports must be prepared in an IEEE paper style consisting of a ***double-column single-space format***, and must adhere to the following:

- Title page - Title of the assignment/project, authors' name, and course name.
- Abstract - Abstract of the assignment/project report.
- Introduction
- Main body of the assignment/project report.
- Figures should be drawn separately from the Cadence Schematic entry program.
- Conclusions
- References - list of the books, journal papers, conference papers, and other publications used in the report. References must be listed using IEEE reference styles. You need to take a look at *IEEE Transactions on Circuits and Systems I - Regular Papers* and *IEEE Journal of Solid-State Circuits* for IEEE reference styles on books, journal papers, conference papers, and technical reports.
- Appendices