ANALOG MICROELECTRONICS (304-534A)
Assignment # 2

Operational Transconductance Amplifier: Schematic and Simulation

Handout Date: Thursday, Oct. 6th, 2016
Due Date: Wednesday, October 19th, 2016

Conditions:

Assignment is to be performed ***individually*** by the student.

Objectives:

The objective of this assignment is to design an operational transconductance amplifier. It is important that the student learn how to design such amplifiers using the methods proposed in this course, as the procedure will be used again during the project phase.

Design Specifications:

A multi-stage amplifier with a differential front-end is to be implemented in 0.13 µm CMOS technology and must meet the following specifications:

1. *DC gain ≥ 60 dB.*
2. *Amplifier poles at approx. 10 kHz and 100 MHz; others above this.*
4. *Output voltage swings of at least 50% of the supply full scale with a distortion less than 0.2% in a unity-gain configuration.*
5. *Input-referred PSD Noise Voltage less than 100 nV/sqrt(Hz) at 1 MHz.*
6. *Static power dissipation less than 200 µW.*

- Your design must meet the above specifications while driving a load capacitance of ≥ 0.5 pF.
- Your design should use a single power supply (V_{DD}) of 1.2 V and a common mode input voltage of 0.5 V (0.5 V represents analog ground, A_GND). Assume that only 1.2 V and 0.5 V voltage supplies are available for you. You cannot use ideal current nor voltage sources to bias your op amp. Instead, you have to incorporate the bias stage into your design.
- When selecting the pole positions, attempt to place the poles first using a shunt compensation capacitor to ground. Once placed, consider using a floating capacitor and observe the location of the zero. Finally, add a compensation series resistor to move the zero to the desired location. Some care is required here, as the dominant pole will first appear at the load side to the amplifier.
- You should design for maximum input/output swing (without dropping below the swing specified above) as it can have a significant impact on your design.
- Minimum power dissipation is a critical differentiating parameter of the different designs created by the class. Please pay particular attention to this parameter.
- Choose the gate length of your transistors at least 2-3 times bigger than the minimum length allowed by the technology, 0.13 µm in this case.

Circuit Simulation Guidelines:

- The following analyses should be performed to ensure the proper operation of the amplifier:
  - *DC analysis*: check for voltage offset, large-signal transfer characteristics.
  - *AC analysis*: check DC gain, 3-db bandwidth, unity-gain frequency and thermal noise.
  - *Transient*: check rise/settling time, and maximum input/output swing. Also, measure distortion.
- Use Cadence and Analog Environment as an interface for drawing the schematics and performing the HSPICE/SpectreS simulations.

Items To Consider For Write-Up:

- In your write-up, you should provide a **first-order hand-analysis** of your multi-stage amplifier performance whenever possible and compare this to what you see through a Spice simulation. Conversely, what you see from your Spice analysis should be confirmed by a first-order hand-analysis.
- Make sure you follow the **design methodology** and **optimization sequence** outlined in the course notes.
- Include plots to substantiate the simulated performance you report.
- Provide a discussion of your results, including a comparison of any differences between your first-order analysis and the simulated performance.
- Provide complete circuit schematics, as well as the path in which your design resides. Make these files readable as soon as you submit the assignment.

Write-Up Guidelines:

All assignments and project reports must be prepared in an IEEE paper style consisting of a double-column single-space format, and must adhere to the following:

- Title page - Title of the assignment/project, authors' name, and course name.
- Abstract - Abstract of the assignment/project report.
- Introduction
- Main body of the assignment/project report.
- Figures should be drawn separately from the Cadence Schematic entry program.
- Conclusions
- References - list of the books, journal papers, conference papers, and other publications used in the report. References must be listed using IEEE reference styles. You need to take a look at *IEEE Transactions on Circuits and Systems I - Regular Papers* and *IEEE Journal of Solid-State Circuits* for IEEE reference styles on books, journal papers, conference papers, and technical reports.
- Appendices