ECSE-534
Analog Microelectronics
Course Project – Initial Phase

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***Abstract*—A first order, single bit, $\Delta\Sigma$ A/D converter was designed, simulated, and analyzed using MATLAB and Cadence. This converter was required to achieve a peak SNDR of at least $60\,\mathrm{dB}$ with a bandwidth of $38.22\,\mathrm{kHz}$ and a full scale input range of $\pm 0.2\,\mathrm{V}$. To meet these goals, a sampling frequency of $10\,\mathrm{MHz}$ was used, which resulted in a peak SNDR of $76.69\,\mathrm{dB}$ in a system level simulation and of $55.7223\,\mathrm{dB}$ in a circuit level simulation. Given that the circuit level simulation SNDR does not meet the specifications, several avenues of inquiry to pursue in the final phase of the project were also suggested.**

I. Introduction

THIS report follows the design, simulation, and analysis of a first order, single bit, low pass $\Delta\Sigma$ A/D converter using a 0.13 micron process from IBM. We used MATLAB and Simulink to perform system level simulations and Cadence and Analog Environment to perform circuit level simulations in said process. The converter was required to meet the following specifications:

- Bandwidth: $(1+\alpha)\cdot 20\,\mathrm{kHz}$, where $\alpha =$ (last 3 digits of student ID) / 1000.
- SNDR (peak): $60\,\mathrm{dB}$ ($>$ 10 bits).
- Input Voltage Range: $\pm 0.2\,\mathrm{V}$ relative to AGND.
- Power Dissipation: Minimum.

In addition, we were assigned a supply voltage of $1.2\,\mathrm{V}$ and an analog ground voltage of AGND $= 0.6\,\mathrm{V}$. To meet these specifications, we first performed a system level simulation using MATLAB and Simulink to determine the high level parameters required. Then, we mapped the system to a circuit and performed a circuit level simulation using Cadence and Analog Environment. Finally, we analyzed the performance of the converter and verified if it meets the specifications.

II. System Level Simulation

We first simulated the ADC at the system level. We began by calculating the requirements of our system. From our student ID, we can determine that $\alpha = 0.911$, which means our bandwidth is $f_{3dB} = 38.22\,\mathrm{kHz}$. To compute our minimal SNR, we assume that the power of the noise in our system will be about equal to the power of the signal harmonics. Thus, we require SNR $=$ 2 SNDR, or SNR $= 63\,\mathrm{dB}$ at the minimum. We can therefore compute our desired oversampling rate as

$$OSR = 10^{(SNR_{peak}-2.61)/30} = 103.04$$

Using this result, we can determine that our minimum sampling frequency must be

$$f_s = 2\ OSR\ f_{3dB} = 7.88\,\mathrm{MHz}$$

To allow for some margin, we chose $f_s = 10\,\mathrm{MHz}$.

Next, we set up the simulation in Simulink, as shown in Figure 1. We used a $0.2\,\mathrm{V}$ amplitude sine wave with a DC offset of $0.6\,\mathrm{V}$ as our input to the system, and we sampled this input at a rate of $10\,\mathrm{MHz}$. We also used $1\,\mathrm{kHz}$ bins for all SNDR calculations.

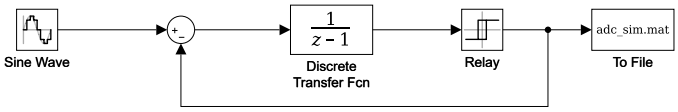

Fig. 1. A system level block diagram of the $\Delta\Sigma$ A/D converter.

To find our peak SNDR, we first set the relay outputs to $0.4\,\mathrm{V}/0.8\,\mathrm{V}$ and swept the input frequency. The results are shown in Figure 2. From this plot, we can see that the frequency with the best SNDR is around $20\,\mathrm{kHz}$. This can be explained by the fact that the first harmonic for this input frequency occurs at $40\,\mathrm{kHz}$, which is outside our bandwidth and hence does not add distortion.

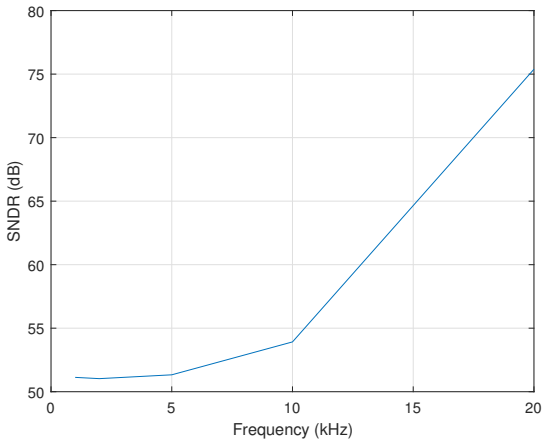

Fig. 2. SNDR vs. input frequency for the $\Delta\Sigma$ A/D converter with the relay outputs set at $0.4\,\mathrm{V}/0.8\,\mathrm{V}$.

Next, we kept the input frequency at $20\,\mathrm{kHz}$ and swept the amplitude of the relay output around a DC offset of $0.6\,\mathrm{V}$. The results are shown in Figure 3. From this plot, we can

see that the peak SNDR of $76.69\,\mathrm{dB}$ occurs when the relay output amplitude is $0.4\,\mathrm{V}$, corresponding to relay outputs of $0.2\,\mathrm{V}/1.0\,\mathrm{V}$.

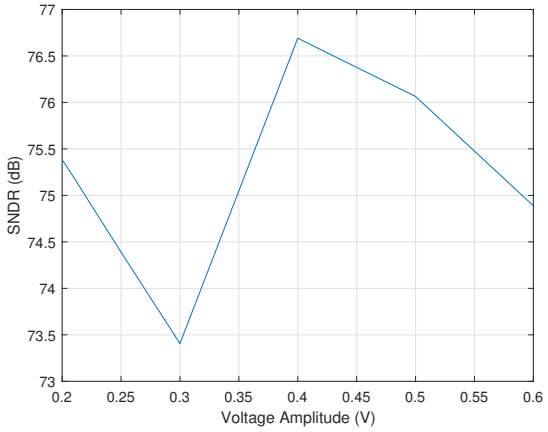

Fig. 3. SNDR vs. relay output amplitude for the $\Delta\Sigma$ A/D converter with the input frequency set at $20\,\mathrm{kHz}$.

Thus, we chose to use an input frequency of $20\,\mathrm{kHz}$ and a relay output amplitude of $0.4\,\mathrm{V}$ for our design. The power spectral density of the output with these settings is shown in Figure 4. This plot clearly shows that the output has a peak at the input frequency of $20\,\mathrm{kHz}$, with the first harmonic occurring outside of our bandwidth at $40\,\mathrm{kHz}$.

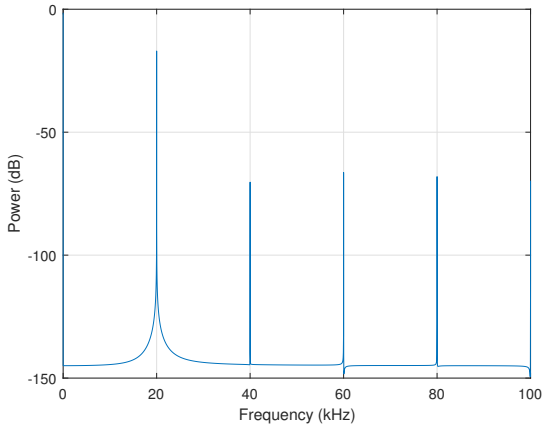

Fig. 4. Power spectral density for the output of the $\Delta\Sigma$ A/D converter with the input frequency set at $20\,\mathrm{kHz}$ and the relay outputs set at $0.2\,\mathrm{V}/1.0\,\mathrm{V}$.

III. Circuit Level Simulation

We next mapped the system to a circuit using Cadence. We reused the operational amplifier designed in Assignments #2 and #3 to implement an integrator. We also used a modified version of the operational amplifier with the compensation network removed to implement a comparator. These are shown in Figure 8 as U_1 and U_2 respectively. The remaining components required digital logic. As a starting point, we used $10\,\mu\mathrm{m}/0.12\,\mu\mathrm{m}$ NMOS transistors and $25\,\mu\mathrm{m}/0.12\,\mu\mathrm{m}$ PMOS transistors for all our digital logic.

We first implemented a NOT gate and a NOR gate to provide building blocks for our other circuit elements. Schematics of these implementations are shown in Figures 5 and 6. Then, we used the NOT gate to implement a basic transmission gate, as shown in Figure 7.

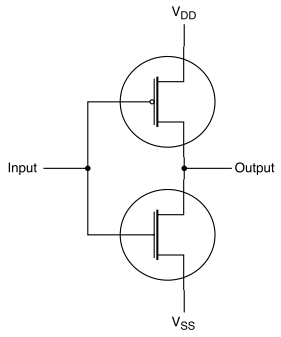

Fig. 5. A schematic of a NOT gate (inverter) implementation.

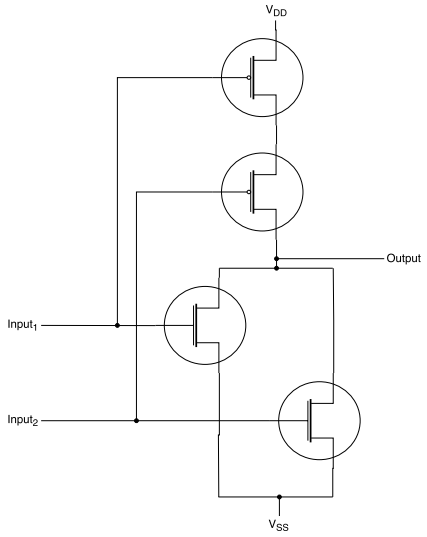

Fig. 6. A schematic of a two-input NOR gate implementation.

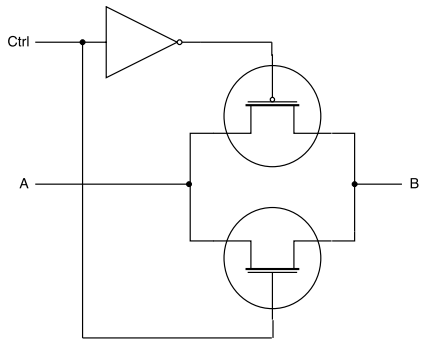

Fig. 7. A schematic of a transmission gate implementation.

Then, we implemented a D flip-flop in order to add a sampling element to our circuit. A schematic of this implementation is shown in Figure 9. This flip-flop is triggered by the falling edge of the clock signal.

Finally, we implemented the circuit shown in Figure 10 to generate a 2-phase clock signal that we could use to operate

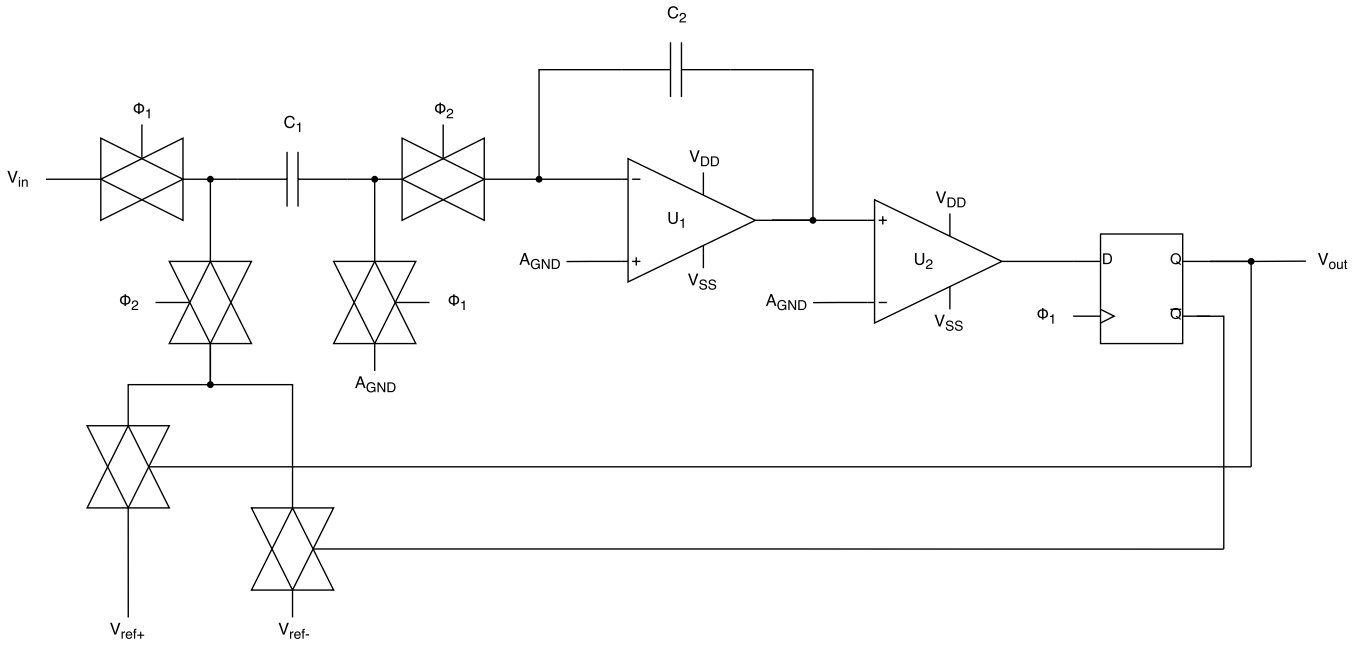

Fig. 8. A schematic of the $\Delta\Sigma$ A/D converter.

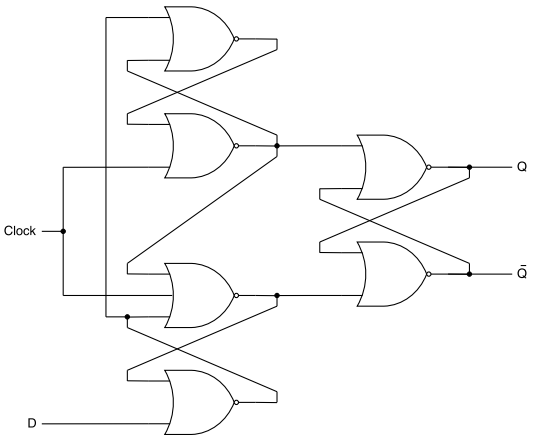

Fig. 9. A schematic of a D flip-flop implementation.

our switched capacitor circuit. We achieved this by simply negating the clock to provide the second phase, and then using an SR latch and a series of buffers to ensure that the two phases never overlap.

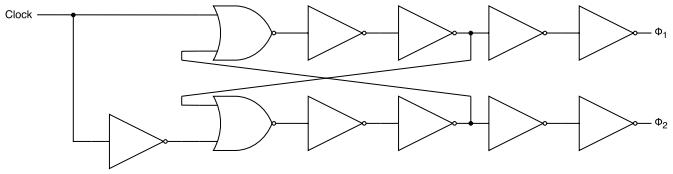

Fig. 10. A schematic of a 2-phase clock generator implementation.

With these subcomponents in hand, we then implemented the complete ADC, as shown in Figure 8. We chose values of $C_1 = C_2 = 0.5\,\mathrm{pF}$ as a starting point, making sure to match them in order to implement a discrete integrator. In addition, we used the reference voltages of $V_{ref+} = 1.0\,\mathrm{V}$ and $V_{ref-} = 0.2\,\mathrm{V}$ that were previously found to give the best SNDR.

We next performed a transient analysis of the circuit. As we did in our system level simulation, we used a $10\,\mathrm{MHz}$ clock and a $0.2\,\mathrm{V}$ amplitude, $20\,\mathrm{kHz}$ sine wave input signal. We then ran the simulation for $2\,\mathrm{ms}$, which allowed us to get $500\,\mathrm{Hz}$ bins in our FFT. One issue we encountered was that the FFT expects uniform sampling while Analog Environment produces non-uniformly sampled outputs. To fix this, we set the `strobeperiod` option of the transient simulation to $10\,\mathrm{ns}$, which produces a uniformly sampled output and gives us 10 points per period of the sampling clock.

A portion of the results are shown in Figure 11. In this plot, we can see the integrator output for a given input signal. We see that in this case, with the signal being greater than analog ground, the negative error when the DAC outputs $1.0\,\mathrm{V}$ produces small steps downward, which eventually leads to crossing the analog ground line. At that point, the DAC output switches to $0.2\,\mathrm{V}$, and the larger positive error causes the integrator output to rise rapidly above the analog ground line. This illustrates how the ADC produces an output whose mean value is correlated with the value of the input signal.

We next processed the simulation data over the entire $2\,\mathrm{ms}$ and obtained a SNDR of $55.7223\,\mathrm{dB}$ over our bandwidth of $38.22\,\mathrm{kHz}$. We used $1\,\mathrm{kHz}$ bins to match the system level simulation. A plot of the power spectral density we obtained is shown in Figure 12.

Finally, we measured the power supply current and multiplied it by $V_{DD} = 1.2\,\mathrm{V}$ in order to calculate the circuit's power dissipation. The results are shown in Figure 13. We can see that large spikes occur when the circuit's digital components are switching. Integrating the curve and dividing by the interval yields an average power dissipation of $195\,\mu\mathrm{W}$.

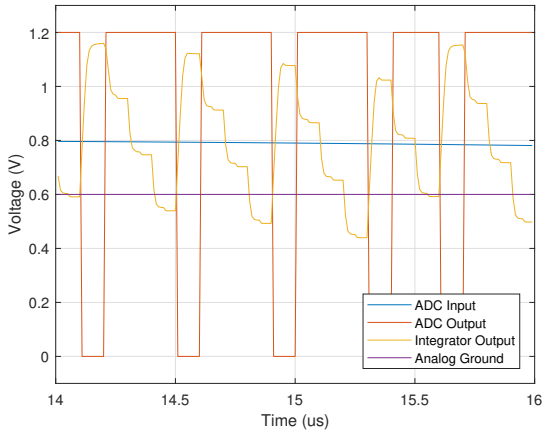

Fig. 11. Transient response of the $\Delta\Sigma$ A/D converter with the input frequency set at 20 kHz and the relay outputs set at $0.2\,\mathrm{V}/1.0\,\mathrm{V}$.

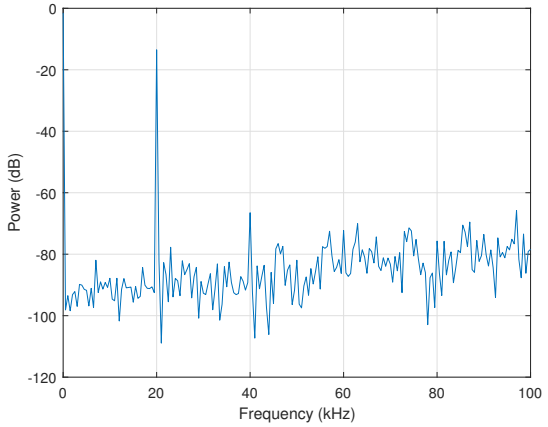

Fig. 12. Power spectral density for the output of the $\Delta\Sigma$ A/D converter with the input frequency set at 20 kHz and the relay outputs set at $0.2\,\mathrm{V}/1.0\,\mathrm{V}$.

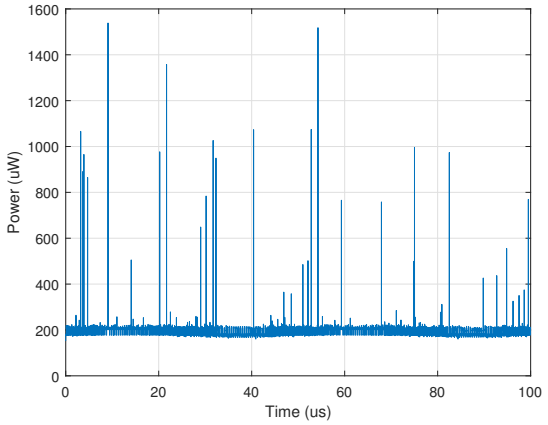

Fig. 13. Power dissipation of the $\Delta\Sigma$ A/D converter with the input frequency set at 20 kHz and the relay outputs set at $0.2\,\mathrm{V}/1.0\,\mathrm{V}$.

IV. Analysis

In terms of SNDR, the circuit level simulation produced a much lower result than the system level simulation. In fact, the value of $55.7223\,\mathrm{dB}$ obtained is below the spec of $60\,\mathrm{dB}$, and far below the system level simulation value of $76.69\,\mathrm{dB}$. This can be explained by several factors. As shown in Figures 4 and 12, the noise floor for the system level simulation is around $-140\,\mathrm{dB}$, while it is around $-90\,\mathrm{dB}$ for the circuit level simulation. This could be a result of additional quantization error, or a result of additional noise being introduced by the other components in the circuit. Since the system level simulation meets the specification, it seems more likely that the latter is the cause. However, more investigation is required for the final phase.

Several possible improvements that we will examine include the use of a 4-phase clock system and the use of bootstrapped transmission gates to reduce charge injection and improve linearity. In addition, we will look at second order effects to try to determine the principal causes of the reduced SNDR.

In terms of power dissipation, we were not given an explicit requirement. However, we can evaluate our implementation by comparing our average power dissipation of $195\,\mu\mathrm{W}$ to the Assignment 2 maximum of $200\,\mu\mathrm{W}$. This comparison shows that our power dissipation is quite low, given that our combined circuit consumes less power on average than the maximum we were given for a single operational amplifier. However, there are some improvements that can be made. In particular, the bias circuits of the operational amplifier and the comparator should be merged in order to save on power and silicon area. This will also improve the layout by reducing the need to lay out multiple current references.

V. Conclusions

In conclusion, we designed, simulated, and analyzed a first order, single bit, $\Delta\Sigma$ A/D converter using MATLAB and Cadence. To meet our specifications of a $38.22\,\mathrm{kHz}$ bandwidth and a peak SNDR of at least $60\,\mathrm{dB}$, we used a sampling frequency of $10\,\mathrm{MHz}$. We then found that our peak SNDR occurs when the input frequency is $20\,\mathrm{kHz}$ and our DAC output voltage levels are $0.2\,\mathrm{V}/1.0\,\mathrm{V}$. With these parameters, our system level simulation yielded a SNDR of $76.69\,\mathrm{dB}$, while our circuit level simulation yielded a SNDR of $55.7223\,\mathrm{dB}$. Given that our circuit level simulation SNDR does not meet the specifications, we also suggested several avenues of inquiry to pursue for the final phase of the project.