ECSE-534
Analog Microelectronics
Final Exam

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I. Introduction

THIS report follows the design, simulation, and analysis of an anti-aliasing filter for a $\Delta\Sigma$ data converter using a 0.13 micron process from IBM. We used Cadence to simulate the design in said process. The filter was required to adhere to the topology shown in Figure 1 and meet the following specifications:

- A DC gain of $1\,\mathrm{V/V}$.
- A passband from DC to $100\,\mathrm{kHz}$.
- A maximum attenuation of $0.1\,\mathrm{dB}$ in the passband.
- A maximum phase shift of 10° in the passband.
- A minimum attenuation of $40\,\mathrm{dB}$ at frequencies over $15\,\mathrm{MHz}$.
- An input resistance of at least $1\,\mathrm{k\Omega}$.
- An output resistance of at most $20\,\Omega$.
- An output voltage swing of $0.9\,\mathrm{V}$ around an analog ground level of $0.6\,\mathrm{V}$.
- A maximum RMS noise level of $100\,\mu\mathrm{V}$.

The filter must meet these specifications while driving a $1\,\mathrm{pF}$ load capacitance that represents the input capacitance of the $\Delta\Sigma$ data converter.

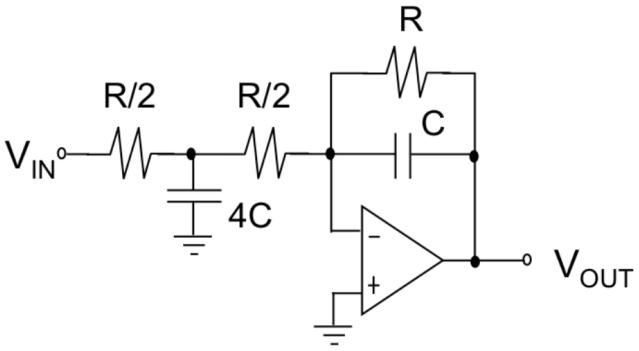

Fig. 1. A schematic of the second-order anti-aliasing filter topology.

To meet these requirements, we first calculated the required values for the passive components of the filter. Then, we modified the operational amplifier we designed in the past assignments to meet the specifications. Next, we assembled the filter and verified that it meets the requirements. Finally, we discussed a rough sketch of the layout of the filter.

II. Filter Design

We first translated the given specifications into restrictions on our circuit. We started by deriving the transfer function of the filter as

$$H(s) = \frac{-R}{1+sRC}\frac{1}{R/2}\frac{1/2}{1+sRC} \tag{1}$$

$$= \frac{-1}{(1+sRC)^2} \tag{2}$$

This result tells us that the DC gain is -1 and the bandwidth is given by $f_{3dB} = 1/2\pi RC$.

In order to gain more insight into the operation of the filter, we added a relative mismatch Δ to the components in the feedback network. We thus obtained

$$H(s) = \frac{-R(1+\Delta_R)}{1+sRC(1+\Delta_R)(1+\Delta_C)}\frac{1}{R/2}\frac{1/2}{1+sRC} \tag{3}$$

$$\approx \frac{-R(1+\Delta_R)}{1+sRC(1+\Delta_R+\Delta_C)}\frac{1}{R/2}\frac{1/2}{1+sRC} \tag{4}$$

This result tells us that the DC gain can be approximated as $-(1+\Delta_R)$ and that there are two poles formed, one at $f_1 = 1/2\pi RC$ and the other at $f_2 = 1/2\pi RC(1+\Delta_R+\Delta_C)$.

The given DC gain requirement means that the feedback resistors in the circuit must match well. In addition, the DC gain of the operational amplifier must be high, say at least $60\,\mathrm{dB}$.

The given attenuation requirements mean that we must have $f_{3dB} \gg 100\,\mathrm{kHz}$ and $f_{3db} \ll 15\,\mathrm{MHz}$. Since a second order filter has a roll-off of about $40\,\mathrm{dB}$ per decade, this translates approximately to $f_{3db} < 1.5\,\mathrm{MHz}$.

The given input resistance requirement means that $R > 1\,\mathrm{kHz}$. The given output resistance requirement means that we must have $2R_{out} < 20\,\Omega$ for the operational amplifier, where R_{out} is the output resistance of the amplifier in the unity gain configuration.

The given voltage swing requirements translate directly into equivalent requirements for the operational amplifier.

The given noise requirement must be separated between two sources: the thermal noise generated by the feedback network and the noise generated by the amplifier. We therefore allocate an RMS noise budget of $50\,\mu\mathrm{V}$ to each.

The RMS thermal noise generated by the feedback network can be approximated as

$$v_{n,rms} = \sqrt{\frac{kT}{C} + \frac{kT}{4C}} \tag{5}$$

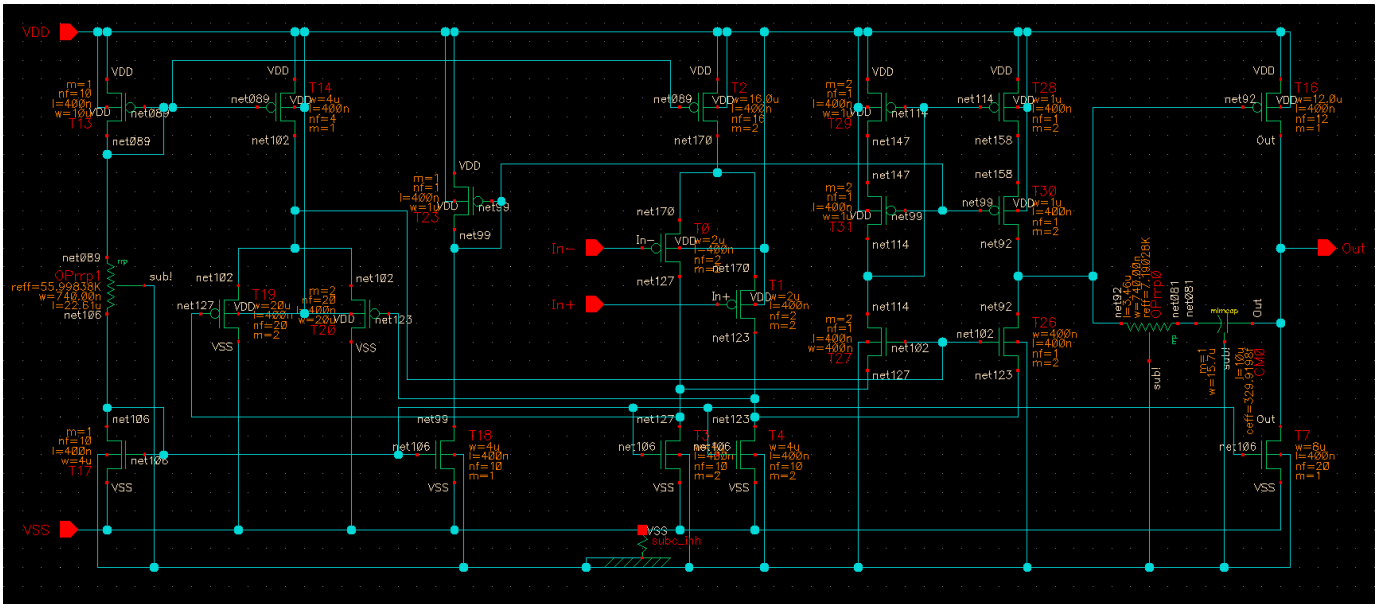

Fig. 2. A schematic of the operational amplifier designed in past assignments.

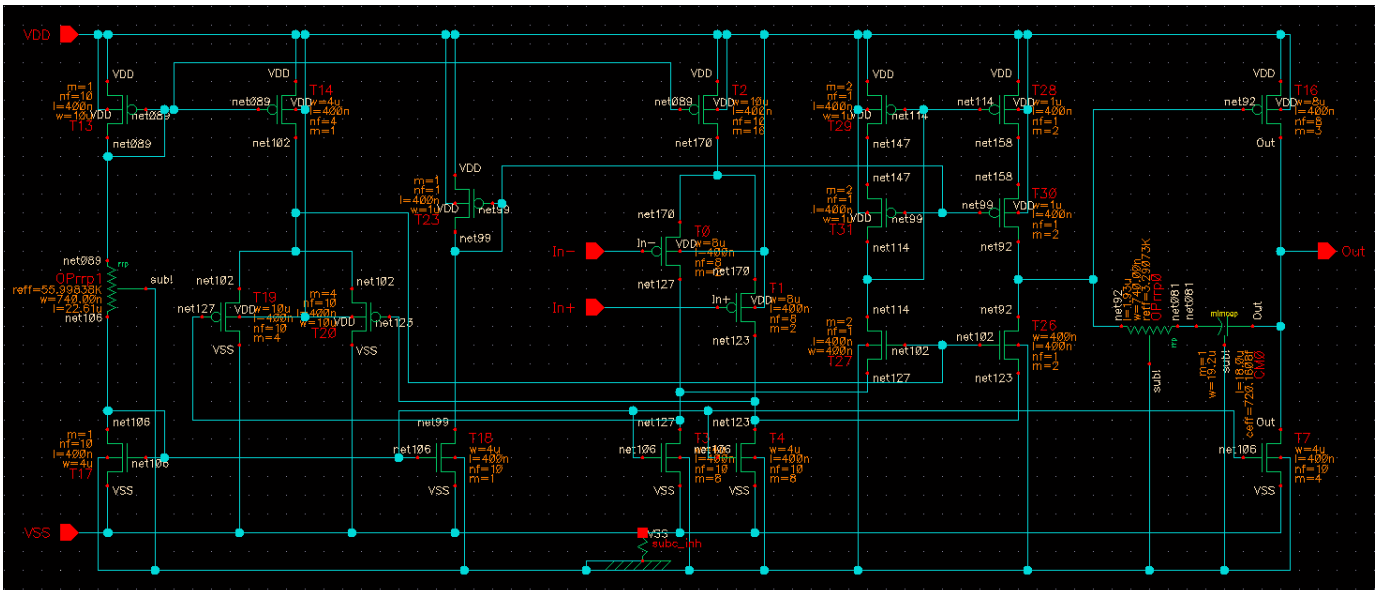

Fig. 3. A schematic of the modified operational amplifier made to meet the requirements.

Therefore, we have

$$v_{n,rms} < 50\,\mu\text{V} \tag{6}$$

$$\sqrt{\frac{kT}{C} + \frac{kT}{4C}} < 50\,\mu\text{V} \tag{7}$$

$$C > 2\,\text{pF} \tag{8}$$

The noise generated by the amplifier is harder to quantify. However, since the feedback gain of our circuit is $1/2$, the output spectral noise density of the amplifier in this circuit will be equivalent to the input-referred spectral noise density measured in open loop simulation times 2. Thus, we require an input-referred RMS noise level of at most $50\,\mu\text{V}/\sqrt{2} = 35\,\mu\text{V}$.

Therefore, the requirements for the feedback network are

$$R > 1\,\text{k}\Omega \tag{9}$$

$$C > 2\,\text{pF} \tag{10}$$

$$100\,\text{kHz} \ll \frac{1}{2\pi RC} < 1.5\,\text{MHz} \tag{11}$$

To minimize the size of the capacitors used, we chose to use $C = 3\,\text{pF}$. Then, to allow for at least a $20\,\%$ margin on the upper bandwidth, we chose to use $f_{3dB} = 1\,\text{MHz}$, and thus $R = 53\,\text{k}\Omega$.

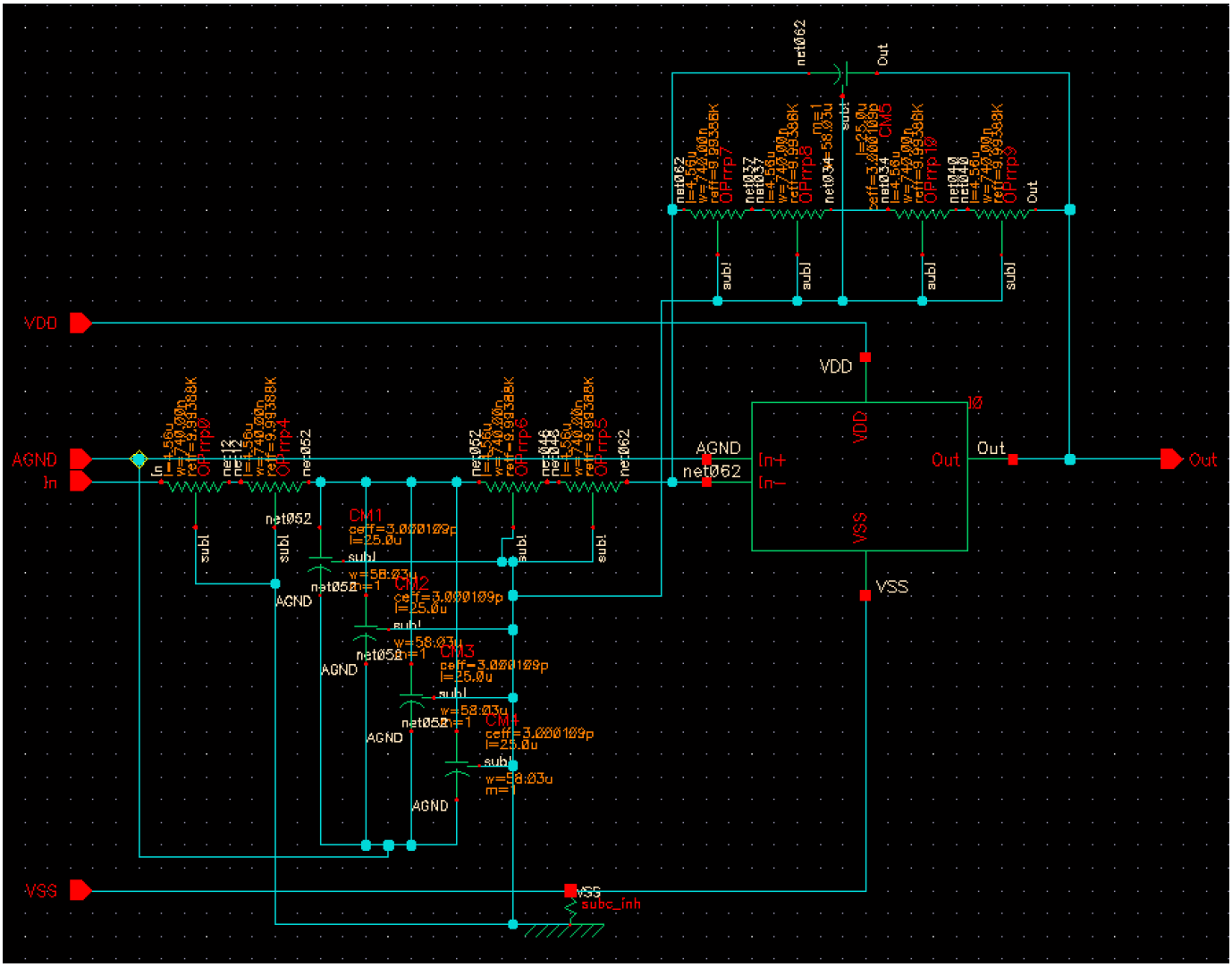

Fig. 4. A schematic of the anti-aliasing filter.

III. Operational Amplifier Design

From the previous section, the main requirements for the operational amplifier are a DC gain of at least 60 dB, a maximum output resistance of 10 Ω in the unity gain configuration, and an input-referred RMS noise level of at most 35 µV over the given bandwidth. In addition, we require that the unity gain frequency of the amplifier should be at least 10 times our chosen filter bandwidth, at 10 MHz.

To meet these specifications, we reused the operational amplifier designed in the past assignments. A schematic is shown in Figure 2. This amplifier has a DC gain of 73 dB, a unity gain bandwidth of 40 MHz, an output resistance in the unity gain configuration of 12.9 Ω, and a total input-referred RMS noise of 65 µV between 1 Hz and 100 kHz.

These results show that the amplifier does not meet the specifications for noise and output resistance. In order to modify the amplifier to meet the specifications, we performed a series of transformations on our initial circuit.

A noise analysis in Cadence indicated that the main contributors to the noise level were transistors T_0, T_1, T_3, and T_4, with a total contribution of 92.68 %. Since flicker noise is inversely proportional to transistor area, we needed to scale the widths of these transistors upward. We achieved this by scaling the widths of T_0, T_1, T_3, and T_4 by a factor of 4, and then scaling the width of T_2 to provide sufficient current to T_0 and T_1 to avoid disturbing the operating point of the other transistors in the circuit. This transistor ended up being scaled by a factor of 5. In addition, to meet the output resistance specification, we needed to scale the current in the output branch upward. We achieved this by scaling the widths of both T_7 and T_{16} by a factor of 2. This also had the effect of scaling our bandwidth upward, so we scaled C_c to 0.72 pF and R_c to 3.3 kΩ to compensate. The resulting amplifier is shown in Figure 3.

We then measured the amplifier's characteristics to confirm that it now met the specifications. The amplifier now had a DC gain of 77 dB, a unity gain bandwidth of 53 MHz, an output resistance in the unity gain configuration of 4.1 Ω, and a total input-referred RMS noise of 32 µV between 1 Hz and 100 kHz. The first two poles were also moved to 8 kHz and 102 MHz, and the first zero was moved to 124 MHz, which

are very close to the values they initially had. In addition, we verified that the amplifier was still stable, with a phase margin of $57°$.

IV. Putting It All Together

We next assembled the circuit together as previously described. The result is shown in Figure 4. Note that we split the resistors into units of size $R/4$ in order to better match them in layout, and we split the capacitors into units of size C for the same reason. After some testing, we also changed the value of R to $40\,\mathrm{k\Omega}$ in order to fully meet the specifications.

To test the performance of the filter, we used the circuit shown in Figure 5, which has a load capacitance of $1\,\mathrm{pF}$.

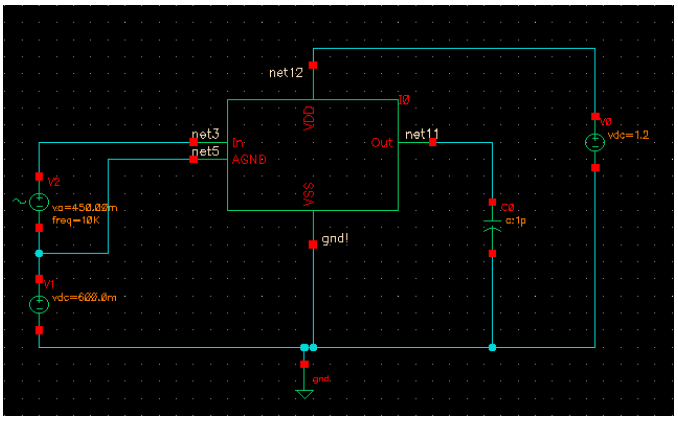

Fig. 5. A schematic of the test-bench used to measure the AC and transient performance of the filter.

We first measured the transient performance of the filter by using a $0.9\,\mathrm{V}$ peak-peak, $10\,\mathrm{kHz}$ sine wave centered around $0.6\,\mathrm{V}$ as an input. The resulting input and output are shown in Figure 6. This figure shows that the output signal has no significant distortion even at full range. In fact, we can compute the total harmonic distortion as only $0.040\,\%$, which shows that the circuit meets the voltage swing requirement of the $\Delta\Sigma$ converter.

We then measured the AC performance of the filter by using small signal analysis. The results are shown in Figure 7. These results show that we have a DC gain of $0.999\,53\,\mathrm{V/V}$, an attenuation of $0.053\,\mathrm{dB}$ and a phase shift of $8.83°$ at $100\,\mathrm{kHz}$, and an attenuation of $41.5\,\mathrm{dB}$ at $15\,\mathrm{MHz}$. Therefore, the filter meets all the AC requirements.

We next measured the noise properties of the filter. After running an AC noise analysis and integrating the results from $1\,\mathrm{Hz}$ to $100\,\mathrm{kHz}$, we obtained the results shown in Figure 8. This figure clearly shows that we have a total RMS output noise of $66\,\mu\mathrm{V}$, which meets the specified maximum noise level for the input to the $\Delta\Sigma$ converter.

Then, we measured the output resistance of the filter using the circuit shown in Figure 9. With the load resistance set to $20\,\Omega$ and the input set to $1\,\mathrm{V}$, we measured a small signal output voltage of $0.6984\,\mathrm{V}$. Using a simple voltage divider equation, we found that the output resistance of the filter was therefore $8.62\,\Omega$, which is smaller than the maximum output resistance requirement.

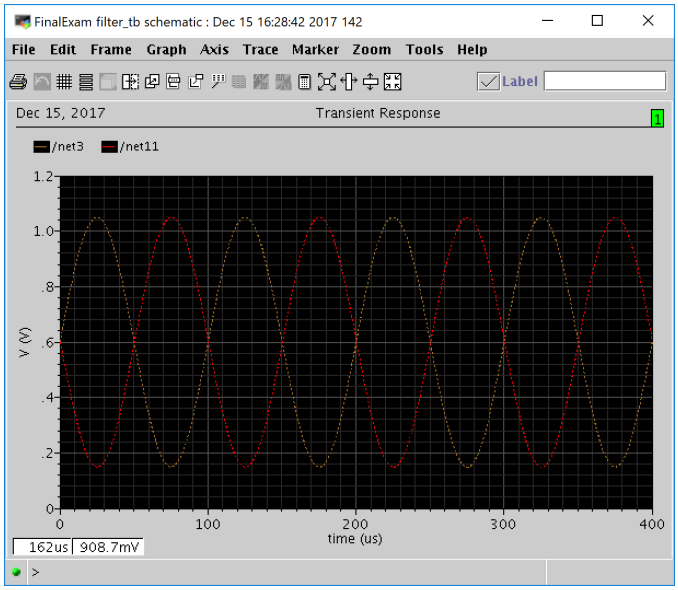

Fig. 6. Transient response of the filter for a $0.9\,\mathrm{V}$ peak-peak, $10\,\mathrm{kHz}$ sine wave centered around $0.6\,\mathrm{V}$. The input waveform is shown in brown and the output waveform is shown in red.

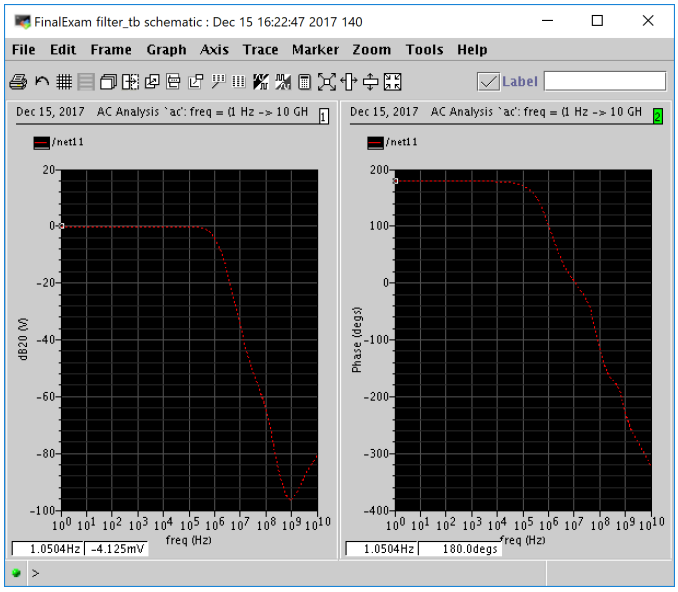

Fig. 7. AC response of the filter. The plot on the left shows the gain in dB and the plot on the right shows the phase in °.

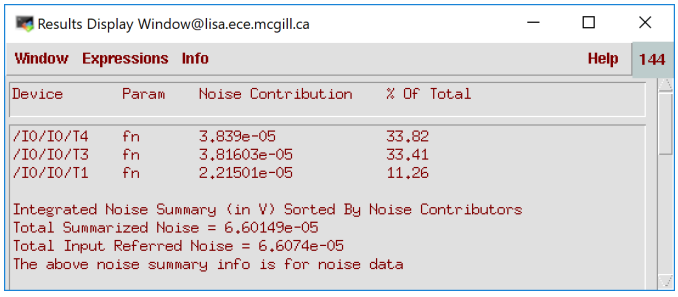

Fig. 8. Noise results for the filter over the bandwidth from $1\,\mathrm{Hz}$ to $100\,\mathrm{kHz}$.

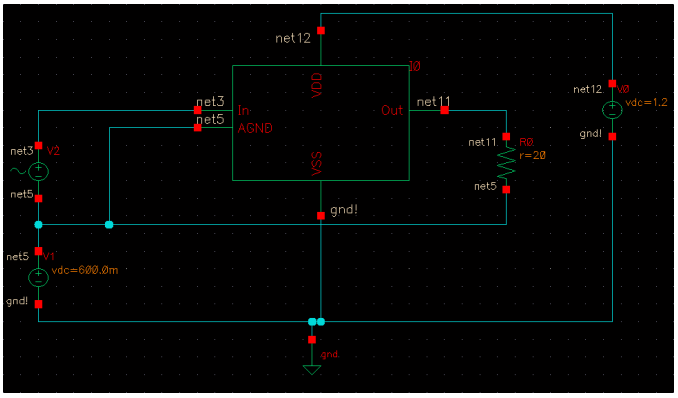

Fig. 9. A schematic of the test-bench used to measure the output resistance of the filter.

Finally, we measured the input resistance of the filter using the circuit shown in Figure 10. With the signal resistance set to $40\,\mathrm{k\Omega}$ and the input set to $1\,\mathrm{V}$, we measured a small signal output voltage of $0.499\,62\,\mathrm{V}$. Using a simple voltage divider equation, we found that the input resistance of the filter was therefore $39.98\,\mathrm{k\Omega}$, which greatly exceeds the specification.

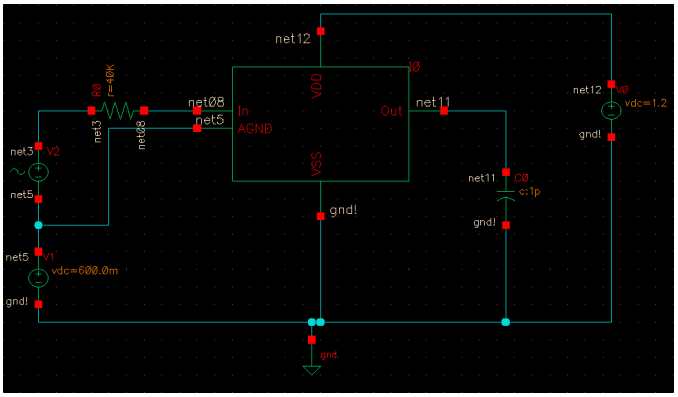

Fig. 10. A schematic of the test-bench used to measure the input resistance of the filter.

V. Layout

Next, we planned out a rough sketch of the layout for the filter. As shown in Figure 3, we made all transistors multiples of a unit size, which reduces the error when trying to match them. We used a combination of the number of fingers to increase the length of a transistor and the multiplicity to increase the width of a transistor, thus ensuring that transistors can be made into rectangular shapes that are not too long and not too wide.

In addition, we made sure that all transistors that need to be matched have a multiplicity of at least 2, which allows us to use a common centroid geometry to eliminate the effect of the first order component of the process gradient in producing matching error. An example of this is shown in Figure 11. In this figure, T_0 and T_1 are placed such that their centroids coincide. In addition, this figure shows the addition of dummy structures to the boundaries of the pair, which ensures that all transistors have a similar environment and thus creates a better matching. The dummy transistors would typically be connected to V_{SS}.

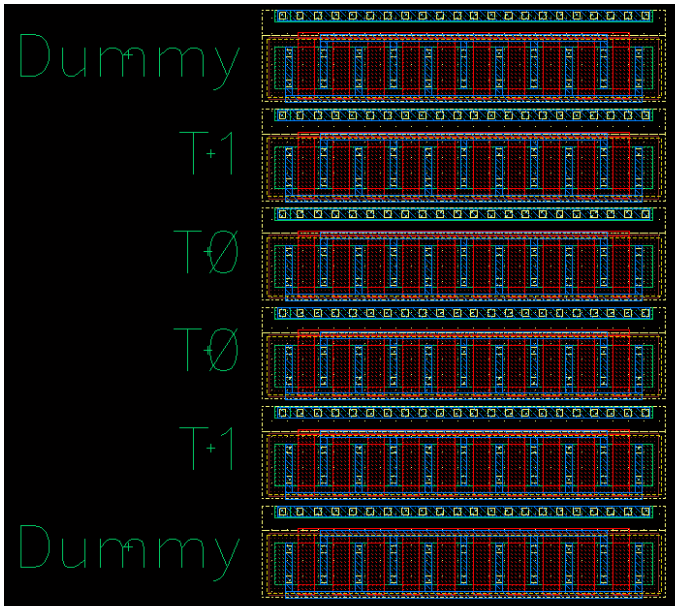

Fig. 11. A common centroid layout for a differential input pair with dummy structures at the boundary. Connections are not shown.

For the passive components, matching was also critical since it controls the DC gain of the filter. In addition, mismatches can split the poles of the filter, causing ringing to occur. To ensure that these components are matched correctly, we again split them into subcomponents of unit size and used a common centroid geometry. A sketch of the layout of the resistors in the circuit is shown in Figure 12, and a sketch of the layout of the capacitors in the circuit is shown in Figure 13. We note here that while the matching of components is critical, the values of the components themselves are not. Since the $\Delta\Sigma$ converter oversamples at a rate of $16\,\mathrm{MHz}$ and the signal bandwidth is only $100\,\mathrm{kHz}$, the resulting pole at around $1\,\mathrm{MHz}$ can vary by $\pm 20\,\%$ while still producing little passband attenuation and sufficient stopband attenuation.

VI. Conclusions

In conclusion, we designed an anti-aliasing filter capable of acting as a preprocessor for the $\Delta\Sigma$ converter specified in the examination question. This filter meets all of the specifications. In addition, we provided a sketch of the approach we would use to lay out such a filter.

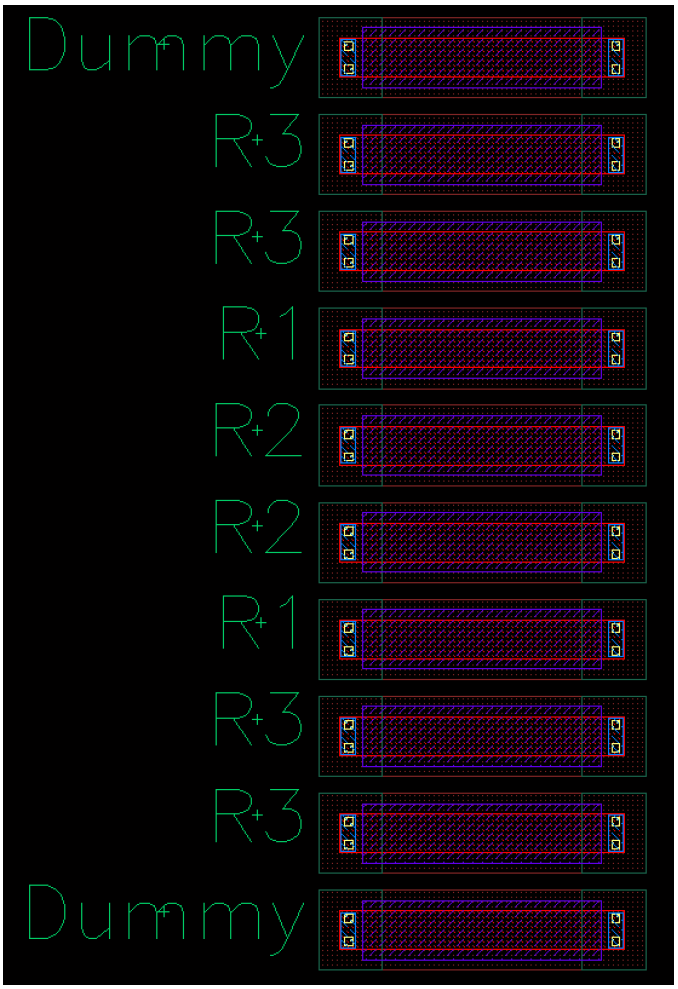

Fig. 12. A common centroid layout for the resistors in the filter. Connections are not shown.

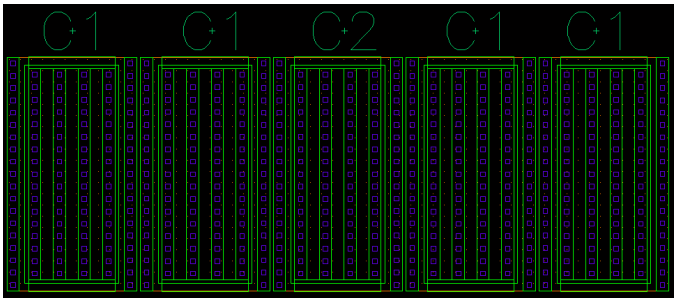

Fig. 13. A common centroid layout for the capacitors in the filter. Connections are not shown.