ECSE-534
Analog Microelectronics
A First Order $\Delta\Sigma$ A/D Converter

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***Abstract*—A first order, single bit, $\Delta\Sigma$ A/D converter was designed, simulated, laid out, and analyzed using MATLAB and Cadence. This converter was required to achieve a peak SNDR of at least $60\,\mathrm{dB}$ with a bandwidth of $38.22\,\mathrm{kHz}$ and a full scale input range of $\pm 0.2\,\mathrm{V}$. To meet these goals, a sampling frequency of $10\,\mathrm{MHz}$ was used, which resulted in a peak SNDR of $63.7303\,\mathrm{dB}$ in a system level simulation, a peak SNDR of $65.4429\,\mathrm{dB}$ in a schematic level simulation, and a peak SNDR of $60.3449\,\mathrm{dB}$ in a layout level simulation. The A/D converter therefore satisfies all the requirements.**

I. Introduction

THIS report follows the design, simulation, layout, and analysis of a first order, single bit, low pass $\Delta\Sigma$ A/D converter using a 0.13 micron process from IBM. We used MATLAB and Simulink to perform system level simulations, and Cadence to perform circuit level simulations and layout. The converter was required to meet the following specifications:

- Bandwidth: $(1+\alpha)\cdot 20\,\mathrm{kHz}$, where $\alpha =$ (last 3 digits of student ID) / 1000.
- SNDR (peak): $60\,\mathrm{dB}$ ($>$ 10 bits).
- Input Voltage Range: $\pm 0.2\,\mathrm{V}$ relative to AGND.
- Power Dissipation: Minimum.

In addition, we were assigned a supply voltage of $1.2\,\mathrm{V}$ and an analog ground voltage of AGND $= 0.6\,\mathrm{V}$.

In the previous phase of the project, we obtained a peak SNDR of $55.7223\,\mathrm{dB}$ for a $20\,\mathrm{kHz}$ signal using a sampling frequency of $10\,\mathrm{MHz}$ and DAC output levels of $0.2\,\mathrm{V}/1.0\,\mathrm{V}$. Since this did not meet the specifications, we first performed a more detailed Simulink simulation to better model the system under test. Then, we mapped the system to a circuit, laid it out, and performed a circuit level simulation using Cadence. Finally, we analyzed the performance of the converter and verified that it meets the specifications.

II. System Level Simulation

We first simulated the ADC at the system level. We began by calculating the requirements of our system. From our student ID, we can determine that $\alpha = 0.911$, which means that our bandwidth is $f_{3dB} = 38.22\,\mathrm{kHz}$. To compute our minimal SNR, we assume that the power of the noise in our system will be about equal to the power of the signal harmonics. Thus, we require SNR $=$ 2 SNDR, or SNR $= 63\,\mathrm{dB}$ at the minimum. We can therefore compute our desired oversampling rate as

$$OSR = 10^{(SNR_{peak}-2.61)/30} = 103.04$$

Using this result, we can determine that our minimum sampling frequency must be

$$f_s = 2\ OSR\ f_{3dB} = 7.88\,\mathrm{MHz}$$

To allow for some margin, we chose $f_s = 10\,\mathrm{MHz}$.

Next, we set up the simulation in Simulink, as shown in Figure 1. This model takes into account several non-ideal circuit parameters in order to provide more accurate results. It includes the kT/C noise which is produced by the switched capacitor and the two transmission gates, with the capacitance C chosen to be $1\,\mathrm{pF}$ as a starting point and the resistance R chosen to be twice the worst case on resistance of our transmission gate, as given in Figure 16. The model also includes the integrator and comparator input referred noise, which was modeled by fitting the data in Figures 20 and 23 to a curve of the form SND $= a + b/s$ to account for both thermal and flicker noise. It also takes into account the integrator offset, the comparator offset, and the finite DC gain of the operational amplifier.

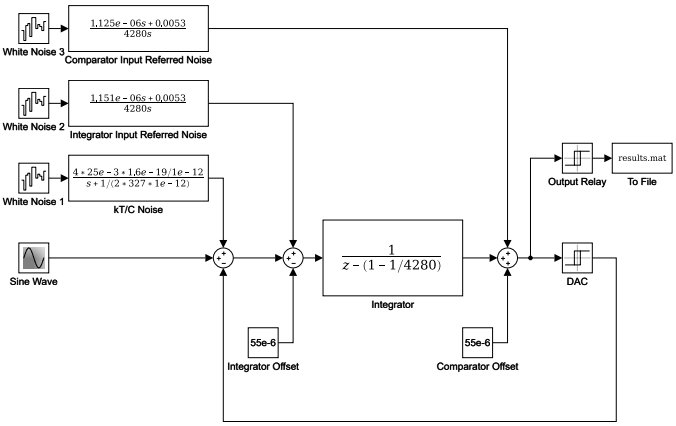

Fig. 1. A system level block diagram of the $\Delta\Sigma$ A/D converter.

We used a $0.2\,\mathrm{V}$ amplitude sine wave with a DC offset of $0.6\,\mathrm{V}$ as our input to the system, and we sampled this input at a rate of $10\,\mathrm{MHz}$. In addition, we used an input frequency of $20\,\mathrm{kHz}$ to push any harmonics out of our bandwidth. For all our simulations, we used a duration of $2.1\,\mathrm{ms}$, discarding

the first $0.1\,\mathrm{ms}$ and obtaining frequency bins of $500\,\mathrm{Hz}$ each for our SNDR calculations.

To find the peak SNDR, we swept the amplitude of the DAC output around a DC offset of $0.6\,\mathrm{V}$. The results are shown in Figure 2. From this plot, we can see that the peak SNDR of $65.7803\,\mathrm{dB}$ occurs when the DAC output amplitude is $0.22\,\mathrm{V}$. However, it is worth analyzing the factors that contribute to this SNDR distribution. For DAC output voltages close to $0.2\,\mathrm{V}$, the minimal error at the integrator input is very close to $0\,\mathrm{V}$, and is thus susceptible to changing sign due to offset and noise. For high DAC output voltages, the maximal error at the integrator input approaches and even exceeds $0.6\,\mathrm{V}$, which can cause the operational amplifier to saturate. Thus, the best SNDR is obtained in the middle range, with the fluctuations there likely being caused by noise and the lack of samples. In order to provide a $20\,\%$ margin for PVT, we chose $0.24\,\mathrm{V}$, corresponding to a SNDR of $63.7303\,\mathrm{dB}$ and DAC outputs of $0.36\,\mathrm{V}/0.84\,\mathrm{V}$. The power spectral density of the output with these settings is shown in Figure 3.

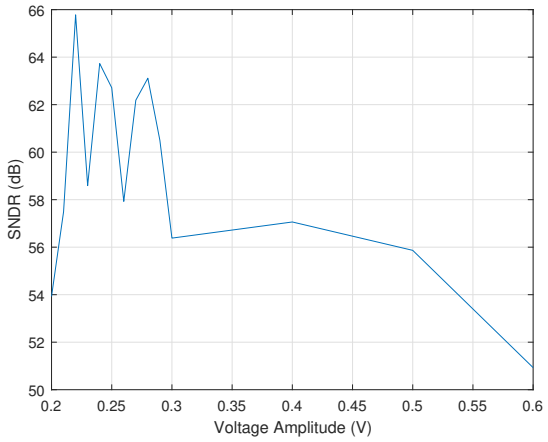

Fig. 2. SNDR vs. DAC output amplitude for the $\Delta\Sigma$ A/D converter.

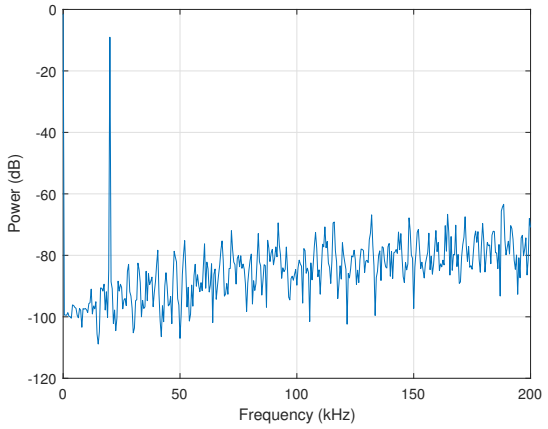

Fig. 3. Power spectral density for the output of the $\Delta\Sigma$ A/D converter with the DAC outputs set to $0.36\,\mathrm{V}/0.84\,\mathrm{V}$.

III. Circuit Level Simulation

We next mapped the system to a circuit using Cadence. To implement the ADC, we first designed and laid out several digital components. We then implemented a transmission gate component for the switched capacitor. Next, we refitted the operational amplifier from Assignments #2 and #3 to implement an integrator, and we modified it to implement a comparator. Finally, we put these components together to create our ADC.

A. Digital Logic

We first implemented a basic inverter. The schematic of this implementation is shown in Figure 4. Since the inverter was not required to drive large capacitances and speed was not a concern, we chose to minimize area and power consumption and used a small size of $0.4\,\mu\mathrm{m}/0.12\,\mu\mathrm{m}$ for our NMOS transistor. To account for the lower mobility of holes, we then chose a size of $1.0\,\mu\mathrm{m}/0.12\,\mu\mathrm{m}$ for our PMOS transistor. A screenshot of the layout is shown in Figure 5.

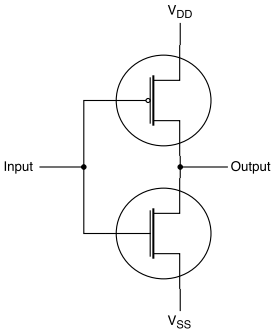

Fig. 4. A schematic of the inverter.

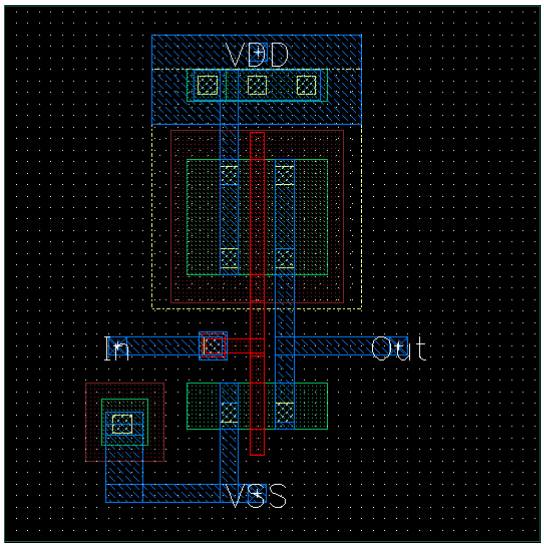

Fig. 5. A screenshot of the layout for the inverter.

Then, we implemented a two-input NOR gate. The schematic of this implementation is shown in Figure 6. To match the speed of the inverter, we selected the size of the NMOS transistors to be $0.4\,\mu\mathrm{m}/0.12\,\mu\mathrm{m}$. Since the PMOS transistors are in series, we used a larger size of $2.0\,\mu\mathrm{m}/0.12\,\mu\mathrm{m}$ to provide an equivalent size to the PMOS transistor of the inverter. A screenshot of the layout is shown in Figure 7.

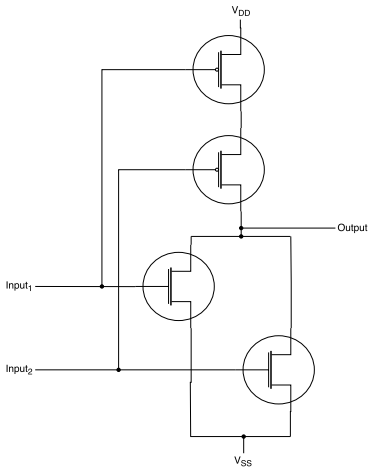

Fig. 6. A schematic of the two-input NOR gate.

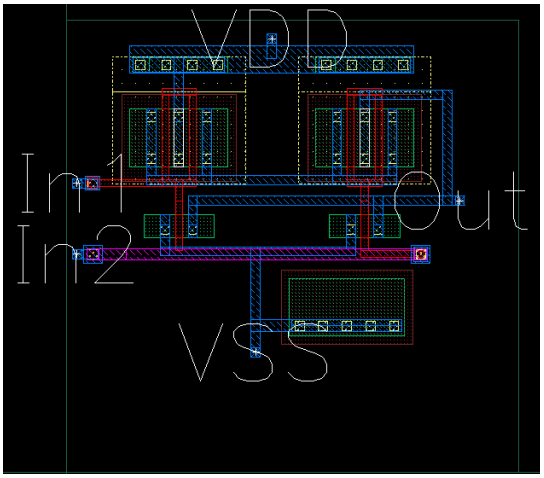

Fig. 7. A screenshot of the layout for the two-input NOR gate.

Next, we implemented a three-input NOR gate. The schematic of this implementation is shown in Figure 8. To match the speed of the inverter, we selected the size of the NMOS transistors to be $0.4\,\mu\text{m}/0.12\,\mu\text{m}$. Since the PMOS transistors are in series, we used a larger size of $3.0\,\mu\text{m}/0.12\,\mu\text{m}$ to provide an equivalent size to the PMOS transistor of the inverter. A screenshot of the layout is shown in Figure 9.

Then, we implemented an edge triggered D flip-flop to serve as a register for our ADC output. The schematic of this implementation is shown in Figure 10. A screenshot of the layout is shown in Figure 11. This circuit is triggered by the falling edge of the clock.

Finally, we implemented a phase splitter in order to generate non-overlapping 2 phase clock signals that we could use to operate our switched capacitor circuit. We achieved this by negating the clock to provide the second phase and then using an SR latch and a series of buffers to ensure that the two phases never overlap. A schematic of this implementation is shown in Figure 12. A screenshot of the layout is shown in Figure 13.

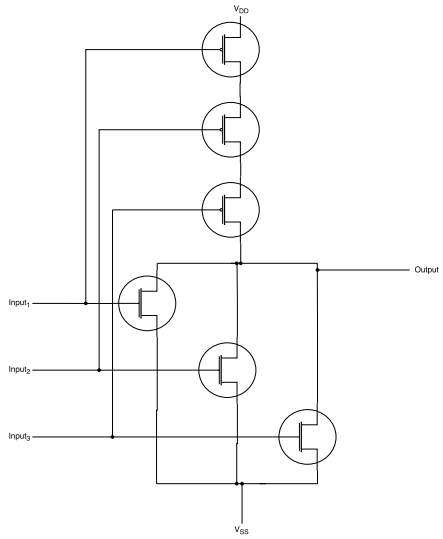

Fig. 8. A schematic of the three-input NOR gate.

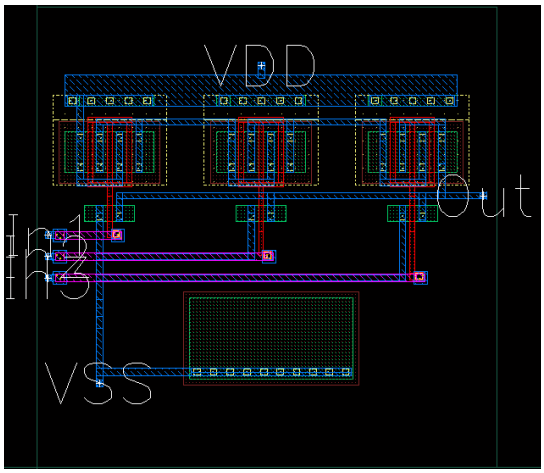

Fig. 9. A screenshot of the layout for the three-input NOR gate.

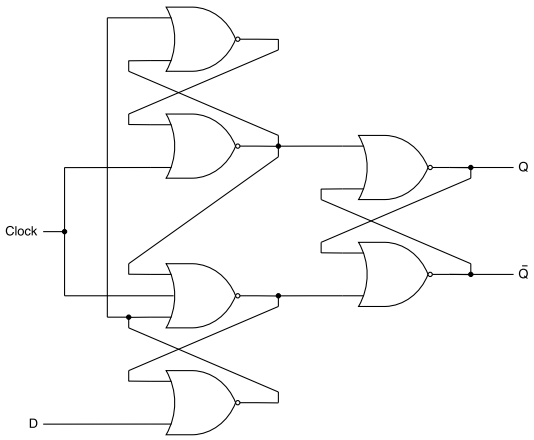

Fig. 10. A schematic of the D flip-flop.

B. Transmission Gates

Then, we used the inverter component to implement a basic transmission gate, as shown in Figure 14. Since these

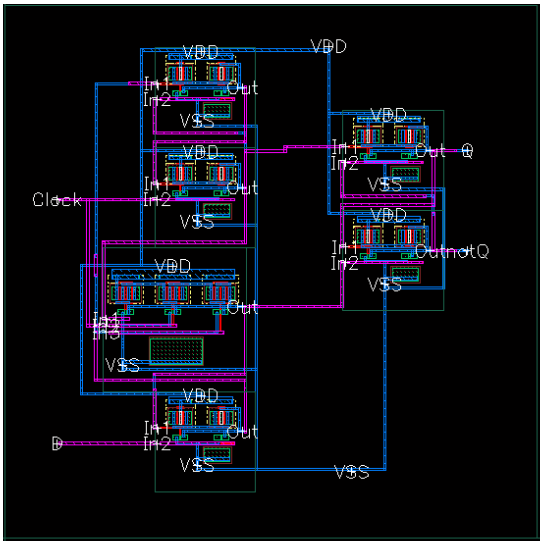

Fig. 11. A screenshot of the layout for the D flip-flop.

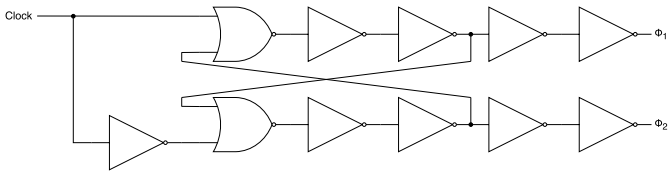

Fig. 12. A schematic of the phase splitter used to generate non-overlapping 2 phase clock signals.

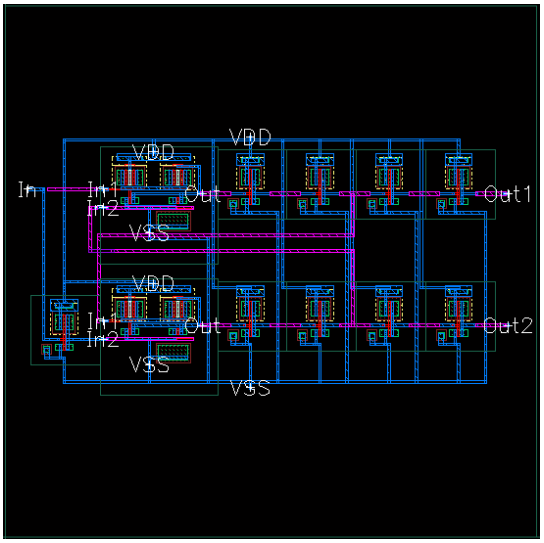

Fig. 13. A screenshot of the layout for the phase splitter.

gates would be required to drive larger capacitances, we used larger sizes of $10\,\mu\text{m}/0.12\,\mu\text{m}$ for the NMOS transistor and $25\,\mu\text{m}/0.12\,\mu\text{m}$ for the PMOS transistor. A screenshot of the layout is shown in Figure 15.

In order to produce a better Simulink simulation and model the kT/C noise, we measured the on resistance of the transmission gate by using it to drive a $10\,\text{k}\Omega$ load and measuring the voltage drop across the gate and the current drawn by the gate for different inputs while the gate was active. The results

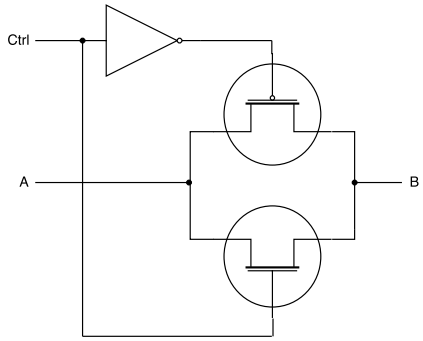

Fig. 14. A schematic of the transmission gate.

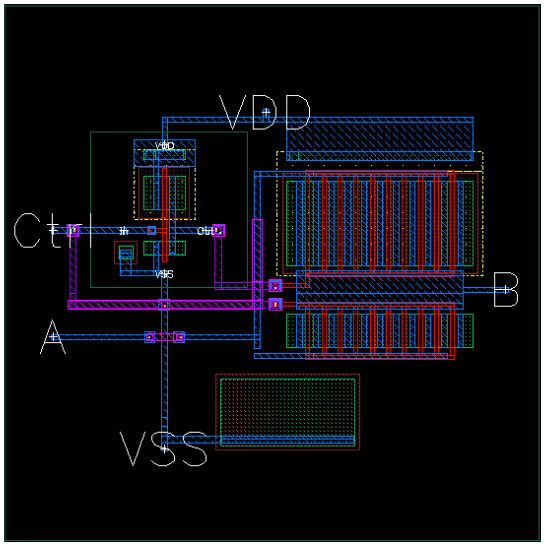

Fig. 15. A screenshot of the layout for the transmission gate.

are shown in Figure 16, which shows that we have a maximum on resistance of $R_{on,max} = 327\,\Omega$.

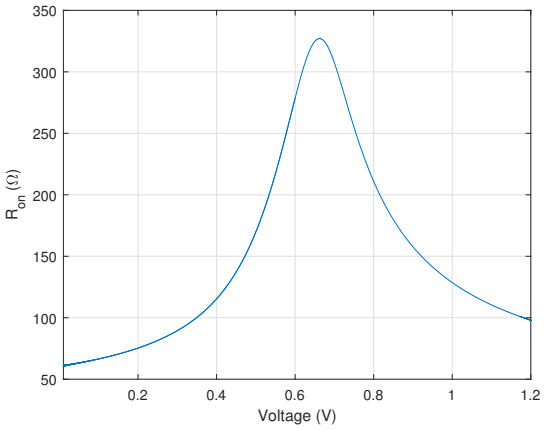

Fig. 16. R_{on} vs. input voltage for an active transmission gate.

C. Operational Amplifier

Next, we used the operational amplifier designed in the previous assignments as an integrator. A full schematic is shown in Figure 17. The layout is shown in Figure 18.

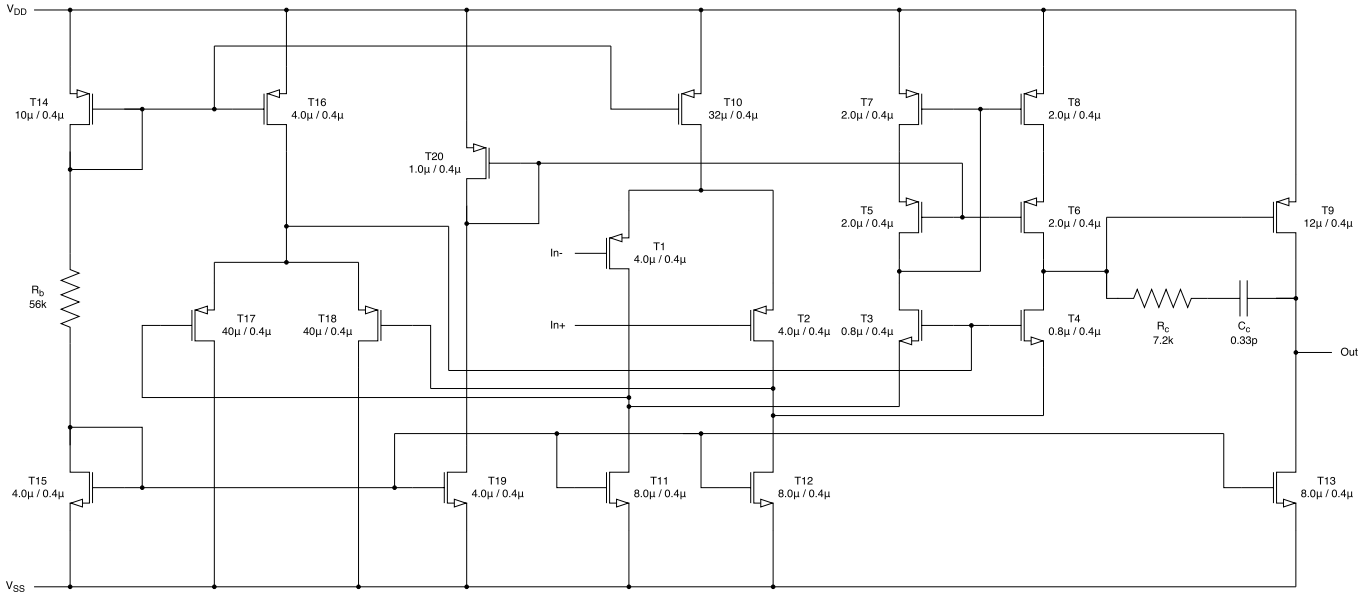

Fig. 17. A schematic of the folded cascode operational amplifier.

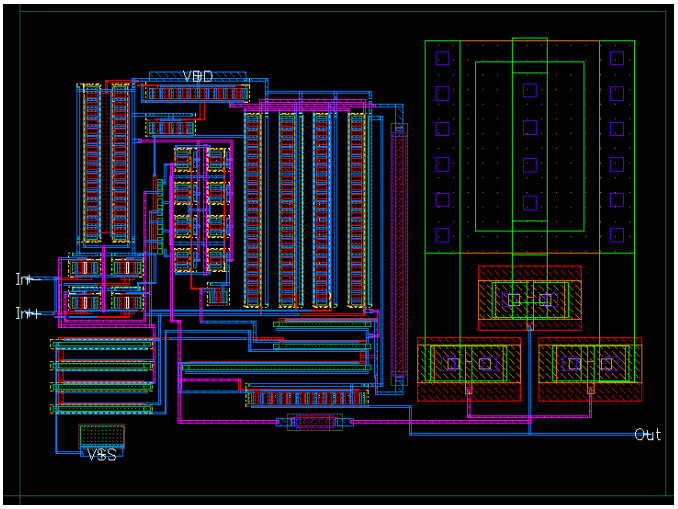

Fig. 18. A screenshot of the layout for the folded cascode operational amplifier.

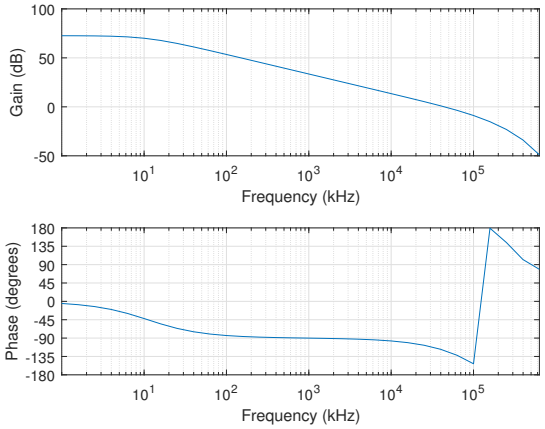

Fig. 19. AC differential mode frequency response of the folded cascode operational amplifier.

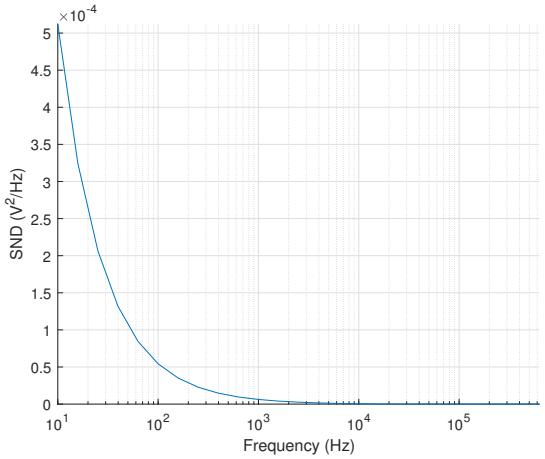

Fig. 20. Output-referred AC noise of the folded cascode operational amplifier.

In the interest of creating a better Simulink model, we measured several parameters of the amplifier. We found an offset voltage of $V_{os} = 55\,\mu\text{V}$, a DC gain of $A = 4.28\,\text{kV/V}$, a bandwidth of $f_{3dB} = 11.07\,\text{kHz}$, and a unity gain bandwidth of $f_t = 44.17\,\text{MHz}$. In addition, the open loop AC response and the output referred AC noise are shown in Figures 19 and 20 respectively.

D. Comparator

We then modified the operational amplifier to produce a comparator by removing C_c and R_c from Figure 17. The layout of this comparator is shown in Figure 21.

In the interest of creating a better Simulink model, we measured several parameters of the comparator. We found an offset voltage of $V_{os} = 55\,\mu\text{V}$, a DC gain of $A = 4.28\,\text{kV/V}$,

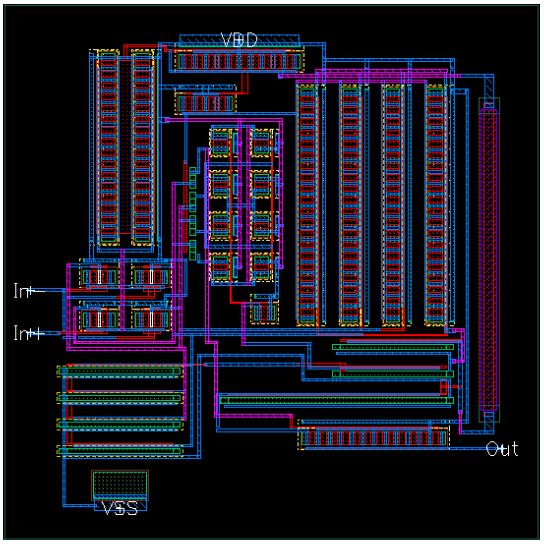

Fig. 21. A screenshot of the layout for the comparator.

and a bandwidth of $f_{3dB} = 500.5\,\text{kHz}$. In addition, the open loop AC response and the output referred AC noise are shown in Figures 22 and 23 respectively.

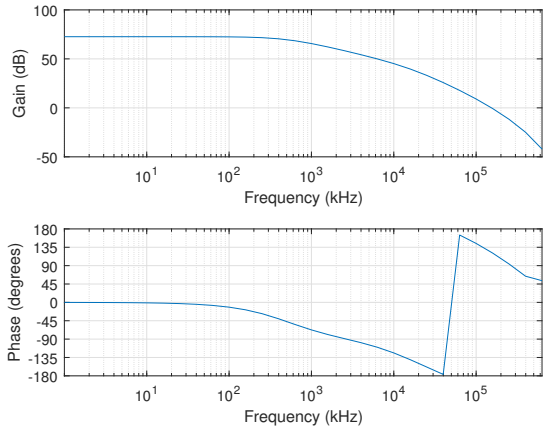

Fig. 22. AC differential mode frequency response of the comparator.

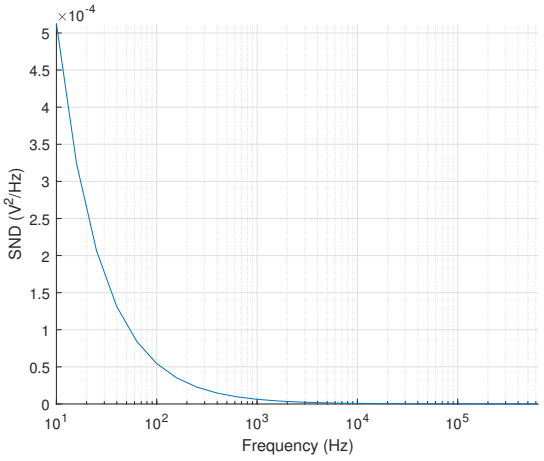

Fig. 23. Output-referred AC noise of the comparator.

E. ADC

With these subcomponents in hand, we then implemented the complete ADC, as shown in Figure 24. We chose values of $C_1 = C_2 = 1.0\,\text{pF}$ as a starting point. In addition, we used the reference voltages of $V_{ref+} = 0.84\,\text{V}$ and $V_{ref-} = 0.36\,\text{V}$ that were previously selected in the system level simulation. Note that instead of using Φ_1 as the clock for the flip-flop, we used an inverted input clock. We did this to ensure that the clocks Φ_1 and Φ_2 drive equal loads so that they are equally delayed and do not overlap. An inverter was required to ensure that the flip-flop clock matches Φ_1.

We next performed a transient analysis of the circuit. As we did in our system level simulation, we used a $10\,\text{MHz}$ clock and a $0.2\,\text{V}$ amplitude, $20\,\text{kHz}$ sine wave input signal. We then ran the simulation for $2.1\,\text{ms}$ and discarded the first $0.1\,\text{ms}$, which allowed us to get $500\,\text{Hz}$ bins in our FFT. One issue we encountered was that the FFT expects uniform sampling while Cadence produces non-uniformly sampled outputs. To fix this, we set the `strobeperiod` option of the transient simulation to $10\,\text{ns}$, which produces a uniformly sampled output and gives us 10 points per period of the sampling clock. In the FFT calculations, we then downsampled this output at our sampling frequency of $10\,\text{MHz}$.

A plot of the power spectral density we obtained is shown in Figure 25. This figure shows that we obtained a SNDR of $65.4429\,\text{dB}$ over our bandwidth of $38.22\,\text{kHz}$.

With the schematic level simulation meeting the specifications, we next moved on to layout. A screenshot of the complete layout is shown in Figure 26, which measures $150\,\mu\text{m}$ by $140\,\mu\text{m}$ in total. We used several approaches to ensure good performance. First, the analog and digital parts were separated into their own sections of the IC. This ensures that the parasitic capacitance between these two parts of the circuit is low and thus that the large, fast digital signals do not couple with the small analog signals. In addition, the power supply lines were split between the two sections. A closer view of the digital section is shown in Figure 27.

The other critical consideration was the intersection of analog and digital signals that occurs in the transmission gates. In order to ensure that the small analog signals are not coupled to the large digital signals, we used shielding wherever these two types of signals got too close. An example is shown in Figure 28, where V_{SS} was extended to act as a shield between the clock signal Φ_1 on the Ctrl line and the analog signal that passes from A to B.

We then extracted the parasitics from this layout and performed a transient analysis of the circuit with the same parameters as for the schematic level simulation. A plot of the power spectral density we obtained is shown in Figure 29. This figure shows that we obtained a SNDR of $60.3449\,\text{dB}$ over our bandwidth of $38.22\,\text{kHz}$, which meets the specifications.

A comparison of the PSD obtained for the different simulations is shown in Figure 30. This figure shows that the results obtained were similar across all simulations types, with the main difference occurring at the low frequencies. At these frequencies, the layout parasitics seem to have caused an increase in noise compared to the other two simulations. This translates to the decrease in SNDR from $63.7303\,\text{dB}$ for

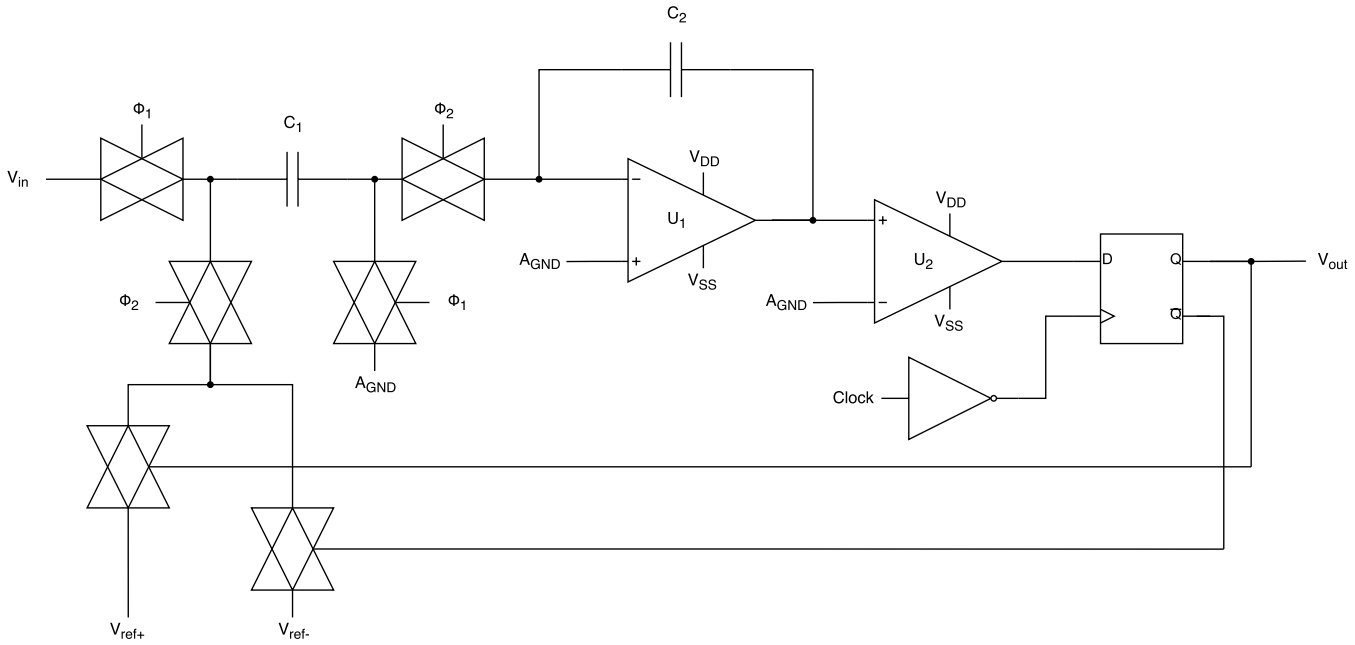

Fig. 24. A schematic of the $\Delta\Sigma$ A/D converter.

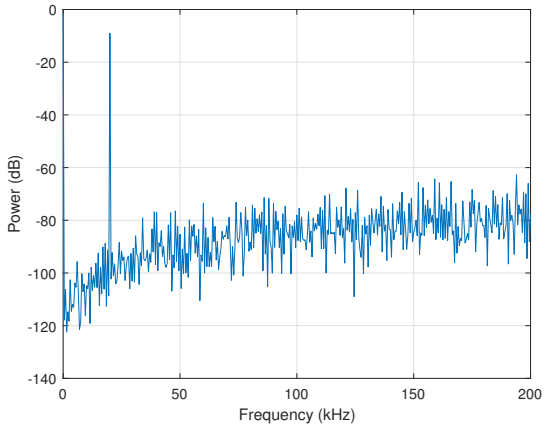

Fig. 25. Power spectral density for the output of the schematic level simulation of the $\Delta\Sigma$ A/D converter.

Fig. 26. A screenshot of the complete layout for the $\Delta\Sigma$ A/D converter.

the system level simulation and $65.4429\,\mathrm{dB}$ for the schematic level simulation to $60.3449\,\mathrm{dB}$ for the layout level simulation.

To further characterize the performance of the ADC, we also measured the gain error and offset. We used MATLAB to create a FIR low pass digital filter with a pass-band frequency of $38.22\,\mathrm{kHz}$, a stop-band frequency of $41.78\,\mathrm{kHz}$, a pass-band ripple of $0.1\,\mathrm{dB}$, and a stop-band attenuation of $80\,\mathrm{dB}$. We then passed our output signal through this filter and measured the error when compared to the original signal.

The filtered output signal on a restricted time interval is shown in Figure 31. The corresponding transfer characteristic is shown in Figure 32. These figures show that the ADC produces a net offset of about $-4.38\,\mathrm{mV}$. In addition, the best fit curve through the transfer characteristic shows a gain of 1.0023, which corresponds to a gain error of $0.23\,\%$.

We next plotted the error with offset subtracted against the input signal value, as shown in Figure 33. This figure shows that the error has a circular shape, which suggests that it is not actually an error but a phase delay in the signal. In fact, we can compute the value of the delay as $Asin(\phi) = \epsilon$, where A is the input signal amplitude and ϵ is the error with no input. The result is that $\phi = 1.06°$, so the total time delay is $\tau = 147\,\mathrm{ns}$, which matches the delay observed in Figure 31.

Finally, we measured the power supply current over a $50\,\mu\mathrm{s}$ time period and multiplied it by $V_{DD} = 1.2\,\mathrm{V}$ in order to calculate the circuit's power dissipation. Partial results are shown in Figure 34. We can see that large spikes occur when the circuit's digital components are switching. The peak power

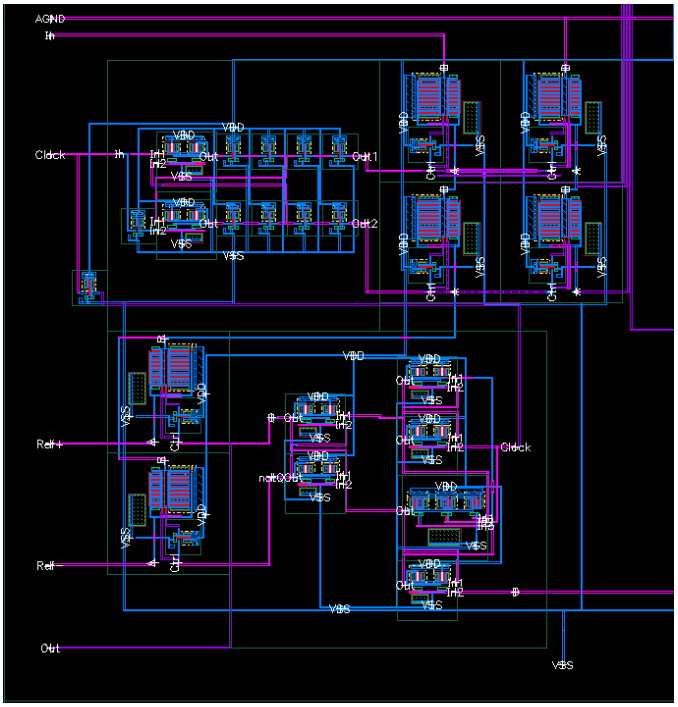

Fig. 27. A screenshot of the layout of the digital components in the ΔΣ A/D converter.

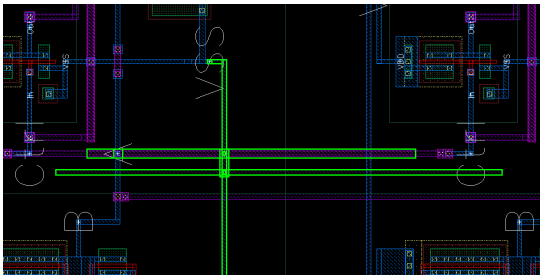

Fig. 28. A screenshot of signal shielding in the layout of the ΔΣ A/D converter.

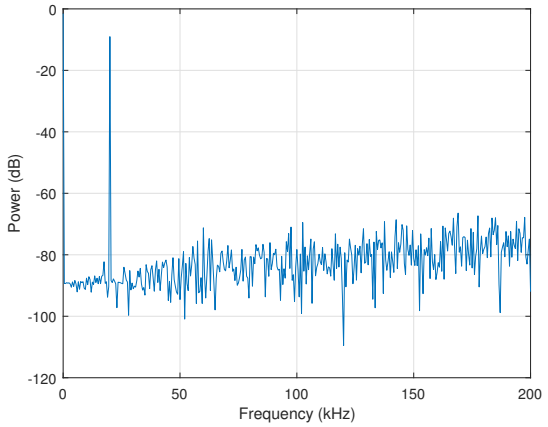

Fig. 29. Power spectral density for the output of the layout level simulation of the ΔΣ A/D converter.

dissipation is therefore 837 µW. Integrating the curve and dividing by the interval yields an average power dissipation of 194 µW.

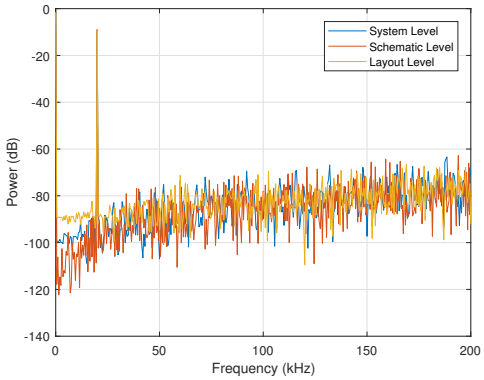

Fig. 30. Power spectral density for the output of the ΔΣ A/D converter for different simulation types.

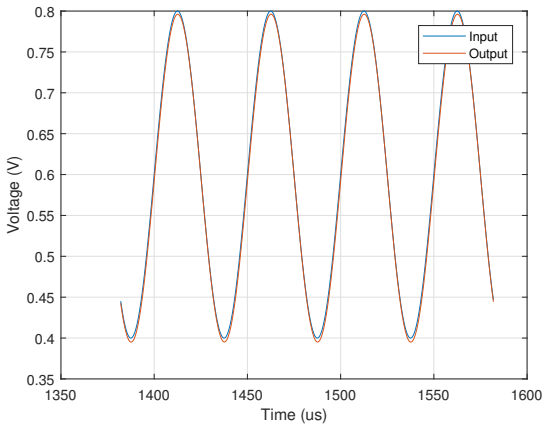

Fig. 31. Filtered output and input for the ΔΣ A/D converter.

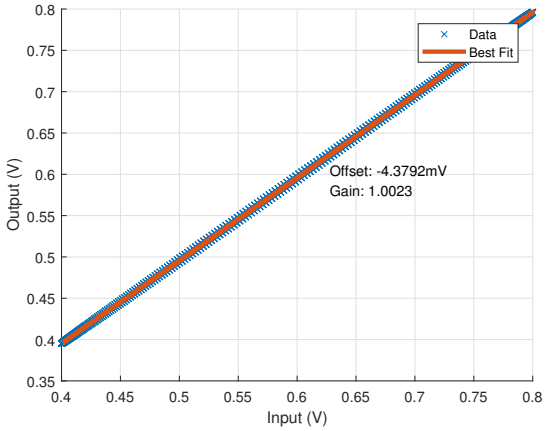

Fig. 32. Filtered output vs. input for the ΔΣ A/D converter.

Since we were not given a quantitative requirement for power dissipation, we can evaluate our implementation by comparing our average power dissipation of 194 µW to the Assignment #2 maximum of 200 µW for a single operational amplifier. This comparison shows that our power dissipation is quite low, given that our combined circuit consumes less power on average than the maximum we were given for a single operational amplifier.

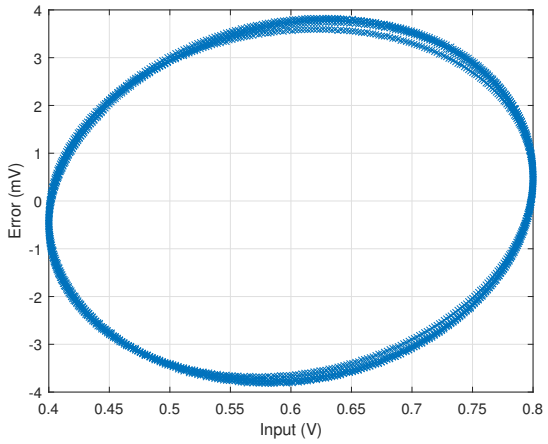

Fig. 33. Error with offset subtracted vs. input for the $\Delta\Sigma$ A/D converter.

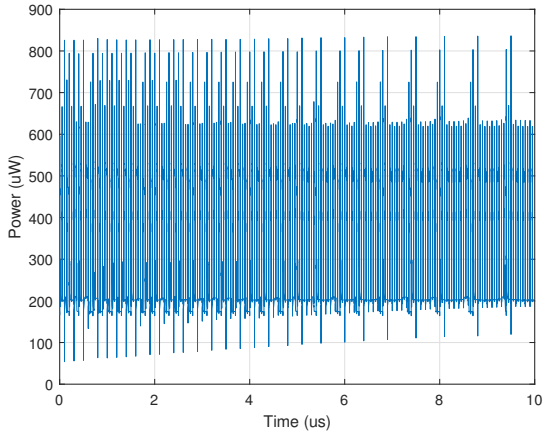

Fig. 34. Power dissipation of the $\Delta\Sigma$ A/D converter.

IV. Conclusions

In conclusion, we designed, simulated, laid out, and analyzed a first order, single bit, $\Delta\Sigma$ A/D converter using MATLAB and Cadence. To meet our specifications of a $38.22\,\mathrm{kHz}$ bandwidth and a peak SNDR of at least $60\,\mathrm{dB}$, we used a sampling frequency of $10\,\mathrm{MHz}$. We then chose DAC output voltage levels of $0.36\,\mathrm{V}/0.84\,\mathrm{V}$ in order to maximize the SNDR while taking PVT into account. With these parameters, our system level simulation yielded a SNDR of $63.7303\,\mathrm{dB}$, our schematic level simulation yielded a SNDR of $65.4429\,\mathrm{dB}$, and our layout level simulation yielded a SNDR of $60.3449\,\mathrm{dB}$. Therefore, our A/D converter satisfies all the given requirements.