ANALOG MICROELECTRONICS (304-534A)
Course Project (Two Phases: Initial & Final)

A First-Order, Single-bit, Lowpass ΔΣ A/D Converter: System-Level and Circuit-Level Implementation

Handout Date: Thursday Nov. 9, 2017
Initial Phase Due Date: Tuesday Dec. 5, 2017
Final Phase Due Date: Thursday Dec. 14, 2017 Before 5 pm

Note that these *due dates* are final. Lateness receives a grade of 0.

Conditions:

Project is to be performed by the student alone.

Objectives:

(a) Design a first-order low-pass delta-sigma analog-to-digital (ΔΣ A/D) converter at the system level (using MATLAB and Simulink) satisfying the following specifications:

Output:	1 bit
Power Supply:	1.2 V
Technology:	IBM CMOS 0.13 μm
Bandwidth:	(1+α) x 20 kHz
SNDR (peak):	60 dB (> 10 bits)
Input Voltage Range:	± 0.20 V relative to AGND
Power Dissipation:	Minimum

where α is to be determined by the following algorithm:

α = *(last 3 digits of student ID#)/1000*

example:

Student ID#: 360171436, α = 436/1000=0.44

Assume all the components to be ideal. This will allow you to use mathematical transfer functions to describe the system behavior. See the project guidelines below for pointers to system level simulation.

(b) Map the system-level block diagram for the ΔΣ A/D converter designed above into a switched-capacitor circuit. Use the op-amp you designed in Assignment #2. Simulate the performance of your switched-capacitor circuit at the schematic level and compare its performance with the system-level (MATLAB/Simulink) simulation from part (a). Only schematic-level simulations are required for the initial phase of this project.

(c) Hand-in the ***initial results*** of this analysis to the instructor for initial grading in a proper written report (see below). This step is necessary to ensure that the designer has a design target in mind. The designer is not required to optimize the schematic design at this point; just confirm that a best-case target has been identified.

(d) This next phase of the project, denoted as the ***final phase***, is to map the circuit design into a physical layout using the virtuoso layout tool in Cadence. Your implementation should include a full layout and should be free of DRC and LVS errors. Measure the performance of an extracted view of your circuit, which includes all parasitic capacitances and resistances, and it should be compared to the best-case target simulation found in parts (b) and (c).

The inputs/outputs to your system simulation should include the following:

- An input analog signal and an output digital single-bit-stream.
- A single reference clock to act as the input to the multi-phase clock generation circuit needed to drive the SC circuit.
- The circuit is to operate off a single 1.2 V supply. You are allowed to modify the analog-ground supply from the nominal of 0.6 V, if needed, to account for the op amp input offset voltage.
- The most positive and most negative DAC reference voltages can be brought in as external ideal voltage references, if deemed necessary.

(e) ***Hand-in the final results*** of your design and analysis to the instructor for final grading in a proper written report (see below). The ultimate objective is to demonstrate a working ΣΔ modulator that meets the performance specifications listed in part (a) above.

Project Guidelines:

Refer to tutorial #3 (Simulating Sigma-Delta Modulators Using MATLAB and Simulink) from the course web site if you need additional help.

(a) Use MATLAB/Simulink to create a system-level simulation.

- Calculate the required SNR, the minimum OSR, and the sampling frequency f_s , that your system will require.
- Implement the ΔΣ A/D converter using a block-level approach in Simulink (Refer to Figure 1 in the tutorial).
- To observe the behavior of the modulator, plot the peak SNDR as a function of the DAC output levels and ensure the peak SNDR is greater than the desired level for an input sinusoidal with amplitude that covers the maximum input range of the modulator.
- Use MATLAB to convert the Simulink data into frequency domain data, which will allow you to interpret your A/D converter performance (Figure 2). You can use, if needed, additional MATLAB processing, such as windowing, to improve your SNR calculations.

(b) Use Cadence/Analog Environment to perform your circuit level simulations (Figure 3).

- You will need to design a high-speed comparator for this assignment. It may be implemented using your op amp and a single flip-flop, or you can resort to a simpler and more compact design. Refer to the class notes for different comparator topologies.
- The switches can be implemented using transmission gates. A good starting point for the transmission gate sizes is 10μ/0.13μ. This is not necessarily the optimum size, as it depends on the values that you choose for the capacitors.
- Set signal ground reference to the most convenient voltage level that maximizes your signal handling capability.
- It is best to import your Cadence simulation data into MATLAB in order to interpret your A/D converter performance.

Submission Guidelines:

- Include your SNR, OSR and F_S calculations, as well as all relevant Simulink and Cadence schematics used in your simulations. Also include the path in which your design files reside.
- Provide a comparison of your system-level simulations with your circuit-level simulations.
- For the ***initial phase*** of the project, it is not necessary that your circuit-level (Cadence) simulations meet the expect SNDR specification. However, if your circuit implementation does not meet this specification, or if there are significant differences between your system-level and circuit-level simulations, then discuss ways of dealing with these issues during the final phase of your project. For example, determine which circuit elements you think may be causing you to lose performance, or discuss ways in which circuit non-idealities might be more accurately modeled in Simulink. It is possible that the comparator could be limiting your performance. Make sure you test it separately (refer to the class notes for static and dynamic testing of comparators).
- For the ***final phase*** of the project, exercise your own judgment in providing a comprehensive description and characterization of your ΔΣ A/D converter. Provide a summary of results the initial phase report, but stick mainly to system-level considerations, which directly affect the performance of your ΔΣ A/D converter. Be sure to include details, which demonstrate your insight into the operation of your system.

Write-Up Guidelines:

All assignments and project reports must be prepared in an IEEE paper style consisting of a double-column single-space format, and must adhere to the following:

- Title page - Title of the assignment/project, authors' name, and course name.
- Abstract - Abstract of the assignment/project report.
- Introduction
- Main body of the assignment/project report.
- Figures should be drawn separately from the Cadence Schematic entry program.
- Conclusions
- References - list of the books, journal papers, conference papers, and other publications used in the report. References must be listed using IEEE reference styles. You need to take a look at *IEEE Transactions on Circuits and Systems I - Regular Papers* and *IEEE Journal of Solid-State Circuits* for IEEE reference styles on books, journal papers, conference papers, and technical reports.
- Appendices