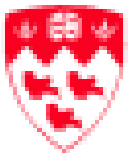

McGill University

Analog Microelectronics 304-534A

Take Home Final Exam

Prof. G. Roberts
(Email) gordon.roberts@mcgill.ca

Handout Date: Friday Dec. 15, 2017 By Email @ 9 AM
Due Date: Friday Dec. 15, 2017 - Return by Email before 9 PM

This paper contains the contents to a final examination for Analog Microelectronics 304-534. It contains a single question. This examination is to be carried out by the student alone, without any consultation with one's peers or known experts. During the marking phase, I will be closely monitoring answers that appear to be solved in similar ways. Marks will be divided between those that shared answers to specific questions. If, at any time, you are not sure what a question is asking, make a practical assumption and proceed from there.

In all cases, even if you cannot meet the desired specification, part marks will be given. So answer as much of the question that you can and avoid getting hung up on low-level details the first time through. Please manage your time carefully, as this is generally where students go wrong with a design-type exam.

The solution to the exam in PDF format can be submitted by email to *gordon.roberts@mcgill.ca* prior to the 9 PM deadline.

Good Luck!

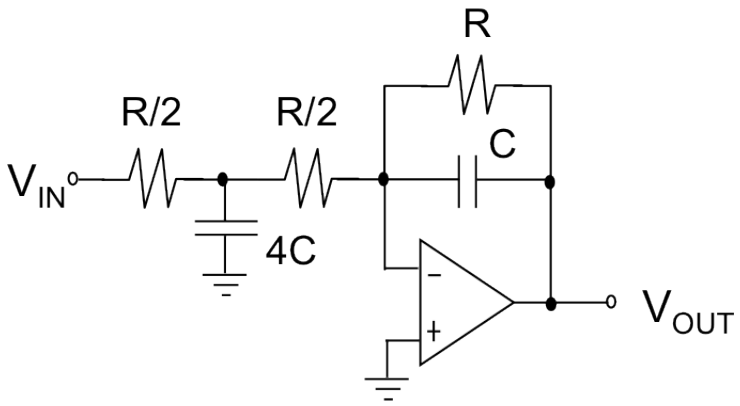

Figure 1: Second-Order Anti-Aliasing Filter Circuit

1. Design the fully monolithic anti-aliasing filter shown in Fig. 1 for a ΣΔ data conversion application developed in the 130 nm CMOS technology from IBM (same technology used in course). The ΣΔ modulator has a peak SNDR of 70 dB and operates over a voltage range of 0.9 V centered around 0.6 V. The passband of the ΣΔ modulator is from DC to 100 kHz and has a sampling rate of 16 MHz.

   The filter should exhibit a DC gain of unity, experience a maximum attenuation of no more than 0.1 dB and a phase shift of no greater than 10 degrees over the passband range of the ΣΔ modulator. In addition, the attenuation of the filter must be greater than 40 dB above 15 MHz.

   The input resistance to the filter should be no less than 1 kΩ, as it will be driven with a source with a nominal low resistance but not carefully controlled. The output resistance of the filter is to be 20 Ω or less in order to drive a 1 pF input capacitance to the ΣΔ modulator with little distortion.

   The noise generated by the anti-aliasing filter circuit must be less than the input-referred quantization noise generated by the ΣΔ modulator, estimated at about 100 μV (RMS).

   For sake of time, consider that a single-ended design is sufficient for the data conversion application described here.

   Consider all practical issues that relate to selecting the aspect ratio of all transistors in your circuit, as well as any passive components that you need. ***Please note that a Cadence layout is not required for this question*** but a discussion and rough sketch of the layout of all passive and active components and their dimensions must be provided with your solutions. It is here where some of the issues related to the practicality of the design can be identified.

   Marks will be attributed in a manner that reflect your design understanding, together with supporting simulation evidence to suggest the design can meet the above-mentioned specifications.