ANALOG MICROELECTRONICS (304-534A)
Assignment # 3

Operational Amplifier Design: Layout and Verification

Handout Date: Wednesday Oct. 24th, 2017
Due Date: Wednesday, Nov. 14th, 2017

Conditions:

Assignment is to be performed ***individually*** by the student.

Objectives:

The objective of this assignment is to create a layout of the multi-stage amplifier that you designed in assignment #2. This exercise will help the student learn the Cadence Design Tools for analog circuits.

Assignment Guidelines:

- The design sequence which must be followed is (1) layout, (2) DRC, (3) extraction with parasitics, (4) LVS and (5) circuit simulation using the extracted layout with parasitics included.
- DRC (Design Rule Checking) is the process through which your layout is examined for manufacturability. It consists of a set of rules which explicitly state what can or cannot be achieved through the manufacturing process (such as the minimum separation between two layers, the minimum width of a metal line, etc...). Use the DRC often - it will help to prevent layout sizing errors, which can be time consuming to fix once your layout is near completion.
- Extraction is the process through which the individual transistors you have laid out are identified and netlisted. Extraction is also used to determine the layout-dependent parasitic capacitances (which you would normally want to minimize) not included in your schematic-level simulation.
- LVS Checking (Layout Versus Schematic Checking) is the process through which the extracted layout netlist is compared to the original schematic netlist for the purpose of detecting any differences between the two (i.e., layout errors such as wrong connections).
- You will be required to re-measure the design specifications (from Assignment #2) for your extracted operational amplifier. This simulation should include a full parasitic extraction.

Some General Layout Considerations:

- A good layout should minimize parasitic capacitances (i.e., you should merge drains and/or sources on frequency-sensitive nodes, and you should avoid long trace lengths along the signal path.)

- Pay careful attention to transistor matching issues (i.e., lay out your transistors with multiple fingers and pay attention to issues such as the common centroid between transistors which need to be closely matched, like the input differential pair.)
- The overall operational amplifier layout should make efficient use of space and should have a simple overall shape (ideally square or rectangular). Also, ensure that all inputs and outputs of the amplifier are easily accessible from the edge of your layout. This will simplify the integration of your operational amplifier into other designs.

Items To Considers In Write-Up:

- Include a plot of your layout (printed out as legible as reasonably possible) and describe any layout considerations, including those described above, which you used in creating your layout.
- Include a comparison between the simulated performance of your amplifier in Assignment #2 (for schematic only) and comment on any differences you encounter.
- Specify the path where your design files reside.

Write-Up Guidelines:

All assignments and project reports must be prepared in an IEEE paper style consisting of a double-column single-space format, and must adhere to the following:

- Title page - Title of the assignment/project, authors' name, and course name.
- Abstract - Abstract of the assignment/project report.
- Introduction
- Main body of the assignment/project report.
- Figures should be drawn separately from the Cadence Schematic entry program.
- Conclusions
- References - list of the books, journal papers, conference papers, and other publications used in the report. References must be listed using IEEE reference styles. You need to take a look at *IEEE Transactions on Circuits and Systems I - Regular Papers* and *IEEE Journal of Solid-State Circuits* for IEEE reference styles on books, journal papers, conference papers, and technical reports.
- Appendices