ECSE-534
Analog Microelectronics
Assignment #3

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***Abstract*—The layout for the CMOS amplifier designed in Assignment #2 was performed using Cadence. The performance of the amplifier with layout parasitics extracted was then compared to the performance of the amplifier using only the schematic models. No significant difference between the two was found, with the largest change being a small degradation of the step response due to the additional capacitances at each node. In particular, the amplifier was found to still meet all the specifications required of it in Assignment #2 after layout.**

I. Introduction

THIS report follows the layout of the amplifier designed in Assignment #2 using a 0.13 micron process from IBM. We used Cadence and Virtuoso to lay out the amplifier, and we used Analog Environment to perform simulation using said process. In the original specifications, the amplifier was required to meet the following specs:

- DC gain $\geq 60\,\mathrm{dB}$.
- Amplifier poles at approx. $10\,\mathrm{kHz}$ and $100\,\mathrm{MHz}$. Others above this.
- Output voltage swings of at least $50\,\%$ of the supply full scale with a distortion less than $0.2\,\%$ in a unity-gain configuration.
- Input-referred PSD Noise Voltage less than $100\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at $1\,\mathrm{MHz}$.
- Static power dissipation less than $200\,\mu\mathrm{W}$.

In addition, we were assigned a supply voltage of $1.2\,\mathrm{V}$, a common mode input voltage of $0.5\,\mathrm{V}$, and a load capacitance of $0.5\,\mathrm{pF}$.

To perform the given task, we first redesigned the amplifier from Assignment #2 to be better suited for layout. Then, we performed the layout, taking into consideration transistor matching and signal path length. Finally, we extracted the parasitics from the layout and compared the resulting performance of the amplifier to that of the amplifier with just the schematic models.

II. Layout-Ready Design

First, we redesigned the amplifier to be more layout friendly. We did this in order to facilitate the use of techniques for transistor matching in the layout process, such as using a common centroid topology. We made all transistors integer multiples of a unit size transistor in order to reduce component parameter variations. We also ensured that every transistor pair that performs the same function has an even multiplicity in order to better match them using a common centroid topology. We also tweaked the transistor widths to meet the specs in the original assignment after these modifications. The final layout-ready amplifier is shown in Figure 1. The transistor dimensions are given in Tables I and II. We also selected $R_b = 56\,\mathrm{k\Omega}$, $C_C = 0.33\,\mathrm{pF}$, and $R_C = 7.2\,\mathrm{k\Omega}$.

TABLE I
Final transistor dimensions (Part 1).

	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10
W (µm)	4.0	4.0	0.8	0.8	2.0	2.0	2.0	2.0	12	32
L (µm)	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4

TABLE II
Final transistor dimensions (Part 2).

	T11	T12	T13	T14	T15	T16	T17	T18	T19	T20
W (µm)	8.0	8.0	8.0	10	4.0	4.0	40	40	4.0	1.0
L (µm)	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4

III. Layout

Next, we performed the actual layout. We first used the Layout XL functionality in Cadence to transfer our schematic components to the Virtuoso layout tool. Then, we carefully placed the components together and routed them, paying attention to matching and signal path issues. The final layout is shown in Figure 2. We note that the passive components take up most of the space in our layout. The main culprit is the massive biasing silicon resistor. We later found out that poly-silicon resistors are also available, and that these are much smaller. We made note of this fact for the final project.

As an example of matching considerations, we can look at the differential input pair in Figure 3. As this figure shows, the input transistors are split into two pieces each and interleaved to form a common centroid. This approach reduces the effect of process gradients on the matching of the pair, which is important considering that a mismatch in the input differential pair gets amplified at the output and causes a large voltage offset. Other transistor pairs in the circuit were laid out in a similar manner.

As an example of signal path considerations, we can look at the main signal transistors in Figure 4. As this figure shows, the signal path from input to output is relatively short compared to the size of the entire layout. In fact, it is the bias

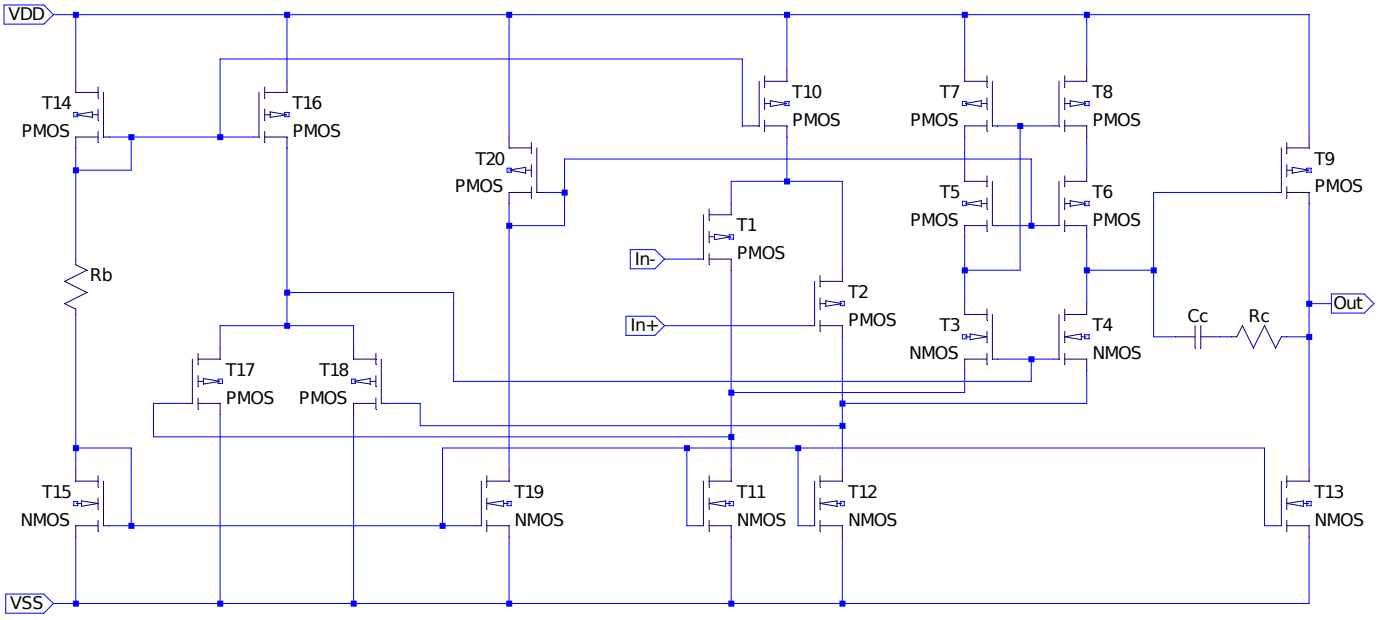

Fig. 1. A schematic of the complete layout-ready amplifier.

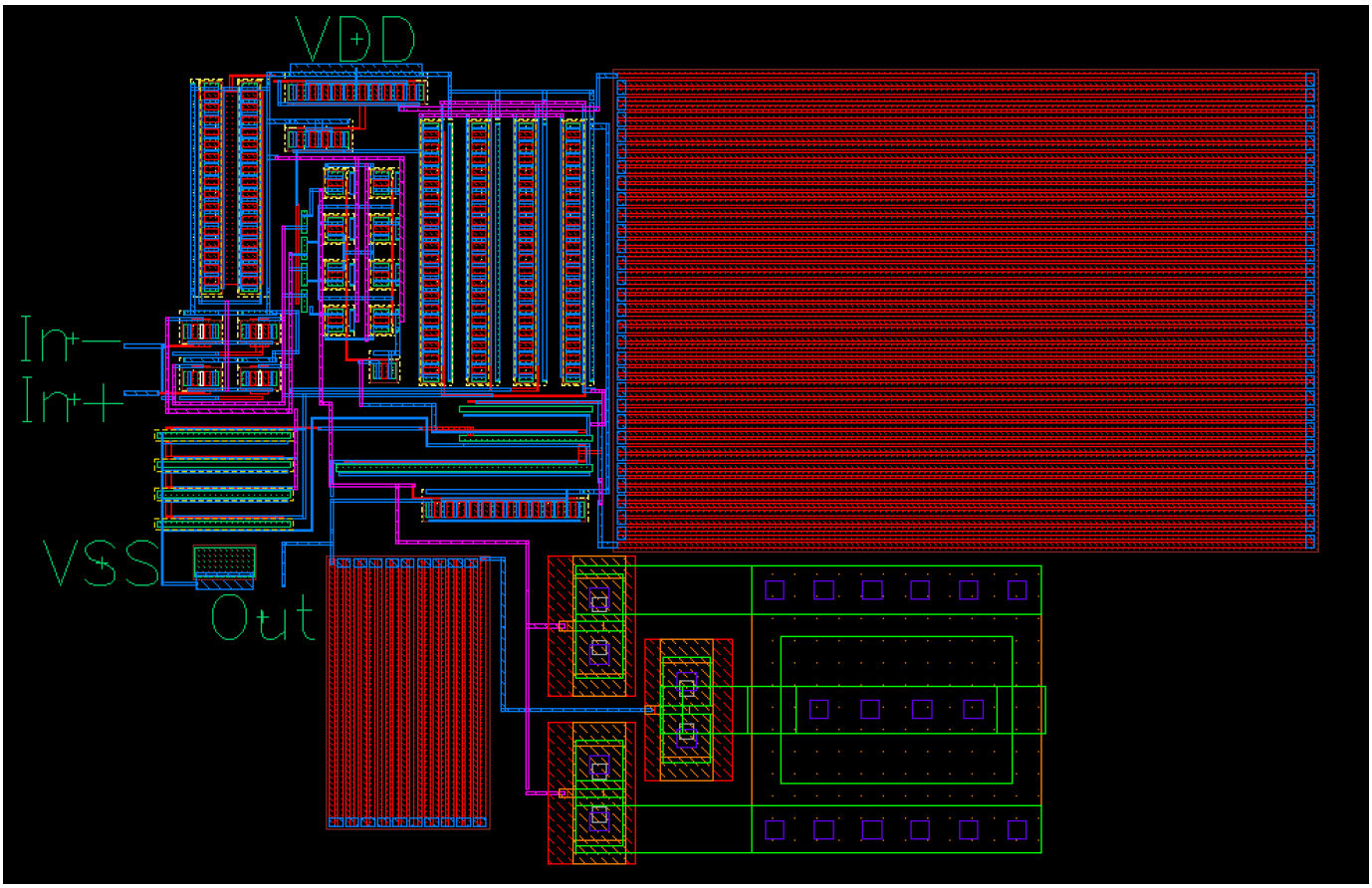

Fig. 2. A screen capture of the complete layout of the amplifier.

network and compensation that take up the majority of the layout space. Therefore, the stray capacitances on the signal path are minimal.

IV. DC Analysis

To measure the DC properties of the amplifier, we used the setup shown in Figure 5.

We first set the common mode voltage V_{cm} to $0.5\,\mathrm{V}$ and

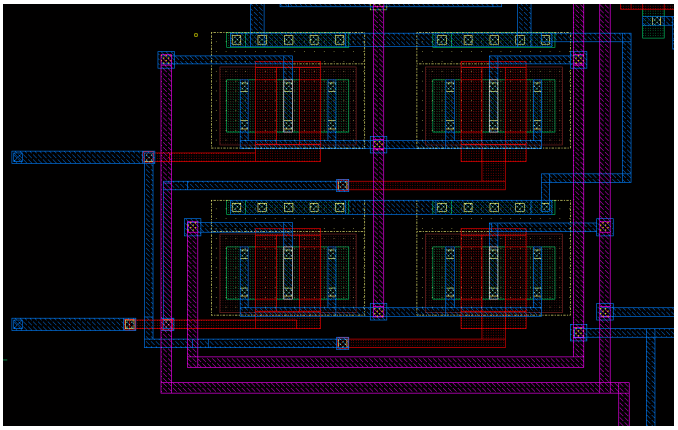

Fig. 3. A screen capture of the input differential pair layout of the amplifier.

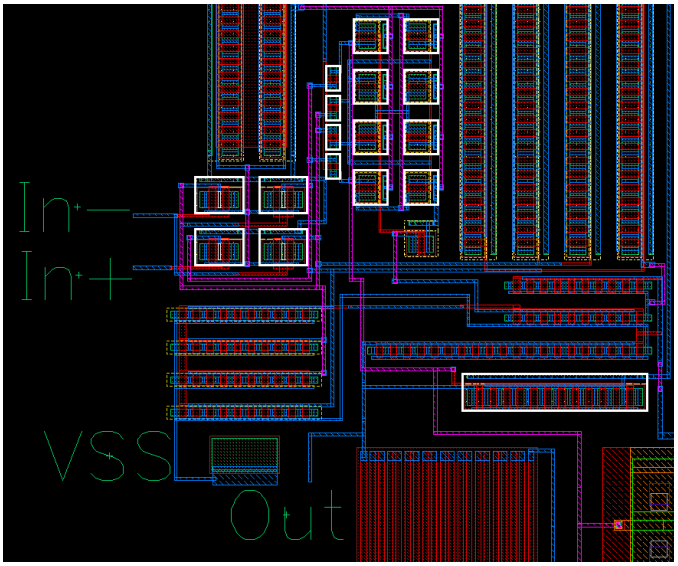

Fig. 4. A screen capture of the signal path layout of the amplifier. The signal transistors are highlighted.

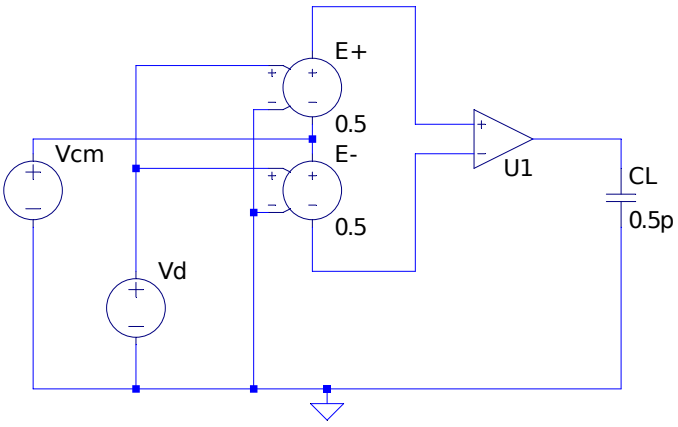

Fig. 5. A schematic of the setup used for taking open loop measurements of the amplifier.

swept the differential mode voltage V_d from $-1\,\mathrm{mV}$ to $1\,\mathrm{mV}$. The results are shown in Figures 6 and 7. From these figures, we can see that the offset voltages are $V_{os} = 64\,\mu\mathrm{V}$ for the schematic simulation and $V_{os} = 51\,\mu\mathrm{V}$ for the layout parasitics simulation. Therefore, the inclusion of the layout parasitics actually reduced our offset voltage slightly.

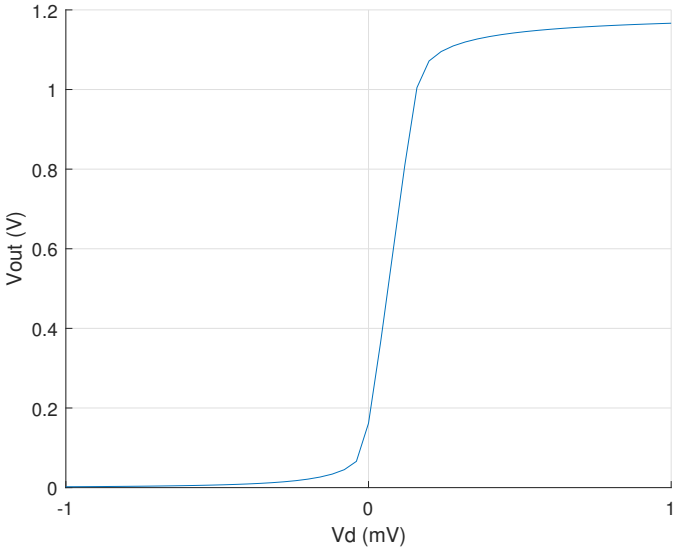

Fig. 6. DC differential mode transfer characteristic of the amplifier with schematic models only.

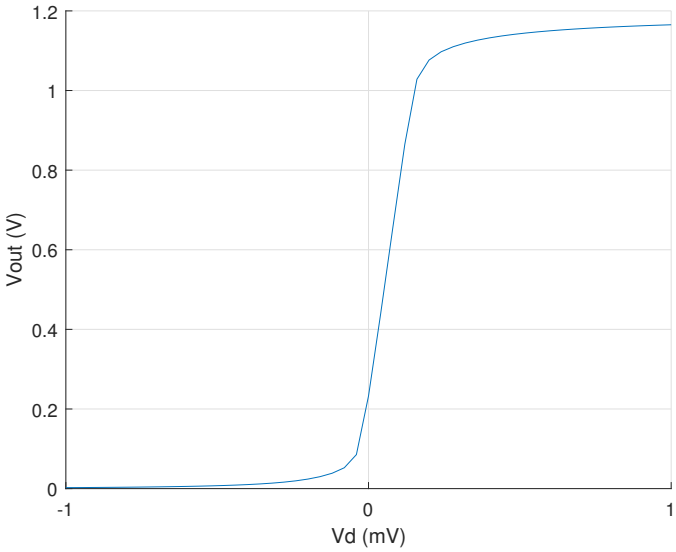

Fig. 7. DC differential mode transfer characteristic of the amplifier with layout parasitics extracted.

We next measured the common mode transfer characteristic by sweeping V_{cm} over the entire supply range with $V_d = 0\,\mathrm{V}$. We also corrected for the offset voltage by adding a source between the two input terminals with voltage V_{os}. The results are shown in Figures 8 and 9. From these figures, we can see that the layout parasitics have little effect on the common mode response.

We also analyzed the power dissipation of the amplifier. During the DC analysis, the amplifier drew a current of $85.58\,\mu\mathrm{A}$ for the schematic simulation, which corresponds to a static power dissipation of $102.7\,\mu\mathrm{W}$. In contrast, the amplifier drew a current of $85.69\,\mu\mathrm{A}$ for the layout parasitics simulation,

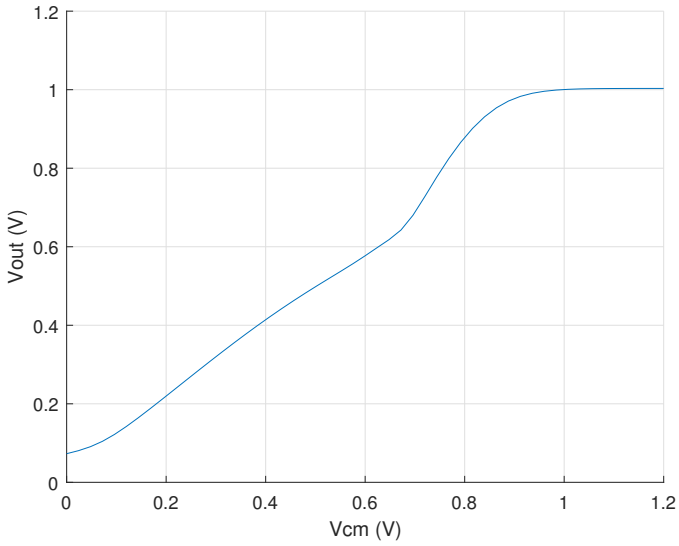

Fig. 8. DC common mode transfer characteristic of the amplifier with schematic models only.

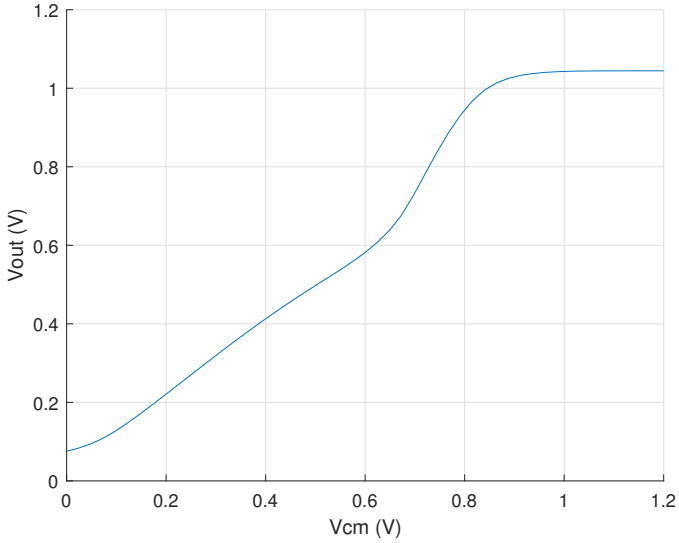

Fig. 9. DC common mode transfer characteristic of the amplifier with layout parasitics extracted.

which corresponds to a static power dissipation of $102.8\,\mu\text{W}$. Thus, we have met the power dissipation goal of $200\,\mu\text{W}$ in both cases, with the layout making no difference.

V. AC Analysis

We next measured the AC properties of the amplifier using the same setup as in Figure 5 with the offset corrected. We first measured the differential mode frequency response, and the results are shown in Figures 10 and 11. From these figures, we can see that the DC gain is $74.9\,\text{dB}$ for the schematic simulation, and $74.6\,\text{dB}$ for the layout parasitics simulation. Both of these gains meet the specification of DC gain $\geq 60\,\text{dB}$. A pole-zero analysis showed that the amplifier has its first two poles at $9.37\,\text{kHz}$ and $102\,\text{MHz}$ for the schematic simulation, and at $9.38\,\text{kHz}$ and $101\,\text{MHz}$ for the layout parasitics simulation. Both of these results are close to the targets of $10\,\text{kHz}$ and $100\,\text{MHz}$, respectively, with no significant difference between the two. In addition, the first zeros were at $115\,\text{MHz}$ for the schematic simulation and $109\,\text{MHz}$ for the layout parasitics simulation, which are both around 1.2 times their respective second pole, thus ensuring a smooth frequency response, as we will see later. We can also see that our unity-gain bandwidth is $48\,\text{MHz}$ for the schematic simulation, and $46\,\text{MHz}$ for the layout parasitics simulation. These results show that the layout parasitics reduce the AC performance of the amplifier slightly, but are not significant.

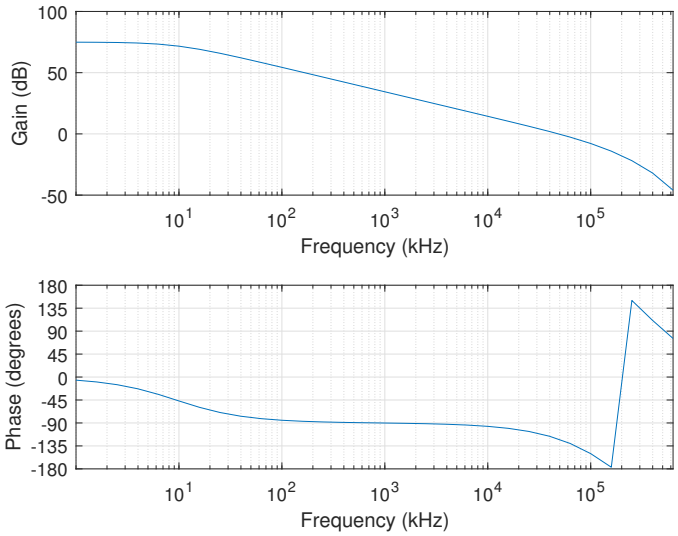

Fig. 10. AC differential mode frequency response of the amplifier with schematic models only.

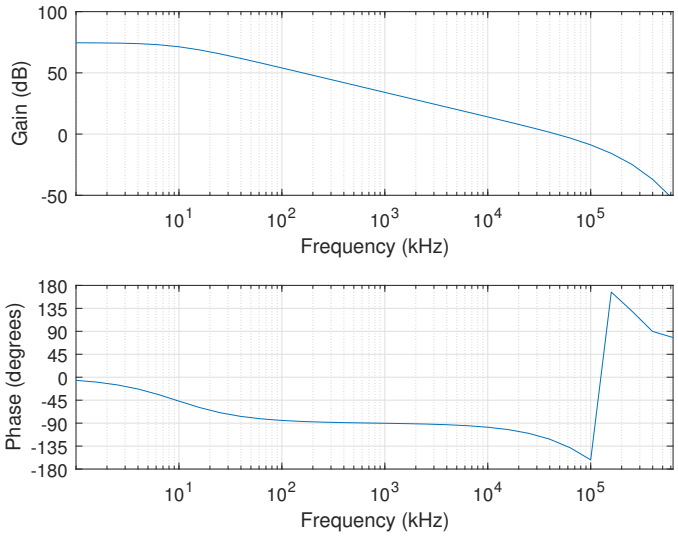

Fig. 11. AC differential mode frequency response of the amplifier with layout parasitics extracted.

Next, we measured the AC noise of the amplifier using the same setup. Using V_d as our noise source, we obtained the output-referred spectral noise density shown in Figures 12 and 13. The noise was measured from $10\,\text{Hz}$ to $1\,\text{MHz}$, with the RMS value over this bandwidth calculated to be $273\,\text{mV}$ for the schematic simulation and $263\,\text{mV}$ for the layout

parasitics simulation. This slight difference is expected since the gain and bandwidth of the laid out amplifier are slightly lower. In addition, we measured the input-referred spot noise at $1\,\mathrm{MHz}$, and found $36.9\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ for the schematic simulation and $37.0\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ for the layout parasitics simulation. Both of these satisfy the upper limit of $100\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ given in the specifications, with no significant difference between the two.

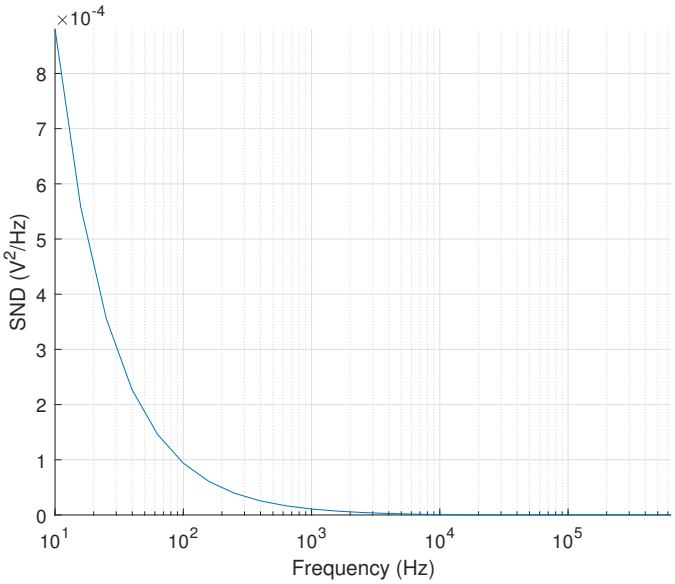

Fig. 12. Output-referred AC noise of the amplifier with schematic models only.

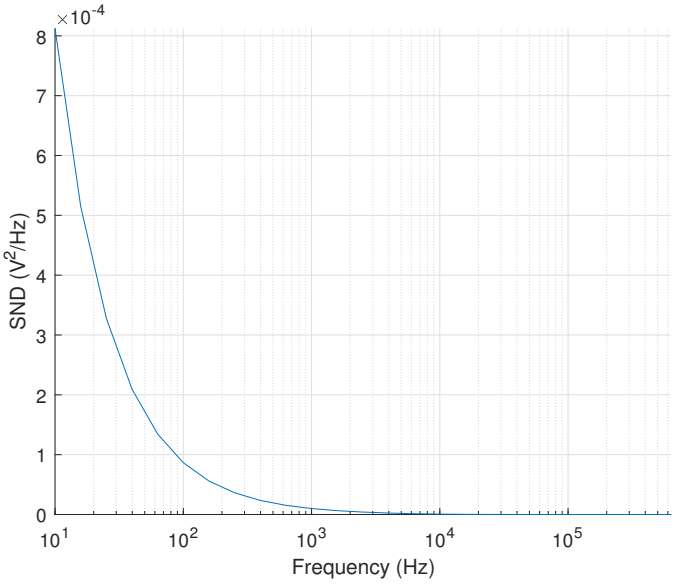

Fig. 13. Output-referred AC noise of the amplifier with layout parasitics extracted.

VI. Transient Analysis

We then measured the closed loop transient behaviour of the amplifier using the setup shown in Figure 14, where the $1.2\,\mathrm{V}$ supply has been omitted for clarity.

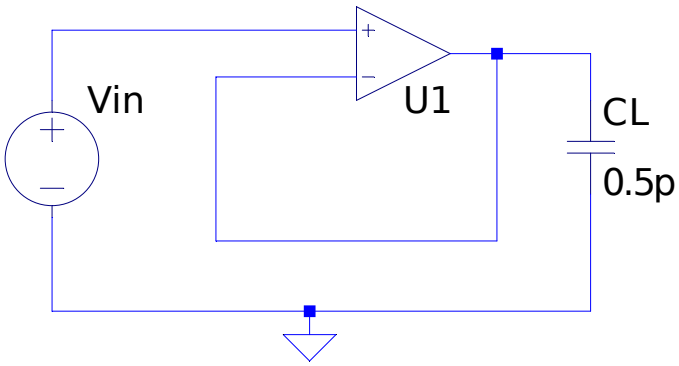

Fig. 14. A schematic of the setup used for taking closed loop measurements of the amplifier.

First, we input a fast $100\,\mathrm{mV}$ pulse to the circuit, starting at a DC bias point of $0.5\,\mathrm{V}$. The resulting output is shown in Figures 15 and 16. From these graphs, we can measure the rise time as $5.56\,\mathrm{ns}$ for the schematic simulation and $5.77\,\mathrm{ns}$ for the layout parasitics simulation. In addition, we can measure the settling time as $7.99\,\mathrm{ns}$ for the schematic simulation and $13.8\,\mathrm{ns}$ for the layout parasitics simulation. Here, we can see that the layout parasitics do have an effect on the step response of the amplifier, slightly degrading its rise and settling times.

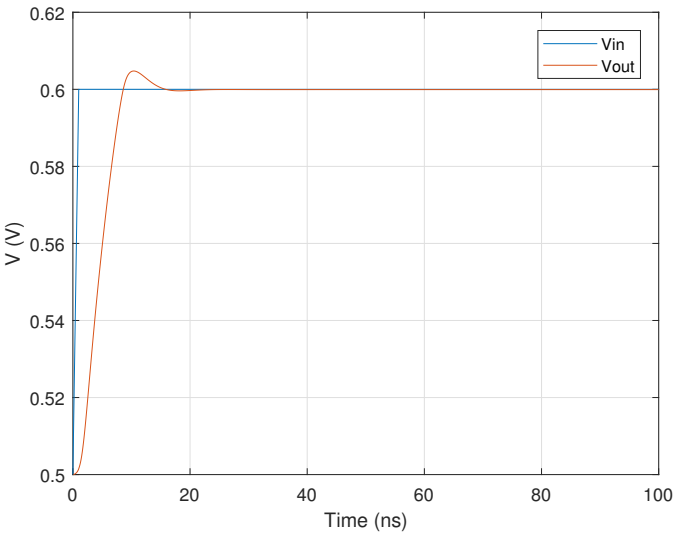

Fig. 15. Transient step response of the amplifier with schematic models only.

Next, we measured the distortion present when we input a $0.6\,\mathrm{V}$ peak-peak sine wave centered around the common mode point of $0.5\,\mathrm{V}$. This corresponds to a swing of half the supply range. The resulting output is shown in Figures 17 and 18. From these figures, we can measure the total harmonic distortion as $0.028\,\%$ for the schematic simulation and $0.053\,\%$ for the layout parasitics simulation. Thus, we have exceeded the specification of $0.2\,\%$ distortion at a swing equal to half the supply range for both cases. Therefore, the amplifier meets all the requirements, both with the schematic models only and with the layout parasitics extracted.

Finally, we measured the maximum input/output swing in the unity-gain configuration. To this end, we input a $1.6\,\mathrm{V}$

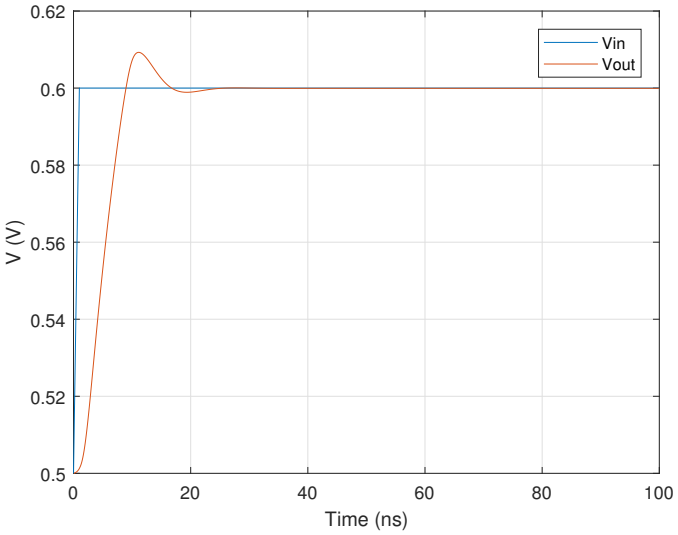

Fig. 16. Transient step response of the amplifier with layout parasitics extracted.

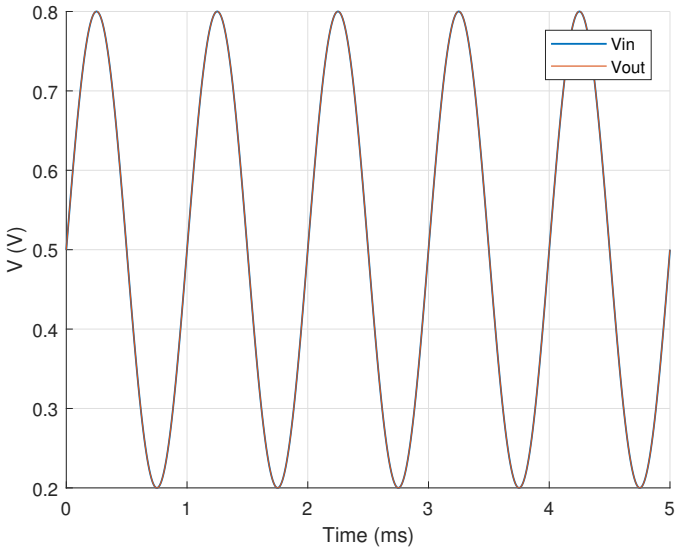

Fig. 17. Transient response of the amplifier with schematic models only to a 1 kHz, 300 mV amplitude sine wave input.

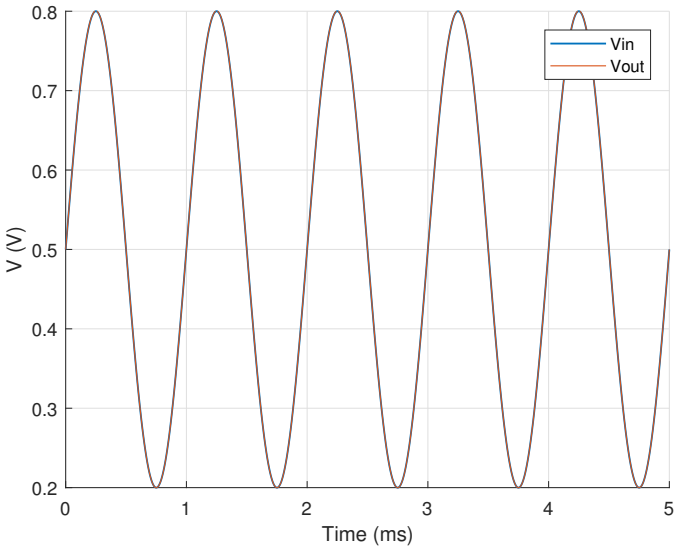

Fig. 18. Transient response of the amplifier with layout parasitics extracted to a 1 kHz, 300 mV amplitude sine wave input.

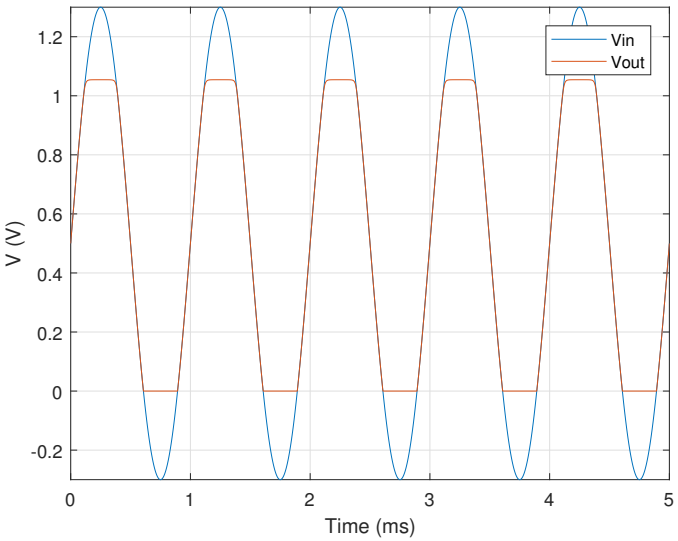

Fig. 19. Transient response of the amplifier with schematic models only to a large 1 kHz sine wave input.

peak-peak, 1 kHz sine wave centered around a DC bias point of 0.5 V and observed the output. The result is shown in Figures 19 and 20. These graphs shows a maximum input/output swing of 0.00 V to 1.00 V for the schematic simulation and 0.00 V to 1.05 V for the layout parasitics simulation. Again, we find no significant difference in the properties of the amplifier with and without layout parasitics.

VII. Conclusions

In conclusion, we performed the layout for a modified version of the amplifier we designed in Assignment #2 and compared its performance when using just the schematic models with its performance when simulating the layout parasitics. We found no significant difference, with the amplifier still meeting all of its specifications, including a DC gain greater than 60 dB, poles at approximately 10 kHz and 100 MHz, low distortion when swinging at half the supply range, low input-referred noise, and a static power dissipation of less than 200 µW.

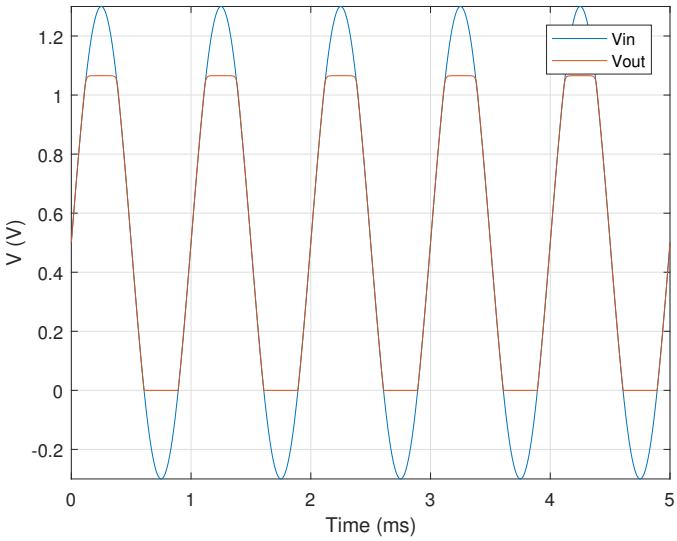

Fig. 20. Transient response of the amplifier with layout parasitics extracted to a large 1 kHz sine wave input.