ECSE-534
Analog Microelectronics
Assignment #1

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***Abstract*—A CMOS amplifier was analyzed using Cadence and its performance was characterized using DC, small signal AC, and transient analysis. The amplifier was found to meet its specifications, with unity gain stability, a DC gain of $54\,\mathrm{dB}$, and a unity gain bandwidth of $425\,\mathrm{MHz}$. In addition, the amplifier was found to have a weak phase margin of 0.8°, suggesting an area of possible improvement.**

I. Introduction

THIS report follows the analysis of a CMOS amplifier that has been designed for unity gain stability in a 0.13 micron process from IBM. The amplifier in question is shown in Figure 15. Note that all NFET transistors have their body connected to V_{SS} and all PFET transistors have their body connected to V_{DD}.

II. Bias Resistance

Before the analysis, we must first set the bias resistance R_{bias} such that the drain current in M_5 is between $100\,\mu\mathrm{A}$ and $150\,\mu\mathrm{A}$. To this end, we sweep the resistance value and simulate the drain current in M_5. The results are shown in Figure 1. Using this graph, we choose a bias resistance $R_{bias} = 100\,\mathrm{k}\Omega$.

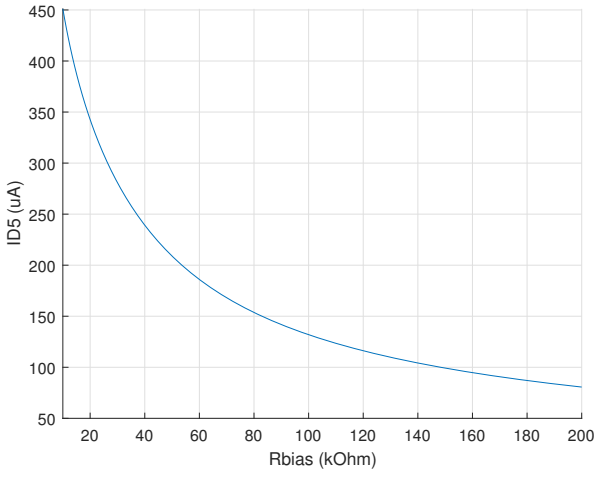

Fig. 1. Drain current in transistor M_5 as a function of R_{bias}.

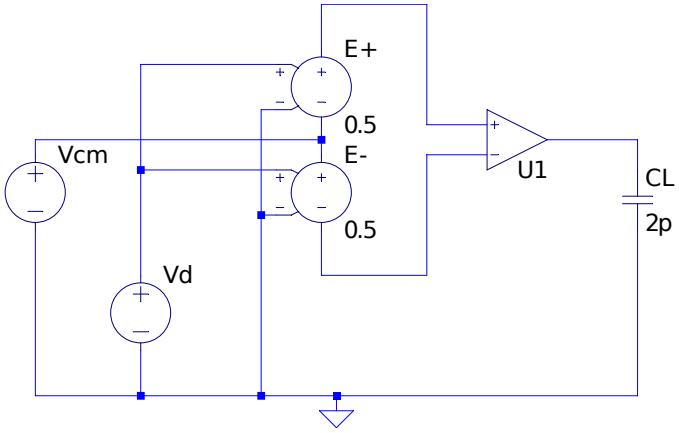

Fig. 2. A schematic of the setup used for measuring the DC and common mode properties of the amplifier.

III. DC Analysis

Next, we measure the DC properties of the amplifier using the setup shown in Figure 2, where the $1.2\,\mathrm{V}$ power supply has been omitted for clarity.

We first sweep the common mode voltage V_{cm} over the entire supply range and measure the output voltage, with $V_d = 0\,\mathrm{V}$. The results are shown in Figure 3. We see that the built-in voltage offset causes saturation regardless of common mode voltage.

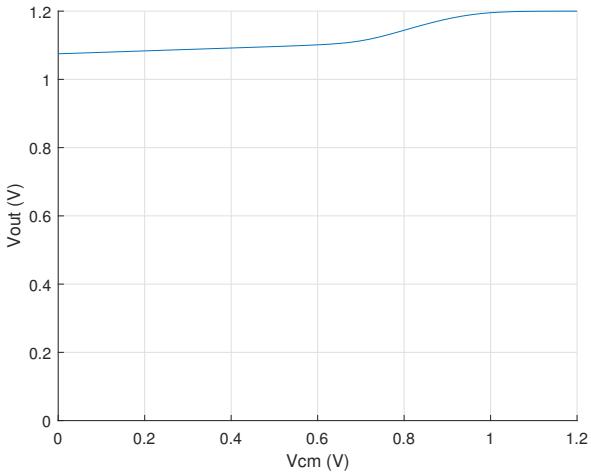

Fig. 3. DC common mode transfer characteristic of the operational amplifier.

Then, we sweep the differential voltage V_d from $-10\,\mathrm{mV}$ to $10\,\mathrm{mV}$, with $V_{cm} = 0.6\,\mathrm{V}$ for proper biasing. The results are shown in Figure 4. From this figure, we find that $V_{os} = -1.4\,\mathrm{mV}$.

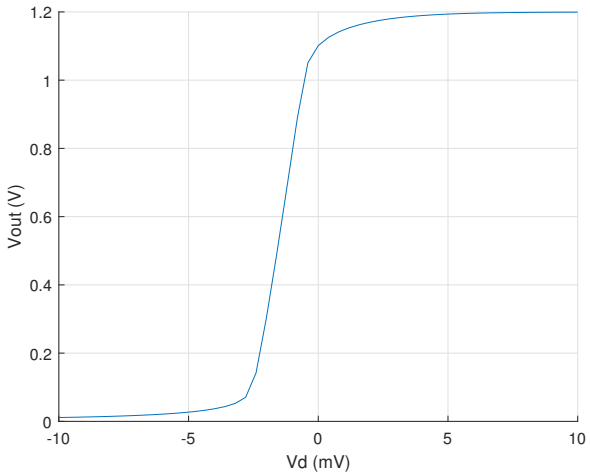

Fig. 4. DC differential transfer characteristic of the operational amplifier.

To find the input and output voltage ranges, we plot the incremental voltage gain in Figure 5. We then choose the voltage range as being the range in which the incremental gain is at most $3\,\mathrm{dB}$ down from the peak value. Thus, we get an input voltage range of $-2.3\,\mathrm{mV}$ to $-0.5\,\mathrm{mV}$ and an output voltage range of $0.18\,\mathrm{V}$ to $1.0\,\mathrm{V}$.

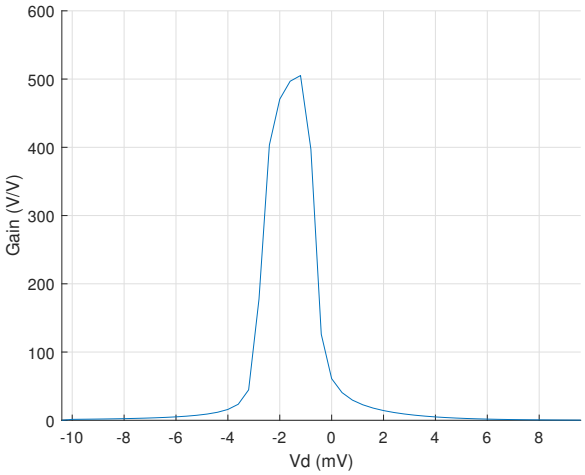

Fig. 5. DC incremental differential gain of the operational amplifier.

IV. AC Analysis

Next, we measure the AC properties of the amplifier. First, we measure the common mode frequency response using the setup in Figure 2, keeping the DC component of $V_{cm} = 0.6\,\mathrm{V}$ and setting $V_d = 0\,\mathrm{V}$. The results are shown in Figure 6. From this figure, we can see that the gain at low frequencies is $-24\,\mathrm{dB}$.

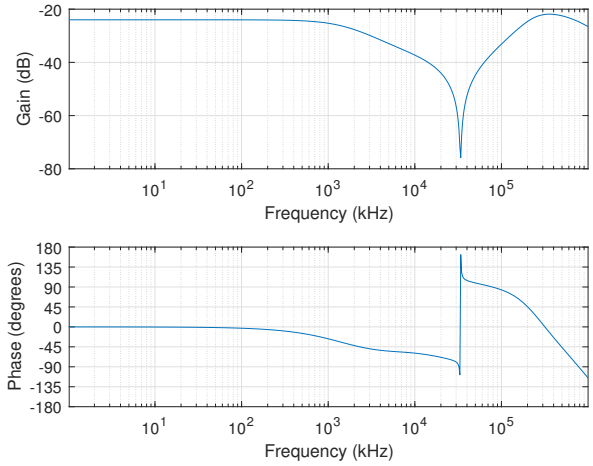

Fig. 6. AC common mode frequency response of the operational amplifier.

Then, we measure the differential mode frequency response using the setup in Figure 7, where the $1.2\,\mathrm{V}$ power supply has been omitted for clarity. In this setup, we have connected the output to the negative input at DC with a large inductor, ensuring bias stability. We then inject the signal through a large capacitor. These components are chosen so large that they do not affect the results of the AC analysis. V_{bias} is set to $0.6\,\mathrm{V}$ for proper biasing.

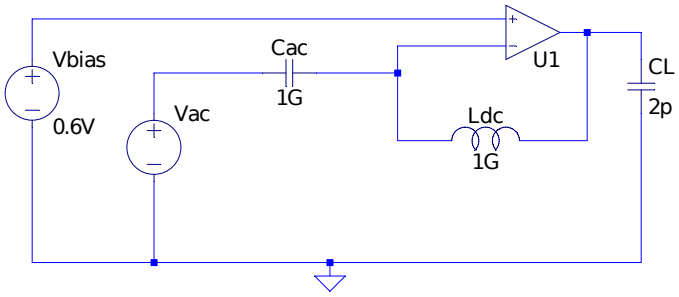

Fig. 7. A schematic of the setup used for measuring the AC properties of the amplifier.

The results of this analysis are shown in Figure 8. From this graph, we can see that the low frequency gain is $54\,\mathrm{dB}$, the unity gain bandwidth is $425\,\mathrm{MHz}$, and the phase margin is $0.8°$. We can also see that the amplifier has a pole at $320\,\mathrm{kHz}$, a zero at around $100\,\mathrm{MHz}$, and two poles around $425\,\mathrm{MHz}$.

Next, we measure the AC noise of the amplifier using the same setup. Using V_{ac} as our noise source, we get the output referred spectral noise density shown in Figure 9. The noise was measured from $100\,\mathrm{Hz}$ to $10\,\mathrm{MHz}$, with the RMS value calculated to be $6.3\,\mathrm{mV}$ over this bandwidth. We note that the noise is dominated by flicker noise.

V. Transient Analysis

Finally, we measure the closed loop transient behaviour of the amplifier using the setup shown in Figure 10, where the $1.2\,\mathrm{V}$ power supply has been omitted for clarity.

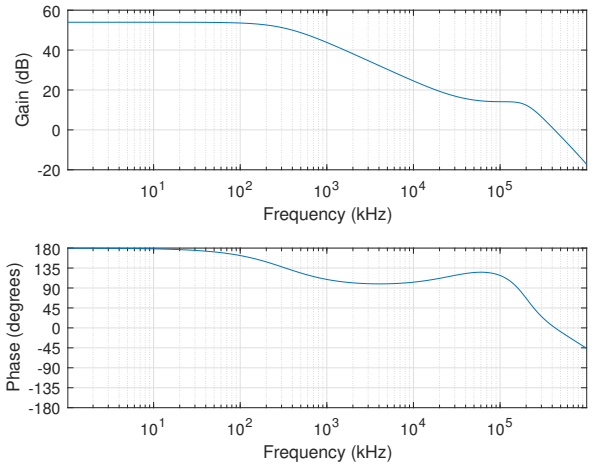

Fig. 8. AC differential frequency response of the operational amplifier.

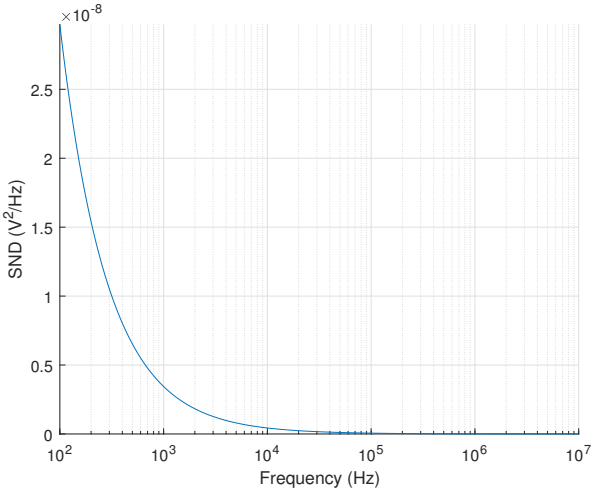

Fig. 9. Output referred AC noise of the operational amplifier.

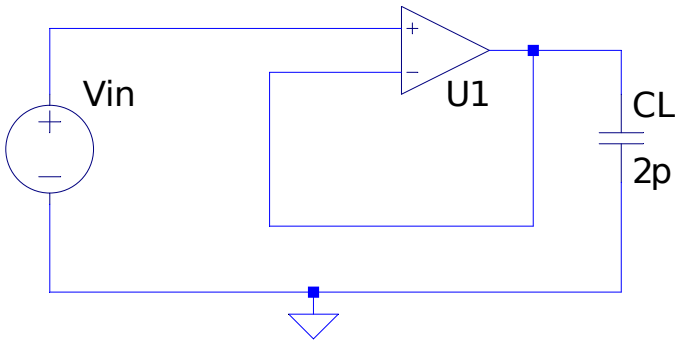

Fig. 10. A schematic of the setup used for measuring the closed loop transient properties of the amplifier.

First, we input a fast $100\,\mathrm{mV}$ pulse to the circuit, centered around a DC bias point of $0.6\,\mathrm{V}$. The resulting output is shown in Figure 11. From this graph, we can measure the slew rate as $64\,\mathrm{V/\mu s}$, the $10\,\%$ to $90\,\%$ rise time as $1.25\,\mathrm{ns}$, and the $5\,\%$ settling time as $26\,\mathrm{ns}$.

Next, we measure clipping by using a large $1\,\mathrm{kHz}$ sine

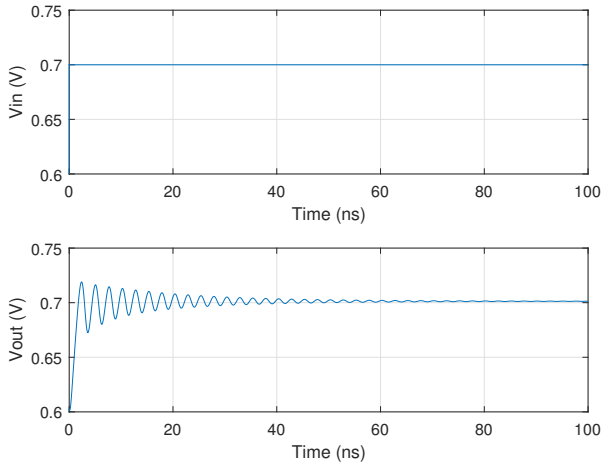

Fig. 11. Transient step response of the operational amplifier.

wave as input to the circuit. The resulting output is shown in Figure 12. From this, we find that the maximum input and output voltage ranges are both $0\,\mathrm{V}$ to $1.19\,\mathrm{V}$.

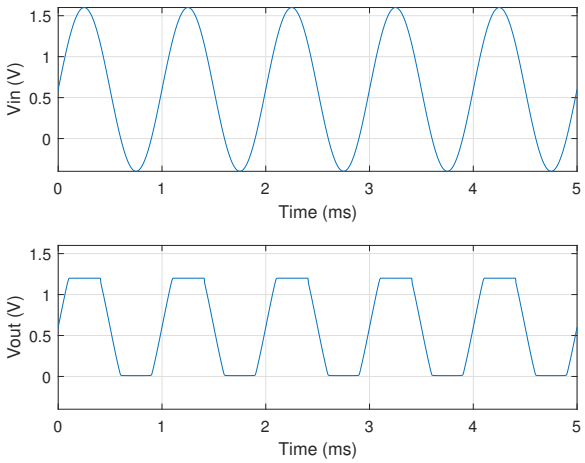

Fig. 12. Transient response of the operational amplifier to a large $1\,\mathrm{kHz}$ sine wave input.

Finally, we measure both common mode and differential mode distortion using the setup in Figure 2. For this purpose, we add a DC offset equal to V_{os} in series with E_+ to ensure adequate biasing. We first set the differential mode voltage $V_d = 0\,\mathrm{V}$, and inject a common mode, $1\,\mathrm{kHz}$, $100\,\mathrm{mV}$ amplitude sine wave on top of a $0.6\,\mathrm{V}$ DC offset. The resulting output is shown in Figure 13, and the total harmonic distortion was calculated to be $39.58\,\%$.

Then, we fix the common mode voltage V_{cm} at $0.6\,\mathrm{V}$, and set the differential voltage to a $1\,\mathrm{kHz}$, $1.2\,\mathrm{mV}$ amplitude sine wave, which was chosen to get an output swing close to the limit. The resulting output is shown in Figure 14, and the total harmonic distortion was calculated to be $6.04\,\%$.

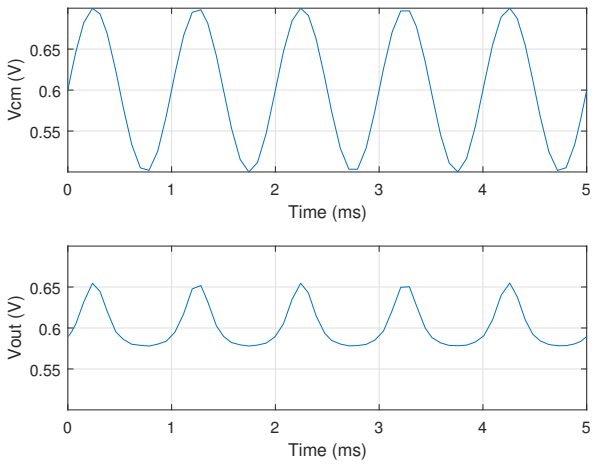

Fig. 13. Transient response of the operational amplifier to a $1\,\mathrm{kHz}$, $100\,\mathrm{mV}$ amplitude common mode sine wave.

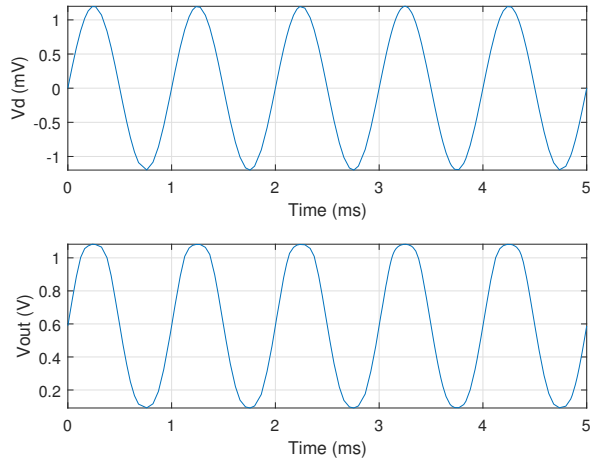

Fig. 14. Transient response of the operational amplifier to a $1\,\mathrm{kHz}$, $1.2\,\mathrm{mV}$ amplitude differential sine wave.

VI. Conclusions

In conclusion, the operational amplifier shown in Figure 15 was analyzed and its performance characterized using DC, small signal AC, and transient analysis. The amplifier performs its tasks adequately, with its main flaws being a low phase margin of $0.8°$, and a relatively low gain of $54\,\mathrm{dB}$. However, it compensates for this with a high unity gain bandwidth of $425\,\mathrm{MHz}$.

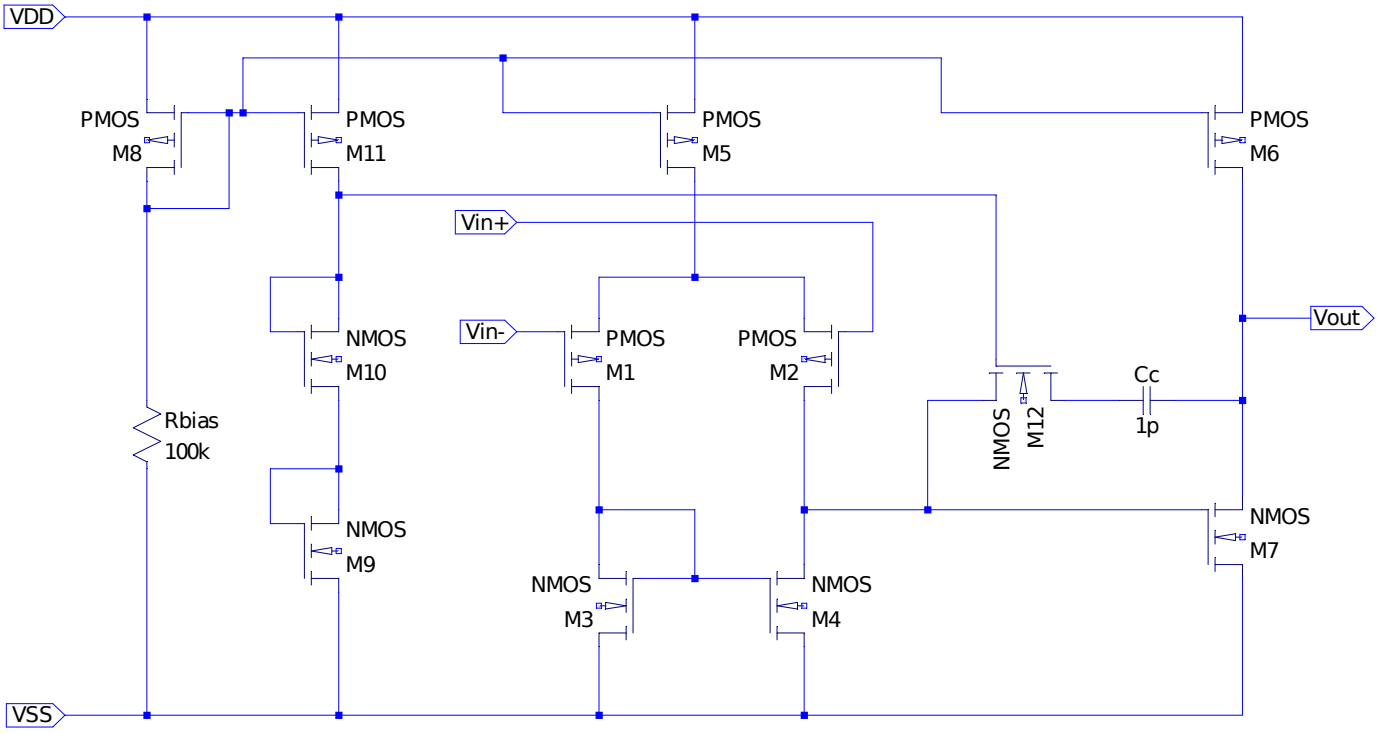

Fig. 15. Schematic of the operational amplifier.