ECSE-487
COMPUTER ARCHITECTURE LABORATORY
Assignment #2

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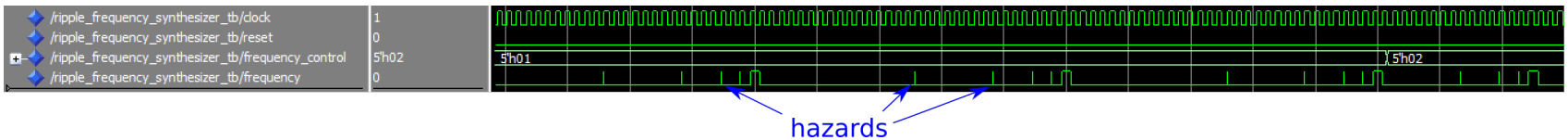
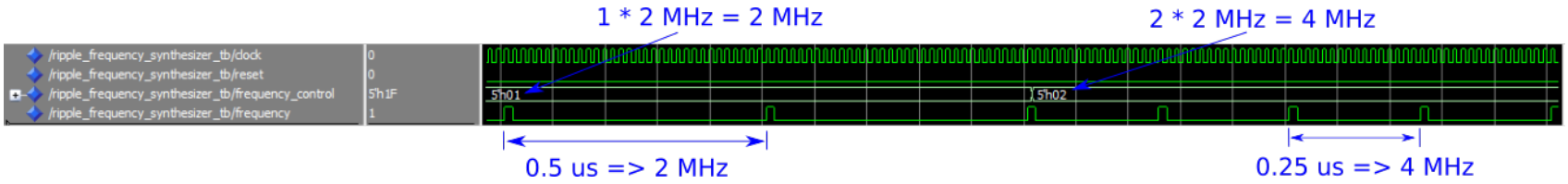
Ripple-carry Frequency Synthesizer

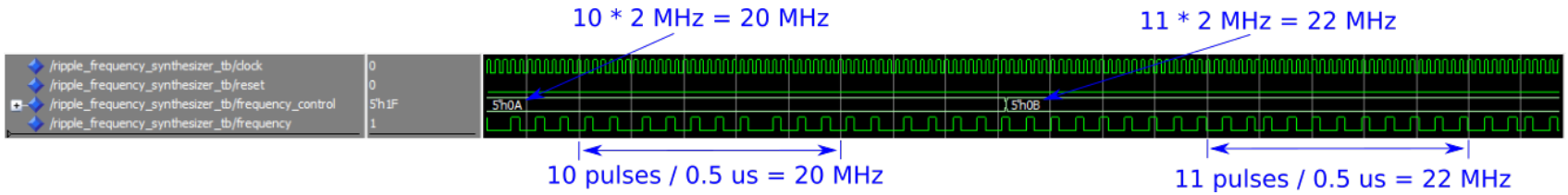
- Data hazards on Cout
- Add a register to eliminate hazards at output

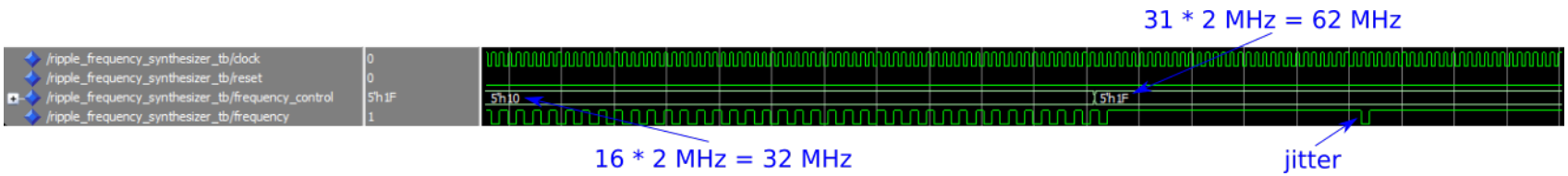


Ripple-carry Frequency Synthesizer

- Results





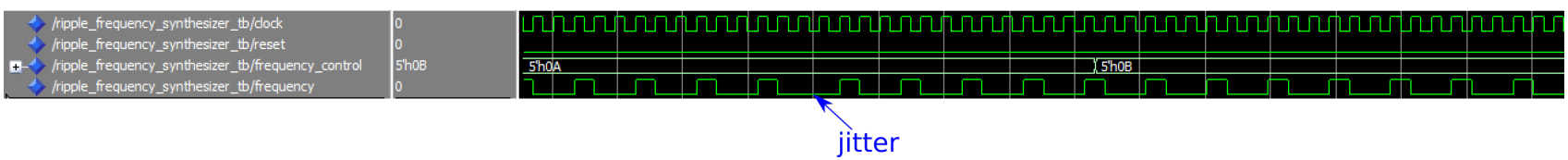


Ripple-carry Frequency Synthesizer

- Only divisors of clock rate can be generated exactly
- Other frequencies experience jitter

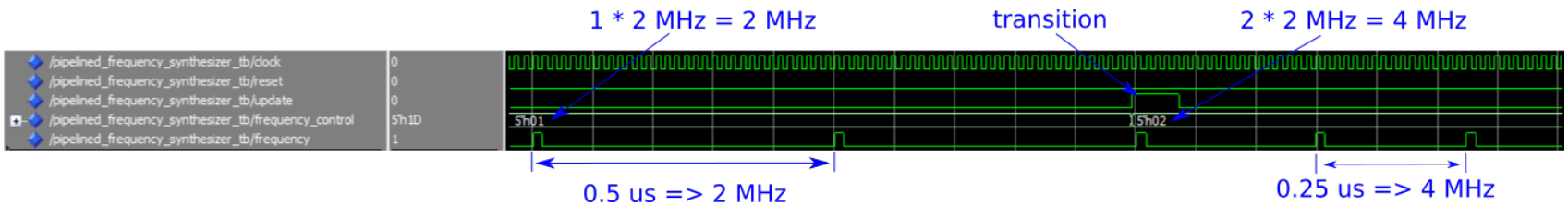
Table: Input of 0x0A

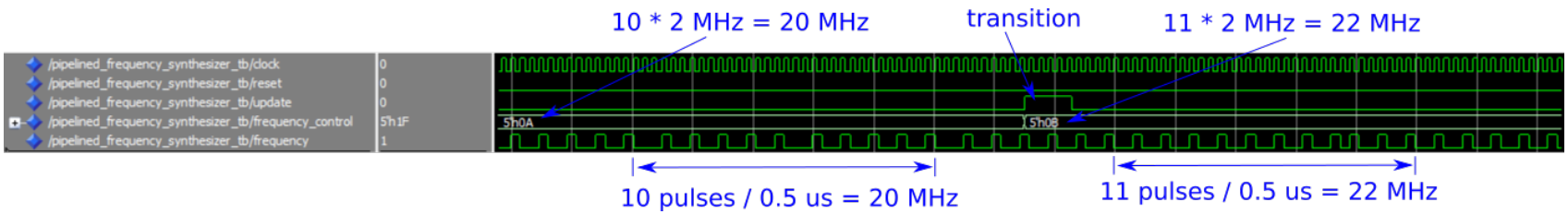
0	8	6	4	2	0
10	18	16	14	12	10
20	28	26	24	22	20
30	38	36	34	32	30
40					40

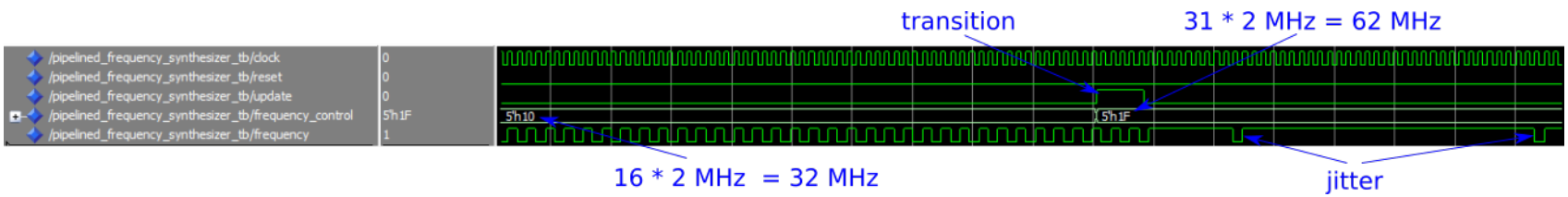


Pipelined Frequency Synthesizer

- Results







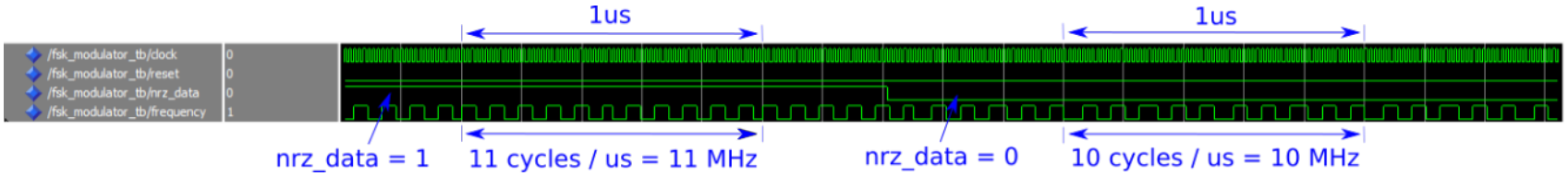
Pipelined Frequency Synthesizer

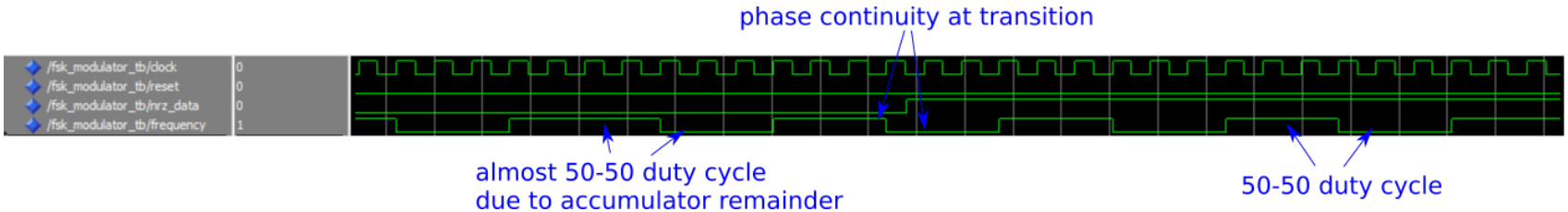
- Synthesis results
- Pipelining has more impact with higher N

	N = 5	**N = 32**
ripple-carry	142.71 MHz	112.23 MHz
pipelined	149.37 MHz	144.01 MHz

FSK Modulator

- Results





Analog Waveform Generator

- Sine wave shifted to [0, 256)
- Results

$$128(1 + sin(\frac{2\pi}{10}t)), t = 0, 1, \ldots 9$$