

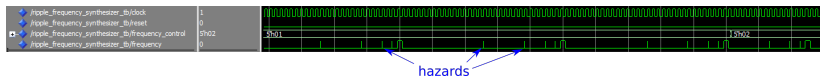
ECSE-487
COMPUTER ARCHITECTURE
LABORATORY
Assignment #2

Andrei Purcarus Craciun
260631911

February 13, 2017

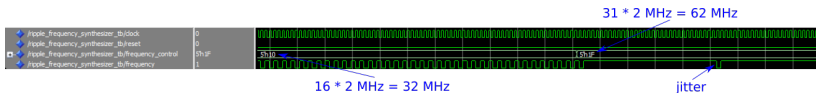
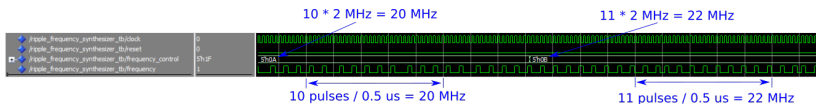
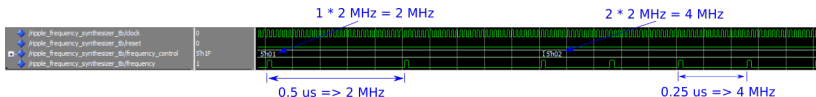
Ripple-carry Frequency Synthesizer

- ▶ Data hazards on Cout
- ▶ Add a register to eliminate hazards at output



Ripple-carry Frequency Synthesizer

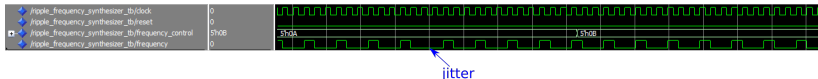
► Results



Ripple-carry Frequency Synthesizer

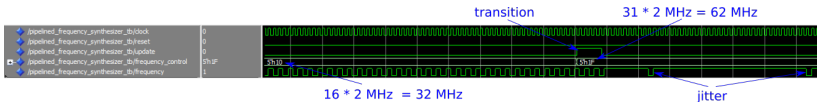
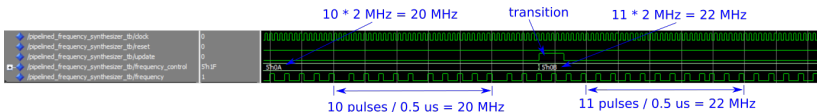
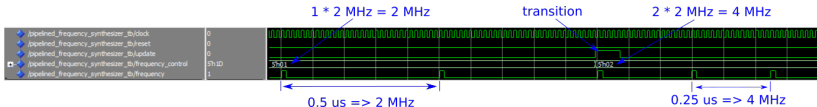
- ▶ Only divisors of clock rate can be generated exactly
- ▶ Other frequencies experience jitter

$$f_{out} = frequency_control * \frac{f_{clk}}{N}$$



Pipelined Frequency Synthesizer

► Results



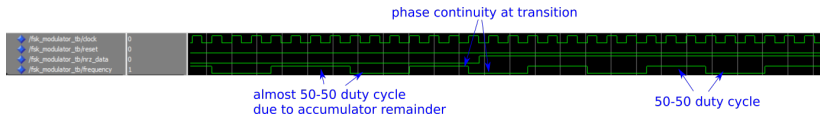
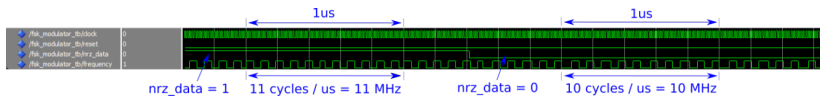
Pipelined Frequency Synthesizer

- ▶ Synthesis results
- ▶ Pipelining has more impact with higher N

	N = 5	N = 32
ripple-carry	142.71 MHz	112.23 MHz
pipelined	149.37 MHz	144.01 MHz

FSK Modulator

► Results



Analog Waveform Generator

- ▶ Sine wave shifted to $[0, 256)$
- ▶ Results

$$128(1 + \sin(\frac{2\pi}{10}t)), t = 0, 1, \dots, 9$$

