Audio Amplifier

Electronic-Workshop II

Varun Shastry (2023112005), Vedant Pahariya (2023112012)
Table 6

January 20, 2025

Contents

1 Introduction

This is Project 1, for the first half of the course Electronics Workshop-II, in the Spring 2025 Semester. The project is to design an audio amplifier, with an appreciable gain and load power, to drive a speaker. Our project aims to design and construct an audio amplifier meeting specific operational and performance criteria. The amplifier's primary purpose is to process weak audio signals, amplify them effectively, and deliver a quality output without significant distortion. It includes four critical stages: a pre-amplifier for initial signal enhancement, a gain stage for boosting the signal to the desired amplitude, a band-pass filter to ensure signal integrity, and a power amplifier to drive the speaker load efficiently.

We have adopted a design approach tailored to drive a 10 Ω speaker load with approximately 0.8 W of power, considering the constraints of the supply voltage rails. The design ensures minimal Total Harmonic Distortion (THD), preserving the fidelity of the output signal to closely match the original input audio. Our simulations provide a voltage gain ranging from approximately 400 to 430, depending on the input voltage, which varies between 20 mVpp and 10 mVpp, respectively. The design approach has been developed through extensive iterations and overcoming numerous setbacks. Various topologies were implemented and tested, ultimately leading to a configuration that, in our opinion, delivers the best performance.

Our implementation comprises four stages, each serving a specific purpose in achieving the desired audio amplification. These stages are discussed in detail in the subsequent sections. Briefly, the **Preamp** stage is responsible for picking up small voice signals from the microphone, this stage filters noise to an acceptable level while providing initial amplification to align the signal with the load-line. A common-emitter differential amplifier is utilized here for its high input and output impedance and effective noise performance.The **Gain** stage further amplifies the signal voltage. By employing a common-emitter amplifier, it ensures adequate voltage amplification while maintaining stability and linearity.

The **Filter** stage to enhance signal fidelity, eliminating low and high-frequency noise, allowing only frequencies within the audible range (20 Hz to 20 kHz) to pass through. An active band-pass filter has been incorporated to meet this requirement. The **Power Amplifier** stage is the final stage, and boosts the signal's power to drive the speaker effectively. A Class AB power amplifier is employed, chosen for its superior efficiency, minimal distortion, and linear response compared to other configurations like Class A or Class B amplifiers. This carefully designed configuration ensures optimal performance, preserving audio quality and achieving a smooth, distortion-free output signal.

It is important to note that the values selected for the components in the circuit design during simulation may not align exactly with those required for actual hardware implementation. Variations can arise due to practical factors such as component tolerances, temperature effects, and real-world non-idealities, which may necessitate adjustments to achieve the desired performance in the physical circuit.

2 Preamp Stage

i Why the preamp stage?

Audio signals from sources like microphones are typically very small, ranging from 10 mV to 20 mVpp in our case. If this tiny signal were sent directly to the gain stage, noise would become a significant issue. All electronic circuits generate some inherent noise, such as faint static hum, and when the signal is this small, the noise can rival the signal itself. This results in a poor Signal-to-Noise Ratio (SNR), making the signal less audible. As the name suggest, preamp is "Pre-Amplifier", therefore, the preamp's goal is to amplify the signal to line-level, the standard strength for audio equipment connections, before any additional amplification. Without this step, amplifying the signal later would also amplify the noise, rendering the output nearly unusable.

ii Circuit preamp specifications

The preamp is designed within the constraints of $\pm$ 5V supply rails and utilizes a differential amplifier topology with bipolar junction transistors (BJTs). This topology was chosen for its high input impedance (partly why this is also used in op-amps), which minimizes current draw from low-power sources like microphones, and its low output impedance, enabling it to drive the next stage effectively. Differential amplifiers also excel at suppressing noise due to their high Common Mode Rejection Ratio (CMRR) and provide low distortion and linear amplification, which are critical for audio applications.

We employ a **Dual Input Unbalanced Output amplifier** in replacement of the more straightforward Single Input Unbalanced Output design. While the latter is less complex and adequate for basic amplification, our choice is driven by the need for higher Common Mode Rejection Ratio (CMRR, which we shall look at in the following sections) and lower THD. The dual-input design more effectively eliminates common-mode noise, making it better suited for our objectives.

A critical aspect of this approach is the impedance matching of the two transistors in the differential amplifier. Proper matching ensures that the amplifier accurately amplifies the difference between the input signals while rejecting common-mode noise or signals shared by both inputs. Mismatched components can introduce unwanted offsets, degrade the CMRR, and ultimately impair the signal quality, which is why careful attention to matching is essential in this design.

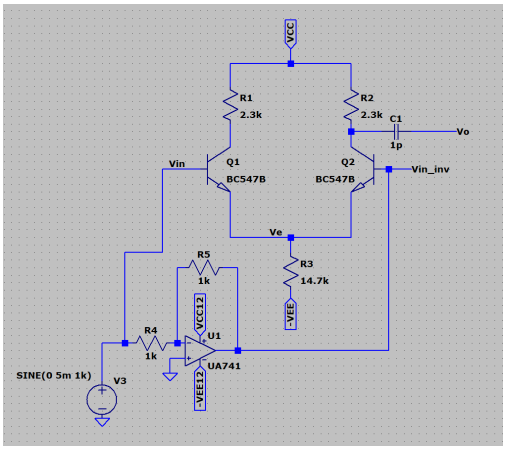

Figure 2.1: Preamp Circuit

iii Assumptions

Some assumptions are considered in design, that $I_C = I_E$, which means $\alpha = 1$ for the BJTs, and that the BJTs are matched, so the topology is symmetrical, implying either output is equivalent to consider as the final output of the circuit. Early effect is not considered, so we would expect lesser gain and other parameters in simulations than theory. Also, for using this circuit in differential mode (for amplification) the input differential needs to be lesser than half the thermal voltage, which is 25.9mV at room temperature. This is to ensure that the **output is proportional to the input differential of the circuit**. Since our input ranges from 10mVpp to 20mVpp, the input differential (note that the second input is an anti-phase version of the original input, i.e., shifted by 180°) ranges from 20mVpp to 40mVpp, and thus our circuit would amplify/behave closer to the theoretical model for smaller inputs.

Ideally, we place a current source with high impedance, at the tail of the transistors, but in real scenarios we consider the resistance because the performance of the circuit depends on the output resistance of the tail current source.

iv Theory

Figure 2.1 above shows the Preamp circuit designed by us. It is called a dual input because, of the fact that the inputs are provided to the bases of both BJTs, and the output is taken at any one end, due to which it is called an unbalanced diff amp. An input is called a **common-mode signal** if it is provided to both the bases, which we typically expect to be noise, since it will affect both inputs equally. Ideally, the common-mode gain is zero, since the input differential is zero, but we see that due to some mismatches, and non-ideal behavior the common-mode gain is finite.

To understand this circuit, we can exploit the symmetry of the circuit and split it into two half circuits, as shown below:

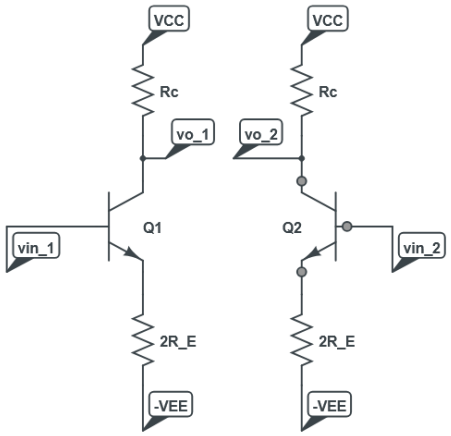

Figure 2.2: Simplified Model of the Circuit

For a common mode input, $vi_1 = vi_2 = v_{icm}$ (say). Now because the transistors are assumed to match, $i_{C_1} = i_{C_2} = \frac{I}{2}$ (say). In an ideal scenario, we would see the gain is 0, but if not, the common-mode gain is similar to the scenario of the common-emitter amplifier (since we are considering a single input), where the gain is given as the ratio of the collector resistor to the emitter resistor.

Thus,

$$\boxed{A_{cm} = \frac{v_o}{v_{icm}} = \frac{R_c}{2R_e}}$$

And as mentioned above, we would get a more ideal behavior with a higher value of R_e, which we have chosen to be $14.7k\Omega$ to keep a collector current of about $150\mu A$, for matching the theoretical gain discussed below.

Before looking at the small signal differential gain, it is important to know the DC transfer characteristic for the case of a large differential input (i.e., $|v_{i_1} - v_{i_2}| > V_T/2$)

$$i_{c_1} = I_s e^{V_{BE_1}/V_T} = I_s e^{(v_{b_1} - v_{e_1})/V_T}$$
$$i_{c_2} = I_s e^{V_{BE_2}/V_T} = I_s e^{(v_{b_2} - v_{e_2})/V_T}$$

Therefore, the ratio,

$$\frac{i_{c_1}}{i_{c_2}} = e^{v_{id}/V_T}$$

Therefore, the normalized currents,

$$\frac{i_{c_1}}{i_{c_1} + i_{c_2}} = \frac{1}{1 + e^{-v_{id}/V_T}}$$

$$\frac{i_{c_2}}{i_{c_1} + i_{c_2}} = \frac{1}{1 + e^{v_{id}/V_T}}$$

Let's coin these terms v_{id}/V_T and $\frac{i_{c_1}}{i_{c_1}+i_{c_2}}$ as normalized input voltage, and normalized current respectively. The diagram of the latter with the former is given below.

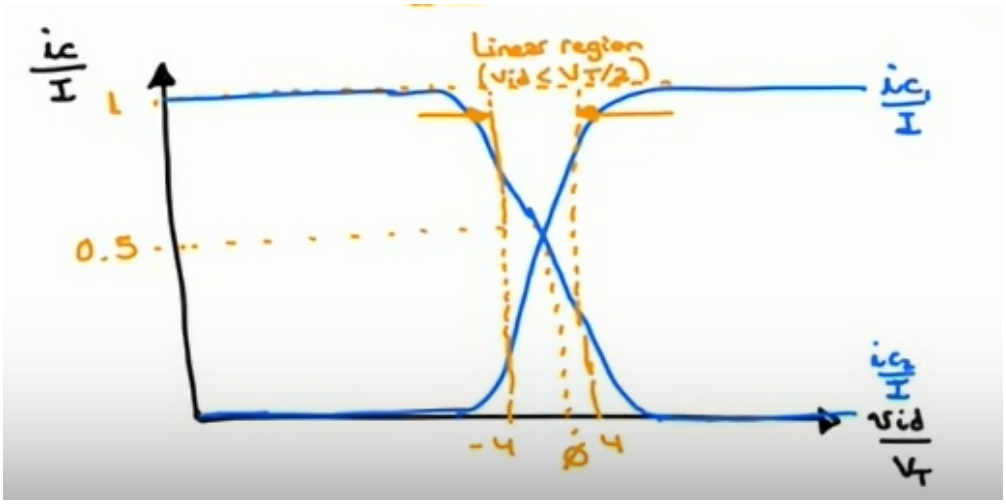

Figure 2.3: Normalized Current vs Normalized Voltage

From this figure, we can see that since the output is proportional to the normalized current, the linear amplification is obtained in a very small range of differential input, which is where the $V_T/2$ value comes about! The differential gain in this region is given by the slope in this linear region!

Now most importantly, we discuss the most important region of operation, the case where the input differential is small ($|v_{id}| < V_T/2$), and produces linear amplification. For the derivation of differential gain, let's consider $v_{i_1} = \frac{v_{id}}{2}$, $v_{i_2} = -\frac{v_{id}}{2}$, so the total current with the small-signal incremental current is given by:

$$i_{c_1} = \frac{I}{2} + \frac{g_m v_{id}}{2} i_{c_2} = \frac{I}{2} - \frac{g_m v_{id}}{2}$$

Thus we get,

$$v_{c_1} = V_{CC} - \left(\frac{I}{2}R_C + g_m \frac{v_{id}}{2} R_C\right)$$

$$v_{c_2} = V_{CC} - \left(\frac{I}{2}R_C - g_m \frac{v_{id}}{2} R_C\right)$$

With the case of an unbalanced output,

$$A_d = \frac{v_o}{v_{id}} = \frac{v_{c_2}}{v_{id}} = \frac{g_m v_{id} R_C}{2 v_{id}}$$

Therefore,

$$\boxed{A_d = \frac{1}{2} g_m R_C}$$

With the formulae for the differential gain and common mode gain now in hand, we can calculate the common-mode rejection ratio (CMRR), which on an absolute scale is defined as the ratio of the differential mode gain to the common-mode gain. Thus,

$$\text{CMRR} = \frac{A_d}{A_{cm}} = \frac{\frac{1}{2} g_m R_C}{\frac{R_C}{2R_E}}$$

Thus,

$$\boxed{\text{CMRR}_{abs} = g_m R_E}$$

On a decibel scale, CMRR = 20log $\left(\frac{A_d}{A_{cm}}\right)$

This supports the above-mentioned theory that the topology behaves like it's ideal model when R_E is higher, since ideally we expect CMRR to be infinite. But at the time of designing, it is important to understand that a high value of R_E will also lead to reduction in the collector current of the BJTs (evident by applying KVL in the loop from one of the bases of the BJTs to the negative supply rail).

The input/output impedance can be defined based on the mode of operation, i.e., common mode/ differential mode. We are typically more interested in the differential mode because that is the mode of operation we operate the diff. amp in! The calculation can be done by applying KVL in the test input loop, in the small signal model, the differential **input impedance** $R_{in} = \frac{2\beta}{g_m}$, which is indeed a high impedance. Whereas, the **differential output impedance** $R_{out} = R_C$, or $R_C||r_o$ where r_o is the resistance considering the Early Effect in BJTs.

As mentioned above, all these derivations rely heavily on the fact that the circuit is **perfectly matched**. Else, since diff. amps are DC-coupled amplifiers, they can suffer from mismatches, which can translate into DC offsets, similar to what we see in op-amps. This can affect the circuit performance. The mismatches could be due to mismatches in R_C, I_s of the BJTs etc. We can also have another topology with emitter degeneration, which increases the region of linearity (due to the introduction of a negative feedback) in Figure 2.3 above, but with the trade-off of reduced gain and CMRR! Anyway, our implementation does not include any emitter degeneration.

v Simulations

With all the theory now at our tips, we can proceed onto the simulations of this circuit topology. All the simulations are run on LTSpice, with an inverting op-amp configuration used to create the anti-phase input [$Z_1 = Z_2$ gives a gain $(-Z_2/Z_1)$ of -1].

The values we have chosen for the circuit elements are as follows: $R_C = 2.3k\Omega$, Transistor model (NPN) BC547B, $R_E = 14.7k\Omega$, $V_{CC}/V_{EE} = +/-5V$. Note that since the differential input is twice the input on one base, $\frac{g_m R_c}{2} = \frac{v_o}{2v_{in}}$

In DC conditions, with no sinusoidal voltage, the collector current I_C was found to be $149.9\mu A \approx 150\mu A$. We assume the small signal model, so $g_m = \frac{I_C}{V_T} = 5.77m\Omega^{-1}$ So the theoretical parameters take the following values:

1. Differential Gain, $A_d = \frac{1}{2} g_m R_c = 6.63$
2. Common Mode Gain, $A_{cm} = \frac{R_C}{2R_E} = 0.078$
3. CMRR (absolute) $= \frac{A_d}{A_{cm}} = 85$
4. CMRR (dB) $= 20\log(\text{CMRR}_{abs}) = 38.6$
5. $\beta \approx 300$, $r_\pi \approx 52k\Omega$

The simulations for the output, with the inputs being 10mVpp, and 20mVpp sinusoidal with 1kHz frequency, are given below.

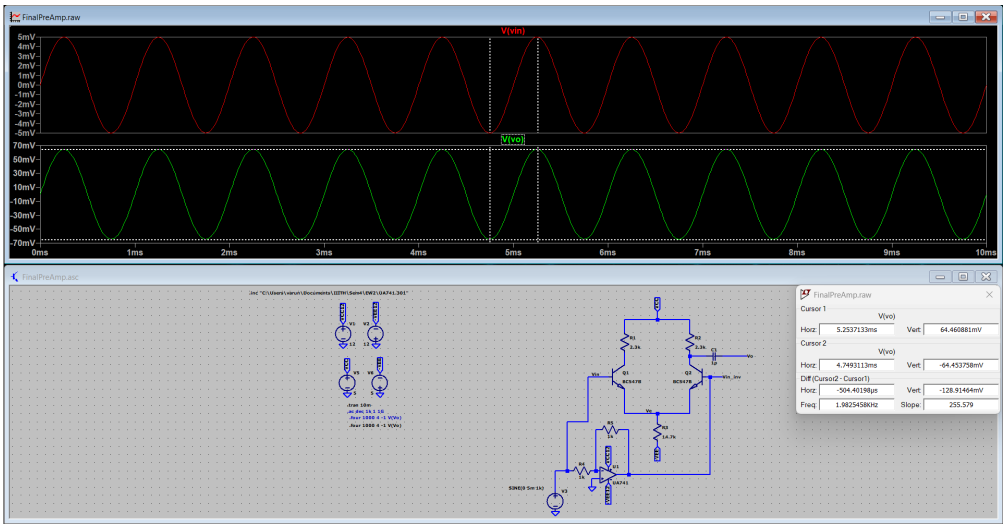

Figure 2.4: Output = 128.83mVpp for 10mVpp sinusoidal input

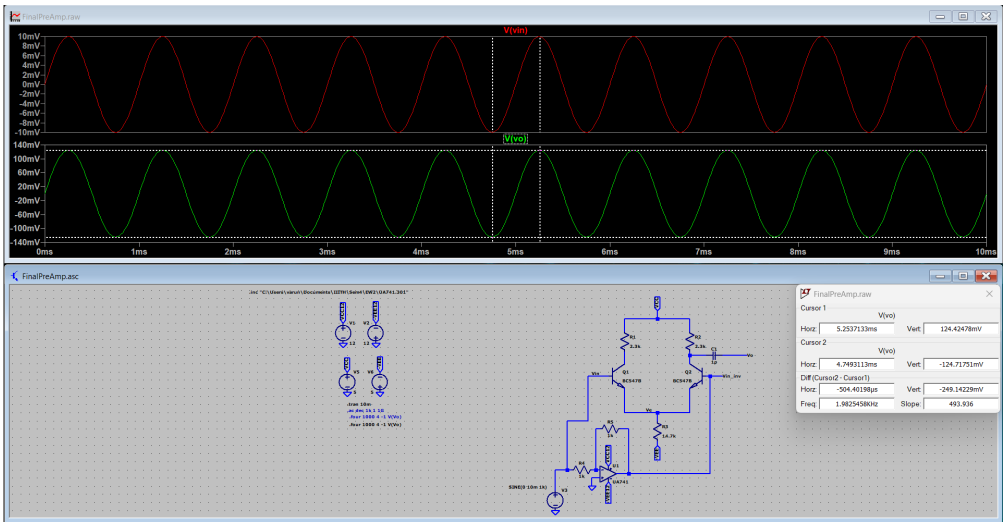

Figure 2.5: Output = 249.3mVpp for 10mVpp sinusoidal input

The gain we get through the simulations for the first case is about **6.44**, while the second case gives a gain of 6.23. Compared to the theoretical gain of 6.63 these results are expected, due to the assumption of several factors, especially the Early effect. Also, as seen above, the 20mVpp input is a larger deviation from the small differential input constraint of half of the thermal voltage, explaining the further reduction in gain value. Overall, these results are satisfactory, and show the working of the differential amplifier.

3 Gain Stage

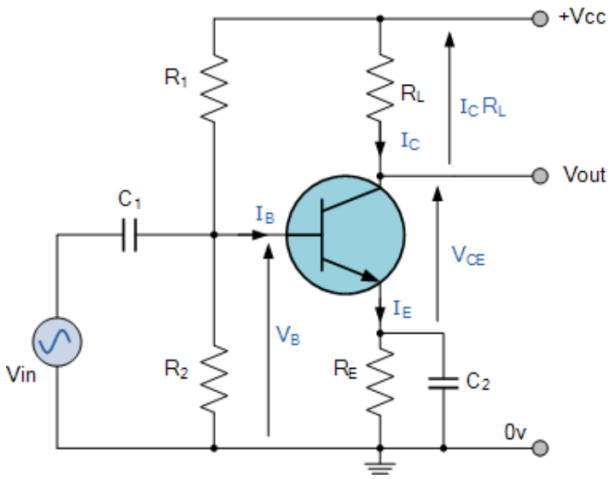

Figure 3.1: Common Emitter Amplifier

i Why the gain stage?

The Gain Stage amplifies the signal from the pre-amplifier to a level suitable for the power amplifier. It ensures the signal has enough strength and fidelity before being sent to the power amplifier.

ii Can we rely solely on the Preamp?

Pre-amplifiers are designed for low-level signal amplification, such as boosting signals from microphones level to line level. They are optimized for low noise, high sensitivity, and precise input matching. Driving higher gain through the pre-amp can introduce distortion, noise, or clipping, as it may exceed the circuit's design limits.
A single stage for full gain would not be able to maintain signal quality, as higher gains amplify noise and distortions along with the signal. Splitting the gain across the preamp, gain stage, and power amp ensures better linearity, low noise, and signal fidelity.
Additionally, the Gain stage also has high input impedance and low output impedance which serves as a buffer.

iii Theory

a. Input Impedance

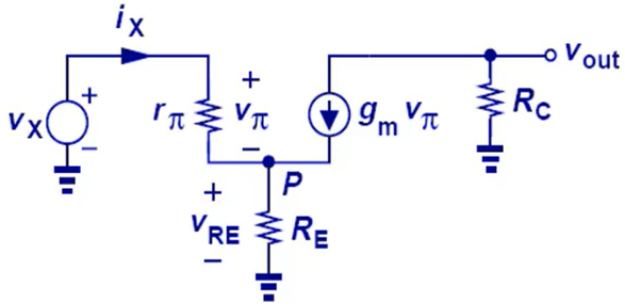

Figure 3.2: Input Impedance of Common Emitter Amplifier

By applying Kirchhoff's Voltage Law (KVL) from the base node to ground through the emitter node, we get:

$$V_x - i_x r_\pi - (i_x + g_m V_\pi) R_E = 0$$

where $V_\pi = i_x r_\pi$, Substituting V_π into the equation:

$$V_x - i_x r_\pi - (i_x + g_m i_x r_\pi) R_E = 0$$

Rearranging the terms, we get:

$$\frac{V_x}{i_x} = r_\pi + (1 + g_m r_\pi) R_E = R_{in}$$

Since $\beta = g_m r_\pi$, the input impedance R_{in} can be expressed as:

$$\boxed{R_{in} = r_\pi + (1 + \beta) R_E}$$

This equation shows that the input impedance is a combination of the base-emitter resistance r_π and the emitter resistance R_E multiplied by the current gain β. This ensures that the input impedance is sufficiently high, minimizing the loading effect on the previous stage.

b. Output Impedance

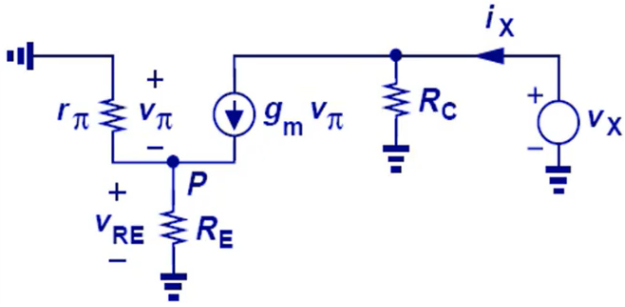

Figure 3.3: Output Impedance of Common Emitter Amplifier

While determining the output impedance, the goal is to measure the resistance seen at the output terminal when all independent sources are deactivated. So, the input voltage is shorted and thus becomes ground. Applying the KVL from Base to Emitter node:

$$V_\pi + \left(\frac{V_\pi}{r_\pi} + g_m V_\pi\right) R_E = 0$$
$$\therefore V_\pi = 0$$

Next, we consider the relationship between the output voltage V_x and the collector current i_c:

$$\frac{V_x}{R_C} + g_m V_\pi = i_c$$

Given that $V_\pi = 0$:

$$\frac{V_x}{R_C} = i_c \implies \frac{V_x}{i_c} = R_C$$

Thus, the output impedance R_{out} is equal to the collector resistance R_C:

$$\boxed{R_{out} = R_C}$$

c. Gain

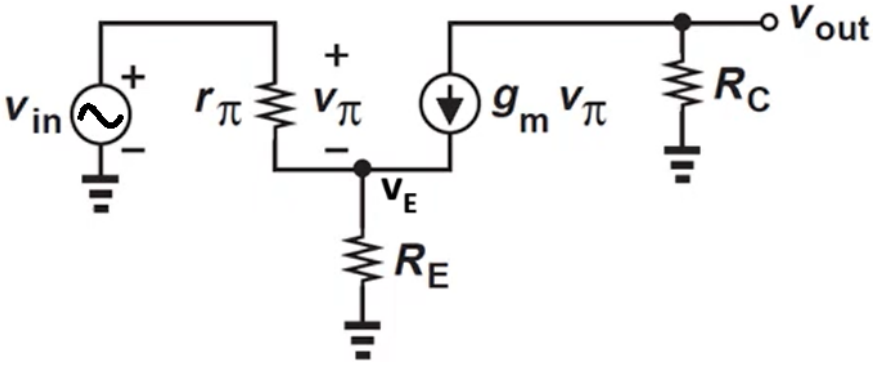

Figure 3.4: Small Signal Model

By applying the KVL at emitter node in the above small-signal circuit, equation is given as:

$$\frac{V_{in} - V_E}{r_\pi} + g_m V_\pi = \frac{V_E}{R_E}$$

Also, the output voltage is:

$$V_{out} = -g_m V_\pi R_C$$

where $V_\pi = V_{in} - V_E$. Substituting V_π:

$$\frac{V_{in} - V_E}{r_\pi} + g_m(V_{in} - V_E) = \frac{V_E}{R_E} \tag{3.1}$$
$$V_{out} = -g_m R_C (V_{in} - V_E)$$

Rearranging:

$$V_{in} - V_E = -\frac{V_{out}}{g_m R_C}$$

$$V_E = V_{in} + \frac{V_{out}}{g_m R_C}$$

Substitute V_E into equation 3.1:

$$\frac{-V_{out}}{g_m R_C r_\pi} + g_m \left(-\frac{V_{out}}{g_m R_C}\right) = \frac{V_{in}}{R_E} + \frac{V_{out}}{g_m R_C R_E}$$

Simplifying:

$$\frac{-V_{out}}{g_m R_C r_\pi} - \frac{V_{out}}{R_C} - \frac{V_{out}}{g_m R_C R_E} = \frac{V_{in}}{R_E}$$

$$\frac{-V_{out}}{V_{in}} = \frac{1}{\frac{1}{g_m R_C r_\pi} + \frac{1}{R_C} + \frac{1}{g_m R_C R_E}}$$

$$\frac{-V_{out}}{V_{in}} = \frac{R_C}{R_E\left(\frac{1}{g_m r_\pi} + \frac{1}{g_m R_E} + 1\right)}$$

$$\frac{-V_{out}}{V_{in}} \approx \frac{R_C}{R_E\left(1 + \frac{1}{g_m R_E}\right)} \quad \text{(assuming } r_\pi \gg R_E\text{)}$$

$$\boxed{A_v = -\frac{R_C}{\frac{1}{g_m} + R_E}}$$

The minus sign indicates that the output is 180 degrees out of phase with the input.

iv Designing

We used the small signal model for analyzing the parameters in the previous section. But the small signal will not hold true completely because the output from the pre-amplifier, which is the input to the gain stage, is in the range of about 200mV amplitude, which is not a small signal.
For designing the gain stage, we will understand the importance of each component and how it affects the gain and other parameters as following:

a. Biasing

The biasing of the transistor is done in the active region for the transistor to work as an amplifier. As shown in the figure, the biasing is done using resistors R1 and R2 as voltage divider biasing circuit. These are some key points which we consider while designing the biasing circuit:

- The biasing voltage should be such that the transistor is in the active region thoughout the complete cycle of amplification. By active region, we mean that the base emitter junction should be forward biased and the collector base junction should be reverse biased.
- The current through base should be much lesser than the current through the Resistor R2.
- The Resistance R1 and R2 should be put as high as possible to avoid the loading effect on the input signal.

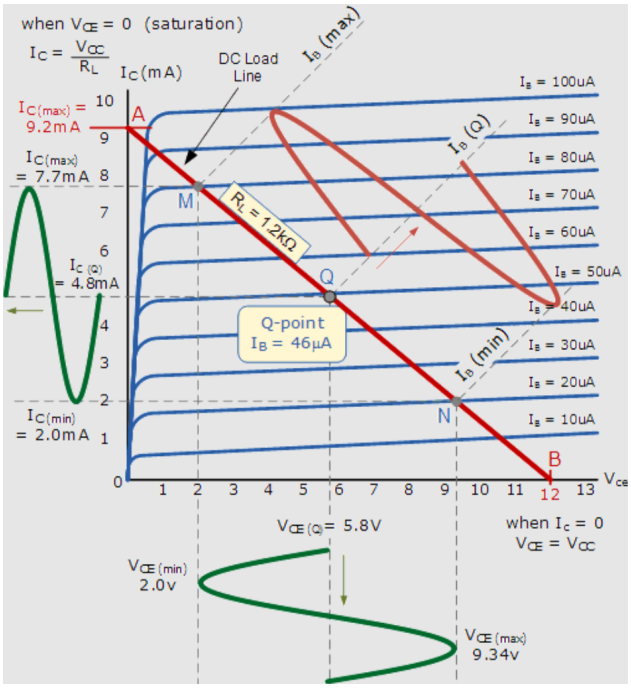

Figure 3.5: Operating Point (Q)

b. Emitter Resistance

The emitter resistance is used to provide stability to the circuit. It also provides negative feedback to the circuit which prevents clipping and distortion in output waveform. The gain of the circuit is given by the formula:

$$A_v = -\frac{R_C}{\frac{1}{g_m} + R_E}$$

The gain of the circuit is inversely proportional to the emitter resistance. So, the gain of the circuit can be controlled by changing the value of the emitter resistance.

c. Bypass Capacitor

Capacitor at the Emitter terminal (C_E) is the bypass capacitor which is used to bypass the AC signal to the ground. It is used to provide a low impedance path to the AC signal. The value of the capacitor is chosen such that the impedance of the capacitor is very low in comparison of Resistance R_E at the operating frequency of the circuit.

d. Coupling Capacitor

Capacitors at input and output terminal C_{in} & C_{out} are coupling capacitors which are used to block the DC component of the signal and allow only the AC component to pass through. These should offer the least impedance at the operating frequency of the circuit so that the signal is not attenuated and doesn't alter the input impedance.

v Design Calculations

Given: The following parameters are provided for the design:

- Input Amplitude (V_{in})= 210 mV
- Supply Voltage (V_{CC}) = 10 V
- Thermal Voltage (V_T) = 26.1 mV
- Current Gain (β) = 294

Output Voltage Amplitude: The desired output amplitude of the amplifier is given as:

$$\text{Output Amplitude } (V_{out}) = 4.2\,\text{V}$$

For calculating the design parameters, we start with some initial value assumptions. These are the DC operating points chosen for the transistor as following:

$$I_C = 1.5\,\text{mA}$$

$$\text{Base Bias Voltage} V_{Bias} = 1\,\text{V}$$

$$\text{Collector Voltage}(V_C) = 5.5\text{V}$$

Calculation of R_C: The collector resistor R_C is calculated using the voltage drop across it and the collector current:

$$\implies R_C = \frac{V_{CC} - V_C}{I_C} = \frac{10 - 5.5}{1.5\,\text{mA}} = 3\,\text{k}\Omega$$

Collector AC Current (i_c): The change in collector current (i_c) corresponding to the output voltage amplitude V_{out} is calculated as:

$$i_c = \frac{V_{out}}{R_C} = \frac{4.2}{3\,\text{k}\Omega} = 1.4\,\text{mA}$$

Transistor Current Analysis: The total collector current can be expressed as:

$$I_C + i_c = I_S e^{\frac{V_{BE}+v_{be}}{V_T}} = \underbrace{I_S e^{\frac{V_{BE}}{V_T}}}_{I_C}\ e^{\frac{v_{be}}{V_T}}$$

Where v_{be} is the small signal base-emitter voltage change. Taking the natural logarithm:

$$v_{be} = V_T \ln\left(\frac{I_C + i_c}{I_C}\right)$$

Substituting the values:

$$v_{be} = 26.1\,\text{mV} \cdot \ln\left(\frac{1.5 + 1.4}{1.5}\right) = 17.20\,\text{mV}$$

Emitter Resistance (R_E):
By applying KVL from the base node to the emitter node, we get the following equation:

$$R_E = \frac{V_{Bias} - V_{BE}}{I_C} = \frac{1 - 0.647}{1.5 \times 10^{-3}} = 235.3\,\Omega$$

The emitter resistance is determined by considering the input amplitude and the change in base-emitter voltage:

$$\implies R_{E_1} = \frac{V_{in} - v_{be}}{i_c} = \frac{210 - 17.20}{1.4} = 137.7\,\Omega$$

$$\implies R_{E_2} = R_E - R_{E_1} = 235.3 - 137.7 = 97.6\,\Omega$$

Voltage Divider Design:
To stabilize the bias point, a voltage divider network is designed. The relationship is given by:

$$\frac{R_2}{R_1 + R_2} V_{CC} = V_{Bias}$$

Putting the values in the equation, we get:

$$\frac{R1}{R2} = \frac{V_{CC}}{V_{Bias}} - 1 = \frac{10}{1} - 1 = 9 \tag{3.2}$$

Also, the base current I_B should be much lesser than the current through the Resistor R_2 to ensure that the voltage divider network provides a stable bias point. If the base current is too high, it will significantly affect the voltage drop across R_2 leading to an unstable bias point and affecting the amplifier's performance. So, we will take the base current to be 10 times lesser than the current through R_2.

$$I_B < \frac{1}{10} I_{R_2}$$

$$\frac{I_C}{\beta} < \frac{I_{R_2}}{10} = \frac{1}{10} \frac{V_{Bias}}{R_2}$$

We get the bound on the value of R_2 as:

$$R_2 < \frac{\beta V_{Bias}}{10 I_C} = \frac{294 \cdot 1}{10 \cdot 1.5 \times 10^{-3}}\,\text{k}\Omega$$

$$\boxed{R_2 = 19.6\,\text{k}\Omega}$$

Using equation 3.2, the value of R_1 is determined as:

$$R_1 = \left(\frac{R_1}{R_2}\right) R_2 = 9 \times 19.6\text{k}\Omega$$

$$\boxed{R_1 = 176.4\text{k}\Omega}$$

Bypass Capacitor (C_E):
The bypass capacitor C_E is chosen to ensure that the impedance at the emitter is negligible at the operating frequency. This can be achieved by ensuring that the impedance of C_E is much less than the emitter resistor R_E at the lowest frequency of interest (20Hz). This is expressed as:

$$\frac{1}{2\pi f C_E} < \frac{R_E}{10}$$

Substituting the values:

$$C_E > \frac{10}{2\pi f R_E} = \frac{10}{2\pi \times 20\,\text{Hz} \times 137.7\ \Omega} = 577.9\ \mu F$$

$$\boxed{C_E > 577.9\ \mu F}$$

Coupling Capacitor (C_{in}):
The coupling capacitor C_{in} is chosen such that the impedance at the input terminal is negligible at the operating frequency to block the DC component. This is expressed as:

$$\frac{1}{2\pi f C_{in}} < \frac{1}{10} R_{in} = \frac{1}{10}\left(R_1 \parallel R_2 \parallel (\underbrace{r_\pi}_{\frac{\beta . V_T}{I_C}} + (1+\beta) R_E)\right)$$

Substituting the values:

$$\frac{1}{2\pi \times 20\,\text{Hz} \times C_{in}} < \frac{1}{10}\left(176.4\ \text{k}\Omega \parallel 19.6\ \text{k}\Omega \parallel (\frac{294 \times 26.1}{1.5}\,\Omega + (1+294) \times 137.7\ \Omega)\right)$$

$$\frac{1}{2\pi \times 20\,\text{Hz} \times C_{in}} < \frac{1}{10}\,(176.4\ \text{k}\Omega \parallel 19.6\ \text{k}\Omega \parallel 45.7\ \text{k}\Omega)$$

$$\boxed{C_{in} > 6.25\ \mu F}$$

The above design calculations for the common emitter amplifier determines the key parameters such as R_C, R_E, R_1, R_2, and C_E to meet the desired specifications.

vi Simulations

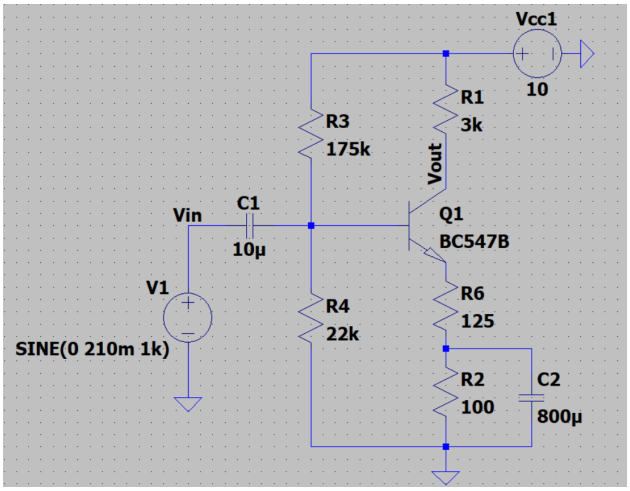

Figure 3.6: Simulated Circuit

The gain stage was simulated using LTspice to validate the design calculations and evaluate the amplifier's performance. The theoretical values were rounded to the nearest standard component values for simulation. The results of the simulation are presented below:

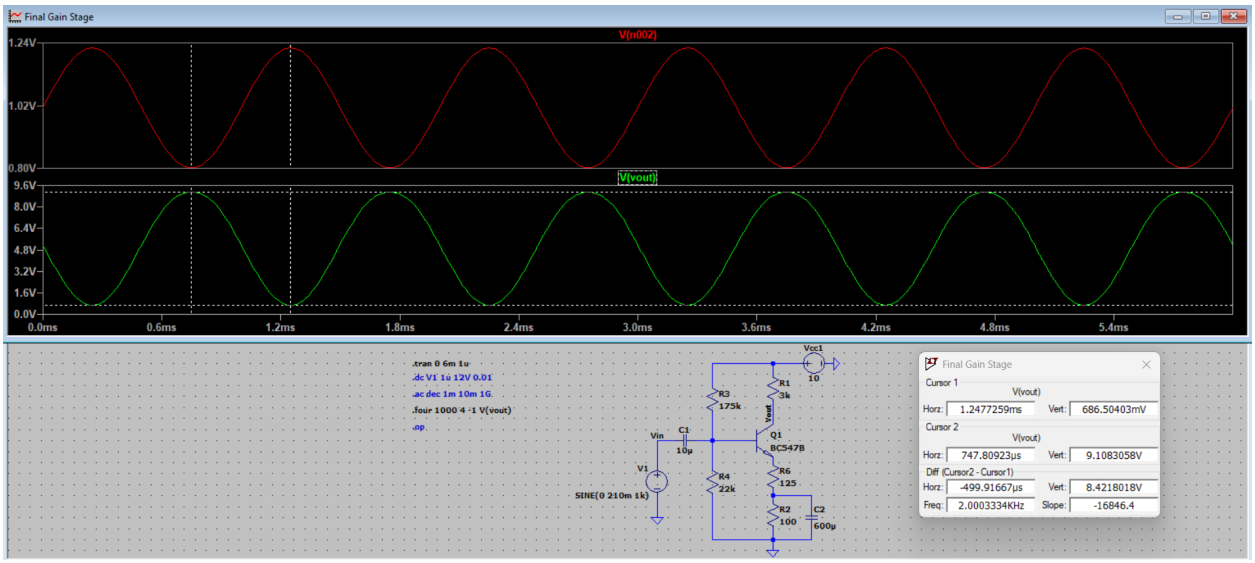

Figure 3.7: Common Emitter Amplifier Waveform Output

The output voltage waveform of the gain stage is shown in the figure above. The input signal of 0.42 Vpp is amplified to 8.4 Vpp, which corresponds to a voltage gain of approximately 20.

We can observe that the output waveform is 180 degrees out of phase with the input waveform, which is expected as the gain is negative.

The signal is amplified effectively without any clipping or significant distortion. This can be verified by the THD analysis which comes out to be 3.52%, which is within the acceptable range for audio amplifiers.

```
Fourier components of V(vout)
DC component:5.06161

Harmonic    Frequency     Fourier     Normalized   Phase       Normalized
 Number       [Hz]       Component    Component  [degree]    Phase [deg]
   1       1.000e+3      4.266e+0     1.000e+0    -90.53°       0.00°
   2       2.000e+3      1.536e-1     3.600e-2     -1.26°      89.28°
   3       3.000e+3      4.363e-2     1.023e-2    -91.60°      -1.06°
   4       4.000e+3      1.167e-2     2.737e-3    178.82°     269.35°
Partial Harmonic Distortion: 3.752747%
Total Harmonic Distortion:   3.528822%
```

Figure 3.8: Total Harmonic Distortion (THD)

Component	Theoretical Value	Simulated Value
R_C	3 kΩ	3 kΩ
R_{E_1}	137.7 Ω	125 Ω
R_{E_2}	97.6 Ω	100 Ω
R_1	176.4 kΩ	175 kΩ
R_2	19.6 kΩ	22 kΩ
C_E	577.9 μF	800 μF
C_{in}	6.25 μF	10 μF

Table 1: Component Values

4 Filter Stage

i Why an Active Band-pass Filter?

The bandpass filter stage is critical for ensuring that only the desired frequency range of the audio signal, typically 20 Hz to 20 kHz (the audible range), is passed through while attenuating unwanted low-frequency noise and high-frequency interference. This enhances the clarity and quality of the amplified signal, after it comes from the preamp and the gain stages.

An active filter is preferred over a passive one due to its ability to maintain or amplify signal strength while filtering, even when unity gain is sufficient. This is particularly valuable for small audio signals, as it prevents signal loss. Active filters, using operational amplifiers, offer better precision, easier tuning, and adjustable cutoff frequencies, making them ideal for achieving the desired frequency response. Additionally, they eliminate the need for bulky and costly inductors while providing better isolation between stages. The isolation is aided by the high input impedance, preventing the loading of the source, and also has low output impedance, allowing to drive the load without affecting the filter response.

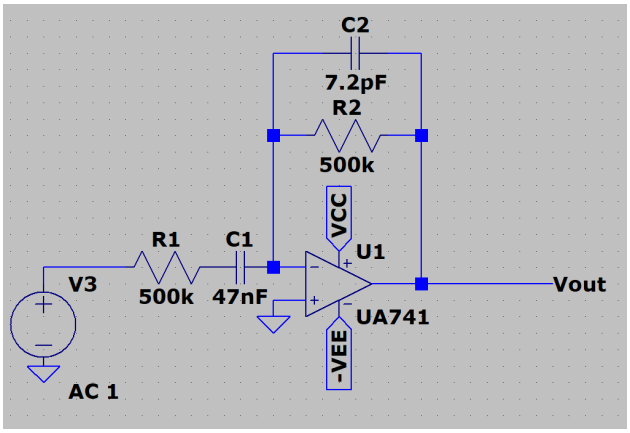

Figure 4.1: Filter Circuit

ii Theory

The circuit for the active bandpass filter, implemented by us, is given above. A high-pass filter is followed by the op-amp, and then a low-pass filter. Firstly, the input first encounters a series combination of R_1 and C_1. For very low frequencies (close to DC), the capacitor C_1 acts almost like an open circuit, i.e., its impedance is very high. This means very low frequencies get blocked. As the frequency increases, C_1's impedance decreases, allowing more signal to pass through. This behavior, blocking low frequencies and passing high frequencies, is exactly what defines a high-pass filter.

In an inverting amplifier, the feedback network determines the gain. For our circuit, R_2 in parallel with C_2 connects the output to the inverting input. At low frequencies, C_2's high impedance makes the gain depend on $-\frac{R_2}{R_1}$. As the frequency increases, C_2's impedance decreases, providing an alternate feedback path that increases negative feedback and reduces gain. At very high frequencies, C_2's low impedance results in significant attenuation of high-frequency signals, creating a low-pass filter effect.

Most importantly, we are given that there should be no attenuation in the pass-band. This in mathematical terms means that the gain must be 0dB in the pass-band, which gives us a condition

that $R_1 = R_2$ (explained below), and we ideally want a steep roll-off, which could have been achieved by higher order filters.

The transfer function of the filter is given in the derivation below:

The op-amp is in inverting configuration, whose gain is given by the formula $-Z_2/Z_1$, where Z_2 is the impedance in the feedback path. Thus, we have:

$$\begin{aligned} A_v &= -\frac{(R_2||\frac{1}{sC_2})}{(R_1+\frac{1}{sC_1})} \\ &= -\frac{\frac{R_2}{1+sC_2R_2}}{sC_1R_1+\frac{1}{sC_1}} \\ &= -\frac{sC_1R_2}{(1+sC_2R_2)(1+sC_1R_1)} \end{aligned}$$

Thus, the transfer function of this filter is obtained to be:

$$\boxed{A_v = -\frac{sC_1R_2}{(1+sC_2R_2)(1+sC_1R_1)}}$$

Imposing the condition that we need 0dB in the passband get the equation:

$$\log\left|\frac{R_2\omega C_1}{(1+j\omega C_1R_1)(1+j\omega R_2C_2)}\right| = 0$$

$$\frac{\omega C_1R_2}{\sqrt{1+\omega^2C_1^2R_1^2}\sqrt{1+\omega^2C_2^2R_2^2}} = 1$$

Now, in the pass-band region, i,$\omega >> \frac{1}{R_1C_1}$, and $\omega << \frac{1}{R_2C_2}$, we get the simplification that the first term in the denominator reduces to ωC_1R_1 and the second term reduces to 1, thus giving us the condition $R_1 = R_2$

We selected the cutoff frequencies to be lesser than 20Hz for the HPF, and greater than 20kHz for the LPF so that the attenuation for these frequencies is minimal. The cutoff frequency is given by the formula, $f_c = \frac{1}{2\pi RC}$. Thus, the cutoffs are listed below:

1. High-Pass Filter cutoff: 6.77Hz
2. Low-Pass Filter cutoff: 44kHz

Although these values seem bizarre given the audio lies in the 20Hz-20kHz region, the minimal attenuation for input with frequencies from 20Hz to 20kHz is a necessary condition to enforce.

iii Simulations

With the specifications laid down for our active bandpass filter, we run the simulations and obtain the Bode plot, by running a frequency response analysis on the circuit. The plot is given below, with the bold green line denoting the gain plot, whereas the faint green represents the phase plot.

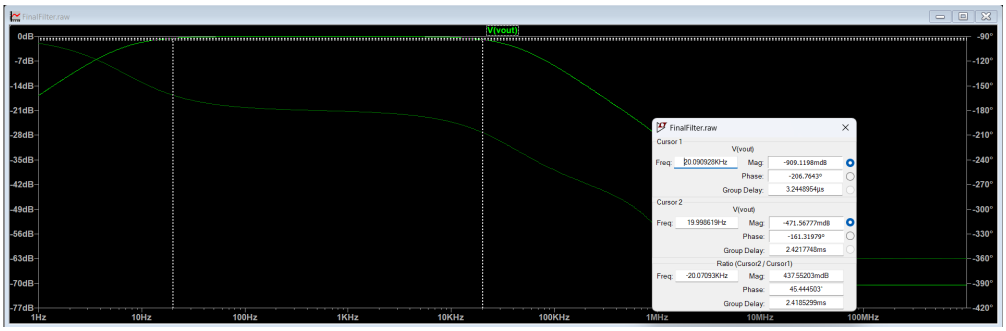

Figure 4.2: Frequency Response of the Filter

5 Power Amplifier Stage

i Why a Power Amplifier?!

The purpose of a power amplifier in an audio amplifier is straightforward: it boosts the low-power audio signal from the source to a level sufficient to drive speakers and produce audible sound. Without it, the output from most sources would be too weak for clear playback through speakers. As the final stage in the amplification chain, the power amplifier enhances the processed audio signal, already refined by the preamp, gain stage, and bandpass filter, providing the necessary power to drive speakers or headphones effectively.

While there are multiple power amplifier topologies, the ones discussed in the project document are class A, B and AB amplifiers. The type of "class" or classification that an amplifier is given really depends upon the **conduction angle**, the portion of the 360° of the input waveform cycle, in which the transistor is conducting.

ii Theory

a. About the Class A Amplifier

The Class A amplifier is the most common, and simplest form of power amplifier that uses a single switching transistor in the standard common emitter circuit configuration. The transistor is always biased "ON" so that it conducts during one complete cycle of the input signal waveform, producing minimum distortion and maximum amplitude of the output signal. Thus, in the Class A amplifier the conduction angle is a full 360°, or 100% of the input signal while in other amplifier classes the transistor conducts during a lesser conduction angle.

But, this topology comes with several issues! The efficiency of this type of circuit is very low (less than 30%) and delivers small power outputs for a large drain on the DC power supply. A Class A amplifier stage passes the same load current even when no input signal is applied, so large heat sinks are needed for the output transistors. Other topologies provide a better power efficiency.

b. About the Class B Amplifier

To improve the full power efficiency of the previous Class A amplifier by reducing the wasted power in the form of heat, it is possible to design the power amplifier circuit with two transistors in its output stage. This creates what is commonly termed as a Class B Amplifier, also known as a push-pull amplifier configuration.

Push-pull amplifiers use two "complementary" or matching transistors, one being an NPN-type and the other being a PNP-type, with both power transistors receiving the same input signal together that is equal in magnitude, but in opposite phase to each other. This results in one transistor only amplifying one half or 180° of the input waveform cycle while the other transistor amplifies the other half or remaining 180° of the input waveform cycle, with the resulting "two-halves" being put back together again at the output terminal.

Then the conduction angle for this type of amplifier circuit is only 180° or 50% of the input signal. This pushing and pulling effect of the alternating half cycles by the transistors gives this type of circuit its amusing "push-pull" name, but are more generally known as the Class B Amplifier.

This design is more efficient but introduces a new issue called **crossover distortion**. It's akin to a baton handoff in a relay race, where there's a brief moment of uncertainty about control.

Similarly, when the audio signal transitions between positive and negative (or vice versa), neither transistor fully conducts because the signal is too small to overcome their threshold voltages. This creates a "dead zone" where neither transistor operates properly.

As a result, instead of a smooth sine wave, the output signal develops small **notches** or discontinuities near the *zero-crossing points*. These distortions can lead to a harsh, scratchy sound, particularly noticeable during quieter audio passages, degrading the overall sound quality.

A simple way to eliminate crossover distortion in a Class B amplifier is to add two small voltage sources to the circuit to bias both the transistors at a point slightly above their cut-off point. This then would give us what is commonly called a Class AB Amplifier circuit.

c. The Class AB Amplifier

The Class AB Amplifier circuit is a compromise between the Class A and the Class B configurations. This very small diode biasing voltage causes both transistors to slightly conduct even when no input signal is present. An input signal waveform will cause the transistors to operate as normal in their active region, thereby eliminating any crossover distortion present in pure Class B amplifier designs.

A small collector current will flow when there is no input signal, but it is much less than that for the Class A amplifier configuration. This means then that the transistor will be "ON" for more than half a cycle of the waveform but much less than a full cycle, giving a conduction angle of between 180° to 360° or 50% to 100% of the input signal, depending upon the amount of additional biasing used. The amount of diode biasing voltage present at the base terminal of the transistor can be increased in multiples by adding additional diodes in series.

For our circuit, we explored various design topologies, ranging from resistor bias models to diode bias and Darlington pairs, all to achieve satisfactory performance within the constraints of the tight voltage supply limits! We started from the typical resistor-bias model given to us in the project document.

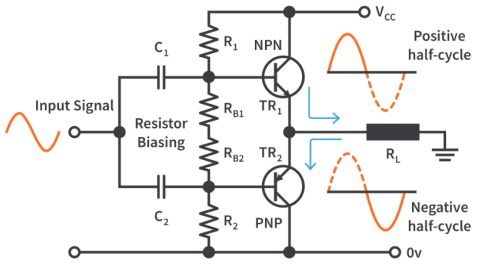

Figure 5.1: Resistor-biased Class AB Amplifier

The circuit comes along with an issue plaguing the circuit, the stability of the bias. The voltage divider resistors have to be very accurate in order to set the transistors right where we want them, and stability is a concern. The problem is that we are trying to use a device with a linear current-voltage characteristic (a resistor) to match the exponential current-voltage characteristic of a PN junction. This problem is exacerbated by the fact that these devices will drift with temperature, and definitely drift in different ways. The solution to this problem is to use a device with better matching characteristics. So what better device to match a PN junction than another PN junction!

The use of diodes for biasing, also brings about a topology, similar to the current mirror, circuit diagram below. To understand it's working, first look at the divider between R and D. The voltage

across R must equal, the supply voltage minus the diode drop (which we **assume to be 0.7V**), which is V-0.7. This sets up a current I_R. If we also *ignore the base current* (if small enough), the same current flows through as I_D. This diode current sets up a specific voltage across the diode, somewhere around 0.7V, though the precise value is immaterial to the understanding.

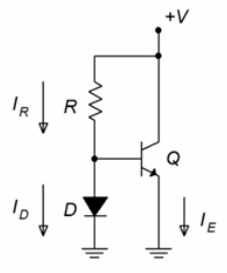

Figure 5.2: Current Mirror Circuit

Now because the diode is in parallel with the base-emitter junction, $V_{BE} = V_D$. If we assume that the I-V (transconductance) curve of the BJT is similar to that of the diode, the emitter current must be the same as I_D. Any change in the diode current would cause a slight change in diode voltage, and since diode voltage and base-emitter voltage are the same, then the emitter current must change in response. In other words, the emitter current mirrors the diode current. We can thus program the diode current (and hence, the emitter current) by setting an appropriate value for R. Whatever the current through R is, that's also the collector.

This theory leads us to the topology of class AB amplifier with diode-biasing, as given below:

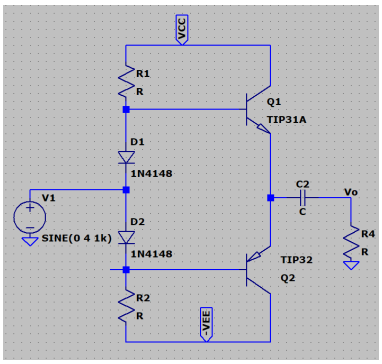

Figure 5.3: Diode-Biased Class AB Amplifier

At first glance, it appears that the positive portion of the input signal would be "going the wrong way" against the diode D_1. What we need to remember is that D_1 **is already forward-biased** due to the DC supply and surrounding resistors. The input signal won't see an open, but will see the dynamic resistance of the diode.

Choosing the capacitor value to eliminate the DC component is important, ensuring that the high-pass cutoff due to the load resistor of 10Ω and this capacitor is less than 20Hz, so that our signals aren't attenuated severely. Choosing a cutoff of slightly less than 20Hz, we get the capacitor C_2's capacitance to be about $940\mu F$, also considering the values of components available in the lab.

Also, given that the load is given to be about 10Ω, we changed the BJT model to the TIP by Texas Instruments, which has a higher current rating than the BC547 family.

But the issue here came down to the fact that our input voltage, came up very close to the supplies of $\pm 5V$, because the gain of the preamp and the gain stage come up to be about 400. This means a 10mVpp input would reach 4V when we supply it as an input to this power amplifier. On running simulations, we realized that the best voltage input that we could give for a clean output, with low THD, is a mere 3V amplitude sinusoid, which is very less in terms of driving the speaker which has a power rating of 0.5W, so here came the need to look for another topology.

After a lot of research, we came across a couple of stack exchange pages (referenced below) which have explained the approach. We shall try to present a brief explanation here for the same.

iii Improving the Push-Pull Amplifier

The solution from the class B to a class AB amplifier, was obvious, to apply a tiny initial voltage (about 0.7V) across each base-emitter junction. This means to add this voltage to the input voltage and apply the sum to Q_1's base, and to subtract it from the input voltage and apply the difference to Q_2's base, which we can implement it by two diodes (D_1 and D_2) connected in series. But with a 10Ω load, we observe the issue of overloading! We see that the Q1's base current and, accordingly, the voltage drop across R_1, have significantly increased.

To understand this situation better, and to explain the clipping observed above, we have the plots of v_{in} and v_{out} below, obtained by DC sweeping the input voltage from -5V to 5V.

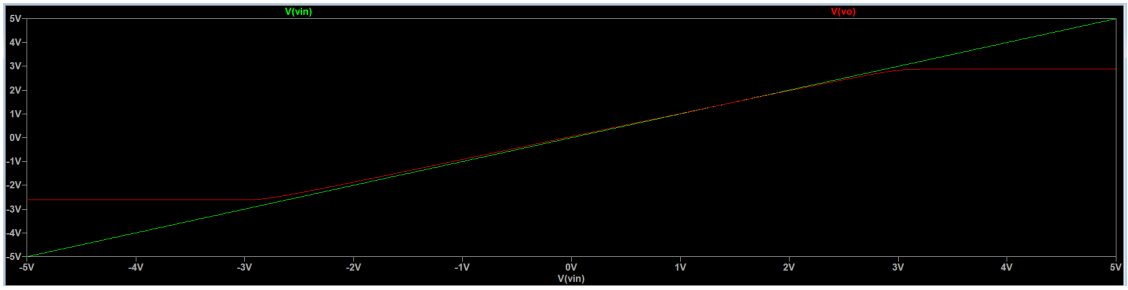

Figure 5.4: Output and input voltage vs input voltage sweep

We can observe the clipping happens much early compared to the $\approx$ 8Vpp input that we are trying to feed to the power amplifier. We can solve this issue by reducing the values of the bias resistors connected to the power supply, at a tradeoff of the diode current being very high.

With this analysis, we understand that the problem is that R_1 and R_2 are constant (static) resistors. So, when V_{in} increases, the voltage drop across and the current through R_1 decreases, and at some point the diode D_1 turns off. The same happens with the negative cycle of input voltage, with D_2. So, the solution is to make R_1 and R_2 *dynamic*, i.e., they have to decrease their resistance when the voltage across them decreases and vice versa! In other words, they have to be **current-stabilizing resistors** (transistors).

We can analyze this by replacing the resistors with constant current sources. The circuit for this is given below.

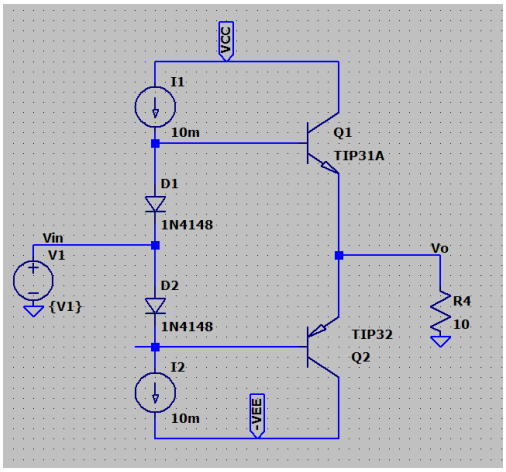

Figure 5.5: Circuit with constant current sources

The sweep plot as seen above, for this circuit in 5.5, can be seen below.

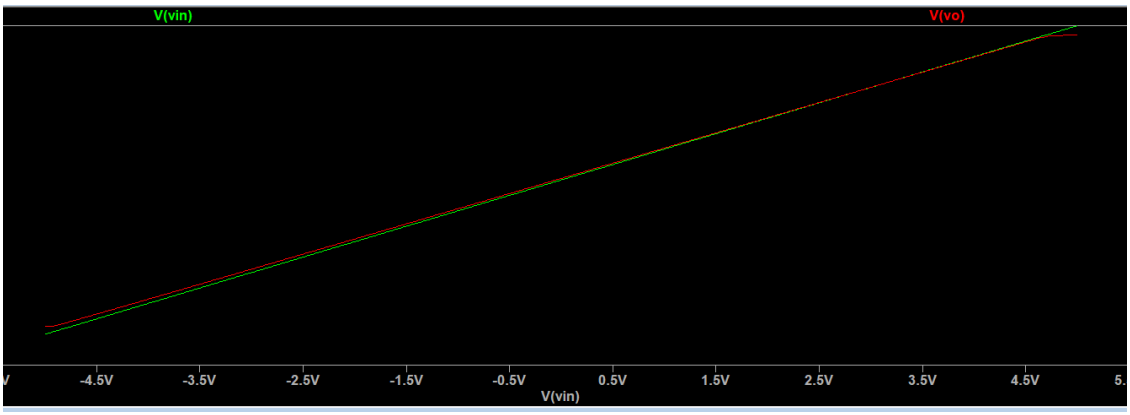

Figure 5.6: V_{out} and V_{in} with V_{in} sweep

To realize these current sources in a circuit, we use transistors with a constant base-emitter (V_{BE}) voltage. On simulations, we realized that the circuit is pretty sensitive to this base-emitter voltage, because a slight change in this voltage, can change the bias current by a significant amount, affecting the circuit behavior.

We would like to mention that we tried the Darlington Pair power amplifier topology as well, but realized that it would have a **DC power component** too, which is bad for the speaker as it is designed to handle AC signals that cause the diaphragm to move back and forth, producing sound. Supplying DC power results in a **constant offset in the diaphragm's position**, potentially pushing it toward one extreme. This static position can overheat and damage the voice coil or permanently deform the diaphragm.

iv Simulations

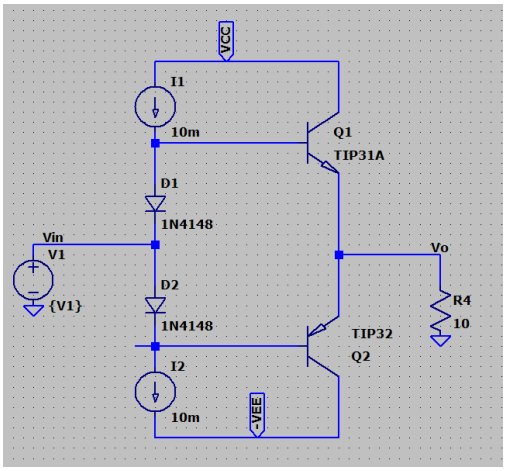

Figure 5.7: Our Power Amplifier circuit

This circuit for an input of 8.2Vpp amplitude sinusoid, produces an output of 8.00Vpp (plot below), with a THD of about 0.44%, which is a value good enough, considering the supply constraints. We do understand that this circuit is sensitive to the base-emitter voltage, and that **if it shall fail in the hardware section, we will replace it with a diode-biased circuit.**

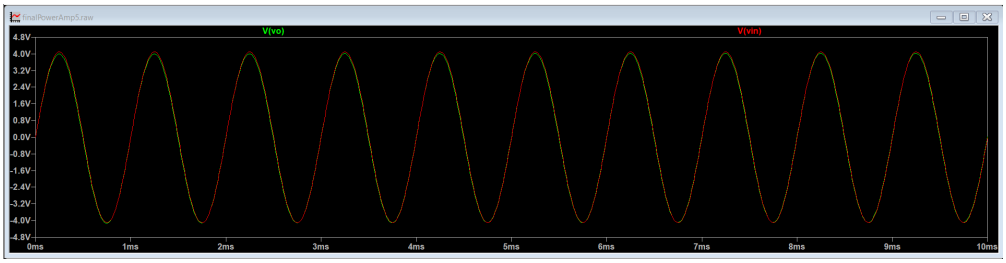

Figure 5.8: Input and Output voltage Plots

Lastly, for the purpose that the circuit was built, the power amplifier increases the current through the load (current gain is about 20), and the power (RMS power measured using the RMS current through the load) comes out to be about 0.8W, for an 8.2Vpp input to the power amplifier.

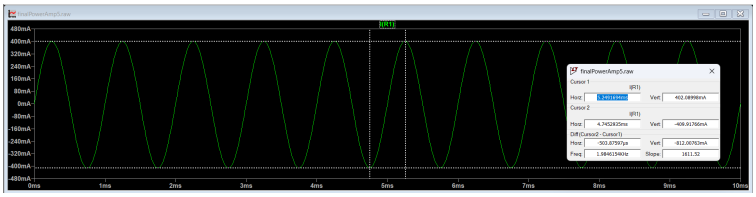

Figure 5.9: Plot of Current through the speaker load

6 Final Circuit Specifications

With the understanding of each component in the audio amplifier, we thus present the final circuit below!

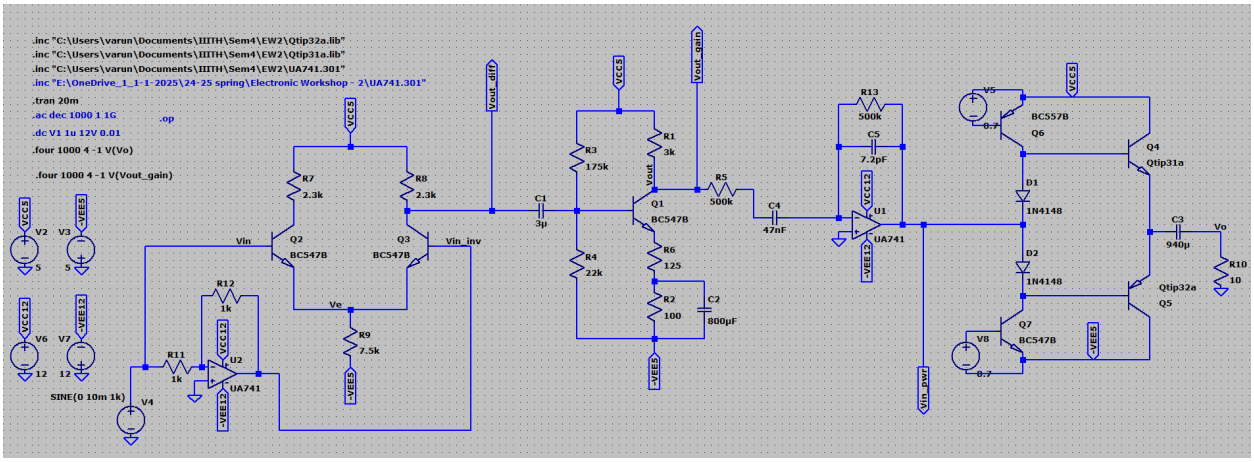

Figure 6.1: Audio Amplifier Circuit

As highlighted in the introduction, the primary focus was to design a circuit with minimal THD while achieving the required voltage and power gains. Careful attention was given to prevent excessive amplification that could lead to issues such as voltage clipping, ensuring the design met the specified requirements without overloading the system.

i Simulation

Below are the plots for the output and the inputs, for the extreme cases of the input voltage.

1. **10mVpp Sinusoidal Input**:
   The output and input voltage waveforms are given in the plot below.

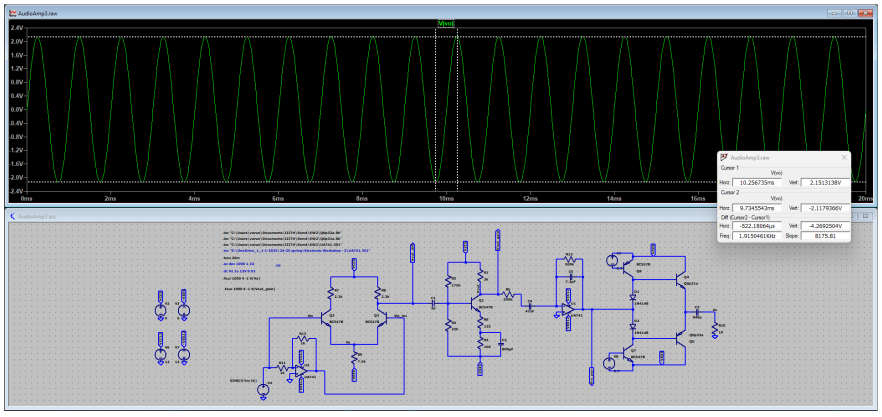

Figure 6.2: Plots for 10mVpp input

We can see that the gain is about a factor of 426. The THD value is about 1.43% which can be seen in the screen snip below.

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]
1	1.000e+3	2.147e+0	1.000e+0	89.95°
2	2.000e+3	2.681e-2	1.249e-2	-177.65°
3	3.000e+3	9.712e-3	4.524e-3	93.59°
4	4.000e+3	4.290e-4	1.998e-4	-11.03°

Partial Harmonic Distortion: 1.328421%
Total Harmonic Distortion: 1.430059%

Figure 6.3: THD for 10mVpp input

Using the plot of the current through the load, we find the peak current, and then find the RMS power, which comes out to be 0.23W

2. **20mVpp Sinusoidal Input**:
The output and input voltage waveforms are given in the plot below.

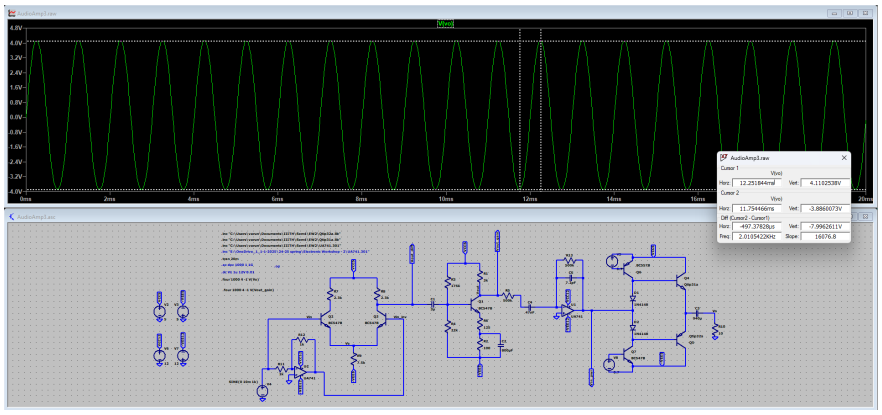

Figure 6.4: Plots for 20mVpp input

We can see that the gain is about a factor of 400. The THD value is about 3.91% which can be seen in the screen snip below.

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component
1	1.000e+3	4.095e+0	1.000e+0
2	2.000e+3	1.337e-1	3.265e-2
3	3.000e+3	8.653e-2	2.113e-2
4	4.000e+3	5.794e-3	1.415e-3

Partial Harmonic Distortion: 3.892135%
Total Harmonic Distortion: 3.907681%

Figure 6.5: THD for 20mVpp input

Using the plot of the current through the load, we find the peak current, and then find the RMS power, which comes out to be 0.80W

7 Bill Of Materials and References

The bill of materials, generated by LTSpice for the full circuit, is given in the screen snippet below.

--- Bill of Materials ---

Ref.	Mfg.	Part No.	Description
C1	--	--	capacitor, 3µF
C2	--	--	capacitor, 800µF
C3	--	--	capacitor, 940µF
C4	--	--	capacitor, 47nF
C5	--	--	capacitor, 7.2pF
D1	OnSemi	1N4148	diode
D2	OnSemi	1N4148	diode
Q1	NXP	BC547B	bipolar transistor
Q2	NXP	BC547B	bipolar transistor
Q3	NXP	BC547B	bipolar transistor
Q4	--	Qtip31a	bipolar transistor
Q5	--	Qtip32a	bipolar transistor
Q6	NXP	BC557B	bipolar transistor
Q7	NXP	BC547B	bipolar transistor
R1	--	--	resistor, 3K
R2	--	--	resistor, 100
R3	--	--	resistor, 175K
R4	--	--	resistor, 22K
R5	--	--	resistor, 500K
R6	--	--	resistor, 125
R7	--	--	resistor, 2.3K
R8	--	--	resistor, 2.3K
R9	--	--	resistor, 7.5K
R10	--	--	resistor, 10
R11	--	--	resistor, 1K
R12	--	--	resistor, 1K
R13	--	--	resistor, 500K
U1	(unknown)	UA741	(unknown 3rd party model)
U2	(unknown)	UA741	(unknown 3rd party model)

Figure 7.1: Bill of Materials

References

1. Stack Exchange Page: Class AB Amplifier Biasing Work Explanation
2. Stack Exchange Page: Class AB BJT Biasing with Diodes
3. Stack Exchange Page: Unexpected Crossover Distortion
4. *Semiconductor Devices: Theory and Application* by James M. Fiore
5. Stack Exchange Page: Use of Diodes and Resistors in Push-Pull Amplifier
6. Stack Exchange Page: Push-Pull Amplifier with Diodes and Resistors (Duplicate Link)
7. *Audio Power Amplifier Design Handbook* by Douglas Self
8. All About Electronics on YouTube
9. Mateo Aboy's series on Differential Amplifiers on YouTube
10. *The Art of Electronics, 3rd Edition* by Paul Horowitz and Winfield Hill
11. Electronics Tutorials: Introduction to Amplifiers
12. George Washington University for the TIP library files: TIP Library Files