Analog Electronics Circuits Project 2024

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I. Introduction

The **Quadrature Down Converter** (abbreviated as the *QDC*) is an essential component in wireless communications, which enables specific frequency signals to be retrieved post carrier-modulation. Our aim here is to explore a compact, precise and dynamic QDC design using a double-integrator loop. The primary advantage that this design provides is amplitude stability alongside the ability to control the selected frequency using a single variable resistance. While preliminary results are promising, they also suggest potential refinements for phase and amplitude correction, which will be explored in the *'Further Developments'* section."

Keywords- Barkhausen Criterion, Closed loop Gain, Modulation

II. Quadrature Oscillator Design

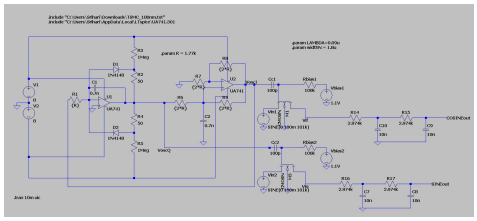

Fig. 1. The QDC Model on SPICE

It is quintessential for any oscillator to satisfy the Barkhausen criterion - the **closed loop phase shift must be equal to 0, and that the closed loop gain must be 1**. Our design exploits the fact that the QDC requires the generation of 90° phase shifted sinusoids, which we know can be inter-converted by integration. Combining these facts, we naturally arrive upon the inverting + non-inverting integrator combination: each integrator individually provides a ± 90 degree phase shift, thus providing an overall 0 degree phase shift, and a closed loop gain of 1. Thus, we would expect to seamlessly inter-convert between the two required sinusoids. Real-world circuits have imperfections. To manage these imperfections, we intentionally set the open-loop gain slightly above 1. This might cause the signal to grow over time, so we use a simple *limiter circuit* with diodes and resistors. This limiter circuit ensures that the oscillating signal's amplitude stays within desired limits.

A. Circuit Analysis and Establishment of Component Relations

1) Relation between Integrators: The following mathematical analysis helps us establish the key relation between the resistors R, R' in the circuit, where R refers to the resistor appearing before the inverting integrator and R' to the resistor appearing before the non-inverting integrator.

The first step is to find the equivalent circuit of a section of the non-inverting integrator as shown below:

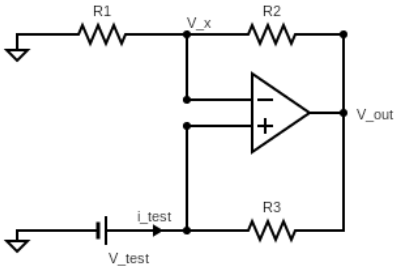

Fig. 2. Finding Equivalent Impedance

To find the equivalent impedance of the circuit, we apply a test source and measure the test current. No current flows through the terminals of the op-amp, thus we have,

$$i_{test} = \frac{V_{test} - V_{out}}{R_3} \tag{1}$$

By voltage division, we get,

$$V_X = \frac{R_1}{R_1 + R_2} V_{out} \tag{2}$$

So we get,

$$V_{out} = \frac{R_1 + R_2}{R_1} V_X \tag{3}$$

Thus we have the test current,

$$i_{test} = \frac{V_{test} - \frac{R_1+R_2}{R_1} V_X}{R_3} \tag{4}$$

We realize that for the configuration to be stable, we must assume virtual shorting (negative feedback and of-course, assumption of linear mode). Hence, $V_+ = V_- \implies V_{test} = V_X$

Thus we have,

$$i_{test} = V_{test}(\frac{1}{R_3} - \frac{R_1 + R_2}{R_3 R_1}) \tag{5}$$

$$\therefore \frac{V_{test}}{i_{test}} = -\frac{R_1 R_3}{R_2} \tag{6}$$

We obtain a negative impedance! This denotes an opposite direction of the current. Now substituting this in the circuit, we get the circuit as:

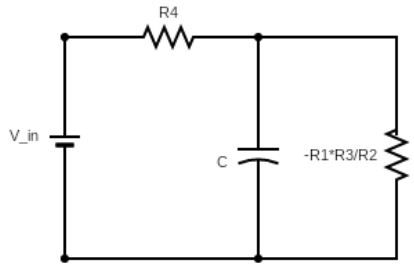

Fig. 3. Equivalent of Deboo Integrator

We can convert the series voltage source R_4 into a current source, parallel to R_4,

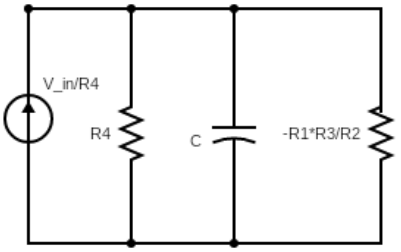

Fig. 4. Voltage to current source

Note that the configuration in Fig. 5 is an integrator:

From the above circuit, we this get the equation:

$$i = C\frac{dV_c}{dt} \tag{7}$$

Hence,

$$\boxed{V_c = \frac{1}{R_4 C}\int V_{\text{in}}\, dt} \tag{8}$$

Thus, this is equivalent to an ideal current source (infinite parallel resistance!), So we take:

$$\frac{1}{R_{parallel}} = \frac{1}{R_4} + \frac{1}{(\frac{-R_1 R_3}{R_2})} \tag{9}$$

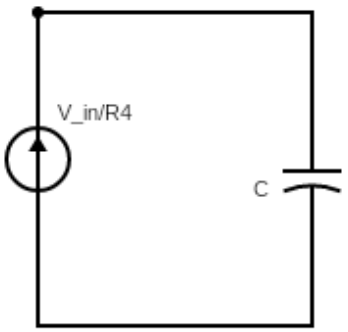

Fig. 5. A direct integrator using a current source

We can obtain $R_{parallel} = \infty$, if

$$\boxed{\frac{R_1 R_3}{R_2} = R_4} \tag{10}$$

and thus we have found the integrator condition. For simplicity, assume $R_1 = R_2 = R_3 = R_4 = R'$

Now we can compute the transfer function. We know:

$$\frac{V_{in(s)}}{sR'C} = V_c(s) \tag{11}$$

Since we have assumed inverting and non-inverting terminals are at the same voltage, and the resistors have the same values:

$$\frac{V_{in}(s)}{j\omega R'C} = \frac{V_{out}(s)}{2} \tag{12}$$

Thus,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{2}{\omega R'C} \cdot -j \tag{13}$$

As we recall from the inverting integrator, $\omega = \frac{1}{RC}$. We will use the same capacitance for our non-inverting integrator.

$$\frac{V_{out}(s)}{V_{in}(s) = \frac{2}{(\frac{1}{RC})R'C} = (\frac{2R}{R'}) \cdot -j} \tag{14}$$

Since we want to achieve a transfer of -j, (-90° phase shift), we must set $\boxed{R' = 2R}$

Thus, the overall loop gain = $H(s)_1 \cdot H(s)_2 = j \cdot -j = 1$, which satisfies the criterion for oscillation.

How does the oscillator select a particular frequency?

- Background Noise: Electronic circuits always contain a degree of random noise spanning a wide range of frequencies. This noise provides the initial "seed" for oscillations.
- Now, Oscillators contain a resonant circuit (like in our case, an RC circuit) that has a preferred frequency of oscillation. This circuit acts like a filter, favoring a specific frequency while suppressing others.

- The op-amp takes a portion of the filtered signal and feeds it back to the resonant circuit's input. If the loop gain (amplification within this cycle) is greater than one, the oscillation grows with each pass.

The following topic is about the choice of resistors in the limiter circuit used.

2) Amplitude Control in Limiter Circuits: As already mentioned above, the amplitude of the oscillator-generated signal is allowed to grow till the value set by our limiter configuration, in this case being $1mV_{pp}$. The limiter is wrapped around the op-amp in a negative feedback loop, irrespective of how the diodes operate.

Let's briefly analyze the working of the Limiter Circuit. Given below is a simple application of the limiter with an op-amp:

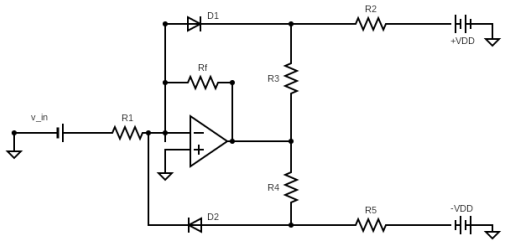

Fig. 6. Limiter configuration

- Consider the case of a small input v_{in} (close to zero), we thus get a small output v_{out}, so that $v_A > 0$ and $v_B < 0$. Clearly, both the diodes are OFF, thus the current only flows through the feedback resistor, and we get the expression for v_{out} as, (inverting amplifier configuration).

$$v_{out} = -\frac{R_f}{R_1} v_{in} \tag{15}$$

This is the *linear* portion (Fig.8) of the circuit's transfer function. As long as we lie in this *linear operation*, we can use superposition to find v_A and v_B in terms of $\pm V_{DD}$ and v_{out}

$$v_A = V_{DD} \frac{R_3}{R_2 + R_3} + v_{out} \frac{R_2}{R_2 + R_3} \tag{16}$$

$$v_B = -V_{DD} \frac{R_4}{R_4 + R_5} + v_{out} \frac{R_5}{R_4 + R_5} \tag{17}$$

- From (15), as v_{in} becomes more positive, v_{out} becomes more negative, thus from (17), v_B becomes more negative, keeping D_2 OFF. However (16) suggests that v_A becomes less positive. So as we increase v_{in} further, eventually we will reach a v_{out} at which v_A becomes $\approx -0.7V$ (diode cut-in), and D_1 conducts (assuming the constant voltage model of the diode). This value of v_{out} at which D_1 conducts, also called the *negative limiting limit*

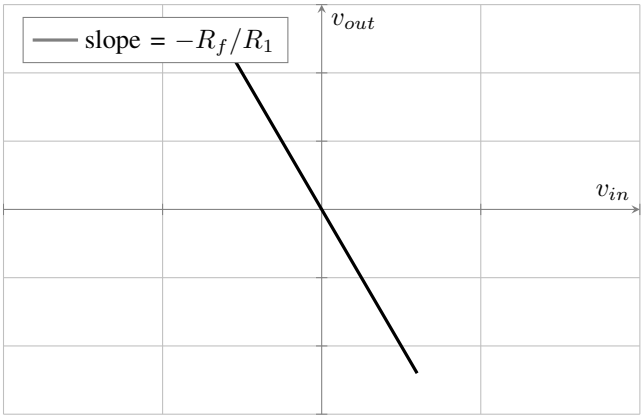

Fig. 7. Voltage Transfer Function in Linear Region

(L_-), can be found from (16), and will be, (assuming the voltage drop across the diode to be V_D),

$$L_- = -V_{DD} \frac{R_3}{R_2} - V_D(1 + \frac{R_3}{R_2}) \tag{18}$$

And the corresponding input voltage can be found by dividing this output voltage by the limiter gain $-R_f/R_1$ is given by,

$$v_{L_-} = -\frac{L_-}{(R_f/R_1)} \tag{19}$$

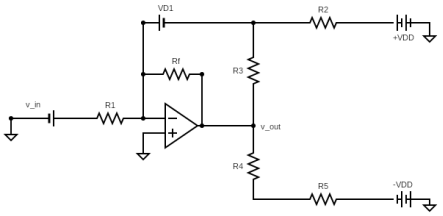

Fig. 8. The limiter when D1 is ON

Now once D_1 turns ON, v_A remains fixed at $-V_{D_1,on}$, therefore as v_{in} keeps increasing, the additional current v_{in}/R_1 can **only flow in** R_3 **and** R_f. (Voltage across R_2 is constant at $V_{DD} - v_A = V_{DD} + V_{D_1,on}$, no AC current flows through R_2).

Thus the AC Circuit is equivalent to Fig. 9, and thus The

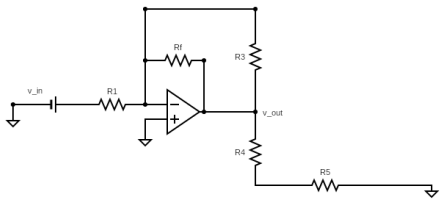

Fig. 9. The AC model of the limiter

voltage transfer function obtained with this is as given below:

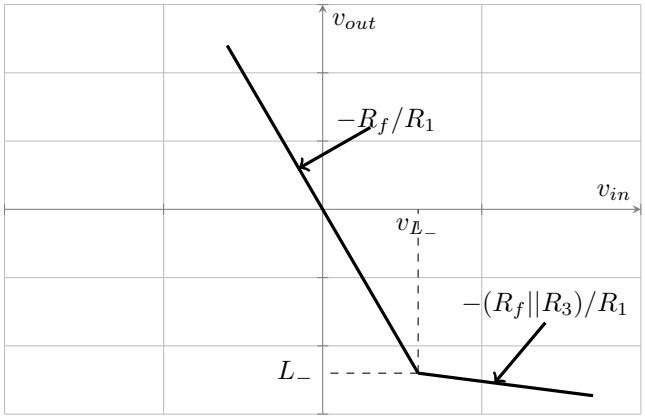

Fig. 10. Voltage Transfer Function including the Negative limiting level

- Similarly, As v_{in} becomes more **negative**, v_{out} becomes more positive, as a result, v_A remains (becomes more) positive and D_1 is OFF. Also, v_B becomes more positive, and as v_{in} continues to decrease, eventually we will reach a positive value of v_{out} at which v_B becomes $\approx 0.7V$ (diode cut-in) and D_2 turns on. This value of v_{out} is given by:

$$L_+ = V_{DD}\frac{R_4}{R_5} + V_D(1 + \frac{R_4}{R_5}) \tag{20}$$

and the corresponding input value can be found by dividing this output by the limiter gain of $(-R_f/R_1)$. Thus,

$$v_{L_+} = -\frac{L_+}{(R_f/R_1)} \tag{21}$$

We thus obtain the complete voltage transfer function as below:
Thus the circuit functions as a soft limiter, with the limiting levels L_+ and L_- and the limiting gains independently adjustable by the selection of appropriate resistor values.

This quadrature oscillator circuit (Fig. 13) provides flexibility in frequency selection. The desired output frequency can be achieved by adjusting the value of resistor $R1$.

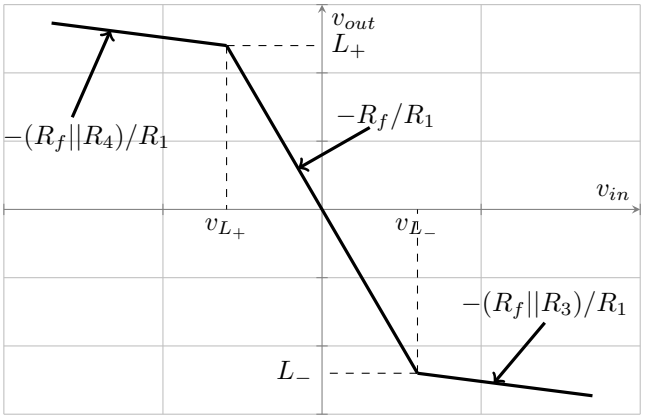

Fig. 11. Voltage Transfer Function of the Diode Limiter

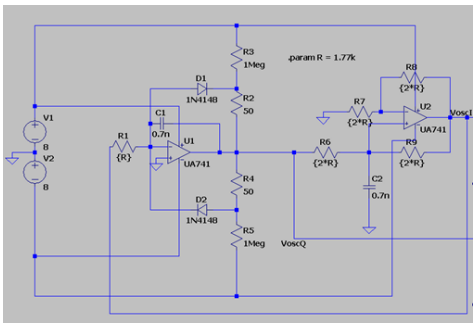

Fig. 12. Design for the Quadrature Oscillator on SPICE

B. Practical Testing and Results

The circuit's ease of construction was demonstrated using the widely available UA741 operational amplifier. Due to it's *transfer characteristic poles occurring around 1MHz*, and our operation being at approximately **100kHz** (i.e. a tenth of the pole frequency), **phase shift effects** caused by the op-amp were anticipated, and confirmed experimentally too. (Fig. 15) From Fig. 15, we obtain a $97.543°$ phase difference between the two output signals, with an expected $90°$ phase difference.

In the previous section, we derived the relations between oscillation frequency, resistances and capacitances in the circuit without accounting for the parasitic capacitances that are present in the UA741. According to the SPICE simulations, we observe that selected R,C values accurately produce oscillation at the calculated frequency when this frequency is of the order of few kHz. However, when designed to attain 100kHz we observe the FFT peaking at a much smaller frequency of $\sim$68kHz. Thus, in our practical design we tuned our RC values to produce a frequency of roughly $\sim 130kHz$ so as to obtain the desired 100kHz quadrature signals (Fig. 14) and (Fig. 16).

Both UA741s are powered by $\pm 8V$ supply rails, and the limiter employs two *IN4148* diodes. The resistances used are tuned to attain $1V_{pp}$ sinusoidal outputs (Fig 15). However, we observe that the final practical results produce a slightly higher amplitude. This is caused by the inherent offset voltages in the op-amps, which also get integrated and add DC offset to the

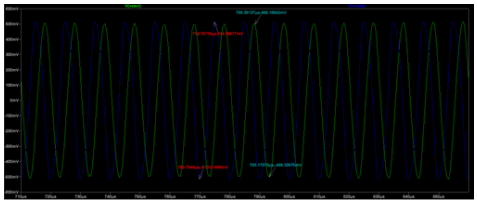

Fig. 13. SPICE Transient Plots of Oscillator Outputs

final outputs.

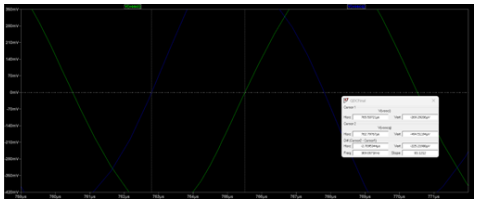

Fig. 14. Phase Difference (SPICE)

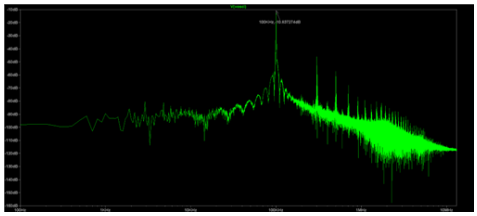

Fig. 15. Oscillator FFT, peak at 100KHz

In the practical analysis in the lab, we obtain the transient plots as below:

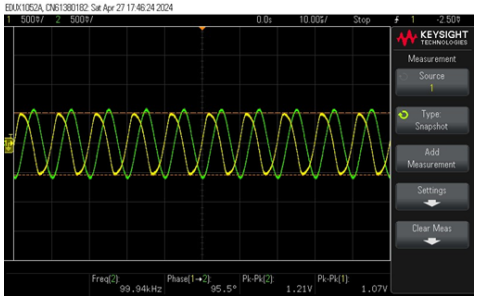

Fig. 16. Trasient Plots of Practical Circuit

III. Mixer Design

The quadrature signals from the previous stage can be fed as inputs into a simple **MOSFET-switch** based *sampler*. The mixer receives the carrier modulated message signal, which we multiply with a train of time-domain impulses which have a frequency corresponding to that of the oscillator. Essentially, we are shifting the modulated signal back into the base-band in the context of convolution in the frequency domain. Thus, Mixing results in frequency translation.

A. Circuit Analysis and Establishment of component relations

The mathematical tool below explains the said translation in frequency domain, achieved by a mixer,

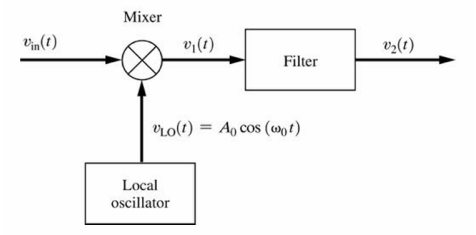

Fig. 17. Mixer Block Diagram

Say, $v_{in}(t) = Re\{g_{in}(t)e^{j\omega_c t}\}$, which is the bandpass input signal.
Now the Mixer output is obtained as,

$$v_1(t) = [A_0 Re\{g_{in}(t)e^{j\omega_c t}\}]cos\omega_0 t \tag{22}$$

$$\therefore v_1(t) = \frac{A_0}{4}[g_{in}(t)e^{j\omega_c t} + {g_{in}}^*(t)e^{-j\omega_c t}](e^{j\omega_c t} + e^{-j\omega_c t})$$

$$\therefore v_1(t) = \frac{A_0}{4}[g_{in}(t)e^{j(\omega_c+\omega_0)t} + {g_{in}}^*(t)e^{-j(\omega_c+\omega_0)t} + g_{in}(t)e^{j(\omega_c-\omega_0)t} + {g_{in}}^*(t)e^{-j(\omega_c-\omega_0)t}]$$

Hence we finally get,

$$v_1(t) = \underbrace{\frac{A_0}{2}Re\{g_{in}(t)e^{j(\omega_c+\omega_0)t}\}}_{f_u=f_c+f_0} + \underbrace{\frac{A_0}{2}Re\{g_{in}(t)e^{j(\omega_c-\omega_0)t}\}}_{f_d=f_c-f_0}$$

The first term corresponds to *up-conversion*, and the second term, which is of more interest with respect to the topic, corresponds to **down-conversion**.

We expect an output as a product of sines, in lines to the waveform below,

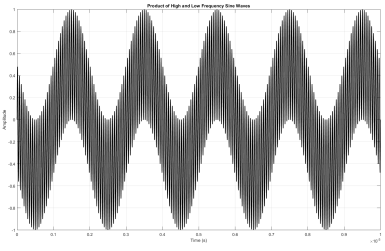

Fig. 18. Expected Mixer Output

Of course, the necessity of the coupling capacitor arises from the fact that an appropriate DC bias must be provided to the MOSFET in addition to the incoming AC signal from the previous stage. To operate the MOSFET as a switch, we want to set a value of V_{BIAS} *similar to the MOSFET threshold voltage*, so that the amplitude of the oscillator signal will

enable continuous transitioning between the cutoff and linear modes of operation.

Since we do not desire any attenuation in the oscillator signal, we aim to select a coupling capacitor C_c and R_{BIAS} such that the $-3dB$ frequency of the high-pass filter configuration is sufficiently lower than the frequency output by the oscillator.

B. Practical Testing and Results

For testing the mixer, we selected R_{BIAS} and C_c values so as to ensure the complete $100kHz$ quadrature signals were passed without attenuation through the high pass filter configuration. A calculated $-3dB$ frequency of $16kHz$ attained by selecting $R_{BIAS} = 100k\Omega$ and $C_c = 100pF$ was sufficient for this. In the practical testing we used a CD4007BE MOSFET device with an *estimated threshold voltage* of between 1 and 1.2V. Thus, our selection of bias voltage equal to 1.2V is appropriate.

Below are the comparisons between the SPICE and lab simulated plots:

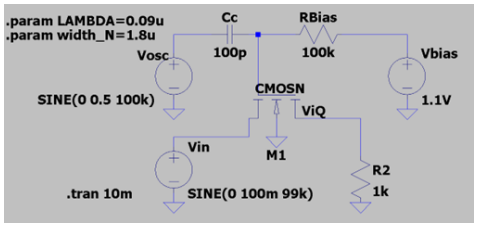

Fig. 19. Mixer Circuit (SPICE)

The SPICE-simulated transient plots is given below:

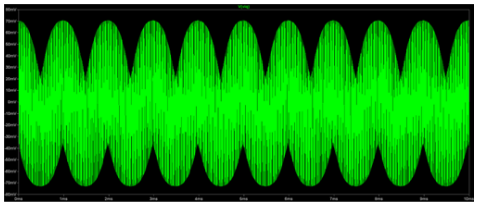

Fig. 20. Mixer Output Transient Plots (SPICE)

Whereas on a real circuit, this was obtained: From the FFT

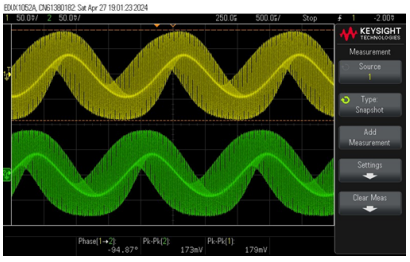

Fig. 21. Mixer Output Transient Plots (LAB)

Analysis, we expect two peaks, at $|f_c - f_0|$ and $f_c + f_0$ as mentioned above.

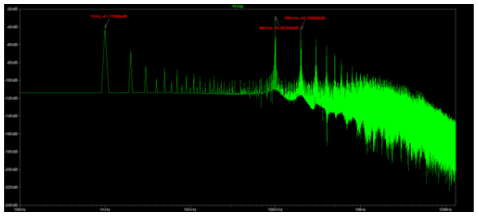

Fig. 22. Mixer FFT Analysis (SPICE)

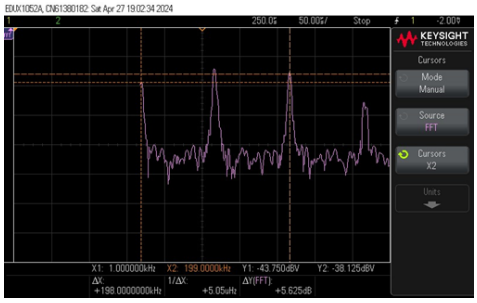

Fig. 23. Mixer FFT Analysis (LAB)

IV. Low-Pass Filter (LPF) Design

In the final stage of our Quadrature Down Converter (QDC), we employ signal filtering to isolate the original message signal from the mixer output. Specifically, low-frequency components are retained while high-frequency signals are suppressed. This process yields the in-phase (I) and quadrature-phase (Q) components of the original message signal.

A. Filter Design and Implementation

Filter Topology A *cascade* of two passive RC low-pass filters (LPFs) is utilized. Each individual LPF possesses a -3dB cutoff frequency exceeding the desired overall cutoff frequency. This configuration effectively replicates the transfer characteristic of a single, sharper LPF.

Rationale A second-order LPF is chosen to provide a smoother output signal due to its modified transfer function in the Laplace domain. While the LPFs introduce a phase shift in both the I and Q signals, the inherent $90°$ phase difference between these components is preserved.

B. Practical Testing and Results

For the purpose of practical testing, we designed the LPF for a cutoff frequency of $2kHz$. For ease of selecting practical values, we approximated R,C values to $3k\Omega$ and $10nF$. Thus, each individual LPF induces a gain of $-1.732dB$ at nearly $2kHz$, so the overall $-3dB$ frequency is calculated to be proximal to $2kHz$.

The circuit used for SPICE simulations is given below:

The SPICE-simulation for phase and attenuation at $1kHz$ is as below: The SPICE-simulation for phase and attenuation at $10kHz$ is as below, (Fig. 27)

And, the frequency response on the SPICE-simulated circuit is given below(Fig, 28)

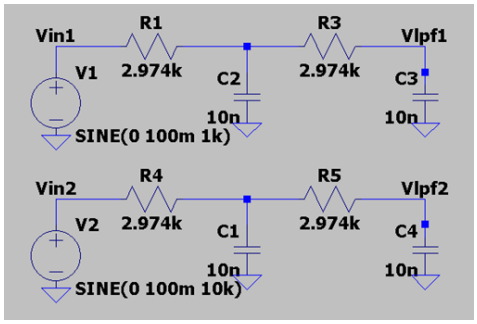

Fig. 24. SPICE Circuit

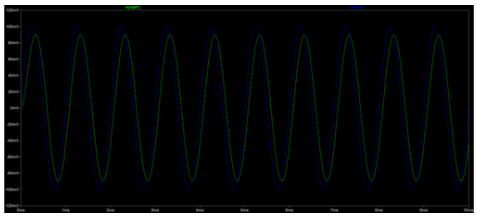

Fig. 25. Phase and Attenuation at $1kHz$ (SPICE)

Now reporting the practical circuit readings,

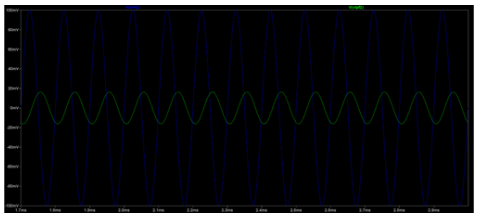

Fig. 26. Phase and Attenuation at $10kHz$ (SPICE)

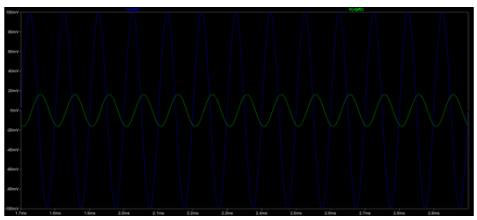

Fig. 27. Frequency Response Analysis (SPICE)

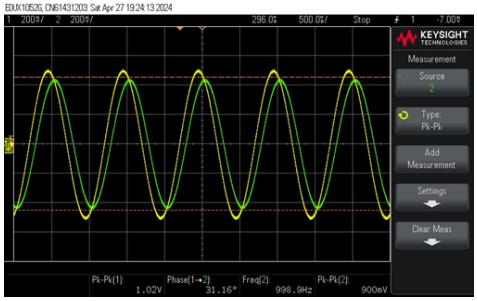

Fig. 28. Phase and Attenuation at $1kHz$ (LAB)

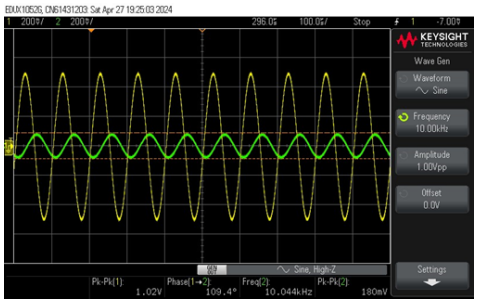

Fig. 29. Phase and Attenuation at $10kHz$ (LAB)

V. COMPLETE CIRCUIT INTEGRATION AND SUMMARY OF RESULTS

For complete testing and comparison between the simulations and practical circuit, we will assume a $101kHz$, $100mV$ sinusoidal input to both mixer configurations.

The FFT obtained in the lab is given below:

The simulated circuit on SPICE is given below,

The Transient plots, including the phase difference of the final outputs (in-phase and quadrature-phase) are given below:

And, the FFT plotted on SPICE is also given below (Fig. 37)

VI. FURTHER DEVELOPMENTS

As observed, the primary concern regarding the operation of the double-integrator loop oscillator is controlling the integration of the op-amp's offset voltage. To mitigate this

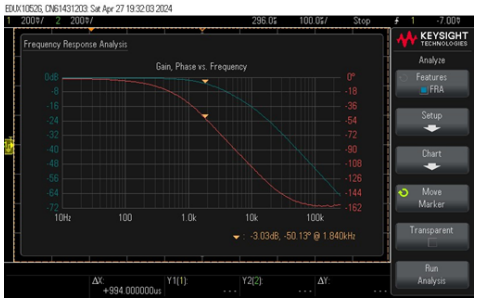

Fig. 30. Frequency Response Analysis (LAB)

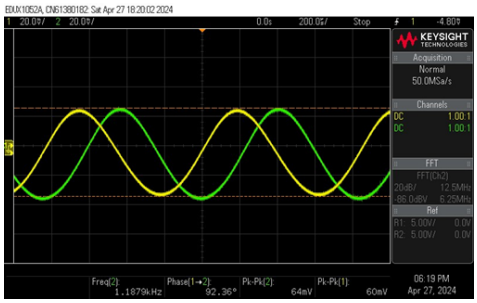

Fig. 31. Final Transient Outputs (LAB)

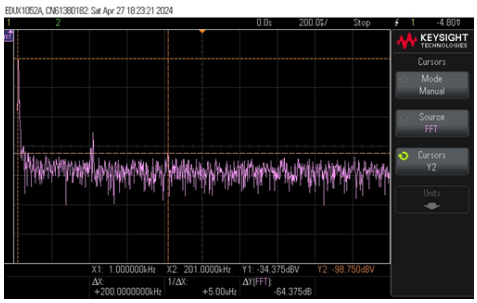

Fig. 32. Final FFT (LAB)

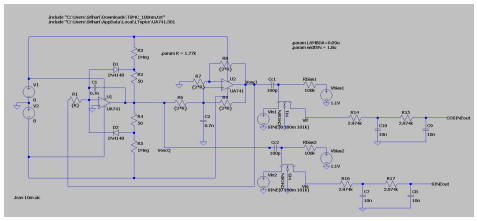

Fig. 33. Final Circuit (SPICE)

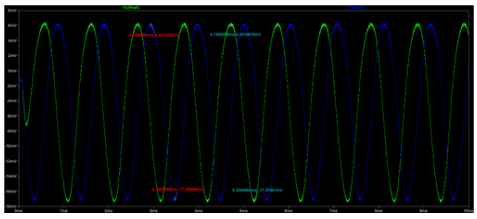

Fig. 34. Transient Plots of $V_{IF_FINAL_I}$ and $V_{IF_FINAL_Q}$

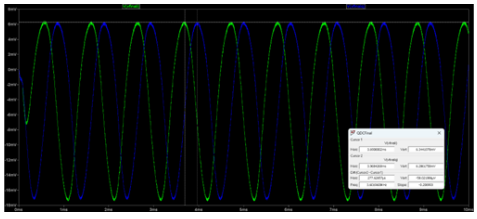

Fig. 35. Phase difference = 99.95°

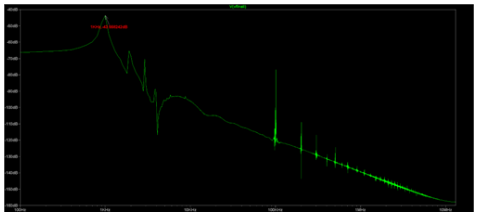

Fig. 36. FFT of Final Output (SPICE)

TABLE I
PRACTICAL CIRCUIT V/S SPICE SIMULATIONS

Parameter	Simulated	Measured
Input Frequency	$101kHz$	$101kHz$
In-phase(OSC)	$0.9985V$	$1.07V$
Q-phase(OSC)	1.0282V	1.21V
V_{BIAS}	1.1V	1.2V
C_c	100pF	100pF
Power Supply	$\pm 8V$	$\pm 8V$
Primary Resistance	$1.77k\Omega$	$1.6k\Omega$
LPF Resistance	$2.974k\Omega$	$3k\Omega$
Final Frequency	1kHz	1.188kHz
In-phase (FINAL)	23.711mV	60mV
Phase difference (FINAL)	99.95°	92.36°

issue, it would be required to explore an *effective offset-nulling technique* that ensures DC offset (and consequently the integration of the offset) is minimized.

The issue of phase-shifting can be dealt with on the basis of what devices are readily available. Access to *higher speed operational amplifiers* than the UA741 will undoubtedly contribute to *more accurate practical results*. Otherwise, a *rectifying phase shifter* may have to be inserted into the circuit, which may reduce the compactness of the design in exchange for higher accuracy.

Additionally, to better match the simulated and practical values, it is required to accurately model the MOSFET device being used in the circuit within the SPICE simulations. In this report, *we observe discrepancies in amplitude and frequency due to differences in the switching actions of the devices.*

REFERENCES AND ACKNOWLEDGEMENTS

REFERENCES

[1] Adel S. Sedra and Kenneth C. Smith, “Microelectronic Circuits” fifth. 2004.
[2] (YouTube video) Quadrature oscillator, 10kHz. Simulations and measurements., MSMTUE
[3] (YouTube video) Howland, Deboo and the non inverting Op Amp integrator, Sam-Ben Yaakov

We would also like to acknowledge the Professor, the Teaching Assistants, and the involved Lab Staff, for the making of the project.